SUBJECT: COMPUTER ORGANISATION (18CS34)

	Questions	Year
1	With a neat diagram explain basic functional units of computer.	
2	With a neat diagram explain basic operational concepts of computer. **(OR)** Explain the concept of communication between memory and processor with the respective registers. (*Also show how to add A + B to form C with the help of same diagram – June19) **(OR)** Define the functions of following processor registers: MAR, MDR, IP & IR.	Jan19(17s) Jan19,17 June19,17,18
3	Explain Bus structure with diagram. Discuss about memory mapped I/O.	Jan17
4	What is performance measurement? Discuss the basic performance equation. (Also explain the methods to improve the performance of the computer)	June19 Jan17,18,19
5	Write a note on: (a) Byte addressability (b) Big-Endian and Little-Endian assignment.	June17 Jan17, 18
6	With a memory layout starting at address 'i' represent how 'ABCD' data is stored in big endian and little endian assignment scheme in a system of word length 16 bits.	Jan19
7	What is an addressing mode? Explain different types of addressing mode with ex.	Jan19(17s),17 June19,17,18
8	Explain the basic instruction types with example.	Jan19(17s)
9	What is subroutine? How to pass parameters to subroutine? Illustrate with an ex.	June18
10	Explain logical and arithmetic shift and rotate instructions, with example.	Jan19(17s),18 June19, 17
11	Compute with initial carry bit as 1 after performing following shift or rotate operations by 2 times. (a) SHR R1,2 (b) SAR R1, 2 [Arithmetic shift] (c) ROR R2,2 (d) RCR R2, 2 [Rotate right with carry]	Jan19
12	Write an assembly program that reads a line of character and displays it.	Jan19(17s)
13	What are assembler directives? Point out and explain various directives with ex.	Jan19(17s)
18	List the steps needed to execute the machine instruction Add LOCA, RO, in terms of transfers between the processor and the memory along with some simple control commands. Assume that the instruction itself is stored in the memory at location INSTR and that this address is initially in register PC. The first 2 steps might be expressed as: • Transfer the contents of Register PC to register MAR. • Issue a Rad command to the memory and then wait until it has transferred the requested word into register MDR. Remember to include the steps needed to update the contents of PC from INSTR to INSTR+1 so that the next instruction can be fetched.	Jan18
19	Consider a computer that has a byte addressable memory organised in 32 bit words according to the big endian scheme. A program reads ASCII characters entered at a keyboard and store them in successive byte location starting at location 1000. Show the contents of the contents of the 2 memory words at locations 1000 and 1004 after the name "Johnson" has been entered. (ASCII codes J=AH, o=6FH, h=68H, n=6EH, S=73H)	Jan18

	Questions	Year
1	Explain the concept of accessing of input output devices in detail.	
2	What is an interrupt? With an ex, illustrate the concept of interrupt.	Jan17,19(17s)
3	Demonstrate the different approaches of handling interrupts for multiple devices. (*Interrupt nesting/priority structure and Daisy chain method–June18)(*simultaneous Interrupt request (Jan18,19), Vectored interrupts (Jan18) Priority Interrupts (June17)	June18,19(17s) June17, Jan19
4	Write short notes on: Daisy chain, Subroutine, Interrupt hardware, Exception.(4m each)	June19
5	With a neat diagram, explain the concept of DMA.	June19, 17 Jan17
6	Define BUS arbitration. With a neat diagram, explain different bus arbitration mechanism.	June18,19(17s) June19,17 Jan18
7	Explain connection between Processor to Keyword & Processor to Printer with diagrams.	June18,17 Jan19
11	With a neat diagram, explain about how data is read in asynchronous bus scheme. (OR) With neat timing diagram illustrate the asynchronous bus data transfer during an input operation. Use Handshake method.	Jan19,18
12	Three devices A, B and C are connected to the bus of a computer. I/O transfers for all three devices use interrupt control. Interrupt nesting for devices A and B is not allowed, but interrupt requests from C may be accepted while either A or B is being services. Suggest different ways in which this can be accomplished in each of the following cases: (i) The computer has one interrupt request line. (ii) Two interrupt request line, INTR1 and INTR2 are available with INTR1 having higher priority. Specify when and how interrupts are enabled and disabled in each case.	Jan18

Memory System

	Questions	Year
1	Define: Memory Latency and Memory bandwidth. (2marks)	June17
2	Explain synchronous DRAMS with block diagram.	Jan19(17s)
3	With a diagram, explain the internal organisation of 2M X 8 asynchronous DRAM chip.	June18, Jan17 June 17
4	With diagram, describe the internal organisation of a 128 X 8 memory chip.	June19
5	With a neat diagram, explain the design of 2M X 32 memory module using 1M X 8 memory chips.	Jan19
6	Draw and explain the working of 16 Mega Bit DRAM chip configured as 2M X 8.	Jan18
7	Describe organisation of a 2M X 32 memory using 512K X 8 memory chips.	Jan18
8	With diagram of basic SRAM (Static RAM) and DRAM (Asynchronous DRAM) chip (cell), explain the read and write operations on each of them.	June19
9	Define ROM. Explain various types of ROMs.	Jan19(17s)
10	Write a short note on Flash memories (4marks)	June17
11	Explain 'Hit Rate and Miss Penalty'.	Jan17,19(17s) June17
12	Define cache memory, explain various types of it with neat block diagram.	Jan19(17s)
13	Define the following with respect to cache memory: ■ Valid bit ■ Dirty data ■ Stale data ■Flush the cache	Jan18
14	Describe any 2 mapping functions in cache. (with diagram)	June18, 19 Jan17
15	Explain Associative mapping technique and set associative mapping technique.	June17
16	Explain in detail the working of set associative mapped cache with 2 blocks per set with relevant diagram.	Jan18
17	In a given system (i) hit rate (n) = 0.5 (ii) miss penalty (M) = 100 ns (iii) Time to access cache memory (c) = 100 ns. Calculate the average access time (t_{avg}) experienced by the processor.	June19
18	Calculate the average access time experienced by processor if miss penalty is 17 clock cycles and Miss rate is 10% and cache access time is 1 clock cycle.	Jan19 (4m)
19	Consider a cache consisting of 256 blocks of 16 words each, for a total of 4096 words and assume main memory is addressable by 16 bit address and it consists of 4K blocks. How many bits are there in each of Tag, block/set and word fields for different mapping techniques?	Jan19 (9m)
20	A block-set associative cache consists of a total of 64 blocks divided into 4 blocks sets. The main memory contains 4096 blocks, each consisting of 128 words. (i) How many bits are there in a main memory address? (ii) How many bits are there in each of the TAG, SET and WORD fields?	Jan18

(Arithmetic)

	Questions	Year
1	Draw 4-bit carry look ahead adder and explain (its operation)	Jan17,19(17s) June18,17
2	Explain the generation and propagation functions used in Carry look ahead adder.	June19
3	Design 16 bit carry look ahead adder using 4-bit adder. Unite the expression for $C_{i+1.}$	Jan18
4	Design and explain the working of 16 bit carry look ahead adder built from 8 bit carry look ahead adder. Compare its performance with 16 bit ripple carry adder built from 8 bit ripple carry adder.	Jan19
6	Design a logic circuit to perform addition/subtraction of 'n' bit number X and Y	Jan17,18
7	Perform the operations on 5-bit signed numbers using 2's complement system. Also indicate whether overflow has occurred. • (i) (-10)+(-13) (ii) (-10) – (-13) (iii) (-2) + (-9) • (ii) (-9) + (-7) (ii) (+7) – (-8) • (iii) 5+10 (iii) -14 + 11 (iii) -5 + 7 (iv) -10 + -13	June18, 17 Jan18
	Multiplication algorithm and problem for unsigned number	