

Model Question Paper- I with effect from 2022

CBCS SCHEME

Third Semester B.E Degree Examination_____

Digital Design and Computer Organization (BCS302)

TIME: 03 Hours

Max.Marks:100

- Note: Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**
- M: Marks, L: Bloom's level, C: Course outcomes.

	Module - 1		M	L	C
Q.1	a	Demonstrate the positive and negative logic using AND gate	5	L1	CO1
	b	Find the POS expression for $F(a,b,c,d) = \Pi(2,3,5,8,10,13,14) + d(1,6,7,11)$ and realize it using NOR gates.	5	L3	CO1
	c	Simplify the Boolean function, $F(w,x,y,z) = \sum(0,1,2,4,6,7,9,12,14)$ using k-map and Write the Verilog Program for realizing the minimized expression.	10	L3	CO1
	OR				
Q.2	a	What is Binary logic? List out any 4 Laws of Logic.	5	L1	CO1
	b	Simplify the following Boolean function and find its SOP: i) $F(x,y,z) = \sum(0,1,4,5,6) + d(2,3,7)$ ii) $F(w,x,y,z) = \sum(5,6,7,12,14,15) + d(13,9,11)$	10	L3	CO1
	c	Write a short note on Hardware Description Language.	5	L1	CO1
	Module - 2				
Q.3	a	Explain the differences between Combinational and Sequential Circuits with their block diagrams and examples.	5	L3	CO2
	b	What are decoders? Implement the following Boolean functions with a decoder: $F1(A,B,C) = \sum m(1, 3,4,7)$, $F2(A,B,C) = \sum m(0,2,3,6)$ and $F3(A,B,C) = \sum m(2,3,6,7)$	5	L3	CO2
	c	What are Multiplexers? Implement the Boolean function $F(A,B,C,D) = \sum m(1,3,4,11,12,13,14,15)$ with a 8:1 MUX	10	L3	CO2
	OR				
Q.4	a	Define Encoder. Design a Four-input Priority Encoder.	5	L3	CO2
	b	Write the Verilog program to Implement Full Adder and Subtractor Circuits.	5	L3	CO2
	c	Write the Characteristic Table and Equations of SR, JK, D and T Flip Flops.	10	L1	CO2
	Module - 3				

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Q.5	a	What do you mean by an Addressing Mode? Explain any 5 Addressing Modes.	10	L1	CO3
	b	Describe the functionality of the following: MAR, PC, IR, MDR and ALU	5	L1	CO3
	c	Explain Basic Performance Equation and SPEC rating.	5	L2	CO3
OR					
Q.6	a	Demonstrate the Branching operations using a loop to add n numbers with block diagram.	8	L3	CO3
	b	The Registers R1 and R2 has decimal values 1200 and 4600. Calculate the effective address of the memory operand in each of the following instructions when they are executed in sequence. i) Load 20(R1), R5 ii) Move #3000, R5 iii) Store R5, 30(R1,R2) iv) Add -(R2), R5 v) Subtract (R1)+, R5	7	L3	CO3
	c	Explain Single Bus Structure.	5	L2	CO3
Module - 4					
Q.7	a	Explain Memory mapped I/O and I/O interface for an input device with a diagram.	10	L2	CO4
	b	Explain I/O operations involving a keyboard and display device with a program that reads one line from keyboard, stores it in buffer and echoes it back to display.	10	L4	CO4
OR					
Q.8	a	Explain how to handle interrupt from multiple devices using daisy chain and priority scheme.	10	L3	CO4
	b	Explain Centralized and Distributed Bus Arbitration approaches.	10	L2	CO4
Module - 5					
Q.9	a	With a diagram, explain the single bus organization of the data path inside a processor.	10	L2	CO5
	b	Describe the Basic idea of Instruction Pipeline.	10	L2	CO5
OR					
Q.10	a	Explain the process of Fetching Word from Memory in processor.	10	L4	CO5
	b	Explain the Pipeline Performance of a Processor and pipeline stalls.	10	L2	CO5