DAYANANDA SAGAR COLLEGE OF ENGINEERING

Shavigemalleshwara Hills, Kumaraswamy Layout, Bengaluru-560111, Karnataka (An Autonomous College affiliated to VTU Belgaum, accredited by NBA & NAAC)

Department of Electronics & Communication Engineering



VI SEM BE MINI-PROJECT (22EC66) REPORT

Implementation of Radix-4 Multiplier using Cadence Virtuoso

Submitted in partial fulfillment of the requirement for the degree of

Bachelor of Engineering

in

Electronics & Communications Engineering - ECE

 b_1

USN: 1DS22EC054 Chaitra Krishna Gouda

USN: 1DS22EC120 Manish S

USN: 1DS22EC170 Ram Prasad H USN: 1DS22EC236 Tejaswi M N

Under the guidance

of

Dr. Vimala P

Professor ECE Dept., DSCE, Bengaluru



VISVESVARAYA TECHNOLOGICAL UNIVERSITY

Jnanasangama, Macche, Santibastwada Road Belagavi-590018, Karnataka 2024-25

Certificate

Certified that the mini-project work (Course Code: 22EC66) entitled "Implementation of Radix 4 Multiplier using Cadence Virutoso" carried out by Chaitra G (1DS22EC236), Manish S (1DS22EC120), Ram Prasad H (1DS22EC170), Tejaswi M N (1DS22EC236) are bonafide students of the Department of ECE of Dayananda Sagar College of Engineering, Bangalore, Karnataka, India in partial fulfillment for the award of Bachelor of Engineering in Electronics & Communication Engineering of the Visvesvaraya Technological University, Belagavi, Karnataka for the VI Semester course during the academic year 2024-25. It is certified that all corrections / suggestions indicated for the mini-project work have been incorporated in the mini-report. This VI semester mini-project report has been approved as it satisfies the academic requirement in respect of mini-project work prescribed for the said degree.

Mini-Project Guide Sign :		
Name : Dr. Vimala P, Prof., ECE, DSCE		
Mini-Project Domain Coordinator Sign:		
Name: Dr. SANTHOSH KUMAR R, Asst. Pr	rof., ECE, DSCE	
Mini-Project Convener & Chief Coordinator S	ign :	
Name: Dr. Trupti Tagare , Asst. Prof. , ECE , D	OSCE	
Dr. Shobha K R :		
Prof. & HOD, ECE, DSCE		
Dr. B.G. Prasad :		
Principal, DSCE		
Mini-Project Viva-Voce (CIE)		
Name of the mini-project examiners (with date):		
1:	Signature :	
2 :	Signature :	

Declaration

Certified that the mini-project work entitled, "Implemenation of Radix 4 Multiplier using Cadence Virtuoso" with the course code 22EC66 (2 Credits, CIE 100 Marks) is a bonafide work that was carried out by ourselves in partial fulfillment for the award of degree of Bachelor of Engineering in Electronics & Communication Engg. of the Visvesvaraya Technological University, Belagavi, Karnataka during the academic year 2024-25 for the VI Semester Autonomous Course. We, the students of the VI sem mini-project group/batch no. 6MP54 do hereby declare that the entire mini-project has been done on our own. The results embedded in this mini-project report has not been submitted elsewhere for the award of any type of degree.

Student Name-1: Ms. Chaitra Krishna Gouda
USN: 1DS22EC054
Sign :
Student Name-2 : Mr. Manish S USN : 1DS22EC120
Sign :
Student Name-3 : Mr. Ram Prasad H USN : 1DS22EC170
Sign :
Student Name-4 : Mr. Tejaswi M N USN : 1DS22EC236
Sign :

Date: / 05 / 2025

Place: Bengaluru

Acknowledgement

It is our profound gratitude that we express our indebtedness to all who have guided us to complete this mini-project successfully. We extend our sincere thanks to the management of DSCE, for providing us with excellent infrastructure and facilities. We are thankful to our principal Dr. B. G. Prasad, for his encouragement and support. We are grateful to our HOD Dr. Shobha K. R for her valuable insights and guidance. We sincerely acknowledge the Mini-Project Convener & Chief Coordinator Dr. Trupti Tagare for her help and constant support. We are thankful to our guide Dr. Vimala.P for his/her valuable guidance, exemplary support and timely suggestions throughout the journey of the mini-project. We would like to thank our Mini-Project Domain Coordinators – Dr. Shashi Raj K, Dr. Santhosh Kumar R, Dr. Yashaswini Gowda, and Prof. Kavita Guddad for their support and coordination.

I also thank the teaching and non- teaching staff members of Department of Electronics and Communication Engineering and also, my family and friends for the help and support provided by them in successful completion of the miniproject. Our accomplishments would be incomplete without my beloved parents, for without their support and encouragement we would not have reached up to this level. We express our gratitude to the Almighty for guiding us throughout this journey.

Thank you all.

Chaitra Krishna Gouda Manish S Ram Prasad H Tejaswi M N

Abstract

The Radix-4 multiplier is an efficient digital circuit designed to perform high-speed binary multiplication by reducing the number of partial products. Based on an improved version of Booth's algorithm, it processes two bits of the multiplier at a time, which minimizes the number of required addition steps. This results in faster computation and improved performance compared to traditional multipliers. The Radix-4 algorithm is well-suited for VLSI implementation due to its balance between speed and hardware complexity. It is widely used in digital signal processing and arithmetic units where speed and efficiency are critical in processing large binary numbers.

Table of Contents

Chapter 1	Introduction	1
Chapter 2	Literature survey	2
Chapter 3	Objectives & Problem Statement	3
Chapter 4	Block diagram & Implementation	4
Chapter 5	Software tools used	10
Chapter 6	Photographs of the circuit & Simulation Results	11
Chapter 7	Results and Discussions	17
Chapter 8	Applications, Advantages, Outcomes & Limitations	20
Chapter 9	Conclusion	22
References		23

List of Figures

Fig. 4.1: Block Diagram of the Radix-4 Multiplier	4
Fig. 4.2: Booth Encoding Table	5
Fig. 4.3: Flow Diagram of the methodology used	7
Fig. 5.1 Cadence Virtuoso logo	10
Fig. 6.1: Booth Encoder	11
Fig. 6.2: Waveform of Booth encoder	11
Fig. 6.3: Partial Product Generator for single bit	12
Fig. 6.4: Partial Product Block	12
Fig. 6.5: CLA adder	13
Fig. 6.6: Symbol of the CLA adder	13
Fig. 6.7: CLA adder waveform	14
Fig. 6.8: 12 bit adder block	14
Fig. 6.9: Radix 4 Multiplier	15
Fig. 6.10: Radix 4 Multiplier test circuit	15
Fig. 6.11: Radix 4 Multiplier input waveform	16
Fig. 6.12: Radix-4 Multiplier output waveform	16
Fig. 7.1: Number Representation in Binary	17
Fig. 7.2: Booth encoding explanation	18
Fig. 7.3: Recoded Multiplier	18
Fig. 7.4: Partial Product Generation and output	19
Fig. 7.5: Verification of the Output	19

Nomenclature and Acronyms

Abbreviations (Alphabetical Order):

DSCE Dayananda Sagar College of Engineering

ECE Electronics & Communication Engineering

IEEE Institute of Electrical & Electronics Engineers