

Mini Project Work (22EC66)  
Phase 1 Presentation  
MARCH 2025, 6<sup>th</sup> Semester



**Dayananda Sagar College of Engineering, Bangalore, Karnataka**  
**Department of Electronics & Communication Engineering**

Mini Project Batch No.:  
6MP54

**IMPLEMENTATION OF RADIX - 4  
MULTIPLIER USING CADENCE VIRTUOSO**

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# OVERVIEW OF THE MINI PROJECT

1. Introduction
2. Literature Review
3. Problem Statement & Objective
4. Clarifications to the comments given during selection phase
5. Methodology adopted with Block-Diagrams & Flow- Charts
6. H/w and S/w tools used
7. Work done so far(50% of the work must have been done)
8. Results
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# INTRODUCTION

## What is a Radix Multiplier?

A Radix Multiplier is a digital circuit that performs binary multiplication using an optimized algorithm to reduce computation steps. Unlike basic multipliers that process bits one-by-one (Radix-2), higher Radix multipliers (e.g., Radix-4, Radix-8) group bits to process multiple bits simultaneously, improving speed and efficiency.

## Why Radix-4?

1. Reduces Partial Products by 50% (vs. Radix-2) by encoding multiplier bits in groups of 3 (with overlap).
2. Enhances Speed
3. Saves Power & Area

*Cadence Virtuoso* is a powerful EDA tool for designing and simulating VLSI circuits.

# LITERATURE REVIEW

TITLE - AUTHOR	YEAR OF PUBLICATION	FOCUS OF THE PAPER
“Design and Implementation of Radix 4 Based Arithmetic Operations” by Saste and A. Sawant	2019	Focusing on improving Arithmetic efficiency in Digital Systems
Design Of High Performance Configurable Radix-4 Booth Multiplier Using Cadence Tools by Dr.T. Esther Rani	2022	Designs a configurable Radix-4 Booth multiplier with a Hybrid Adder in Cadence, achieving 17.1ns delay (29% faster than Radix-2) and 1.12mW power.
Modified Booth Encoding Radix-4 8-bit Multiplier by Da Huang, Afsaneh Nassery	2020	Implements an 8-bit Radix-4 Booth multiplier in 0.5µm CMOS, using Booth Encoder + CLA, achieving 0.2092mW power and 38-gate delay.
A Fast Multiplier Using Modified Radix-4 Booth Algorithm With Redundant Binary Adder For Low Energy Applications R.Mallikarjuna Sharma, K.Raju	2018	Proposes a low-energy Radix-4 multiplier using a modified Booth algorithm and Redundant Binary Adder, simulated in Cadence (180nm) to reduce power and delay.



# PROBLEM STATEMENT & OBJECTIVES

## Problem Statement

- Large area requirement on the chip
- High power consumption due to the many gates involved
- Relatively long delay time

## Objectives

- To understand the Radix Multiplier concept
- To implement the Radix Multiplier in Cadence Virtuoso
- To analyse the time delay and power

# Clarifications to the comments given during selection phase

## Manual Calculations

Step ①: Number representation

$$+13 \times -7$$

$\swarrow$   $\searrow$

multiplicand multiplier

Binary representation.

$$+13 \rightarrow 1101$$

$$-7 \rightarrow 1011$$

$$\begin{array}{l} 13 \rightarrow 01101 \\ -7 \rightarrow \frac{10111}{\text{sign.}} \end{array}$$

Step ②: Bit pair recoding of multiplier.

$$\text{multiplier} \rightarrow -7 \rightarrow 11001$$

Booth Encoding Table

$i+1$	$i$	$i-1$	$M_i$	$X$	$X_2$	Booth Encoding
0	0	0	0	0	0	$+0 \cdot M$
0	0	1	0	1	0	$+1 \cdot M$
0	1	0	0	1	0	$+1 \cdot M$
0	1	1	0	0	1	$-1 \cdot M$
1	0	0	1	0	1	$-2 \cdot M$
1	0	1	1	1	0	$+0 \cdot M$
1	1	0	1	1	0	$-1 \cdot M$
1	1	1	1	0	0	$-2 \cdot M$

$$\begin{array}{l} IP = F- \times S \\ M_i = i_{+1} \end{array}$$

$$X = i + i-1$$

$$X_2 = \overline{i_{+1}} i_{+1} + \overline{i_{+1}} \overline{i_{+1}}$$

$$\boxed{1010010111}$$

$$\begin{aligned} V &= -2(i+1) + (i) \\ &\quad + (i-1) \end{aligned}$$

$$\boxed{1101101000}$$

$$\begin{array}{r}
 & & c_{i+1} & c_i & c_{i-1} & c_{i+1} & c_i & c_{i-1} \\
 & & 1 & 1 & 1 & 0 & 0 & 1 \\
 \hline
 & 0 & & -2 & & +1 &
 \end{array}$$

$\Downarrow$   
recoded multiplier

NOTE:

append 0 if (+)ve no.  
append 1 if (-)ve no.

### Step ③ : Multiplication

multiplicand  $\rightarrow 13 \rightarrow 01101$

recoded multiplier  $\rightarrow 0 -2 +1$

here,

multiplication with,

- (i) 0  $\rightarrow 0 (00000)$
- (ii) +1  $\rightarrow$  multiplicand (01101)
- (iii) -1  $\rightarrow$  2's complement of multiplicand  
(10011)
- (iv) +2  $\rightarrow$  shift multiplicand left by 1 bit  
(011010)
- (v) -2  $\rightarrow$  2's complement of shifted  
multiplicand (100110)

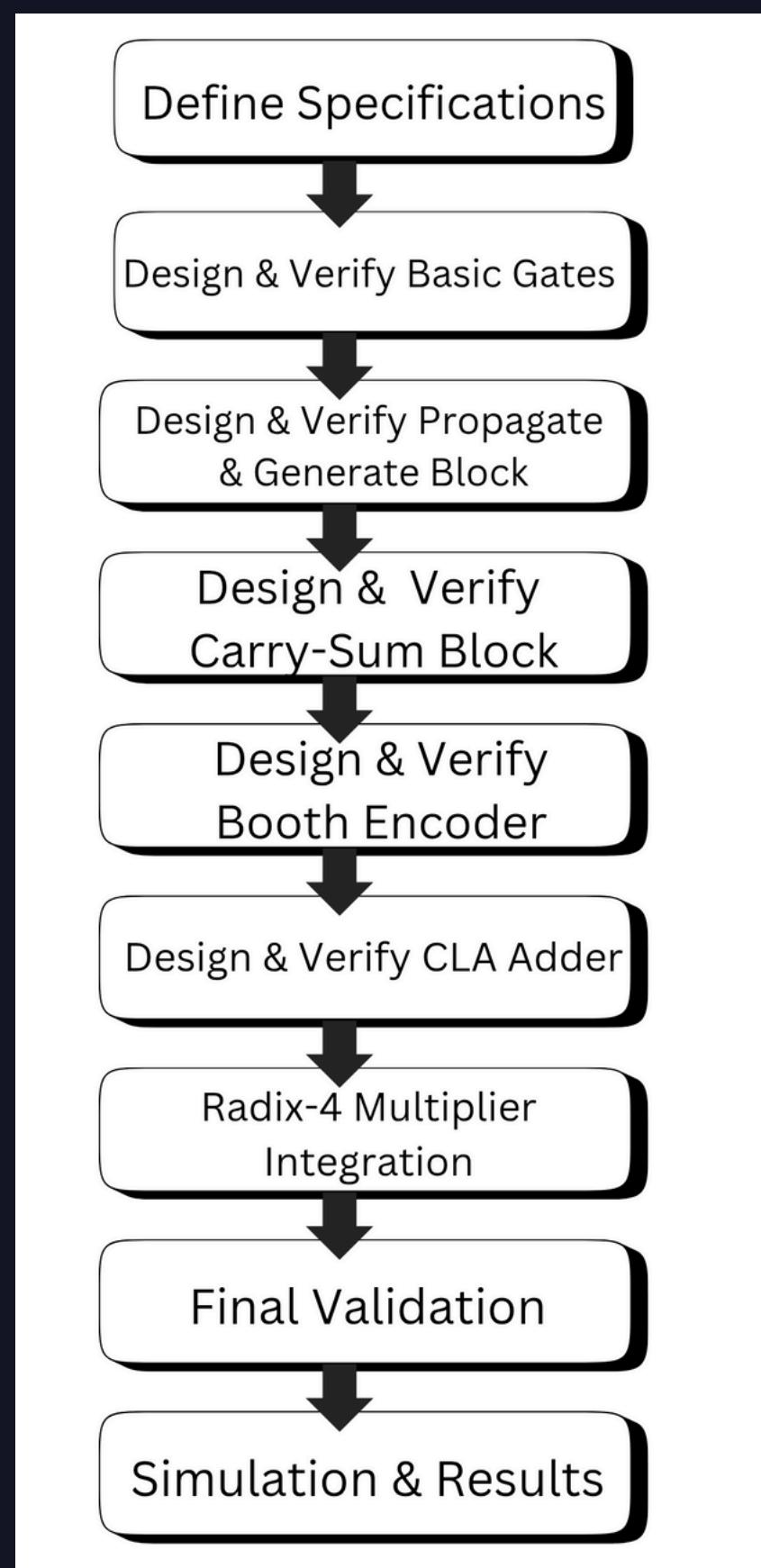
0 1 1 0 1  $\rightarrow$  multiplicand (5 bits)  
0 -2 +1  $\rightarrow$  recoded multiplier (5 bits)

$$\begin{array}{r}
 & \overline{0\ 0\ 0\ 0\ 0} & 0\ 1\ 1\ 0\ 1 & (10\text{ bits}) \\
 \text{appended} \nearrow & \overline{1\ 1\ 1\ 0\ 0\ 1\ 1\ 0} & & \\
 & \overline{0\ 0\ 0\ 0\ 0\ 0} & & \\
 \hline
 & \overline{1\ 1\ 1\ 0\ 1\ 0\ 0\ 1\ 0\ 1} & &
 \end{array}$$

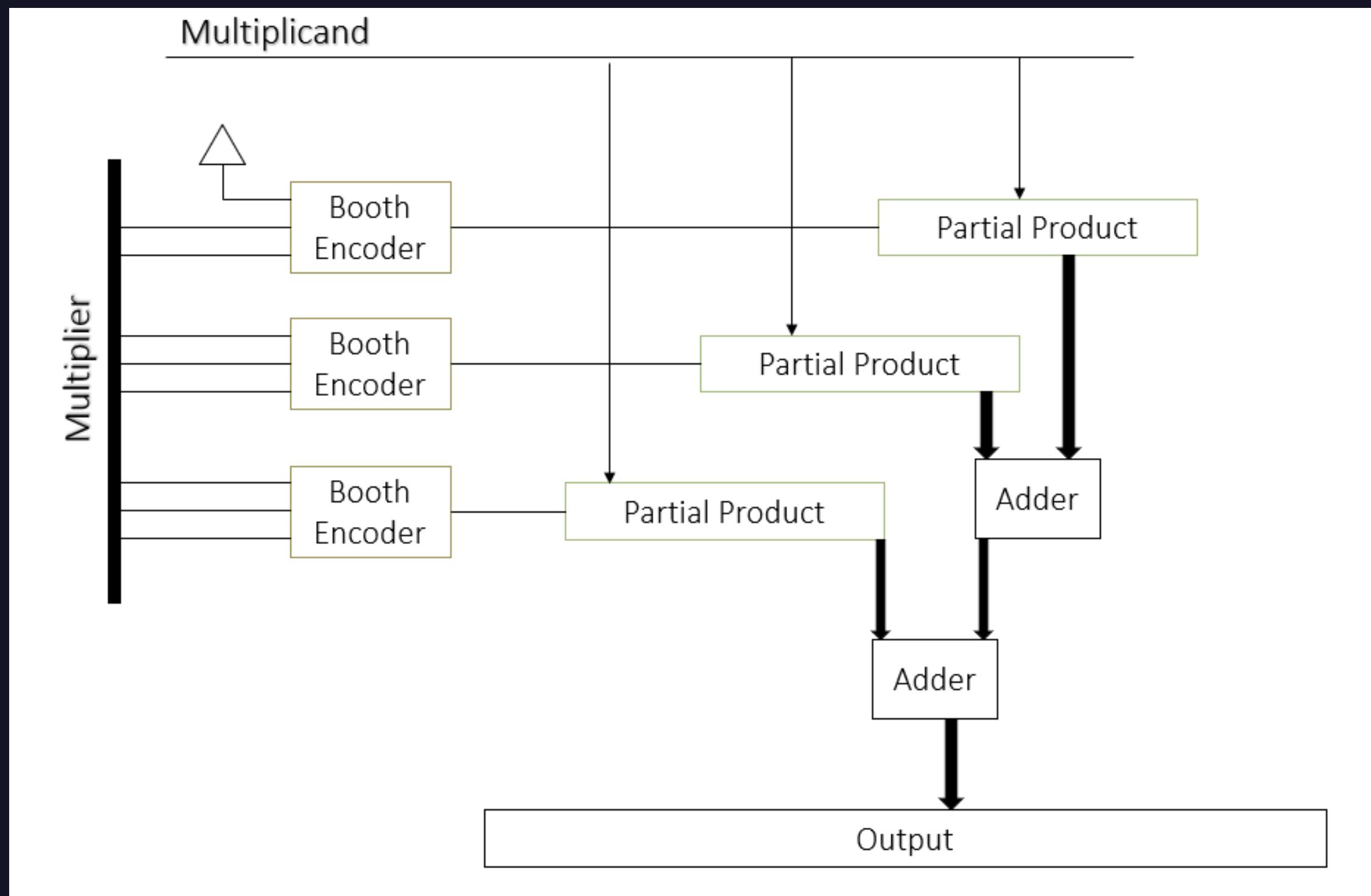
# METHODOLOGY ADOPTED

The methodology for the project will involve designing, simulating, and optimizing a radix-based multiplier circuit in Cadence Virtuoso, utilizing its tools for schematic capture, layout, and verification to ensure high performance and accuracy.

# Flow Chart:



# Block Diagram:



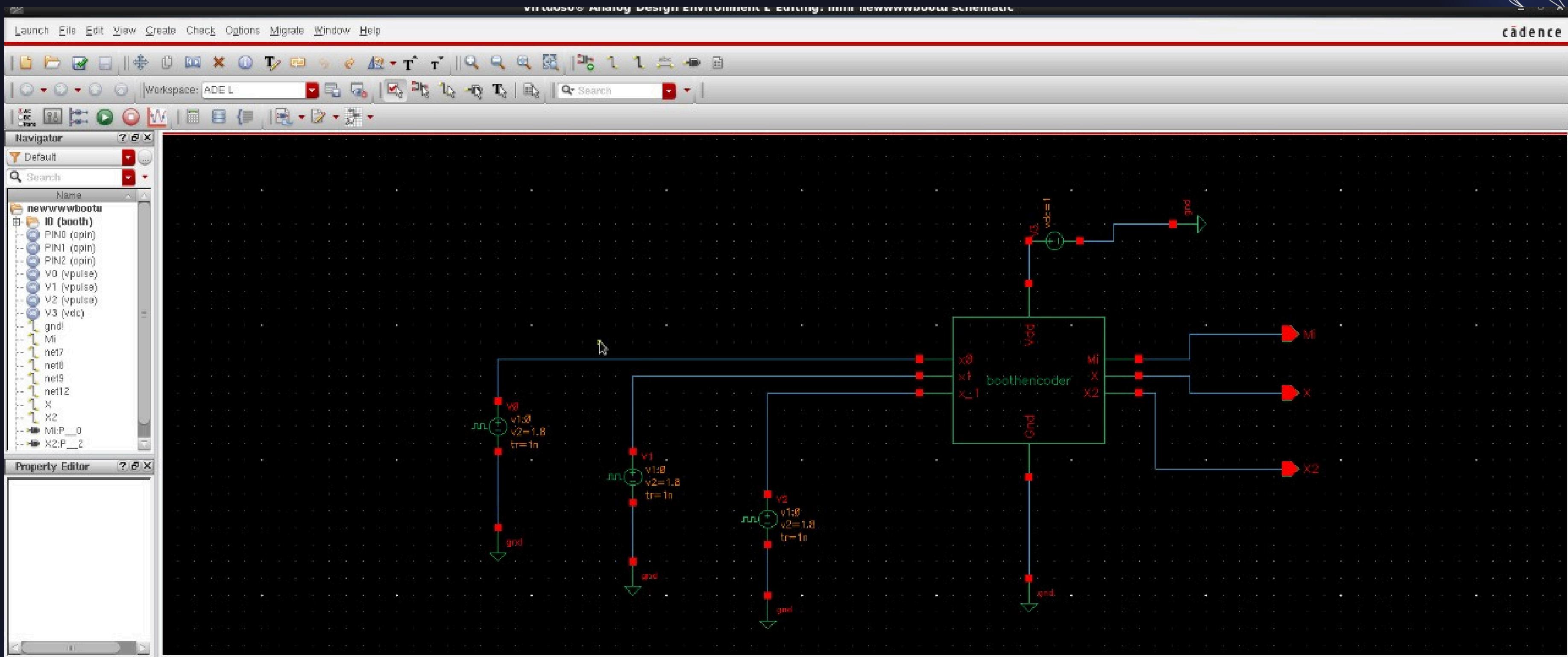
# SOFTWARE TOOLS USED

## Cadence Virtuoso

Industry-leading EDA tool for schematic design and transistor-level simulation of ICs

- Used for schematic design and transient simulation.
- Designed basic gates (NOT, AND, OR, XOR) to build higher-level components.
- Constructed Full Adder, Booth Encoder, an Generator.
- Integrated all modules to form the Radix-4 Multiplier.
- Performed transient analysis to verify functionality and timing.

# Work done so far



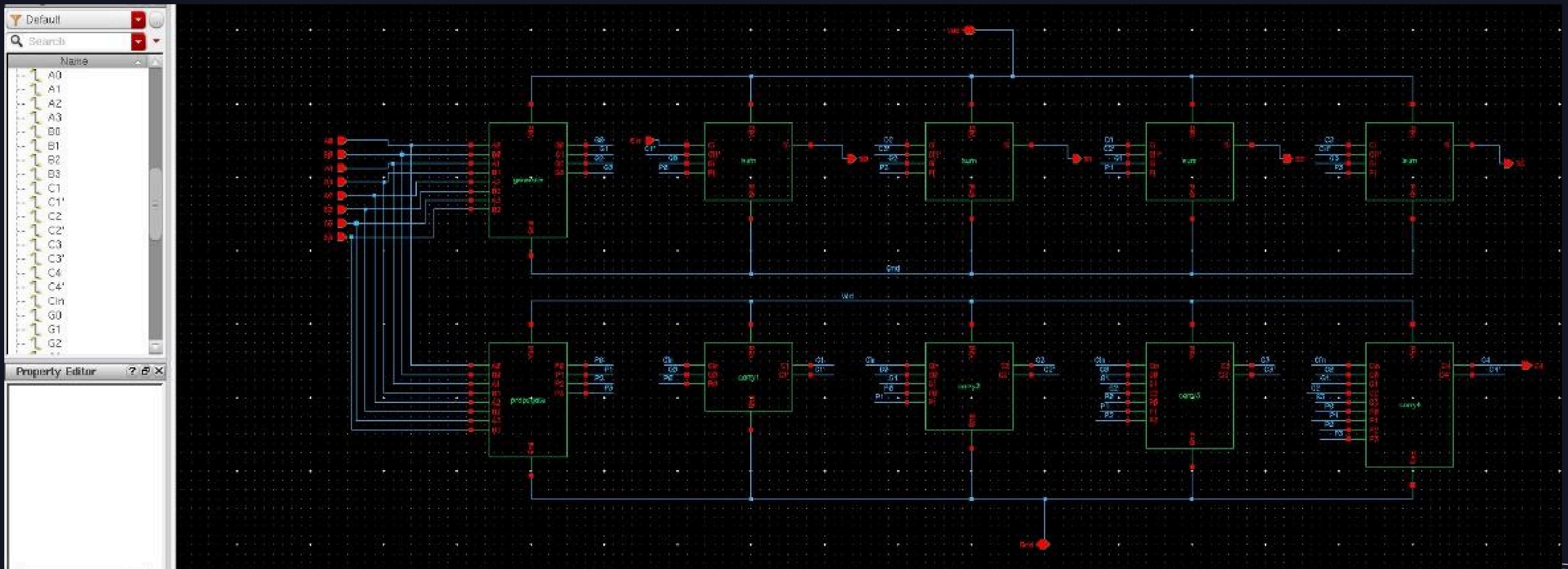
# Wave Form of Booth Encoder

X X

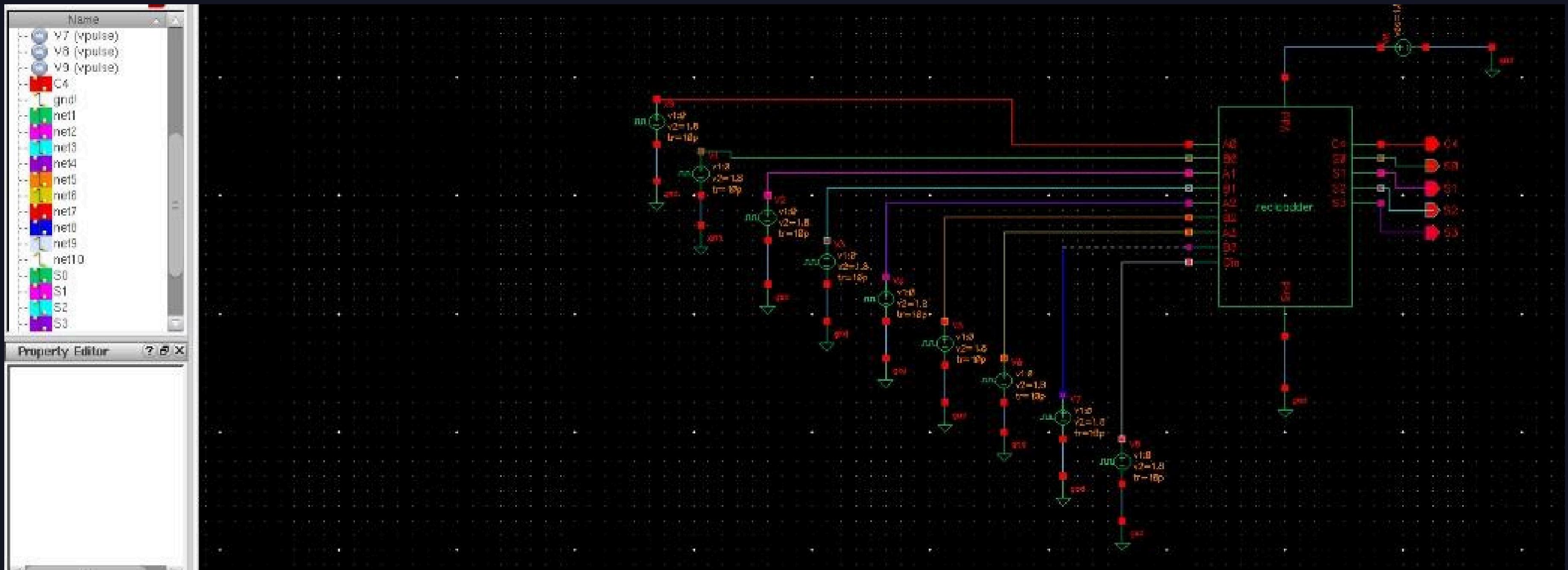


# Result Of CLA Adder

X X

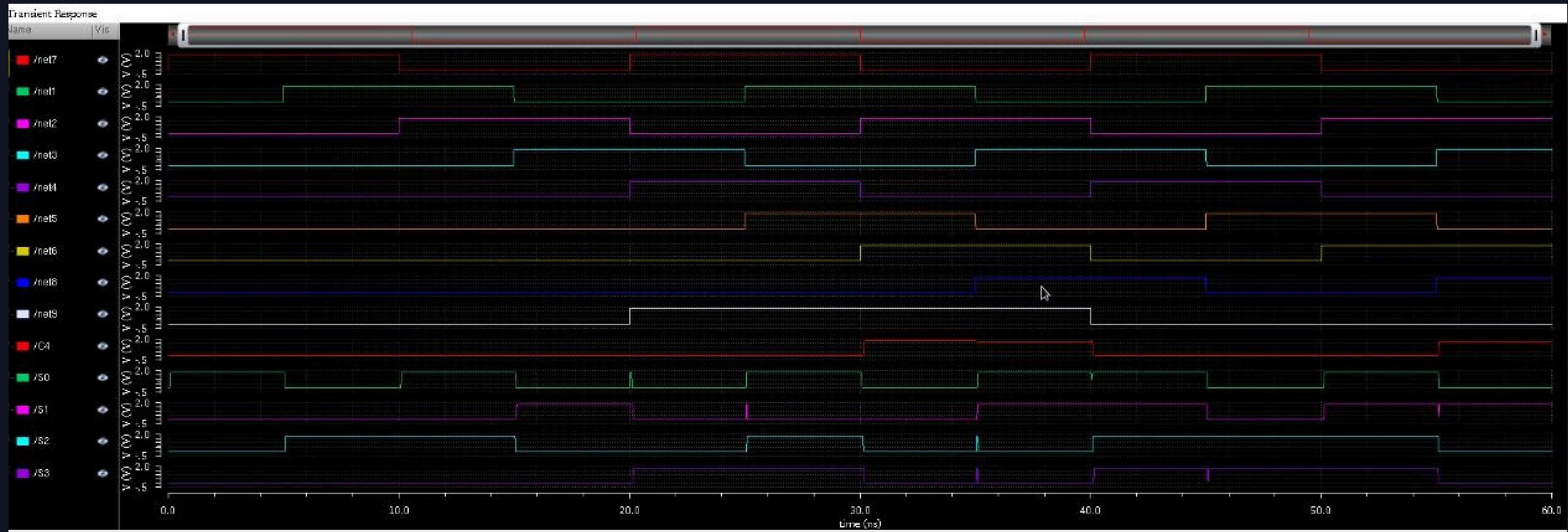


X X



# Wave Form Of CLA Adder

X X



# FUTURE IMPLEMENTATION

- Design of the Partial Product Generator.
- To Implement & Verify the Radix-4 Multiplier in Cadence Virtuoso .
- To Analyse the Time delay and Power.



# TIMELINE

Month	Flow of Project Work
March	To Understand and Design Booth Encoder and CLA Adder using Cadence Virtuoso.
April	To Implement & Verify the Radix-4 Multiplier in Cadence Virtuoso .
May	To Analyse the Time delay and Power.

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# REFERENCES

- Saste and A. Sawant, "Design and Implementation of Radix 4 Based Arithmetic Operations," *Dept. of Electronics & Telecommunication, Trinity College of Engineering & Research, Pune, India.*
- S. Shafiulla Basha and Syed Jahangir Badashah, "Design and Implementation of Radix-4 Based High Speed Multiplier for ALU's Using Minimal Partial Products," *Asstt. Prof., E.C.E Department, Y.S.R.E.C of Y.V.U, Proddatur, Y.S.R. District, A.P., India.*
- T. Esther Rani, "Design of high performance configurable radix-4 Booth multiplier using Cadence tools," *CVR College of Engineering, Dept of ECE, Hyderabad, India*



THANK  
you !!!

