# DAYANANDA SAGAR COLLEGE OF ENGINEERING

## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

**6th Semester Mini-Project Work (22EC66) - 2024-25**

## PO, PSO and SDG Mapping for Mini-Project Work

**Mini-Project Group No.:6MP54**

| USN | Name |
|---|---|
| 1DS22EC054 | CHAITRA KRISHNA GOUDA |
| 1DS22EC120 | MANISH S |
| 1DS22EC170 | RAM PRASAD H |
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**Mini-Project Title: Implementation of Radix-4 Multiplier using Cadence Virtuoso**

**Guide Name: Prof. Dr. Vimala P**

## PO & PSO mapping table

| PO 1 | PO 2 | PO 3 | PO 4 | PO 5 | PO 6 | PO 7 | PO 8 | PO 9 | PO 10 | PO 11 | PO 12 | PSO 1 | PSO 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ✓ | ✓ | ✓ | ✓ | ✓ | | | ✓ | ✓ | ✓ | | ✓ | ✓ | ✓ |

## Justification for PO & PSO mapping

| Mini-Project Title | | Implementation of Radix-4 Multiplier using Cadence Virtuoso |
|---|---|---|
| PO | Levels 3/2/1 | Justification |
| PO1 | 2 | We have applied the basic knowledge of electronics knowledge for the design of the model. |
| PO2 | 2 | Analysing the multiplier using Cadence Virtuoso and reduce the size of partial product and saves area for better efficiency. |
| PO3 | 2 | By using different blocks such as cla adder, partial product generator, half adder to design a multiplier which is more efficient. |
| PO4 | 2 | Researching on the different types of adders and encoder to reduce the size of partial product and saves area. |
| PO5 | 2 | Usage of Cadence Virtuoso software for the design of multiplier. |
| PO6 | | |
| PO7 | | |
| PO8 | 3 | Ensuring accurate and reliable data collection for honest reporting and analysis. |
| PO9 | 3 | Working in a team to design and took individual works as a part of the team. |
| PO10 | 3 | Regular communication among the team to increase the mutual understanding and to improve the project. |
| PO11 | | |
| PO12 | 3 | Hands on experience with design of the multiplier and verification. |
| PSO1 | 2 | Application of the analog electronics knowledge for development of Multiplier. |
| PSO2 | 2 | Implementation of radix 4 Multiplier using Cadence Virtuoso. |

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## SDGs Mapping

Project Title: **Implementation of Radix-4 Multiplier using Cadence Virtuoso.**

SDGs Mapped: 8,9

Justification for SDGs mapping: Generates jobs in design, verification (Analog) using Cadence Virtuoso and Developing compact, efficient multiplier promotes technological innovations.

**Signature of Guide**