



**Dayananda Sagar College of Engineering**  
**Department of Electronics and Communication Engineering**

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**A REPORT ON NMOS INVERTER AND and OR GATE**

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## CADENCE VIRTUOSO

- Cadence virtuoso is a very important EDA tool for electronics students learning about IC design/analysis and PCB design/analysis.
- At undergraduate level, virtuoso is majorly used for custom design and analysis of circuits based on MOS technologies, especially in the CMOS VLSI course.
- The Virtuoso System Design Platform allows IC designers to easily include system-level layout parasitic in the IC verification flow, enabling time saving by combining package/board layout connectivity data with the IC layout parasitic electrical model.
- It enables engineers to design concurrently across chip, package, and board, saving time and minimizing errors. It is ideal for designs that integrate multiple heterogeneous ICs, including RF, analog, and digital devices.

Some key benefits of Cadence Virtuoso are:

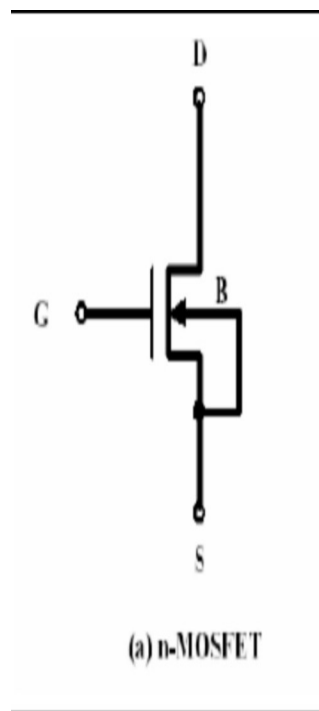
1. Easy to use, easy to understand software with an interactive interface.
2. Supports circuit design by using symbols and structures in the workspace and also allows textbased design.
3. Great platform for beginners in the core industry to start learning about design and synthesis.
4. Allows the user to analyse the designs on various parameters like power consumption, area usage and delay.

The logo for Cadence, featuring the word "cadence" in a lowercase, bold, sans-serif font. A small red horizontal bar is positioned above the letter "a".

## INTRODUCTION

NMOS is a N channel metal oxide semiconductor system. It has P type Substrate and n<sup>+</sup> type region in the drain and source. It is used to pass strong logic zero and weak logic 1.

PMOS is a P channel metal oxide semiconductor system. It has N type Substrate and p<sup>+</sup> type region in the drain and source. It is used to pass strong logic one and weak logic zero.



### **Structure:**

An NMOS transistor consists of three main regions:

**Source (S):** This is the terminal through which the majority charge carriers (electrons) enter the channel.

**Drain (D):** This is the terminal where the electrons flow out of the channel.

**Gate (G):** The gate is the control terminal that modulates the flow of current between the source and the drain. The gate is electrically isolated from the channel by a thin layer of oxide (usually silicon dioxide).

## **NMOS INVERTER**

An **NMOS inverter** is a basic digital logic circuit that performs the logical NOT operation (inversion) on an input signal. It uses a single NMOS transistor to achieve this functionality. In digital terms, an inverter outputs the opposite of its input: when the input is **high** (logic 1), the output will be **low** (logic 0), and vice versa.

### **Structure and Working**

The **structure of an NMOS inverter** consists of:

1. **NMOS Transistor:** The core component with three terminals:
  - **Gate (G):** Input signal (A) is applied here.
  - **Drain (D):** The output signal (Y) is connected here.
  - **Source (S):** Connected to ground (GND).
2. **Pull-up Resistor (R):** Connected between the **output (Y)** and **V<sub>dd</sub>** (supply voltage), ensuring the output is pulled high when the NMOS transistor is off.
3. **Input Signal (A):** Applied to the gate of the NMOS transistor. It controls whether the NMOS is on or off.
4. **Output Signal (Y):** The output is connected to the drain of the NMOS transistor, providing the inverted version of the input signal.

### **Advantages :**

#### **Simplicity:**

- The NMOS inverter is simple to design, requiring only an NMOS transistor and a pull-up resistor, making it a cost-effective solution for basic logic operations.

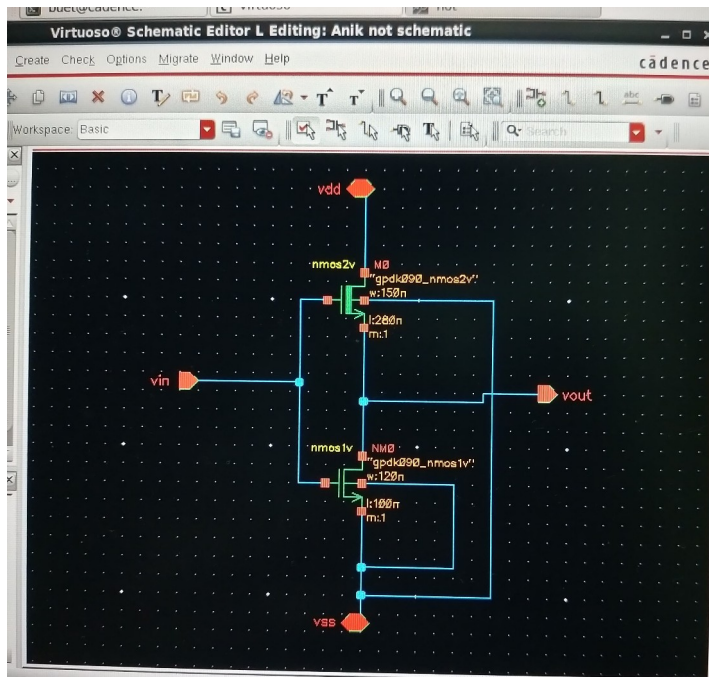
### **Low Power Consumption (in specific conditions):**

- When the NMOS transistor is off (input is low), there is little to no current flowing, resulting in low static power consumption.

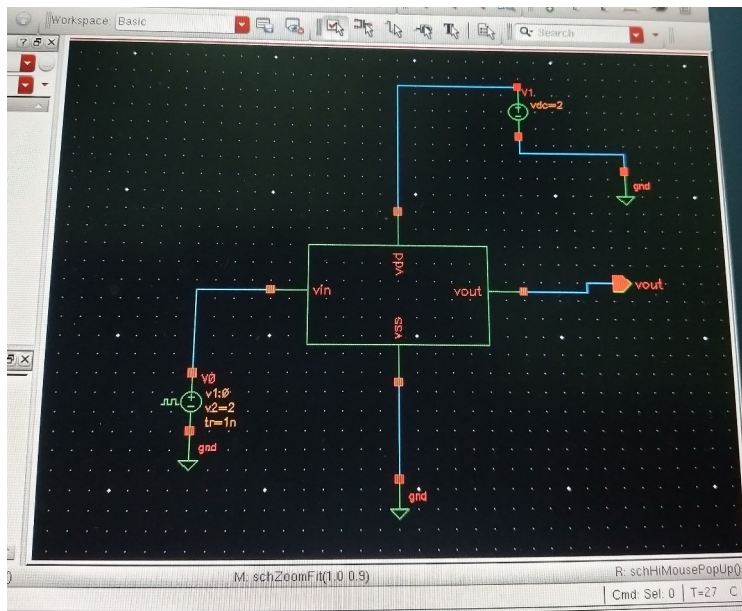
### **Fast Switching:**

- NMOS transistors are typically faster than PMOS transistors in terms of switching speed, making NMOS inverters useful in high-speed digital circuits.

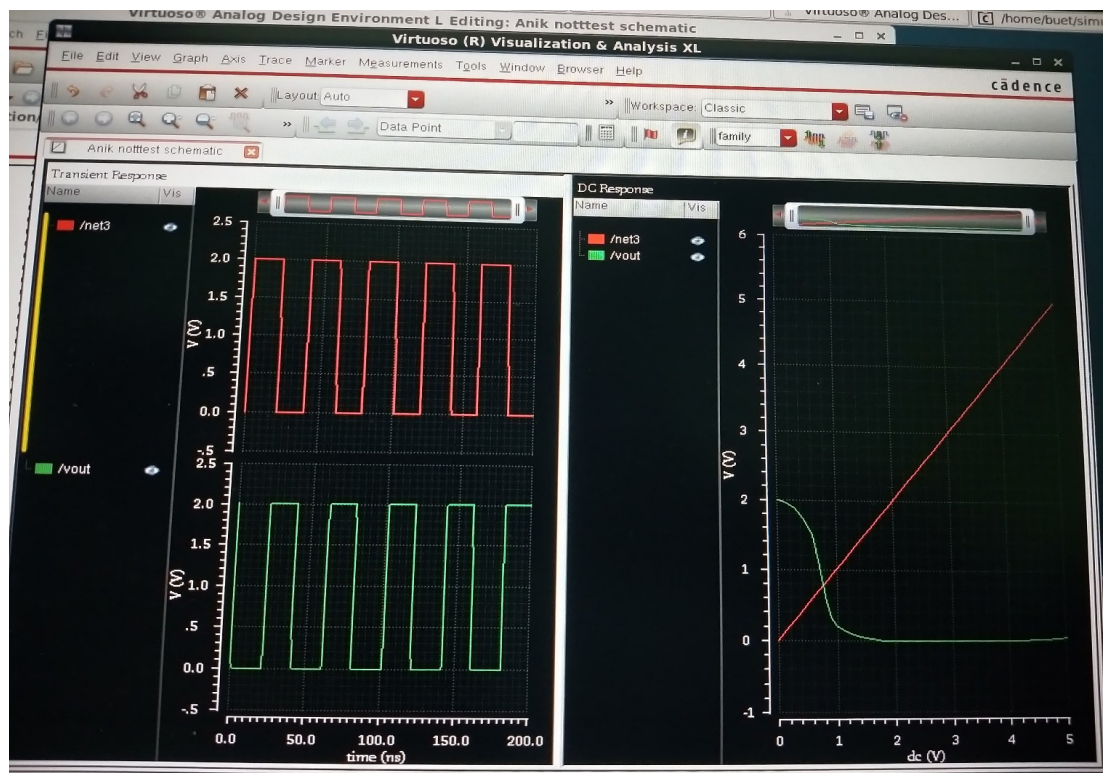
## Circuit diagram:



## TEST SCHEMATIC FOR RIPPLE CARRY ADDER:



## OUTPUT WAVEFORM:



## **NMOS OR GATE:**

An NMOS OR gate is a digital logic gate that performs the logical OR operation using NMOS transistors. In a typical OR gate, the output is high (1) if at least one of the inputs is high (1). The NMOS OR gate uses NMOS transistors arranged in a particular configuration to achieve this behavior.

### **Structure of NMOS OR Gate:**

To construct an NMOS OR gate, two NMOS transistors are connected in parallel, as shown below:

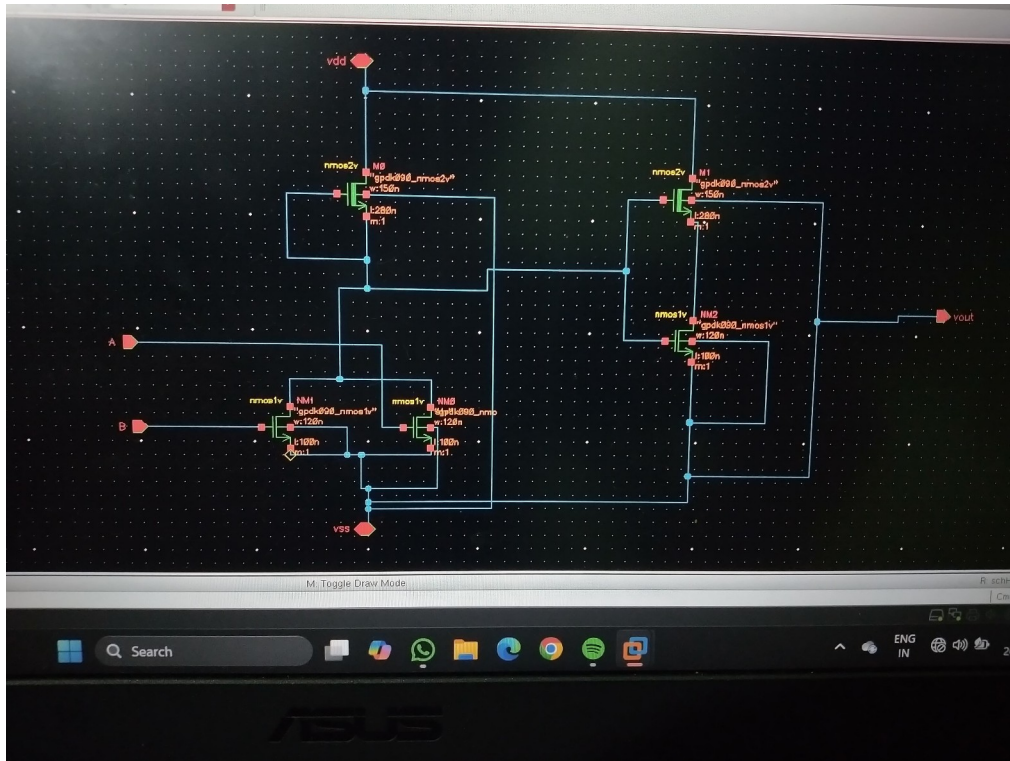
1. Inputs (A and B) are applied to the gates of the two NMOS transistors.
2. The source of both transistors is connected to ground (GND).
3. The drains of the two transistors are connected together to form the output (Y).
4. A pull-up resistor is connected between the output and the positive supply voltage  $V_{dd}$  to ensure the output is pulled high when both NMOS transistors are off.

### **Working of the NMOS OR Gate:**

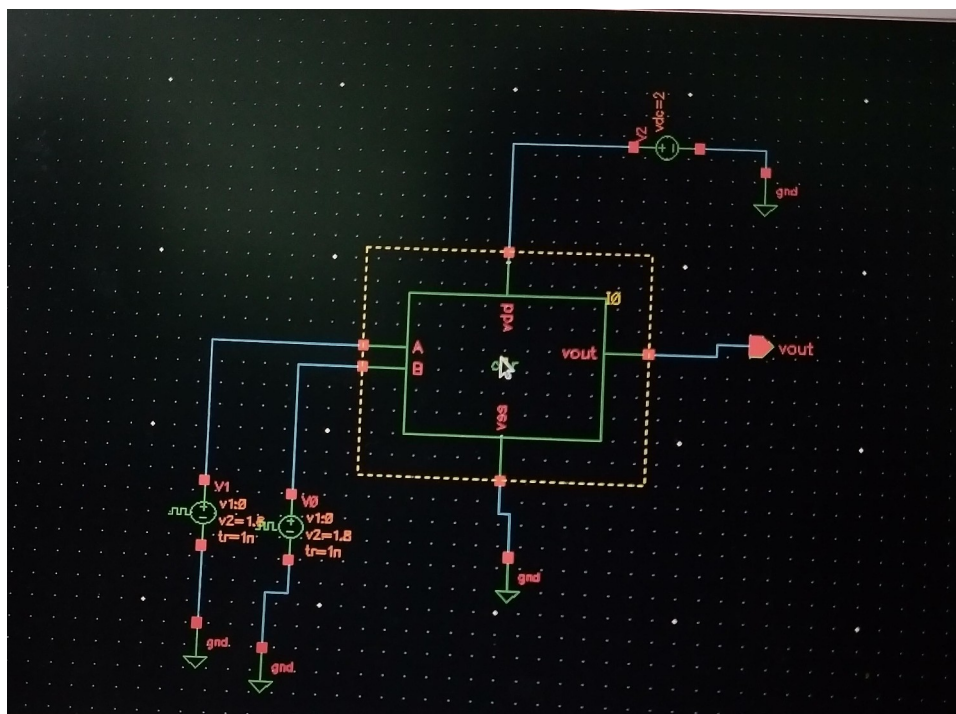
- When both inputs A and B are low (0):
  - Both NMOS transistors are off because the gate-source voltage ( $V_{GS}$ ) is below the threshold voltage ( $V_{th}$ ).
  - The pull-up resistor pulls the output to high (1), so  $Y = 1$ .
- When either A or B is high (1):
  - If input A is high (1), the NMOS transistor connected to input A turns on, and if input B is low (0), the other NMOS transistor is off.
  - The output is pulled to ground (0) through the conducting NMOS transistor, so  $Y = 0$ .
- When both inputs A and B are high (1):
  - Both NMOS transistors turn on because  $V_{GS}$  exceeds the threshold voltage for both inputs.
  - The output is pulled to ground (0), so  $Y = 0$ .



### Circuit diagram:

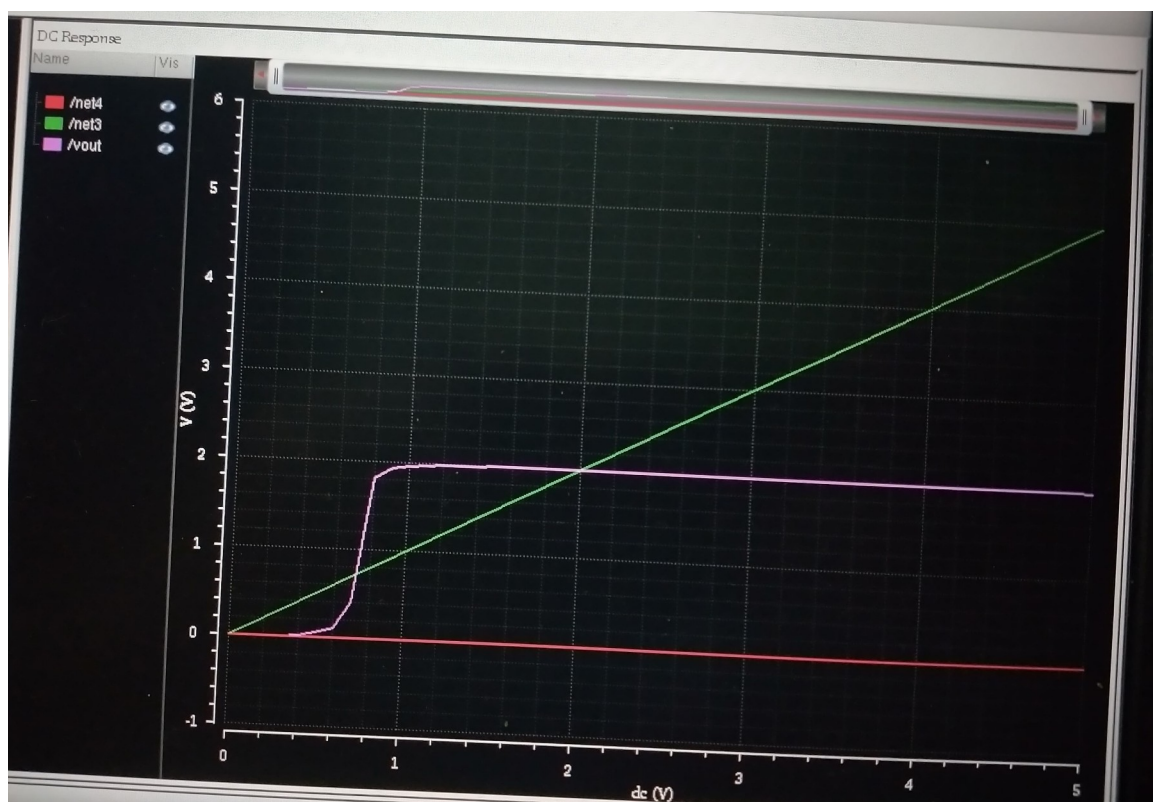
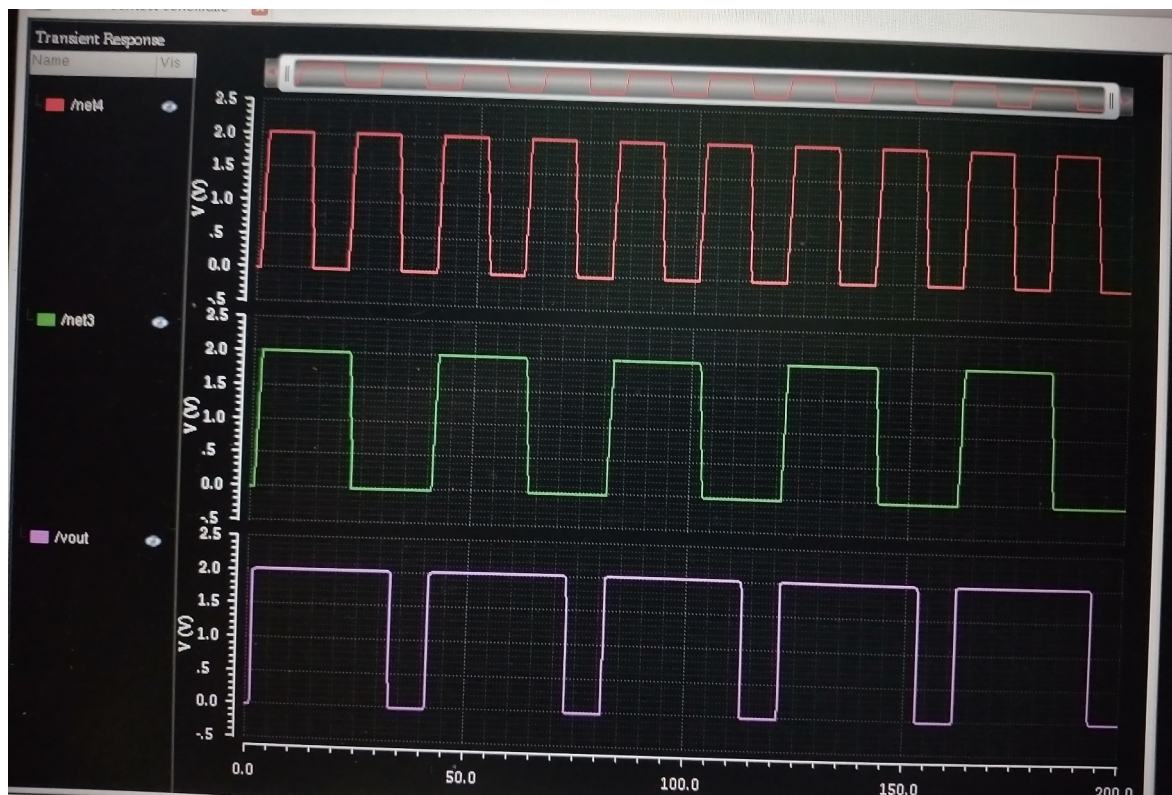


### TEST SCHEMATIC FOR RIPPLE CARRY ADDER:





## OUTPUT WAVEFORM:



## **NMOS AND GATE:**

An NMOS AND gate is a basic digital logic gate that performs the logical AND operation using NMOS transistors. The output of an AND gate is high (1) only when both of its inputs are high (1). In an NMOS-based AND gate, NMOS transistors are arranged in a series configuration.

### **Structure of NMOS AND Gate:**

1. Two NMOS Transistors: The two input signals (A and B) are applied to the gates of two NMOS transistors.
  - The source of both transistors is connected to ground (GND).
  - The drains of the two transistors are connected together to form the output (Y).
2. Pull-up Resistor (R): A pull-up resistor is connected between the output node and the supply voltage ( $V_{dd}$ ) to ensure the output is pulled to a high voltage when both NMOS transistors are off.

### **Working of the NMOS AND Gate:**

The key idea is that NMOS transistors conduct (turn on) when the gate-source voltage ( $V_{GS}$ ) exceeds the threshold voltage ( $V_{th}$ ), creating a low-resistance path to ground. Since the transistors are connected in series, both must be on to pull the output to ground (0).

- When both inputs A and B are low (0):
  - Both NMOS transistors are off because their gate-source voltages ( $V_{GS}$ ) are below the threshold voltage ( $V_{th}$ ).
  - The pull-up resistor pulls the output to high (1).
  - Output  $Y = 1$ .
- When one input is high (1) and the other is low (0):
  - Only one NMOS transistor will be on, and the other will be off.
  - Since the transistors are in series, the output is pulled to high (1) because there is no complete path to ground.
  - Output  $Y = 1$ .
- When both inputs A and B are high (1):

- Both NMOS transistors are on, creating a complete path from the output to ground.
- The output is pulled to ground (0).
- Output  $Y = 0$ .

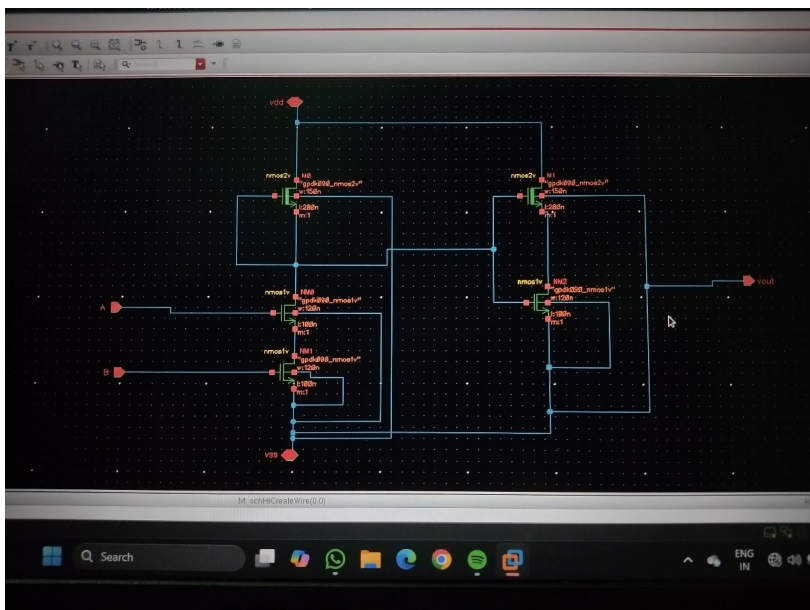
Truth Table for NMOS AND Gate:

Input A	Input B	Output Y
0	0	1
0	1	1
1	0	1
1	1	0

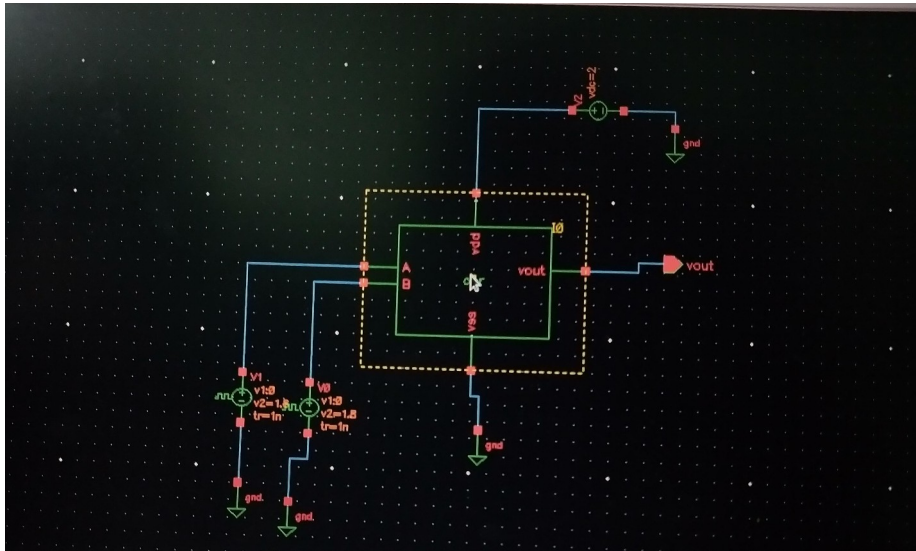
Explanation of the Truth Table:

- When both inputs are low (0), both NMOS transistors are off, and the pull-up resistor pulls the output to high (1).
- When one input is high (1) and the other is low (0), one NMOS transistor is off, and the other is on. Since the transistors are in series, the output stays high (1).
- When both inputs are high (1), both NMOS transistors are on, providing a low-resistance path to ground and pulling the output to low (0).

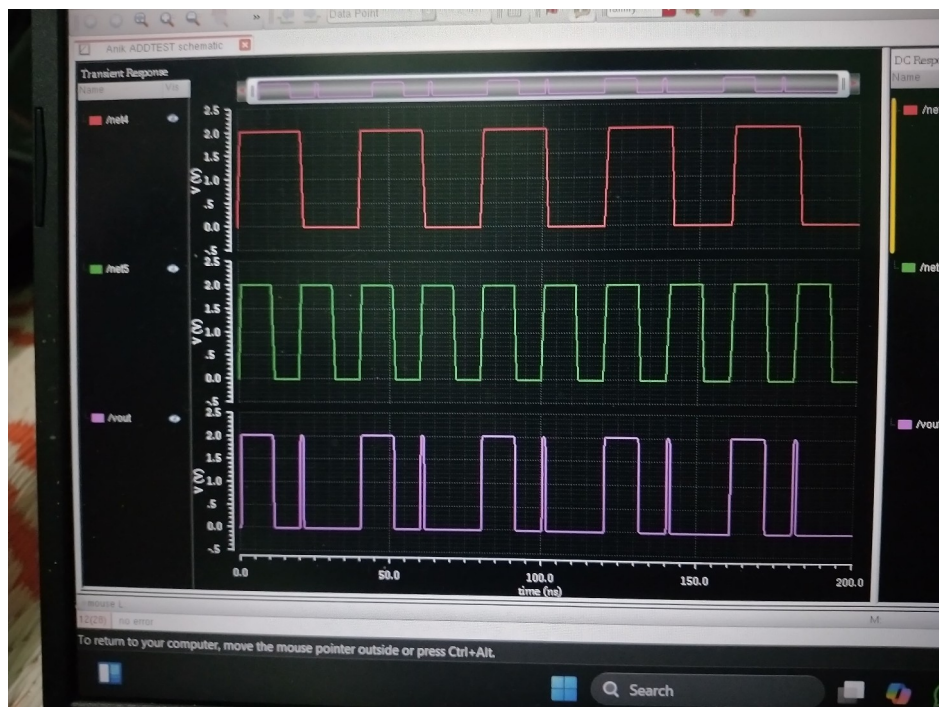
### Circuit diagram:



## TEST SCHEMATIC FOR RIPPLE CARRY ADDER:



## OUTPUT WAVEFORM:



## **CONCLUSION:**

In conclusion, NMOS AND, OR, and Inverter gates are fundamental building blocks in digital logic design, each serving crucial roles in basic logic operations. The NMOS inverter provides a simple way to invert an input signal, but it requires a pull-up resistor and has limitations in driving high output levels, making it less efficient compared to CMOS inverters. The NMOS AND gate utilizes two NMOS transistors in series to perform the AND operation, but its reliance on a pull-up resistor and its inability to drive high output levels make it less suitable for high-performance applications. Similarly, the NMOS OR gate, which uses two NMOS transistors in parallel, is simple and fast but suffers from the same limitations as the AND gate in terms of efficiency and output drive. While NMOS logic gates are fast and simple, they are typically less power-efficient and less versatile than CMOS logic gates, which use both NMOS and PMOS transistors. As a result, while NMOS gates are useful in specific applications requiring low complexity, CMOS technology is preferred in modern designs for its superior power efficiency, performance, and scalability.

