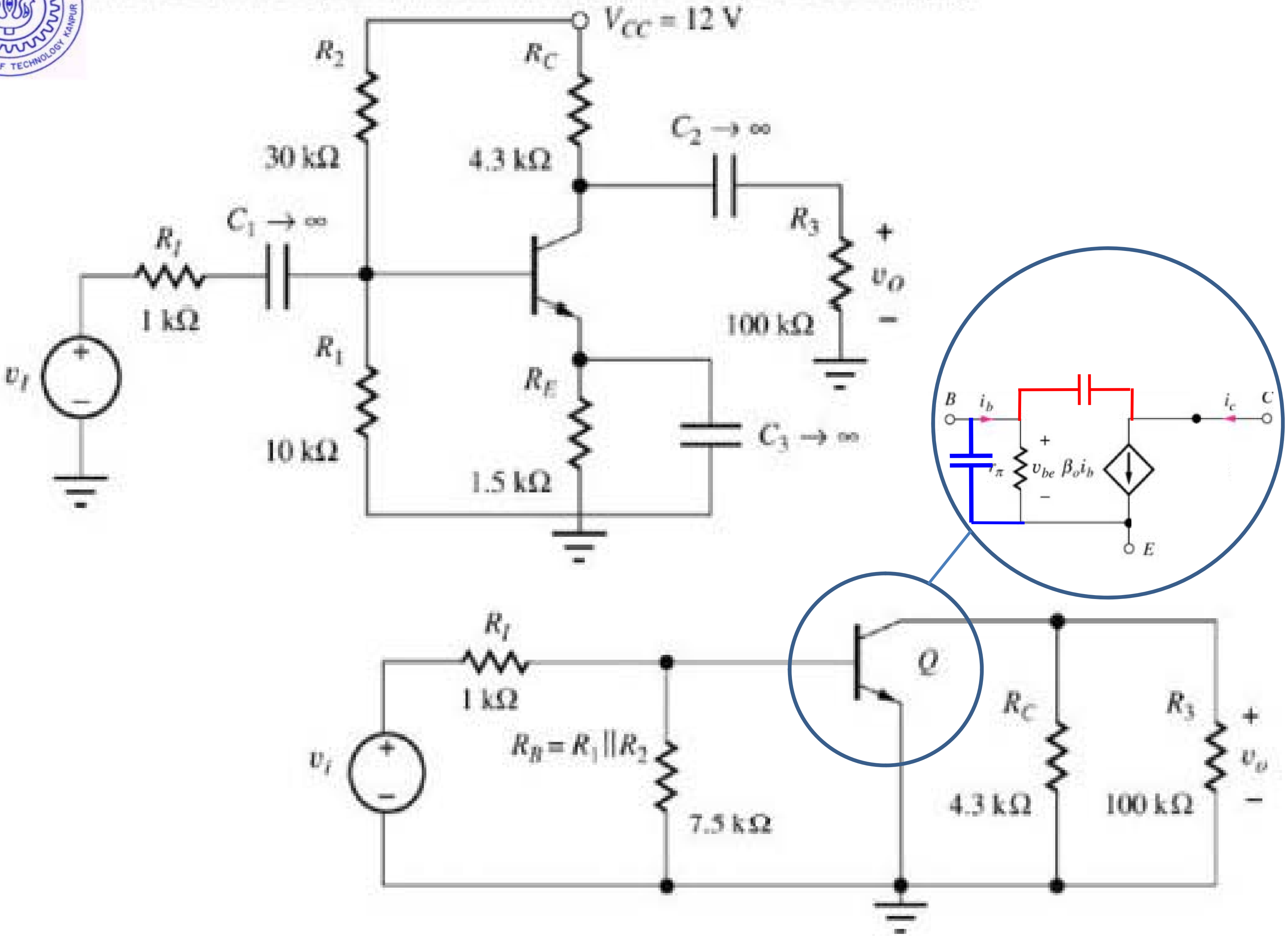
ESc201, Lecture 21: BJT Amplifier (Small signal Model & frequency response)



C-E Amplifier Voltage Gain with R_E: Example

Problem: Calculate voltage gain, Given data:

β_F =100, $V_A = \infty$, Q-point is (1.45mA, 3.41V), R_1=10 kΩ, R_2=30kΩ, R_3=100kΩ, R_C= 4.3kΩ,

R_i =1kΩ, R_E= 1.5kΩ, V_T=25mV.

Assumptions: Transistor is in active region, $\beta_O = \beta_F$.

Signals are low enough to be considered small signals.

Analysis:

$$g_m = 40 I_C = 40(1.45\text{mA}) = 58.0\text{mS} \qquad R_B = R_1 \| R_2 = 7.5\text{k}\Omega$$

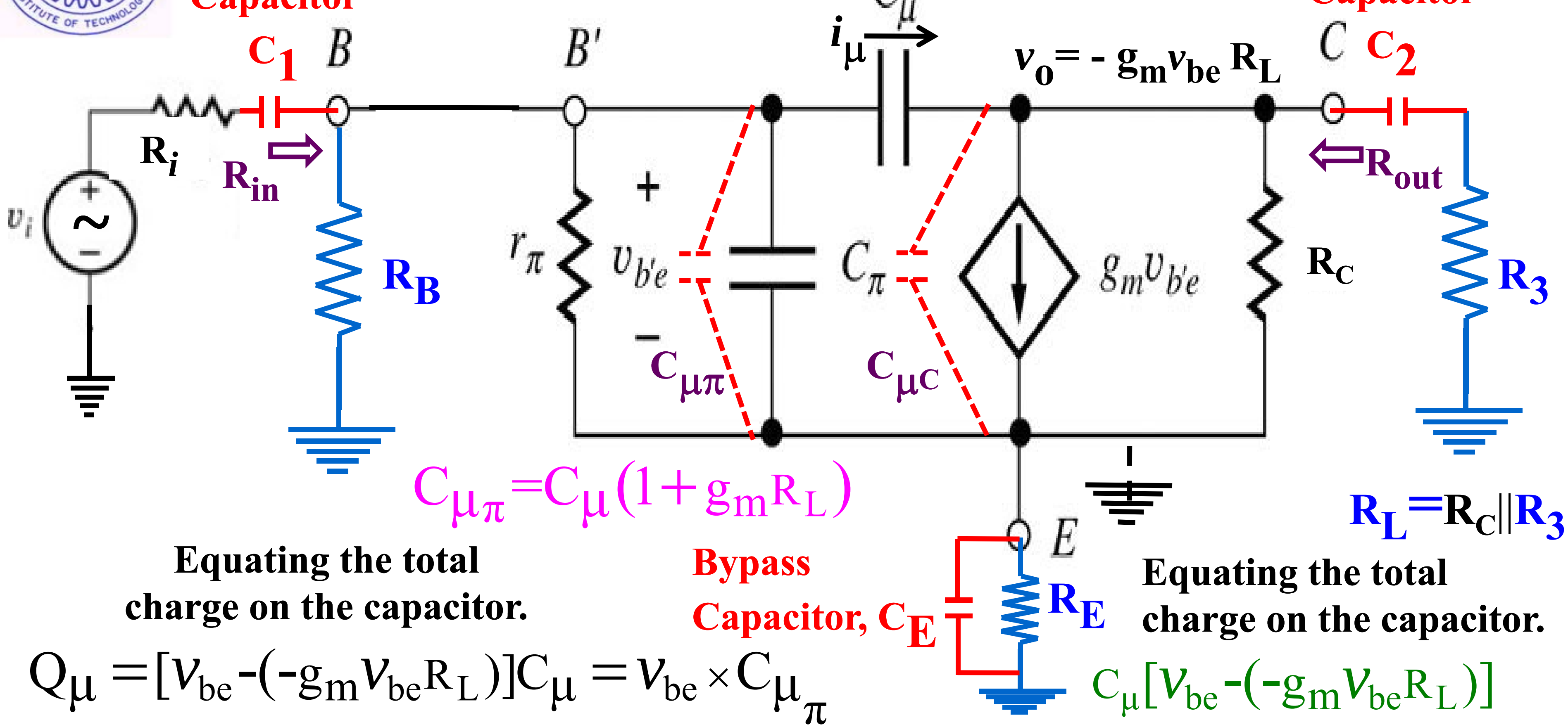
$$R_L = R_C \| R_3 = 4.123\text{k}\Omega \qquad A_v = -g_m R_L \left[\frac{R_B \| r_\pi}{R_i + (R_B \| r_\pi)}\right] = -130 = 42.3\text{dB}$$

Absolutely no change in the voltage gain as long as C_E is a short at the frequency of interest

$$v_i \le (0.005\text{V})\left[\frac{R_i + (R_B \| r_\pi)}{(R_B \| r_\pi)}\right] = 8.57\text{mV}$$

But if C_E is removed then calculate to check that the new $A_{v_{new}} = A_{v_{old}}/(1+g_m R_E)$

ESc201, Lecture 21: BJT Amplifier (frequency response)



$$C_{\mu\pi} = C_\mu (1 + g_m R_L)$$

$R_L = R_C || R_3$

Equating the total charge on the capacitor.

$$Q_\mu = [v_{be} - (-g_m v_{be} R_L)] C_\mu = v_{be} \times C_{\mu_\pi}$$

The equivalent capacitor at B' is increased by a factor of $(1+g_m R_L)$.

$C_\pi >> C_\mu$ but $C_{\mu\pi} >> C_\pi$. Therefore $C_{in} \approx C_{\mu\pi}$.

Equating the total charge on the capacitor.

$$C_\mu [v_{be} - (-g_m v_{be} R_L)]$$

$$= C_{\mu_C} [v_{be} - (-g_m v_{be} R_L) - v_{be}]$$

$$v_{be} C_\mu (1 + g_m R_L) = v_{be} C_{\mu_C} g_m R_L$$

A full calculation gives, but the last term ~ 1, so $g_m R_L$ dominates.

$$C_{\mu\pi} = C_\mu \left(1 + g_m R_L + \frac{R_L}{r_\pi || R_B || R_i}\right)$$

$$C_{\mu C} = C_\mu \frac{(1 + g_m R_L)}{g_m R_L} \cong C_\mu$$

$$C_{\mu C} << C_{\mu\pi}$$

For further reference check: Sedra & Smith, Microelectronic Circuits, Oxford publishers.

ESc201, Lecture 21: BJT Amplifier (Small signal Model frequency response)

At LOW frequencies $C_{\mu\pi}$ and $C_{\mu C}$ may be considered to be open and the at mid band of frequencies R_E is also shorted by C_E. And load is only resistive.

$$A_v(s)=\frac{V_o(s)}{V_i(s)}=A_{mid}F_L(s) \qquad A_{mid}=-g_mR_L\frac{R_B\|r_\pi}{R_i+R_B\|r_\pi}$$

The low frequency response can be calculated to be:

$$F_L(s)=\frac{s \times (s+(1/C_ER_E)) \times s}{\left(s+\frac{1}{C_1(R_i+R_B\|r_\pi)}\right)\left(s+\frac{1}{C_E\left[(1/g_m)\|R_E\right]}\right)\left(s+\frac{1}{C_2(R_C+R_3)}\right)}$$

The three zero locations are:

$s = 0$, 0, and $-1/(R_EC_E)$.

$$\omega_L \cong \sum_{i=1}^{n}\frac{1}{R_{i_{Short}}C_i},$$

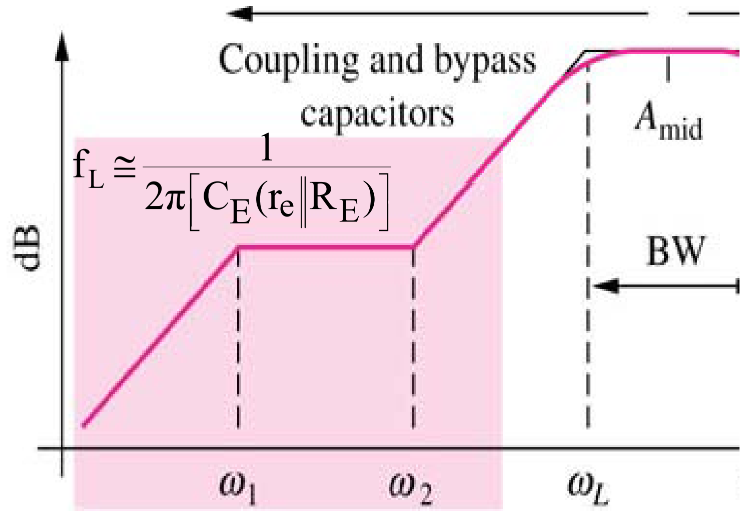
R_{i_s} is the resistance seen by C_i when other capacitances are shorted.

$(s+(1/C_ER_E))$ zero is far away from unity gain freq. and need not be considered.

The three pole locations are: $s=-\frac{1}{C_1(R_i+R_B\|r_\pi)},\ -\frac{1}{C_E\left[(1/gm)\|R_E\right]},\ -\frac{1}{C_2(R_C+R_3)}$

Each independent capacitor in the circuit contributes one pole and one zero. Series capacitors C_1 and C_2 contribute the two zeros at $s = 0$ (dc), blocking propagation of dc signals through the amplifier. Third zero due to parallel combination of C_E and R_E occurs at frequency where signal current propagation through BJT is blocked (becomes the dominant zero). C_E is usually the largest capacitor (~ few μF) and R_E is the smallest (< 0.5kΩ). C_1 & C_2 ~ 0.5-1μF. R_i <1kΩ, R_B ~10s of kΩ, r_π ~1-5 kΩ.

Note $1/g_m = r_e$ ~ 10s of Ω.



At HIGH frequencies C_1, C_2 and C_E may be considered to be shorted and the load is only resistive. Then it is easy to show that the only detrimental capacitance is $C_{in} = C_\pi + C_{\mu\pi}$ and $C_{\mu C} \approx C_\mu$. But C_μ being small, will not provide the upper cut-off.

$$A_v(s) = \frac{V_o(s)}{V_i(s)} = A_{mid} F_H(s) \qquad F_H(s) = \frac{1}{\left(1 + sC_{in}(R_i + R_B \| r_\pi)\right)} \qquad C_{in} = C_\pi + C_\mu(1 + g_m R_L)$$

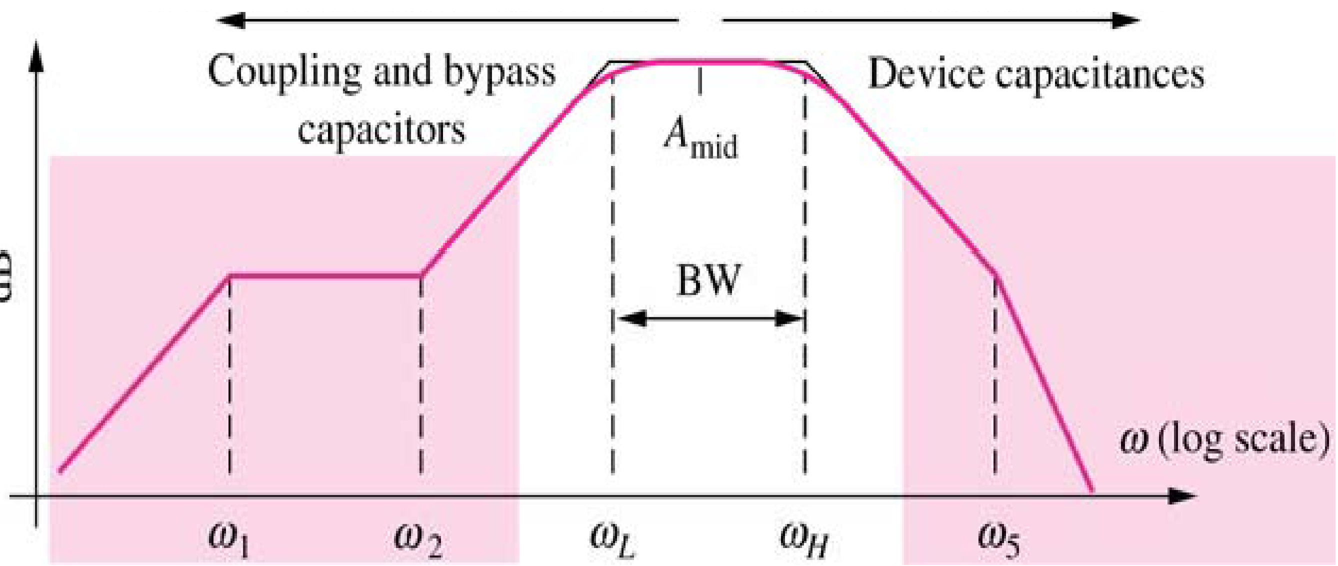
$$\omega_H \cong \frac{1}{R_i \| R_B \left(\frac{C_\pi}{1 + g_m R_E}\left(1 + \frac{R_E}{R_i \| R_B}\right) + C_\mu \left(1 + \frac{g_m R_L}{1 + g_m R_E} + \frac{R_L}{R_i \| R_B}\right)\right)} \cong \sum_{i=1}^{m} \frac{1}{R_{i_{Open}} C_i}$$

$R_{i_{Open}}$ is the resistance seen by C_i when other capacitances are opened.

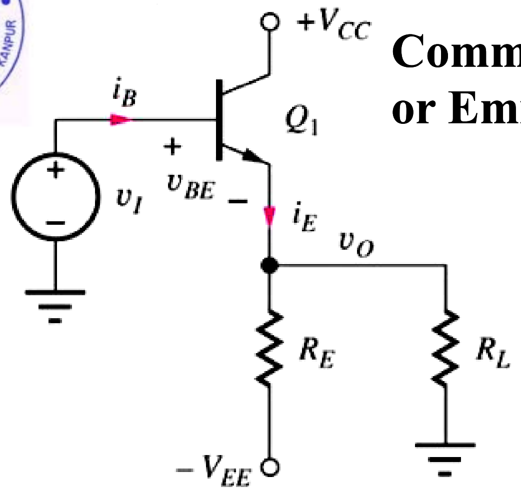
In general for n-poles and n-zeros

$$\omega_L \cong \sqrt{\sum_{i=1}^{n} \omega_{p_n}^2 - 2 \sum_{i=1}^{n} \omega_{z_n}^2}$$

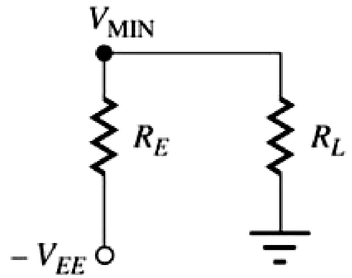
If dominant poles do not exist one need to do the full calculaion.



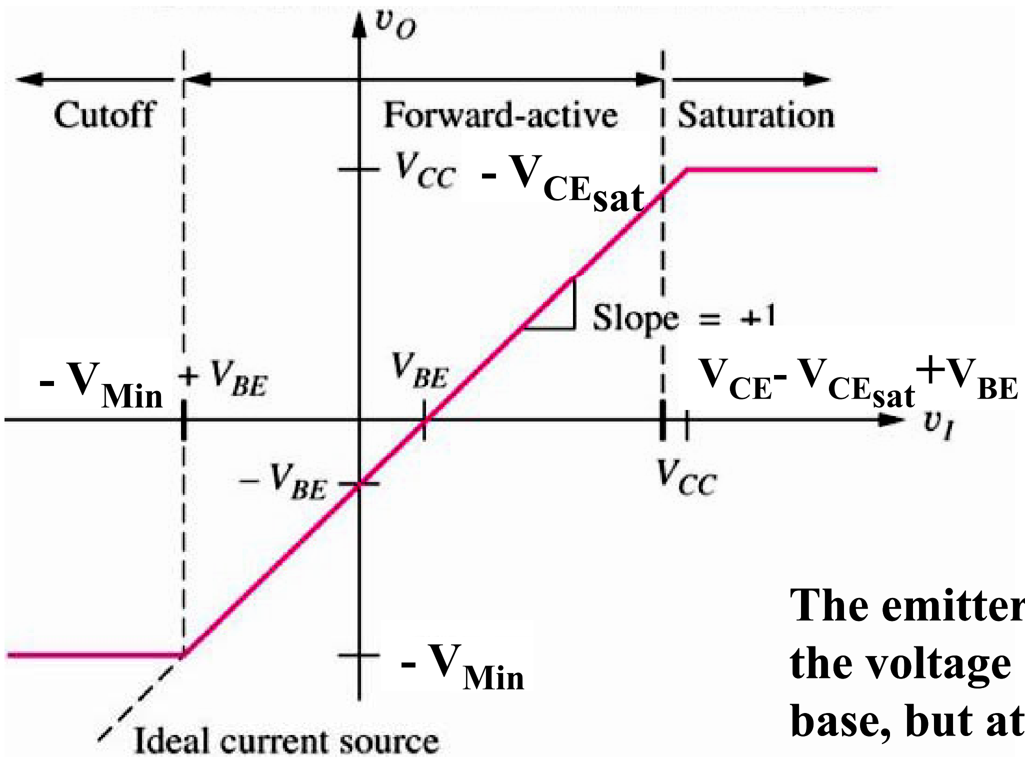
ESc201, Lecture 21: BJT Logic Circuits (ECL) Emitter Coupled Logic



Common Collector (CC) or Emitter Follower.



1. **Bipolar switch circuits**
2. **Emitter-coupled logic (ECL)**
3. Behavior of the bipolar transistor as a saturated switch
4. Transistor-transistor logic (TTL)
5. **Schottky clamping techniques for preventing saturation**
6. Operation of the transistor in the inverse-active region
7. Voltage reference design
8. **BiCMOS logic circuits**

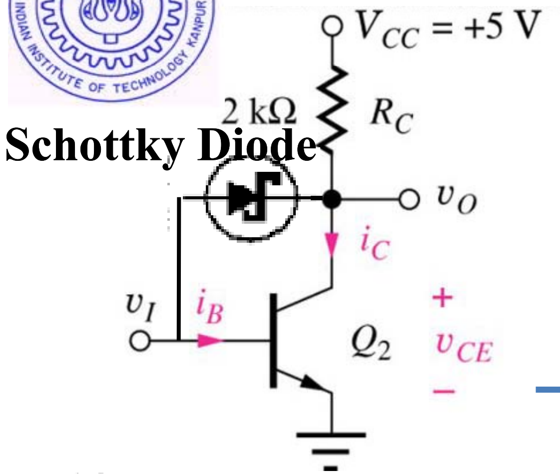


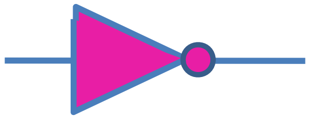
$$V_{Min} = \frac{R_L}{R_L + R_E}(-V_{EE})$$

The emitter follower (CC-BJT) is called such since the voltage at the emitter follows the votlage at the base, but at an offset which can be seen in the ideal Voltage Transfer Characteristic.

ESc201, Lecture 21: BJT Logic Circuits (Saturating Bipolar Inverter)

- One of the most basic circuits for BJT logic gates is the saturating bipolar inverter
- The resistor pull the output high when v_i is low, and the output goes to v_{CE} when v_i is high





β_F=20, β_R=0.1, $V_{CE_{sat1}}$=0.4V, $V_{CE_{sat2}}$=0.2V, V_T=26mV

$V_{IL} \cong 0.7\text{-}V_{CE_{Sat1}} = 0.66\text{V}$, $V_{OH} \cong V_H - V_T \cong V_H = 5\text{V}$

$V_{IH} \cong V_{BE2} = 0.8\text{V}$, $V_{OL} \cong V_L = V_{CE_{Sat2}} = 0.2\text{V}$

$NM_L \cong 0.66\text{-}0.15 = 0.51\text{V}$, $NM_H \cong 5.0\text{-}0.8 = 4.2\text{V}$