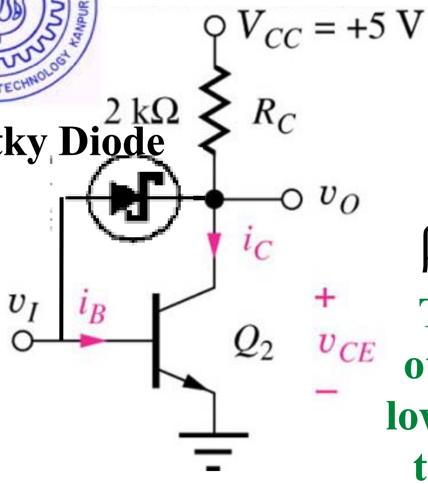
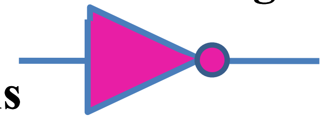
ESc201, Lecture 22: BJT Logic Circuits (Saturating Bipolar Inverter)

LECTURE 21 contd.

Schottky Diode



- One of the most basic circuits for BJT logic gates is the Saturating Bipolar Inverter



- Can be configured in various topologies to produce digital gates: *AND, OR, NAND, NOR, etc.*

$\beta_F = 20$, $\beta_R = 0.1$, $V_{CE_{sat1}} = 0.4V$, $V_{CE_{sat2}} = 0.2V$, $V_T = 26mV$

The resistor pull the output high when v_i is low, and the output goes to v_{CE} when v_i is high

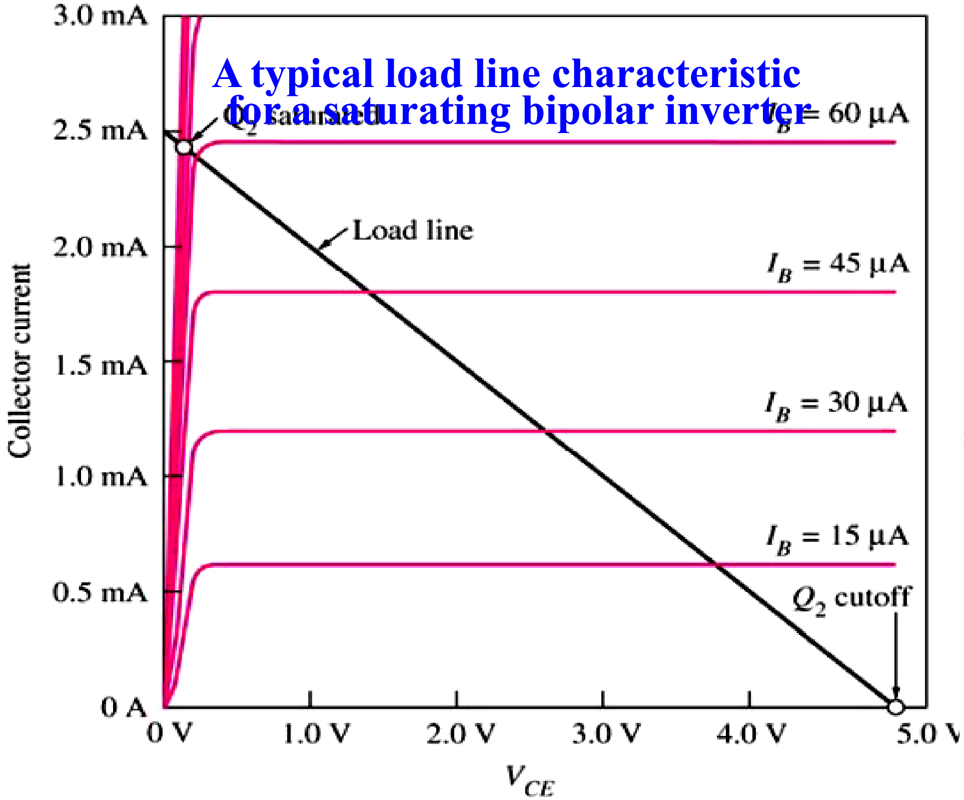
Any logic can be built with either NAND or NOR gates.

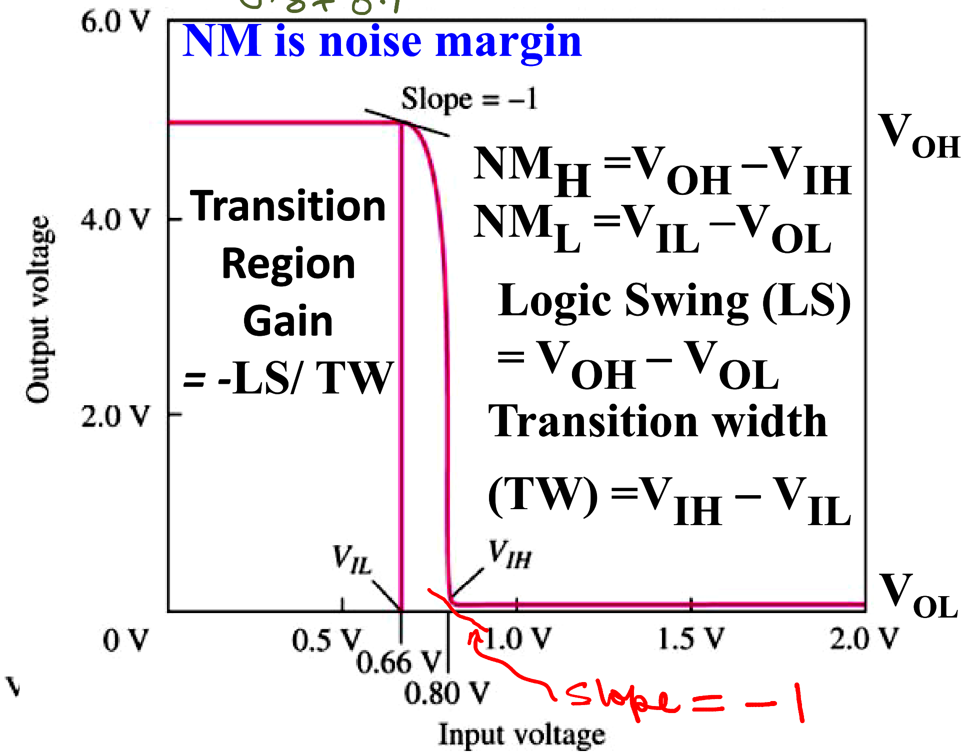
$V_{IL} \cong 0.7 - V_{CE_{Sat1}} = 0.66V$, $V_{OH} \cong V_H - V_T \cong V_H = 5V$

$V_{IH} \cong V_{BE2} = 0.8V$, $V_{OL} \cong V_L = V_{CE_{Sat2}} = 0.2V$

$NM_L \cong 0.66 - 0.15 = 0.51V$, $NM_H \cong 5.0 - 0.8 = 4.2V$

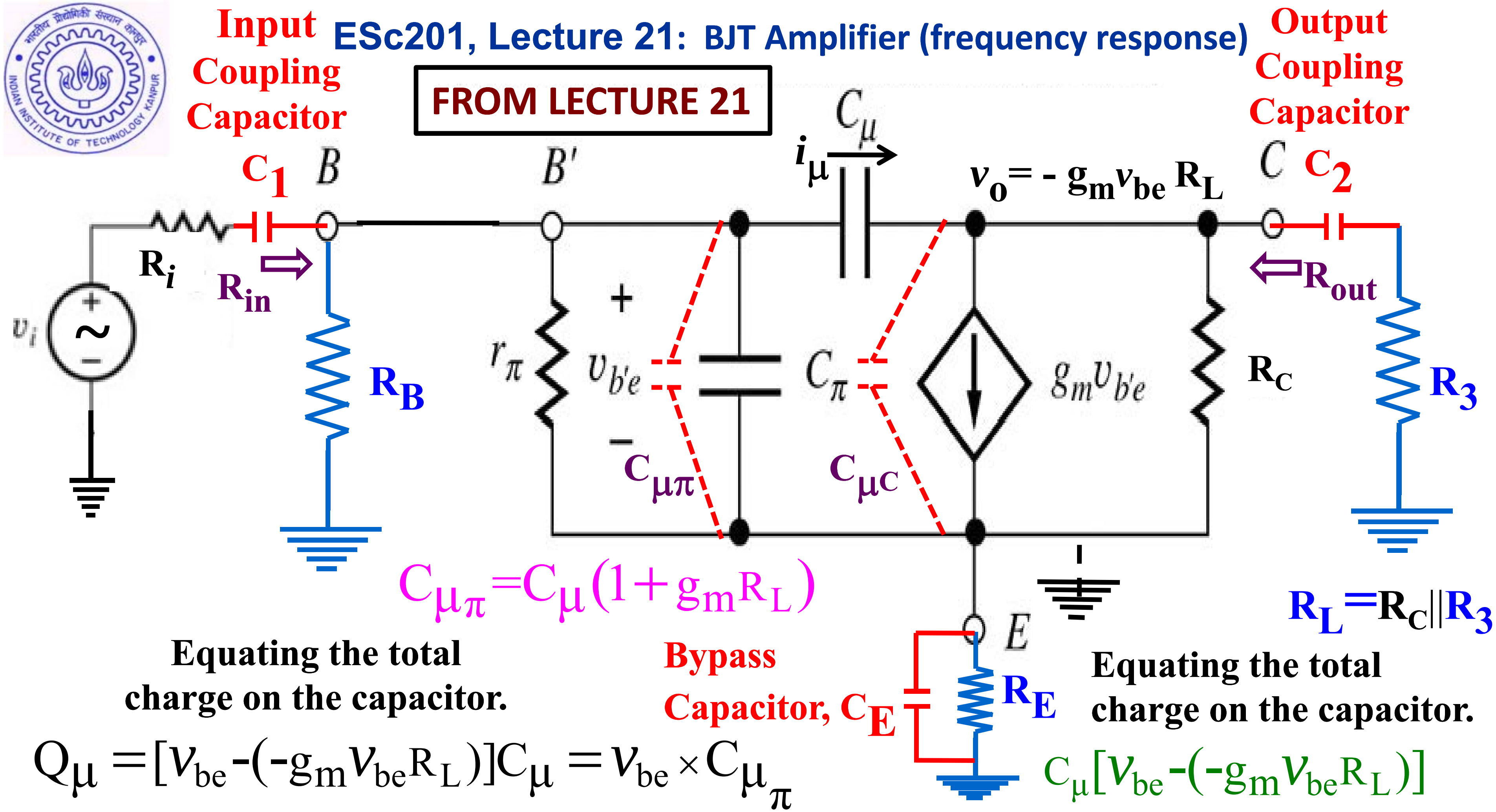
0.8 + 0.7





ESc201, Lecture 21: BJT Amplifier (frequency response)

FROM LECTURE 21



$$C_{\mu\pi}=C_{\mu}(1+g_mR_L)$$

$R_L = R_C || R_3$

Equating the total charge on the capacitor.

$$Q_{\mu}=[v_{be}-(-g_m v_{be}R_L)]C_{\mu}=v_{be}\times C_{\mu_{\pi}}$$

The equivalent capacitor at B' is increased by a factor of $(1+g_mR_L)$.

$C_{\pi} >> C_{\mu}$ but $C_{\mu\pi} >> C_{\pi}$. Therefore $C_{in} \approx C_{\mu\pi}$.

A full calculation gives $C_{\mu\pi}=C_{\mu}\left(1+g_mR_L+\dfrac{R_L}{r_{\pi}||R_B||R_i}\right)$

Equating the total charge on the capacitor.

$$C_{\mu}[v_{be}-(-g_m v_{be}R_L)]$$

$$=C_{\mu_C}[v_{be}-(-g_m v_{be}R_L)-v_{be}]$$

$$v_{be}C_{\mu}(1+g_mR_L)=v_{be}C_{\mu_C}g_mR_L$$

$$C_{\mu C}=C_{\mu}\frac{(1+g_mR_L)}{g_mR_L}\cong C_{\mu}$$

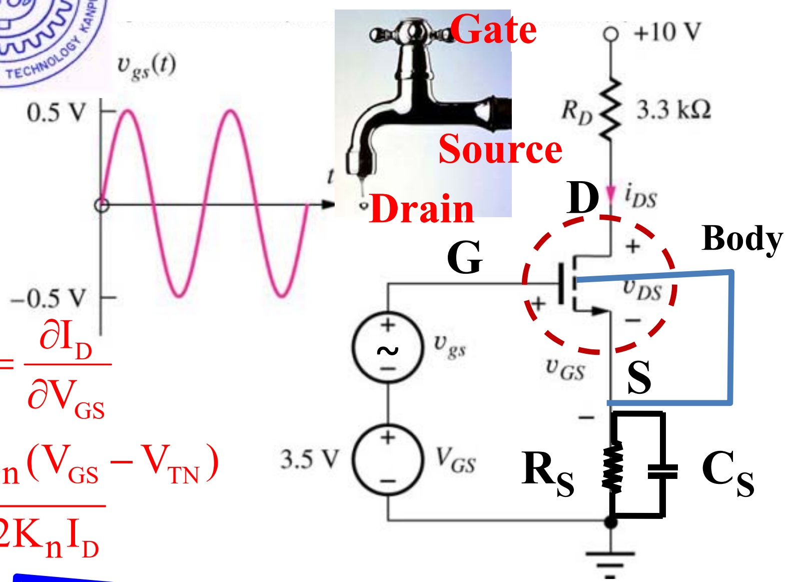
$$C_{\mu C} << C_{\mu\pi}$$

For further reference check: Sedra & Smith, Microelectronic Circuits, Oxford publishers.

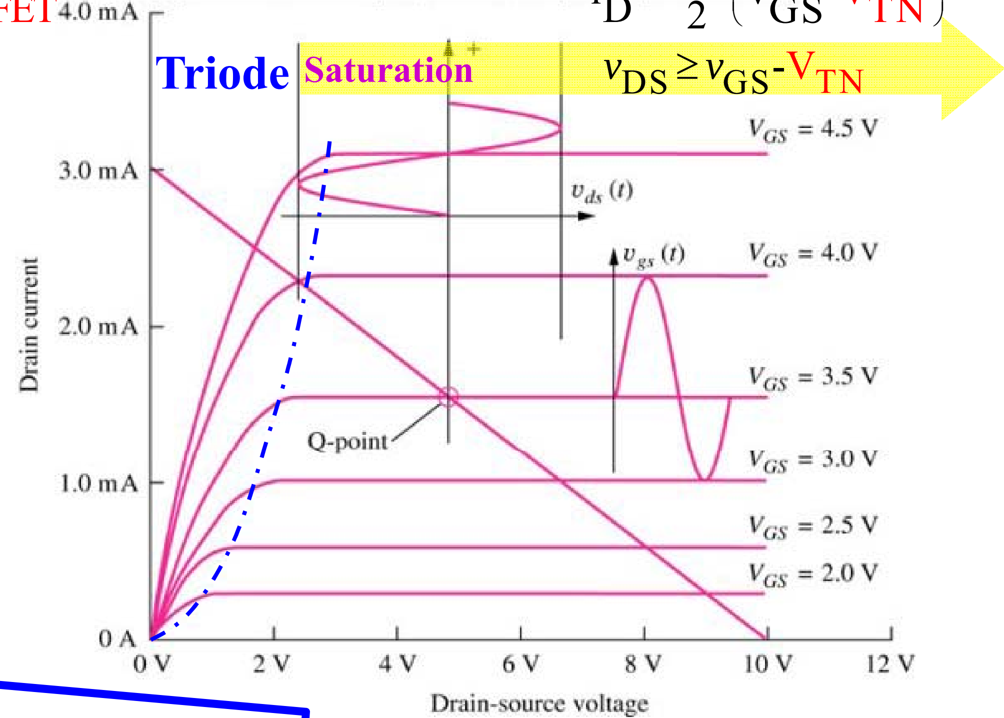
ESc201, Lecture 22: MOSFET Common Source (CS) Amplifier

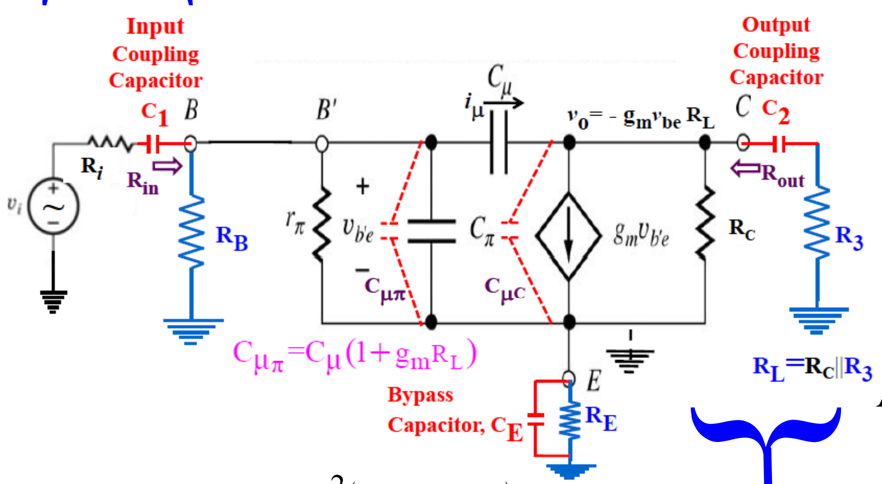
$V_{TN} \equiv$ Threshold voltage of n-Channel MOSFET

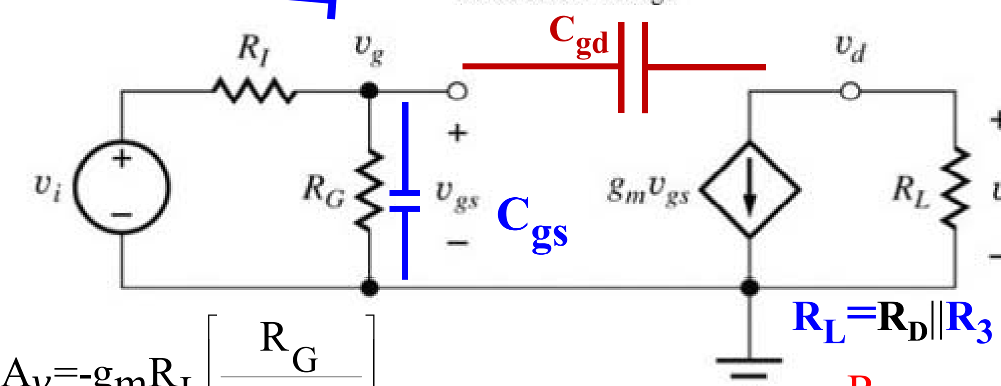
$$i_D = \frac{K_n}{2}\left(v_{GS} - V_{TN}\right)^2$$



$$g_m = \frac{\partial I_D}{\partial V_{GS}} = K_n\left(V_{GS} - V_{TN}\right) = \sqrt{2K_n I_D}$$







$R_L = R_D \| R_3$

$$A_V = -g_m R_L \left[\frac{R_G}{R_i + R_G}\right]$$

$$A_{mid} = -g_m\left(R_3 \| R_D\right)\frac{R_G}{R_G + R_i}$$

$$F_L(s) = \frac{s^2\left(s + (1/C_S R_S)\right)}{\left(s + \frac{1}{C_1(R_i + R_G)}\right)\left(s + \frac{1}{C_S\left[(1/g_m)\|R_S\right]}\right)\left(s + \frac{1}{C_2(R_D + R_3)}\right)}$$

The three zero locations are: $s = 0, 0, -1/(R_S C_S)$.

The three pole locations are: $s = -\frac{1}{C_1(R_i + R_G)}, -\frac{1}{C_3\left[(1/g_m)\|R_S\right]}, -\frac{1}{C_2(R_D + R_3)}$

ESc201, Lecture 22: Amplifier OpAmp

The frequency at which the magnitude of the gain becomes unity (i.e., 0dB) is known as the -*Unity-gain cut-off frequency* (f_T)

$In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ Pseudomorphic HEMT $f_{H(3dB)}$=740GHz & f_T=1.04THz.

100nm Gate length InGaAs/InAlAs HEMT MIMIC technology: 1–157 GHz Bandwidth with 5dB gain (today's Snapdragon Silicon chip is of 7nm Gate length)

InGaAs–InP HBT Differential Transimpedance Amplifier with 47-GHz Bandwidth

SiGe HBTs' f_T ~ 0.5THz till 2006, still the best InGaAs HEMT beats it by ~0.2THz.

Not all applications require such high frequency operation and hence at lower frequencies there are better options. Operational Amplifiers (OpAmps) is one such versatile device.

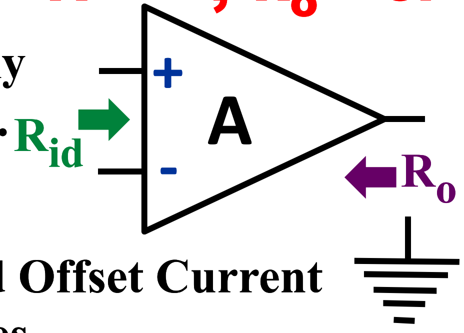
OpAmps are essentially voltage amplifiers which has two inputs. The difference signal is $v_d = v_1 - v_2$ is a *floating signal* (i.e., a signal that is measured between the two input points *none of which may be ground*). The output v_o is always measured with respect to ground.

OpAmps have two inputs for powering the device with a positive supply and ground OR more commonly a positive as well as a negative supply.

Rejects signals common to both inputs → Common-Mode Rejection Ratio (CMRR) [very high CMRR → suppresses noise]

Ideal OpAmp :

$R_{id} \rightarrow \infty$, $A \rightarrow \infty$, $R_o \rightarrow 0$.



The word 'Operational' has stuck as they were earlier used for Analog Computer Operations & the acronym 'OpAmp' remains.

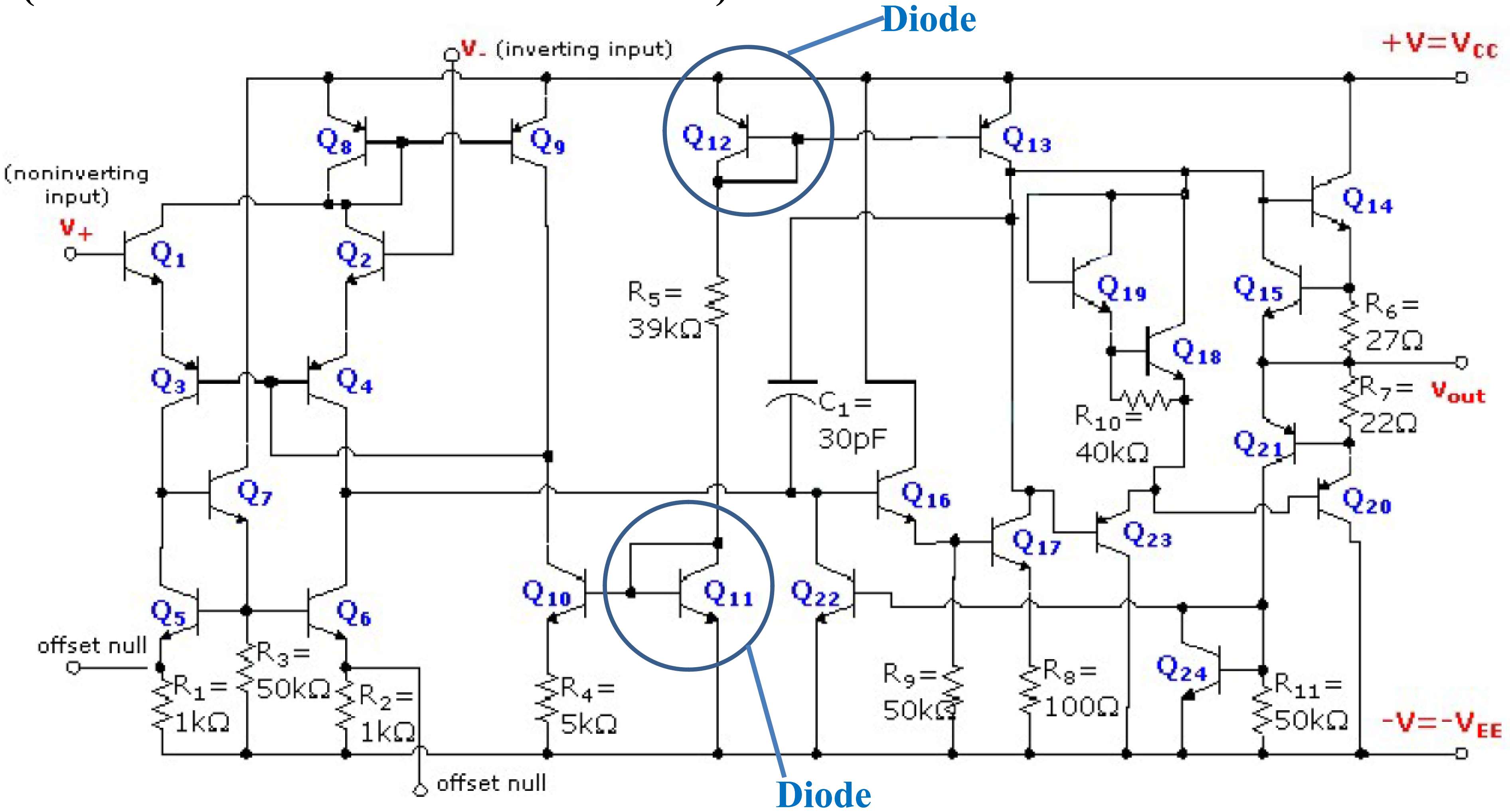
Limitations:

1. Offset Voltage and Offset Current
2. Saturation Voltages
3. Slew Rate: The rate at which the output voltage changes with respect to time.
4. Minimum Allowed Supply Voltage

ESc201, Lecture 22: Operational Amplifier

Representative Circuit internal diagram of a 741 OpAmp Integrated Circuit.
This chip would be handled by you in your laboratory.
Shows the usage of 24 Transistors.

In fact there are many more in the actual circuit used for protection against misuse. (Remember Resistors are avoided in an IC)



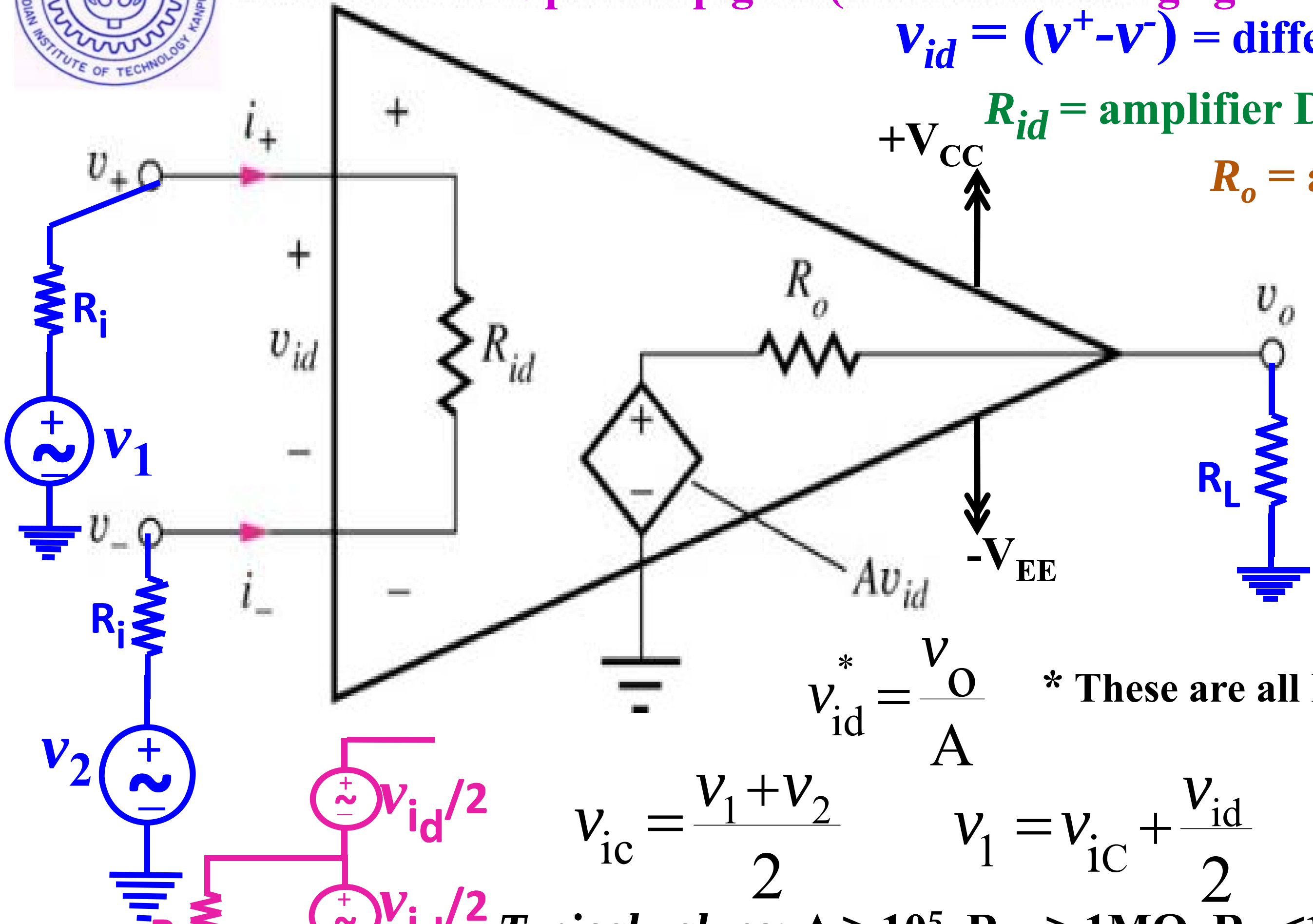
ESc201, Lecture 22: Operational Amplifier

A = Open-loop gain (maximum voltage gain available from the device)

$v_{id} = (v^{+} - v^{-})$ = differential input signal voltage

R_{id} = amplifier Differential Input resistance

R_o = amplifier Output resistance

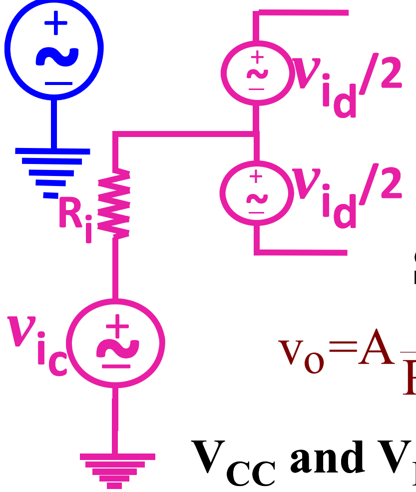


Signal developed at amplifier output is: in phase with the voltage applied at + input (non-inverting) terminal and 180° out of phase with that applied at - input (inverting) terminal.

$$v_{id}^{*} = \frac{v_o}{A}$$

* These are all Phasors

$$\lim_{A\to\infty} v_{id} = 0$$



$$v_{ic} = \frac{v_1 + v_2}{2} \qquad v_1 = v_{iC} + \frac{v_{id}}{2} \qquad v_2 = v_{iC} - \frac{v_{id}}{2}$$

Typical values: $A \geq 10^5$, $R_{in} \geq 1M\Omega$, $R_o \leq 100\ \Omega$, CMRR ≥ 80dB (10^4)

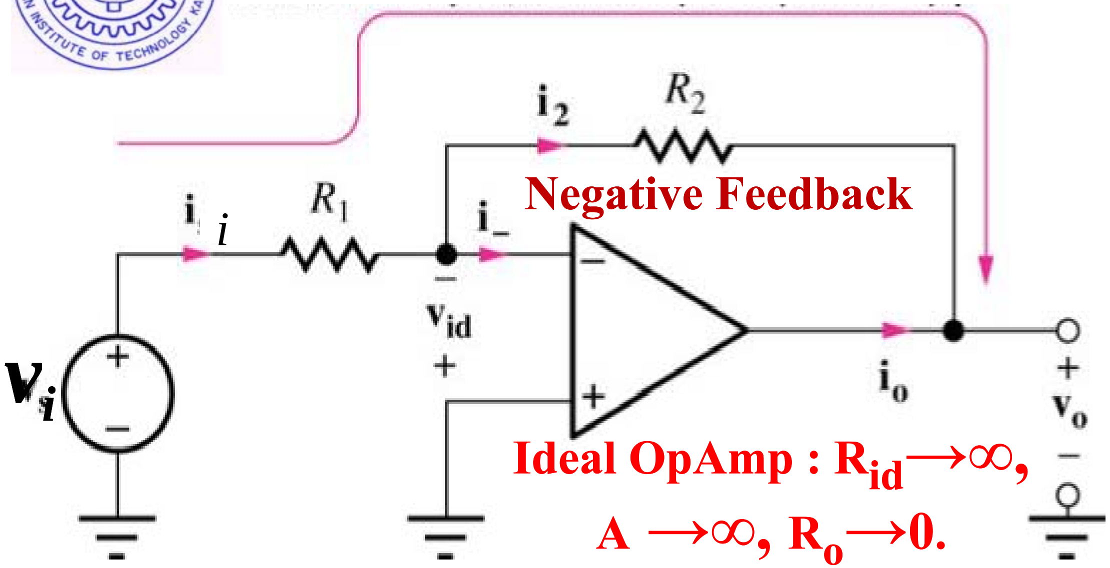
Slew Rate: 0.5-2V/µsec.

$$v_o = A\frac{R_L}{R_o + R_L} v_{id} \qquad v_{id} = v_i \frac{R_{id}}{R_{id} + R_i} \qquad A_{dv} = \frac{v_o}{v_{in}} = \frac{R_{id}}{R_{id} + R_i} \times \frac{R_L}{R_o + R_L}$$

V_{CC} and V_{EE} = ± 3 V (minimum) -- ± 15 V (Typically on the higher side)

Uncompensated Bandwidth 1 MHz ---- Compensated Bandwidth 10 Hz

ESc201, Lecture 22: OpAmp Inverting Amplifier (IDEAL OPAMP)



Ideal OpAmp : $R_{id} \to \infty$, $A \to \infty$, $R_o \to 0$.

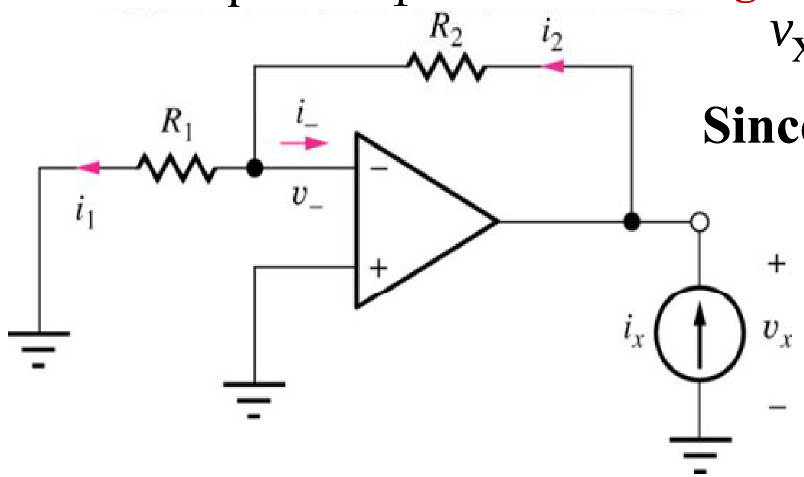
- Negative voltage gain implies 180^0 phase shift between dc/sinusoidal input and output signals.
- Gain greater than 1 if $R_2 > R_1$
- Gain less than 1 if $R_1 > R_2$
- Inverting input of op amp is at ground potential (not connected directly to ground) and is said to be at *Virtual ground.*

$$v_i - i_1 R_1 - i_2 R_2 - v_O = 0$$

But $i_i = i_2$ and $v_- = 0$ (since $v_{id} = v_+ - v_- = 0$) $\quad \therefore i_1 = \dfrac{v_i}{R_1}$

$$\text{and } A_v = \frac{v_O}{v_i} = -\frac{R_2}{R_1}$$

R_{out} is found by applying a test current (or voltage) source to amplifier output and determining the voltage(or current) and turning off all independent sources. Hence, $v_s = 0$



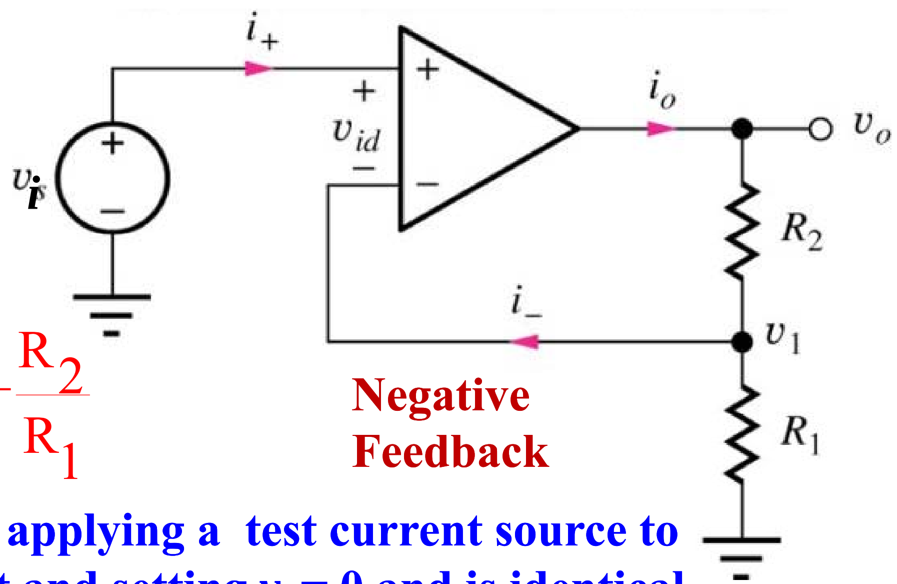
$$v_X = i_2 R_2 + i_1 R_1 \qquad \textbf{But } i_1 = i_2 \qquad \therefore v_X = i_1 (R_2 + R_1)$$

Since $v_- = 0$, $i_1 = 0$ and $v_x = 0$ irrespective of the value of i_x. $\quad \therefore R_{out} = 0$

Therefore, keeping R_2 fixed, reduce R_1 to increase gain (A_v), but that would reduce (R_{in}).

Negative Feedback→Stable System: All disturbances die down automatically.

ESc201, Lecture 22: OpAmp Non-Inverting Amplifier (IDEAL OPAMP)



Since i_-=0 $\quad v_1 = v_o \dfrac{R_1}{R_1+R_2}$

and $\quad v_i - v_{id} = v_1$

But v_{id} =0 $\quad \therefore v_i = v_1$

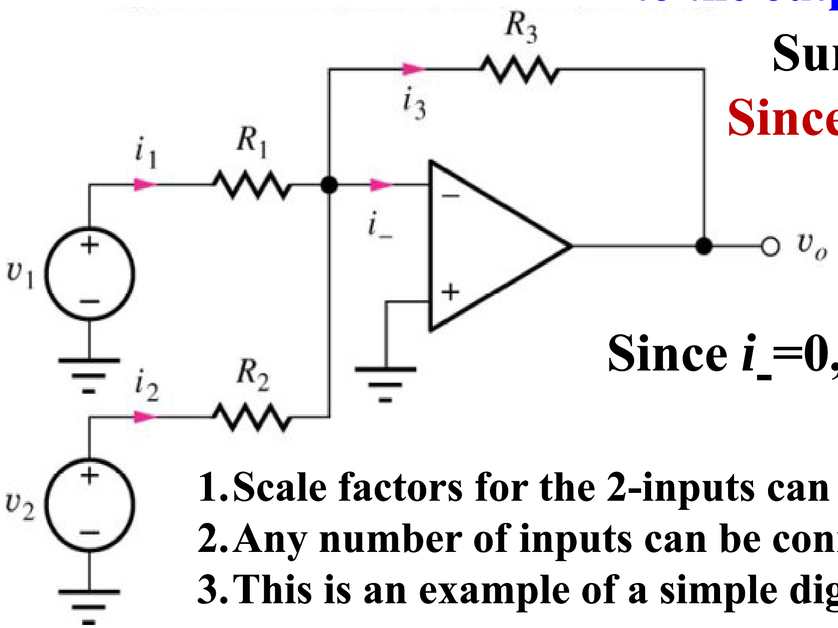
$$v_o = v_i \frac{R_1+R_2}{R_1} \qquad \therefore A_v = \frac{v_o}{v_i} = \frac{R_1+R_2}{R_1} = 1+\frac{R_2}{R_1}$$

Negative Feedback

Since i_+=0 $\quad R_{in} = \dfrac{v_i}{i_+} = \infty$

R_{out} is found by applying a test current source to amplifier output and setting $v_i = 0$ and is identical to the output resistance of inverting amplifier i.e. R_{out} =0

Summing Amplifier



Since negative amplifier input is at virtual ground,

$$i_1 = \frac{v_1}{R_1} \qquad i_2 = \frac{v_2}{R_2} \qquad i_3 = -\frac{v_o}{R_3}$$

Since i_-=0, $i_3 = i_1 + i_2$, $\quad v_o = -\dfrac{R_3}{R_1} v_1 - \dfrac{R_3}{R_2} v_2$

1. **Scale factors for the 2-inputs can be independently adjusted by proper choice of R_2 and R_1.**
2. **Any number of inputs can be connected to summing junction through extra resistors.**
3. **This is an example of a simple digital-to-analog converter.**