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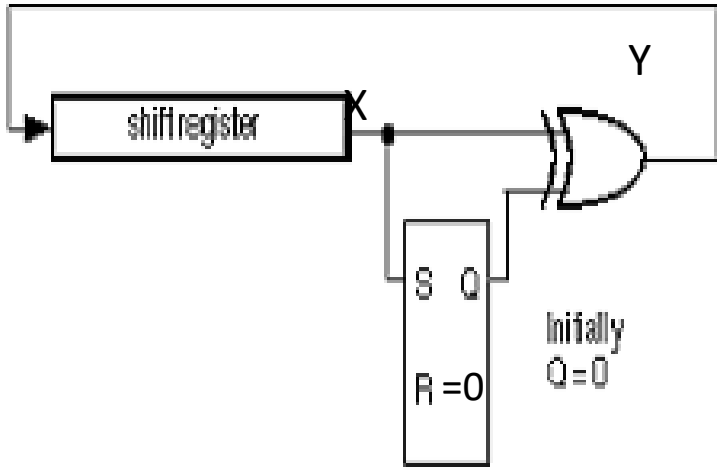
Check if the arguments are correct !!!

Remember that when the clock shifts the register SR-flip-flop also changes state depending on what was stored on its input earlier. So shift and state change happens at the same time.

00101100→(1's Compliment) 11010011 →(2's Compliment) 11010100



X	Q	Y
0	0	0
0	0	0
1	0	1
1	1	0
0	1	1
1	1	0
0	1	1
0	1	1

Inputs		Outputs	
S	R	Present State, Q_n	Next State, Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	invalid	
1	1	invalid	

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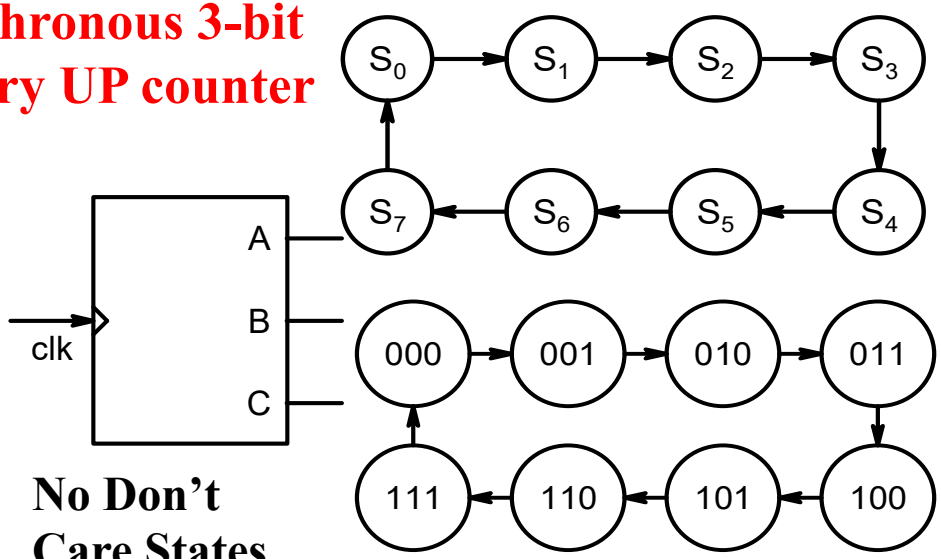
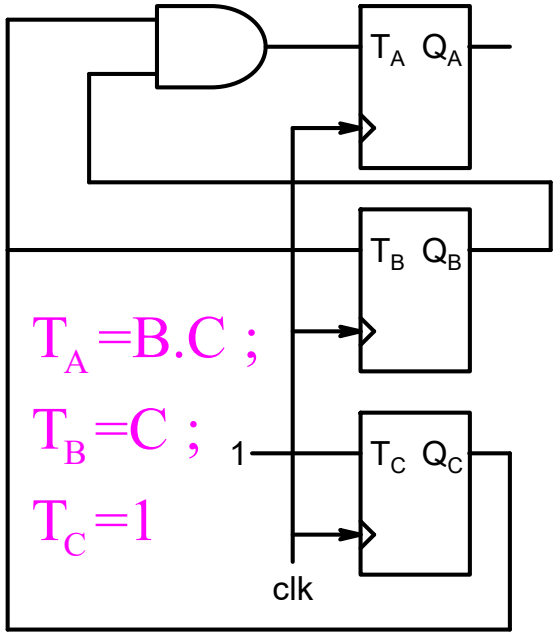
Synchronous 3-bit Binary UP counter

Q_A	Q_B	Q_C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1



No Don't Care States

PS A B C	NS A B C	T_A T_B T_C
0 0 0	0 0 1	0 0 1
0 0 1	0 1 0	0 1 1
0 1 0	0 1 1	0 0 1
0 1 1	1 0 0	1 1 1
1 0 0	1 0 1	0 0 1
1 0 1	1 1 0	0 1 1
1 1 0	1 1 1	0 0 1
1 1 1	0 0 0	1 1 1



$T_B = C$

AB / C	00	01	11	10
0				
1	1	1	1	1

$T_A = B.C$

AB / C	00	01	11	10
0				
1		1	1	

$T_C = 1$

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Synchronous 4-bit Binary UP counter

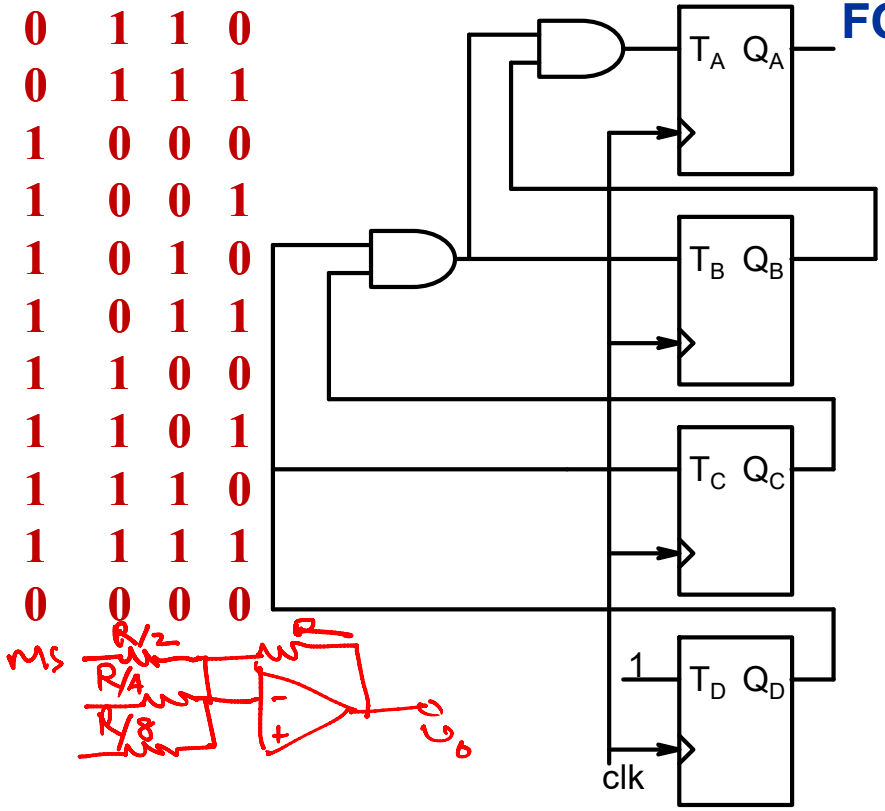
T FF toggles when T=1

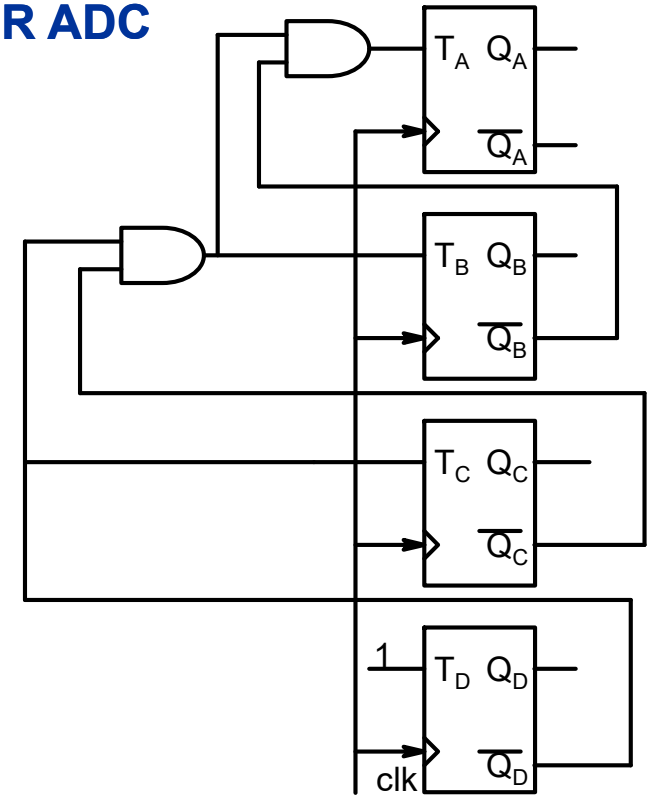
Q_A	Q_B	Q_C	Q_D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1
0	0	0	0

- $-Q_D$ toggles every clock cycle
- $-Q_C$ toggles only when $Q_D = 1$
- $-Q_B$ toggles only when Q_C & $Q_D = 1$
- $-Q_A$ toggles only when Q_B, Q_C , $Q_D = 1$

- $-Q_D$ toggles every clock cycle
- $-Q_C$ toggles only when $Q_D = 0$
- $-Q_B$ toggles only when both Q_C & $Q_D = 0$
- $-Q_A$ toggles only when Q_D, Q_C, $Q_B = 0$

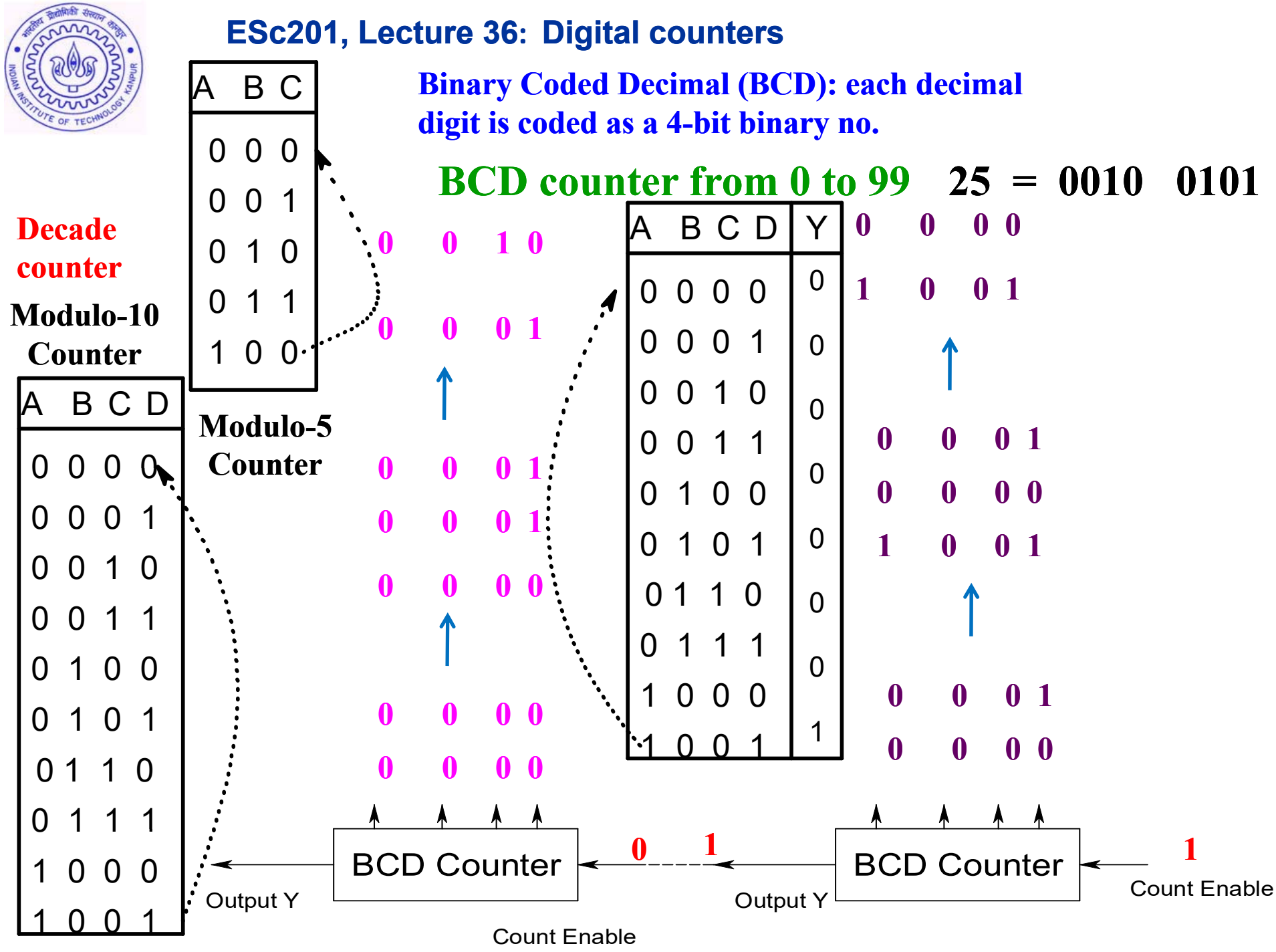
REQUIRED FOR ADC





4-bit Down Counter

Q_A	Q_B	Q_C	Q_D
1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
1	0	1	1
1	0	1	0
1	0	0	1
1	0	0	0
0	1	1	1
0	1	1	0
0	1	0	1
0	1	0	0
0	0	1	1
0	0	1	0
0	0	0	1
0	0	0	0
1	1	1	1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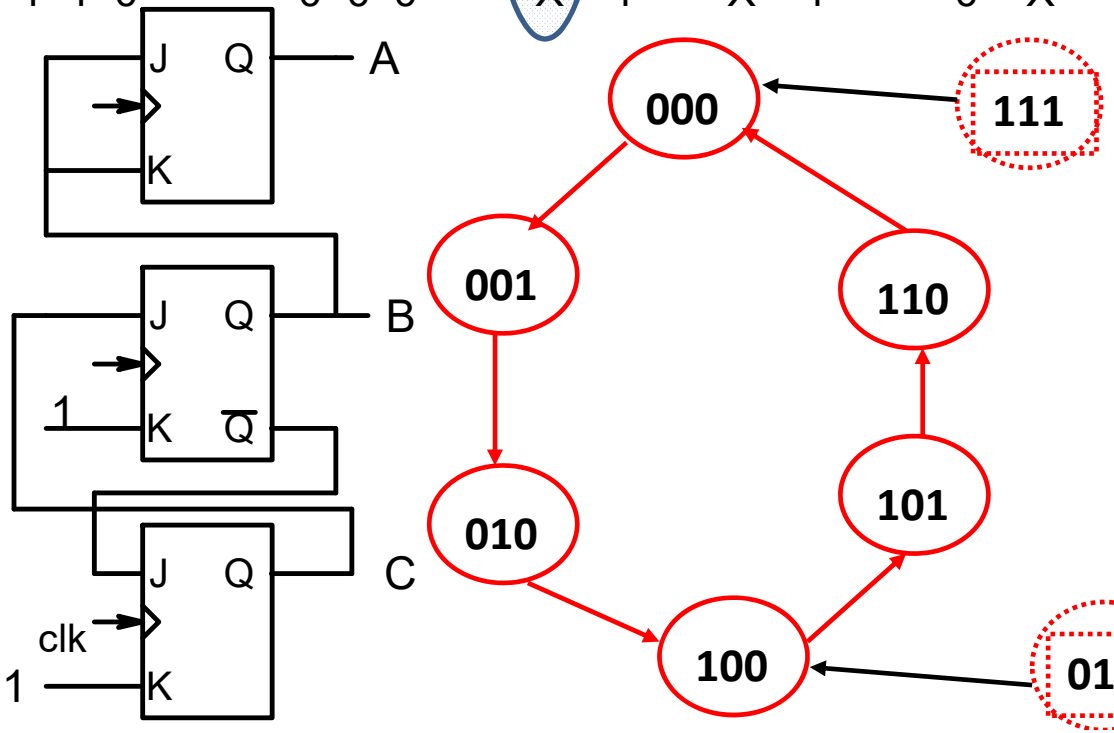
Binary Coded Decimal (BCD): each decimal digit is coded as a 4-bit binary no.
BCD counter from 0 to 99 25 = 0010 0101
Decade counter
Modulo-10 Counter
Modulo-5 Counter
A B C
0 0 0
0 0 1
0 1 0
0 1 1
1 0 0
A B C D
0 0 0 0
0 0 0 1
0 0 1 0
0 0 1 1
0 1 0 0
0 1 0 1
0 1 1 0
0 1 1 1
1 0 0 0
1 0 0 1
A B C D Y
0 0 0 0 0
0 0 0 1 0
0 0 1 0 0
0 0 1 1 0
0 1 0 0 0
0 1 0 1 0
0 1 1 0 0
0 1 1 1 0
1 0 0 0 0
1 0 0 1 1
0 0 1 0
0 0 0 1
0 0 0 1
0 0 0 0
0 0 0 0
0 0 0 0
1 0 0 1
0 0 0 1
0 0 0 0
1 0 0 1
0 0 0 1
0 0 0 0
BCD Counter
BCD Counter
0
1
1
Output Y
Output Y
Count Enable
Count Enable

Counter with Unused States

PS			NS								
A	B	C	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X



BC / A	00	01	11	10
0	0	0	X	1
1	X	X	X	X

$J_A = B$

$J_A = B,\ K_A = \overline{B}\quad J_B = C, K_B = 1$

$J_C = \overline{B}, K_C = 1$

After synthesizing the circuit, one needs to check, if by chance the counter goes into one of the unused states, after one or more clock cycles, it enters a used state and then remains among the used states

We can see that if by chance the counter goes into unused states 111 or 011, then after a clock cycle it enters one of the used states.

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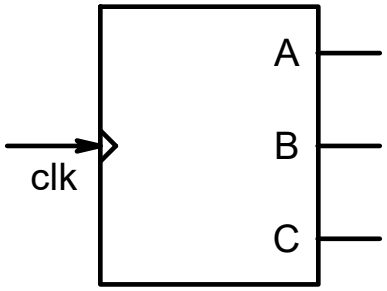
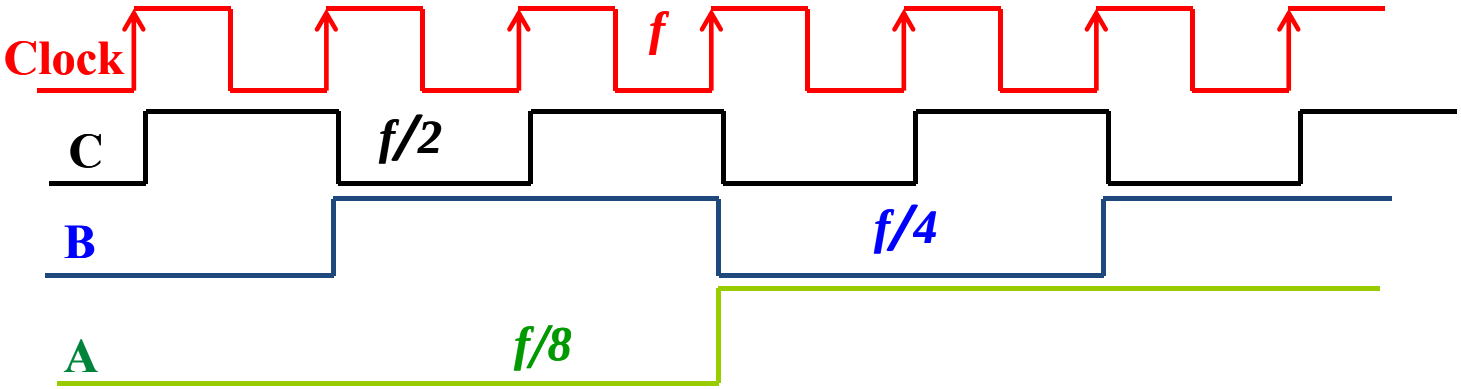
Counter as frequency divider

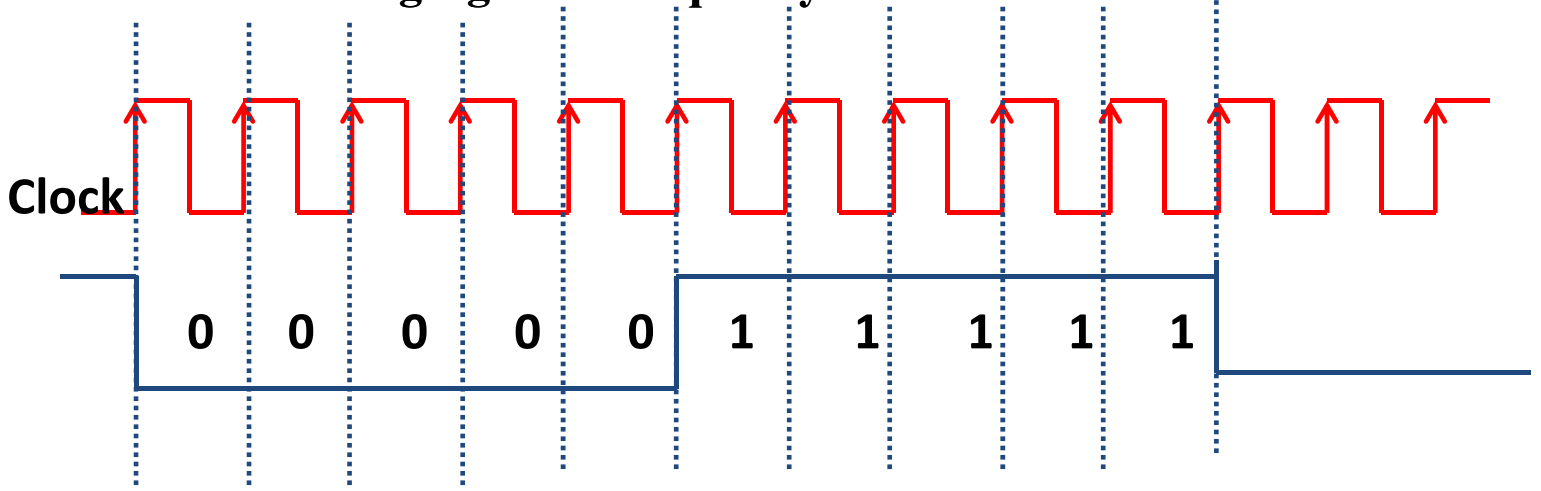


A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1



A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1

Example: From a frequency of 10KHz, generate the following signal of frequency 1KHz.



This will have a frequency of 1KHz but it will not have the same waveform

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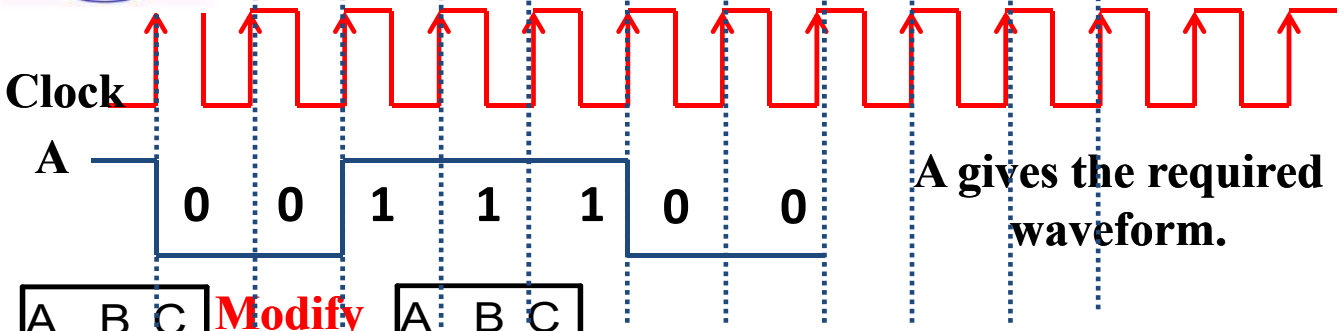
Example: From 10KHz, generate the following signal of frequency 2KHz



A gives the required waveform.

A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0

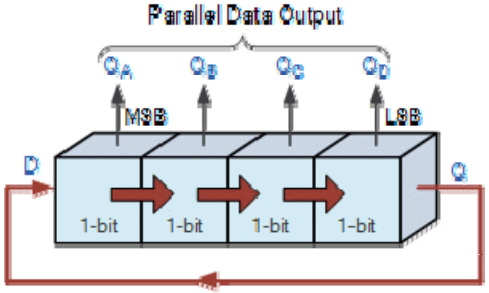
Modify

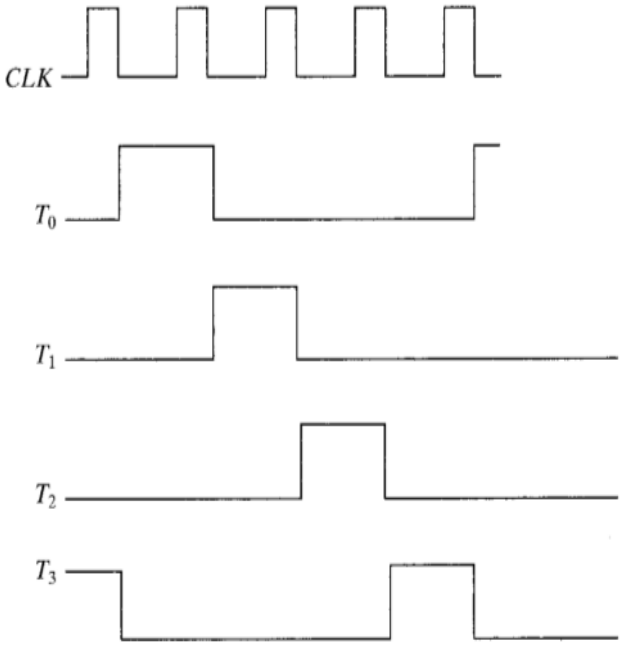
A	B	C
0	0	0
0	0	1
1	1	0
1	1	1
1	0	0

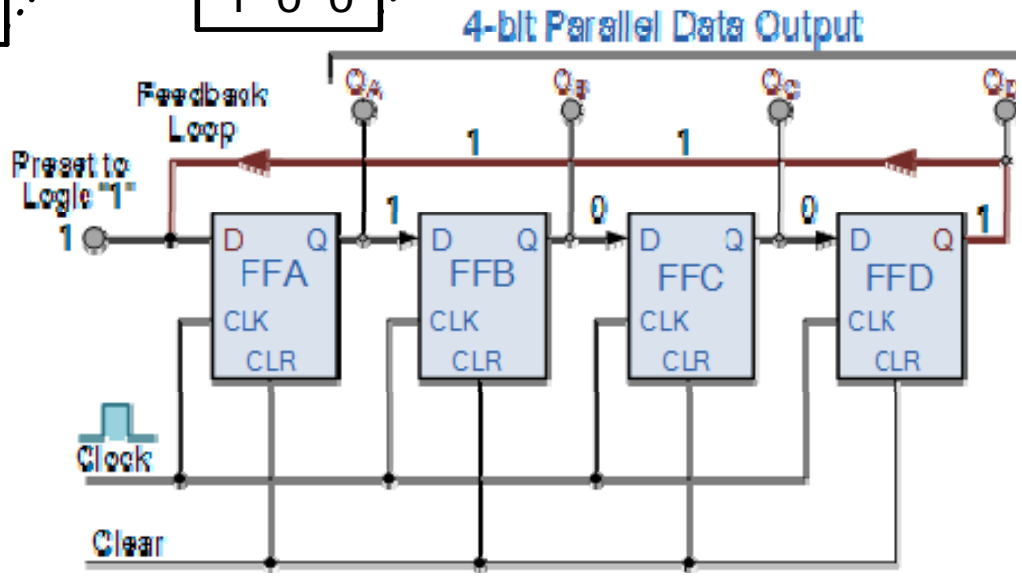
A divide by 5 counter is required that has 5 states.

Ring Counter

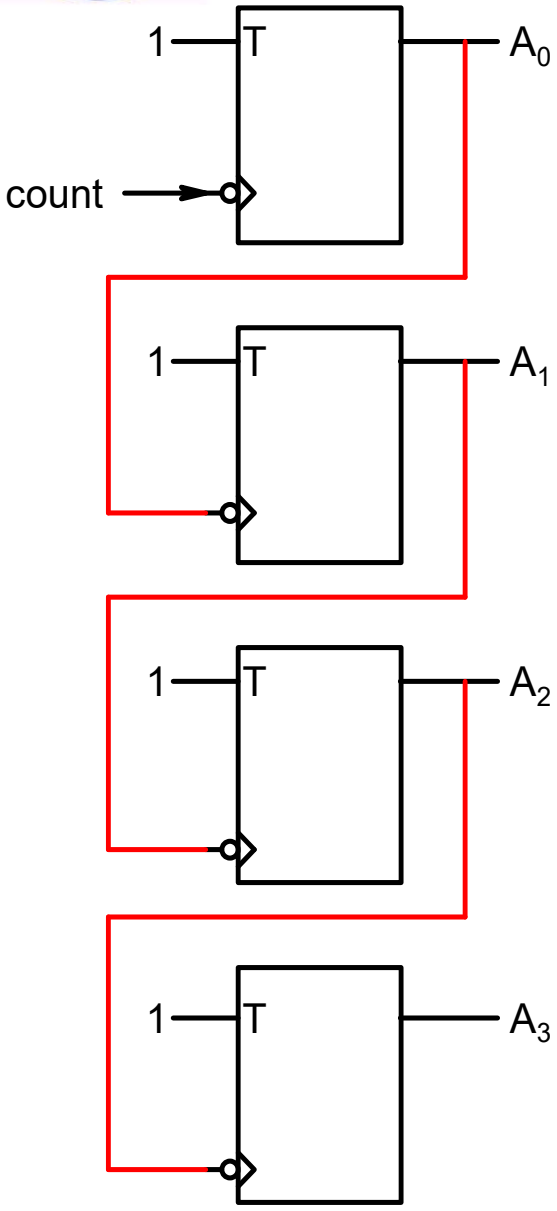
T_3	T_2	T_1	T_0
0	0	0	1
0	0	1	0
0	1	0	0
1	0	0	0







Asynchronous Ripple Counter



0 1 2 3 4 5 ------15

0 1 0 1 0 1 ------1 0

$A_3A_2A_1A_0$

0 0 1 1 0 0 ------1 0

$A_3A_2A_1A_0$

0 0 0 0 1 1 ------1 0

$A_3A_2A_1A_0$

0 0 0 0 0 0 ------1 0

$A_3A_2A_1A_0$

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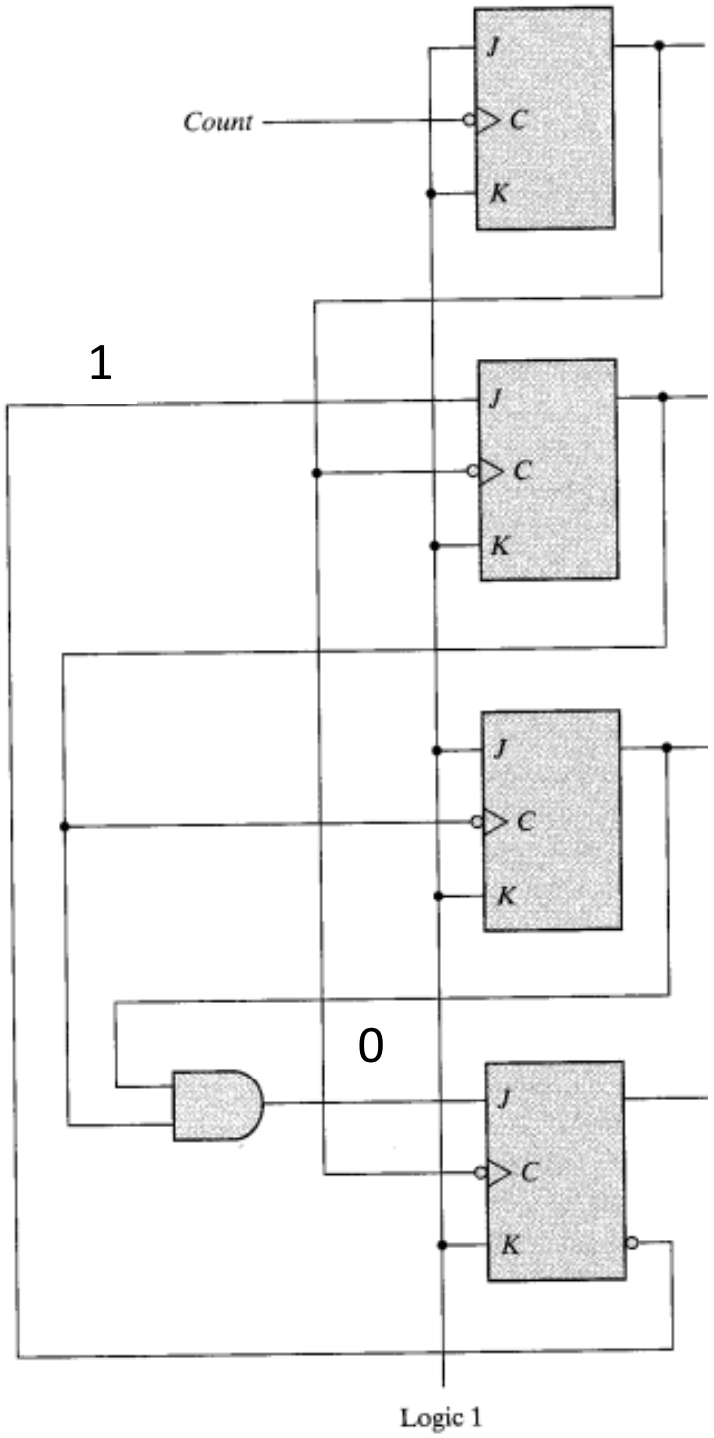
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



A_0	0	1	...	1	0	1	0
A_1	0	0	...	1	0	0	0
A_2	0	0	...	1	0	0	0
A_3	0	0	...	0	1	1	0