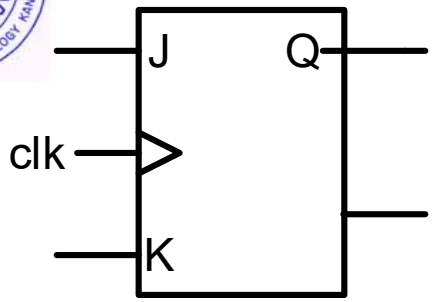
ESc201, Lecture 37: FF Converters & Counting ADC

Characteristic table of FFs

JK Flip-flop



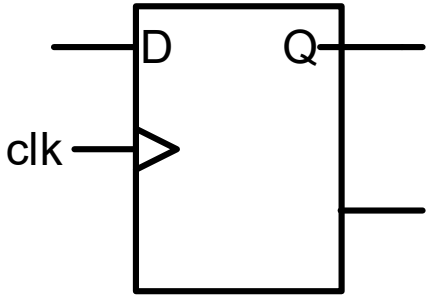
Truth table:

J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Characteristic equation:

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

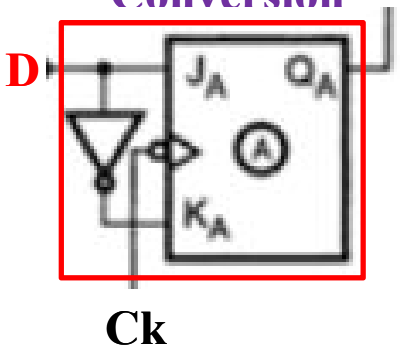
D Flip-flop



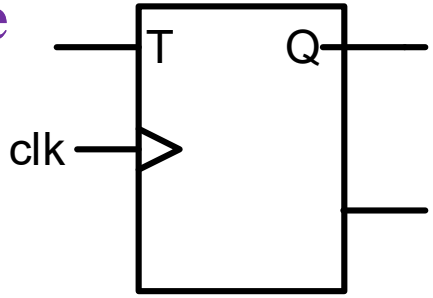
D_n	Q_{n+1}
0	0
1	1

$$Q_{n+1} = D$$

Conversion

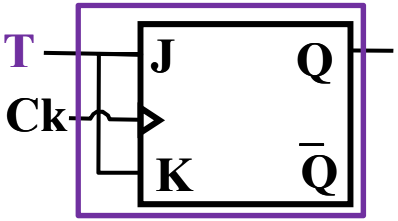


Toggle or T Flip-flop



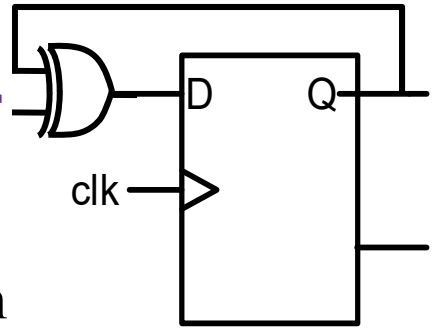
Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$$Q_{n+1} = T \oplus Q_n$$



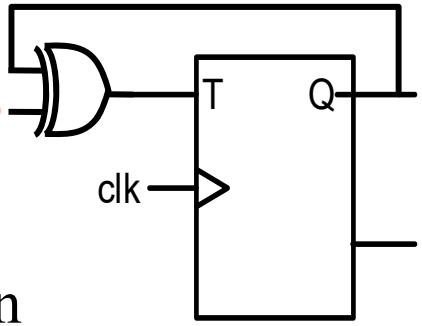
D Flip-flop to T Flip-flop

$$T_n = D_n\bar{Q}_n + \overline{D_n}Q_n = D_n \oplus Q_n$$



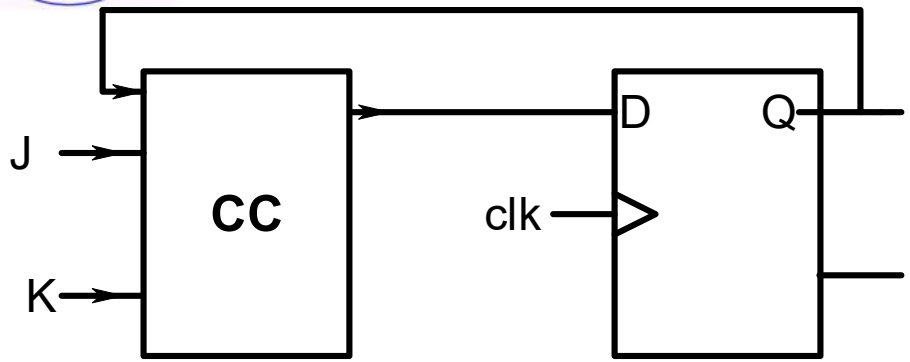
T Flip-flop to D Flip-flop

$$D_n = T_n\bar{Q}_n + \overline{T_n}Q_n = T_n \oplus Q_n$$

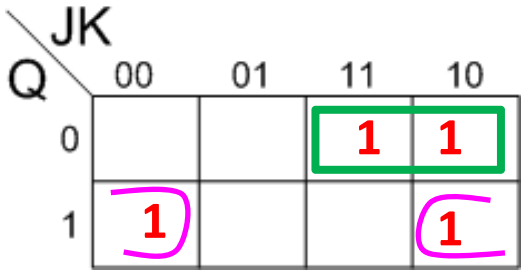


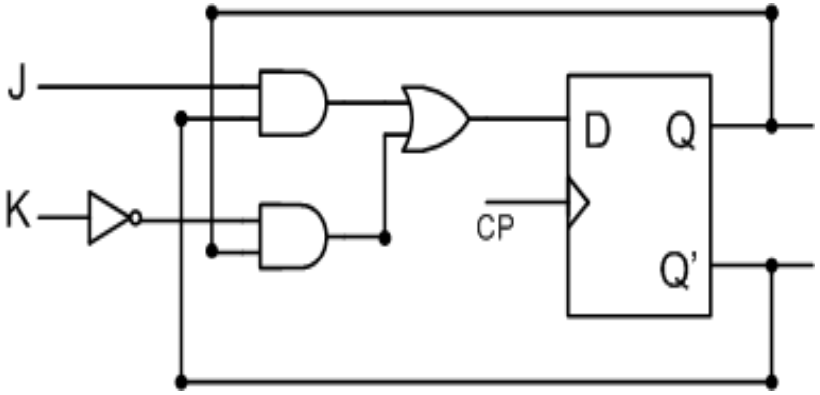
ESc201, Lecture 37: Digital counters and counting-ADC

Convert a D FF to JK FF



J	K	Q	Q(t+1)	D
0	X	0	0	0
1	X	0	1	1
X	1	1	0	0
X	0	1	1	1





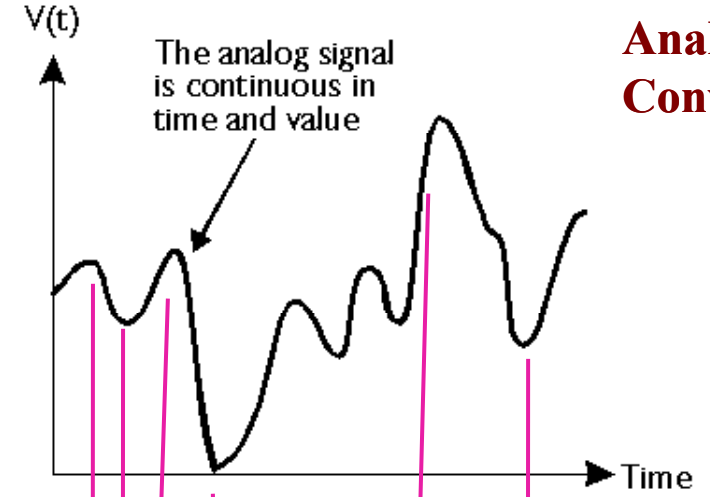
$$D=\overline{Q}.J+Q.\overline{K}$$

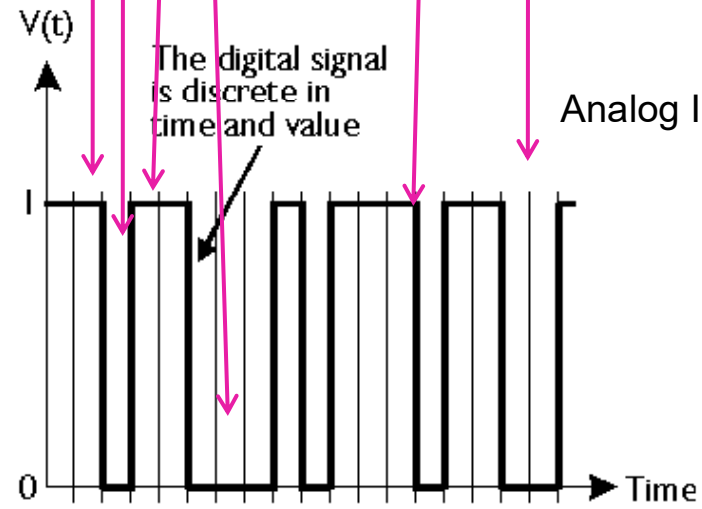
Q	J	K	D	Q_{n+1}
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	0	0
1	1	0	1	1
1	1	1	0	0

ESc201, Lecture 37: Digital counters and counting-ADC

Sampling and Quantization-How to represent real-valued (X&Y) signals as bits?

Quantization and Encoding



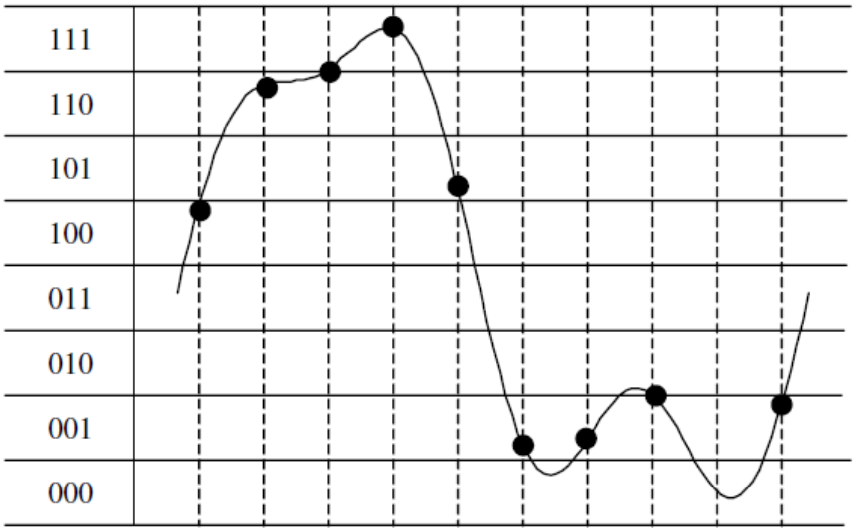


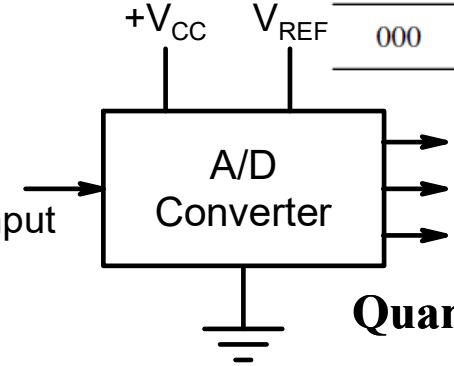
$$V_0 = \frac{V_{REF}}{2^3} \times (A_2 2^2 + A_1 2^1 + A_0 2^0)$$

Analog to Digital Converter (ADC)

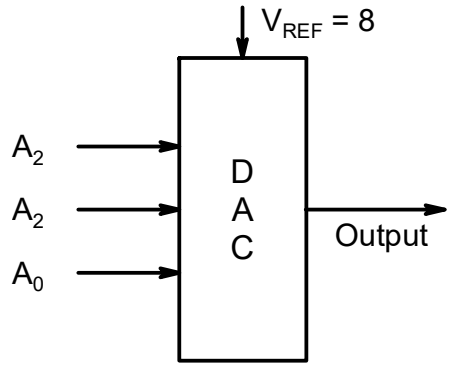
Resolution = 3 bits;

1 LSB = $V_{REF}/2^N = 1V$





Quantization error



So 101 gives 5 x 1 = 5V

$0V < V_{in} < 1V \rightarrow 000$

$1V < V_{in} < 2V \rightarrow 001$

$2V < V_{in} < 3V \rightarrow 010$

$3V < V_{in} < 4V \rightarrow 011$

$4V < V_{in} < 5V \rightarrow 100$

$5V < V_{in} < 6V \rightarrow 101$

$6V < V_{in} < 7V \rightarrow 110$

$7V < V_{in} < 8V \rightarrow 111$

ESc201, Lecture 37: Digital counters and counting-ADC

Error can be as large as 1V or 1LSB

$0V<V_{in}<1V \rightarrow 000$

$1V<V_{in}<2V \rightarrow 001$

$2V<V_{in}<3V \rightarrow 010$

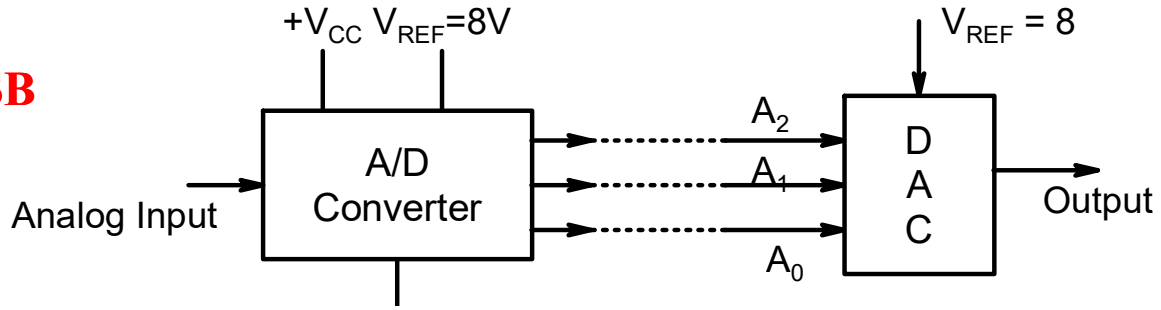
$3V<V_{in}<4V \rightarrow 011$

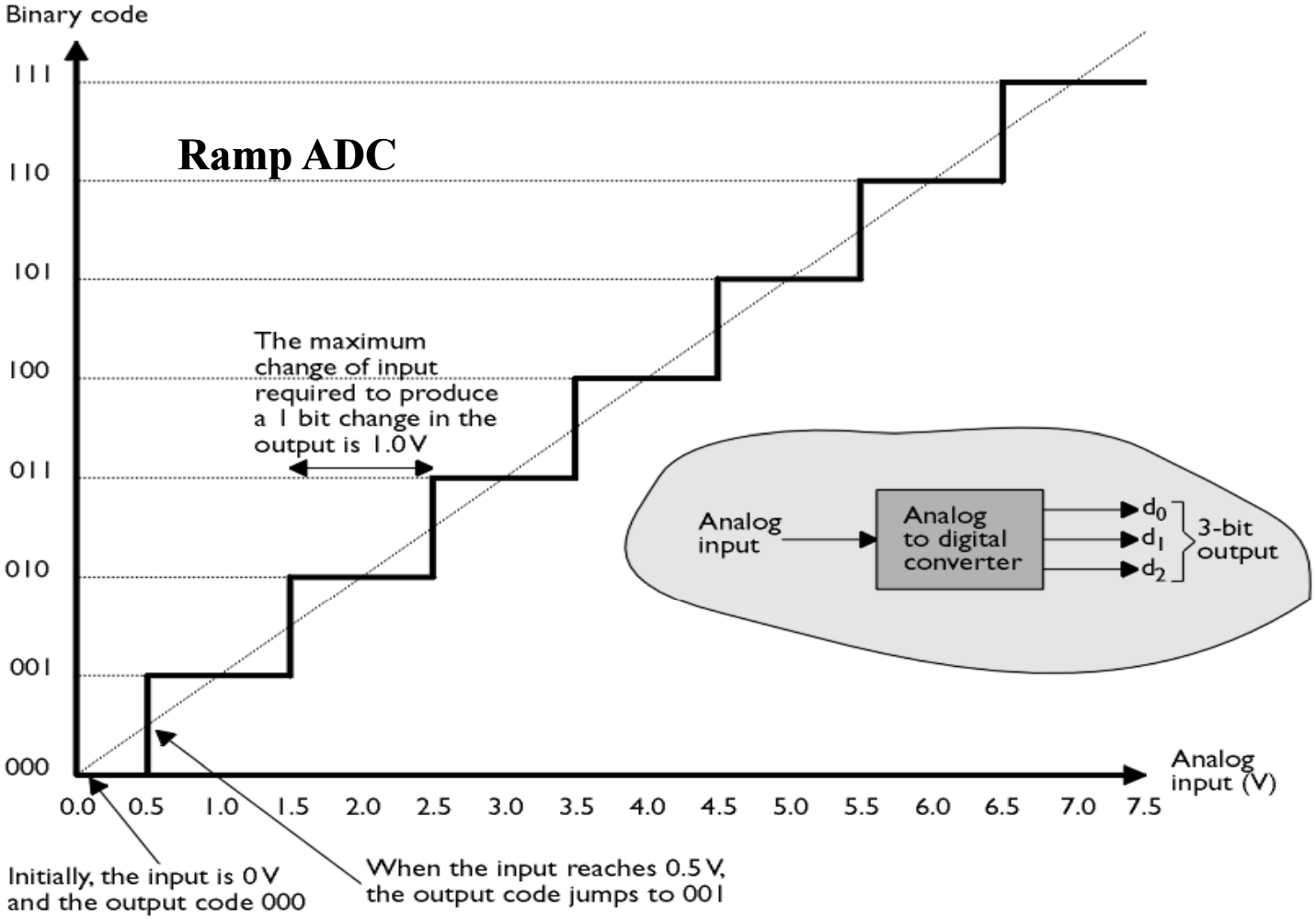
$4V<V_{in}<5V \rightarrow 100$

$5V<V_{in}<6V \rightarrow 101$

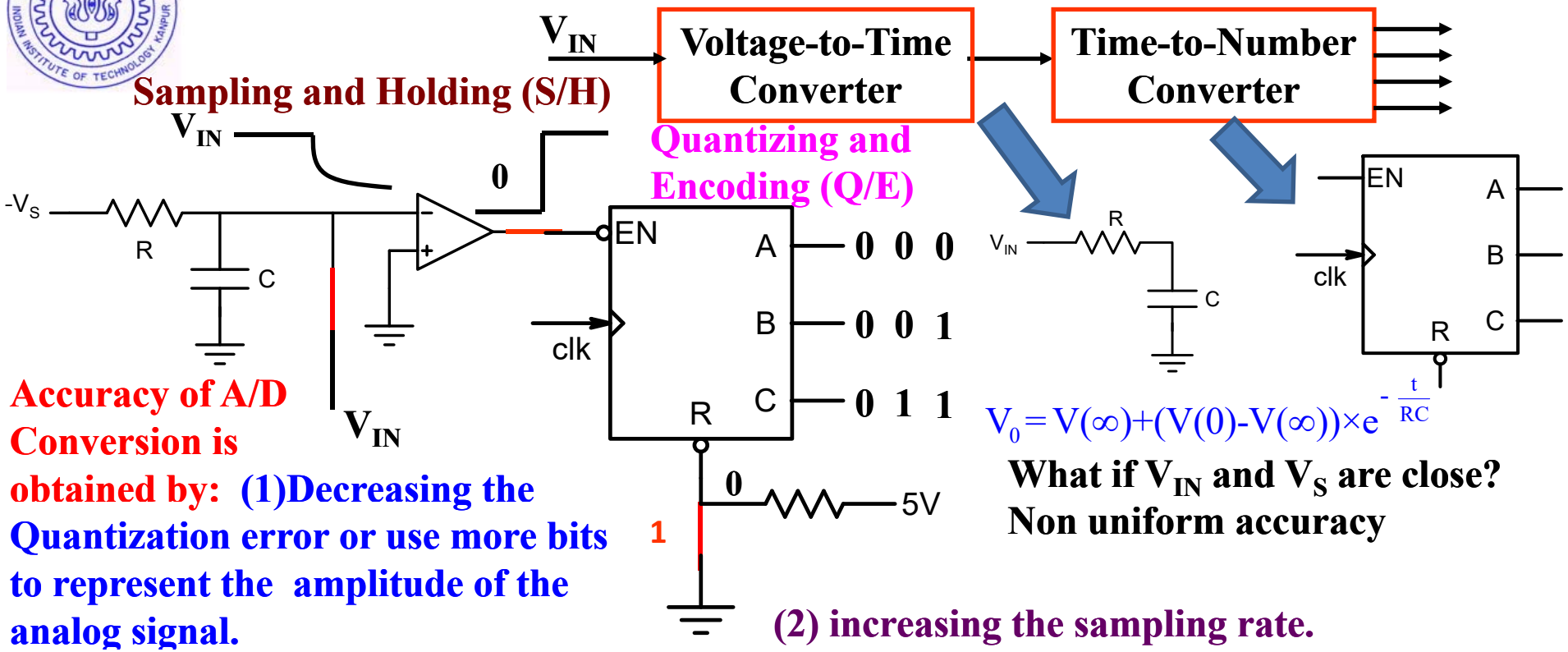
$6V<V_{in}<7V \rightarrow 110$

$7V<V_{in}<8V \rightarrow 111$





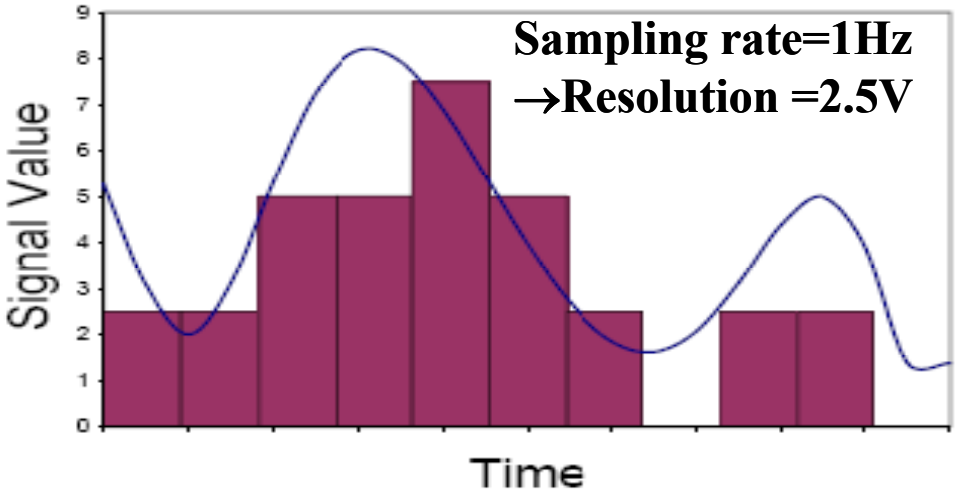
ESc201, Lecture 36: Digital counters and counting-ADC

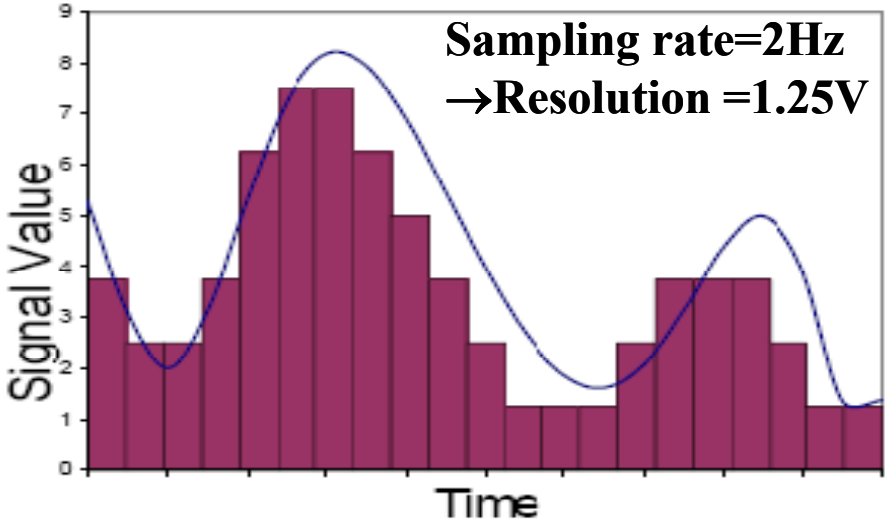


Accuracy of A/D Conversion is obtained by: (1)Decreasing the Quantization error or use more bits to represent the amplitude of the analog signal.

What if V_{IN} and V_S are close? Non uniform accuracy

(2) increasing the sampling rate.

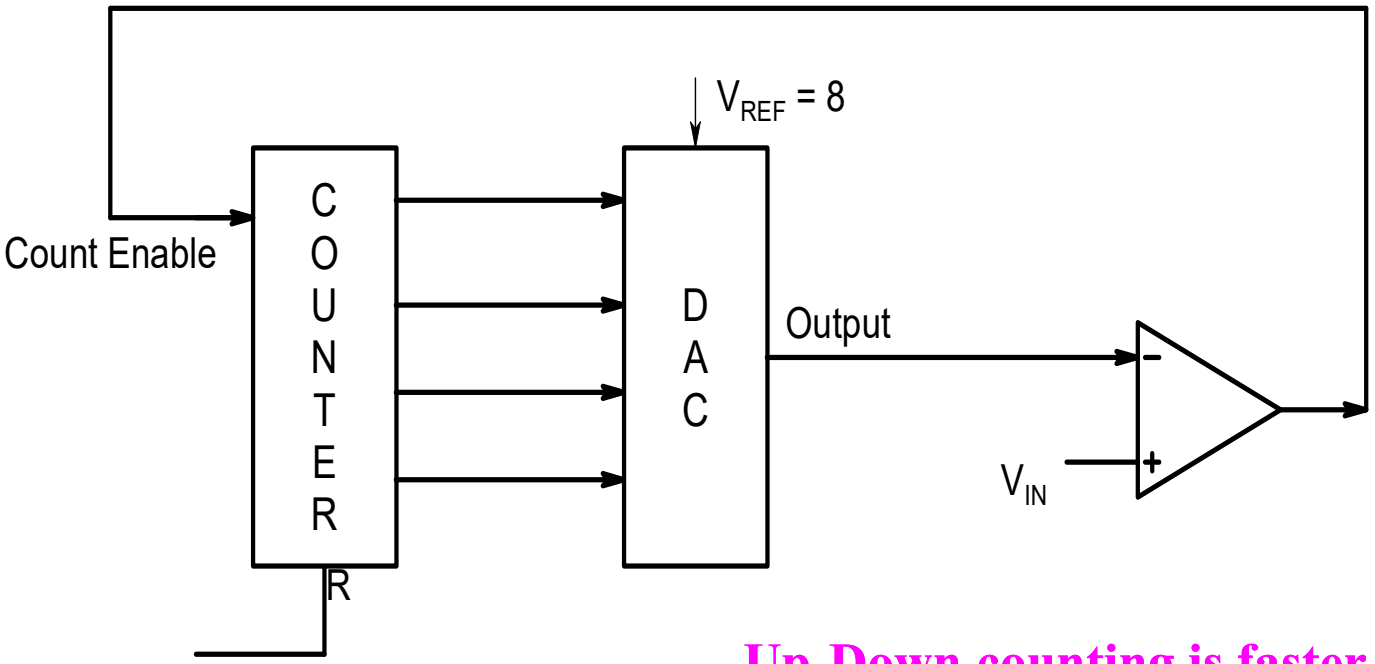




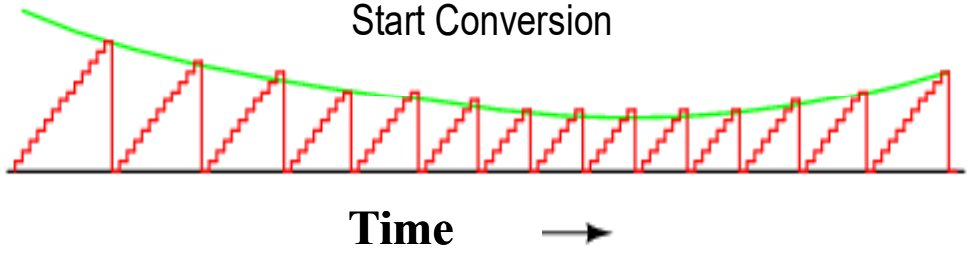
ESc201, Lecture 37: Digital counters and counting-ADC

Digital word corresponding to 1.2V is 0010

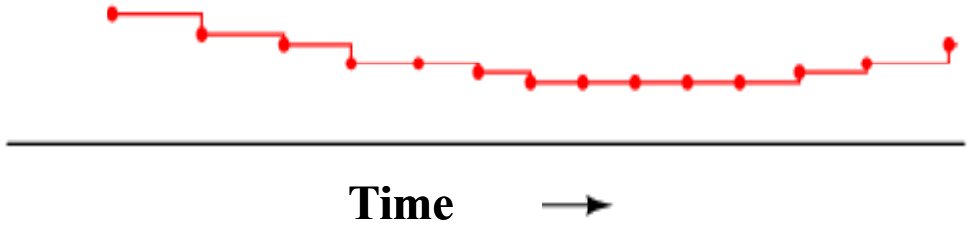
Worst case conversion time is 8 clock periods



AnalogInput

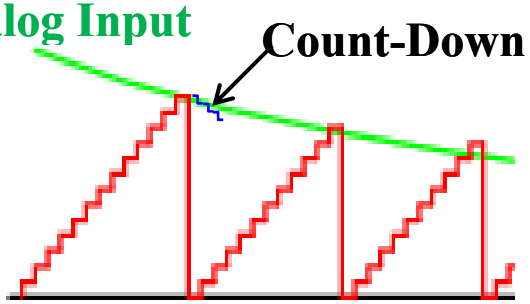


Digital Output

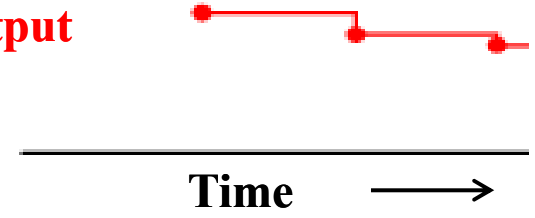


Up-Down counting is faster

Analog Input



Digital Output



ESc201, Lecture 37: Digital counters and Dual Slope ADC

Integrates an unknown input voltage (V_{IN}) for a fixed time (T_{INT}), and then "de-integrates" (T_{DEINT}) using a reference voltage (V_{REF}) for a variable time.

Fundamental components :
1)Integrator
2)Electronic Switches
3)Counter
4)Clock
5)Control Logic
6)Comparator

At t<0, S1 is set to ground, S2 is closed, and counter=0.

1)At t=0 a conversion begins and S2 is open, and S_1 is set so the input to the integrator is V_{IN}.

2) S_1 is held for T_{INT} which is a constant predetermined time interval.

3)When S_1 is set the counter begins to count clock pulses, the counter resets to zero after T_{INT} .

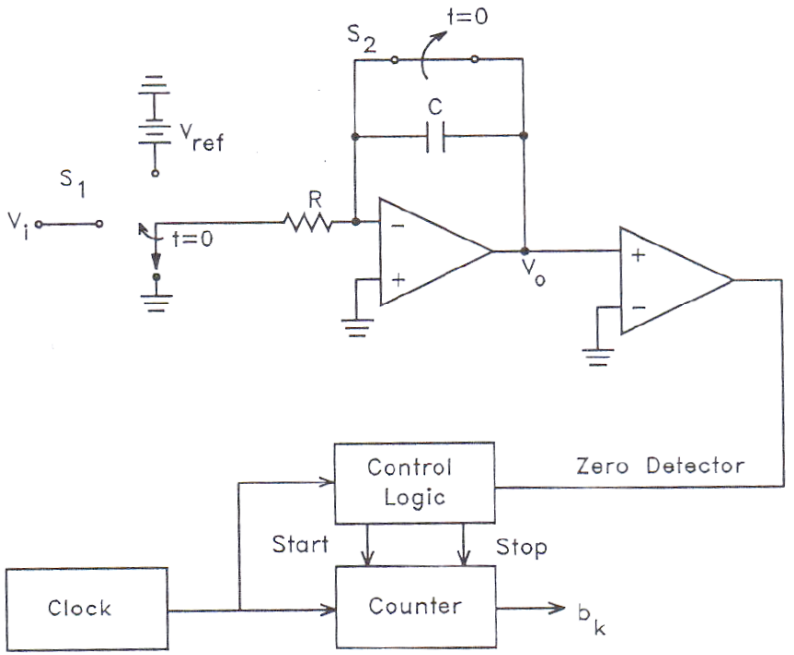
4)Vout of integrator at t=T_{INT} is $(V_{IN}T_{INT}/RC)\ \alpha V_{IN}$

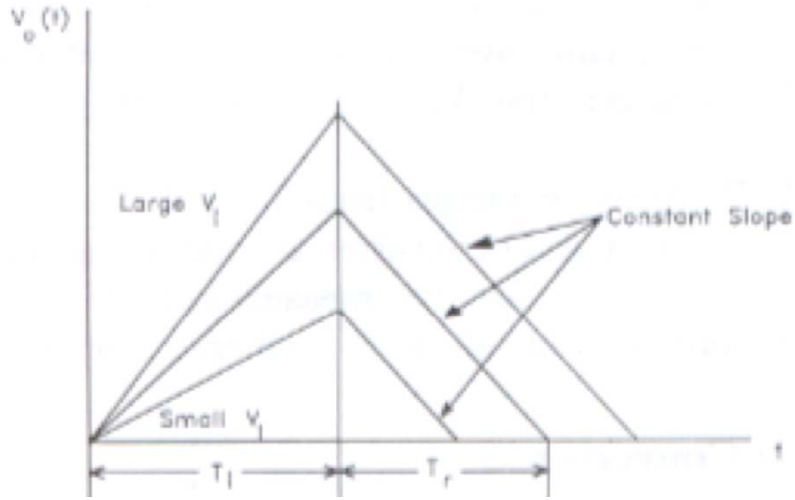
5)At t= T_{INT} S_1 is set so $-V_{REF}$ is the input to the integrator which has the voltage $V_{IN}T_{INT}/RC$ stored in it.

6)The integrator voltage then drops linearly with a slop $-V_{REF}/RC$.

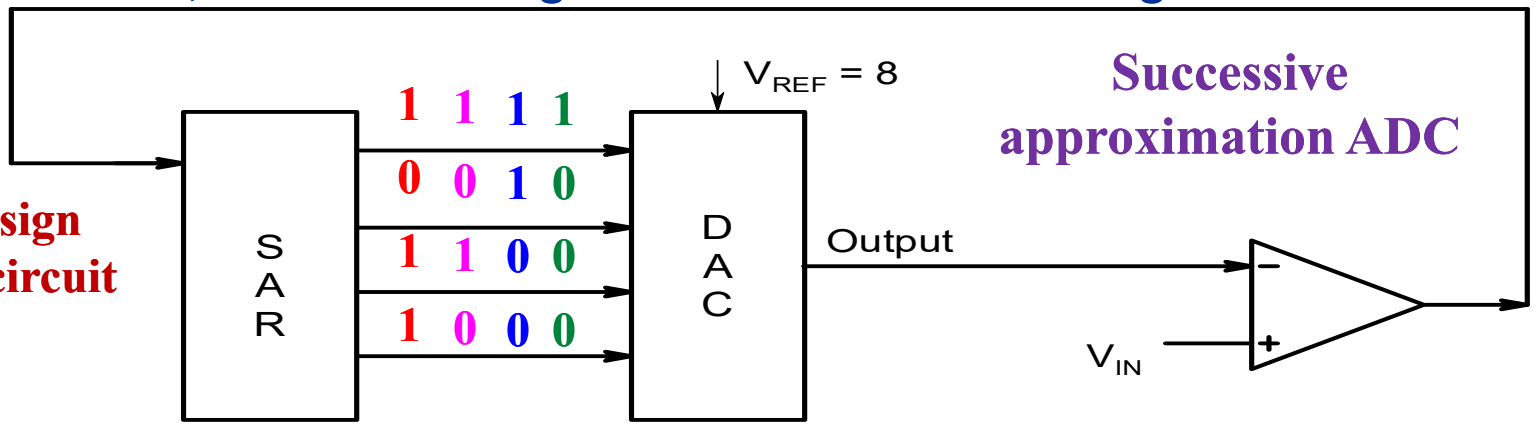
7)A comparator is used to determine when the output voltage of the integrator crosses zero

8) When it is zero the digitized output value is the state of the counter





ESc201, Lecture 36: Digital counters and counting-ADC



To do: Design the logic circuit for SAR

Type	Speed (relative)
Dual Slope	Slow
Flash	Very Fast
Successive Appoximation	Medium – Fast
Type	Cost (relative)
Dual Slope	Med
Flash	High
Successive Appoximation	Low