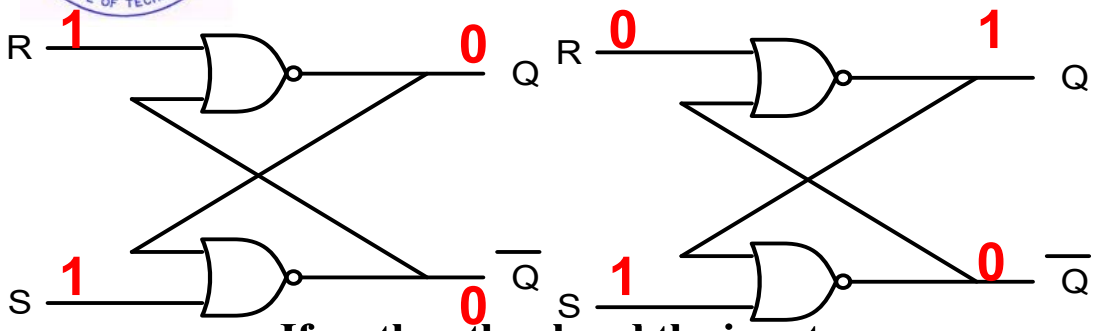
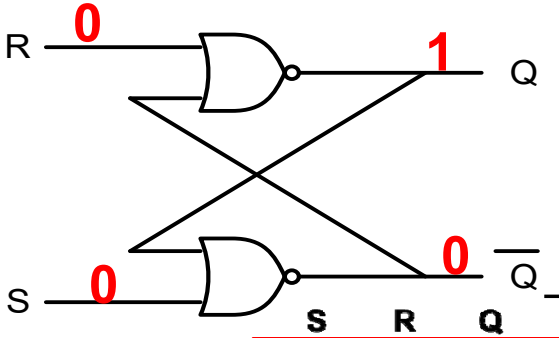
The inputs do not change simultaneously and arises a situation of 11 → 01* → 00

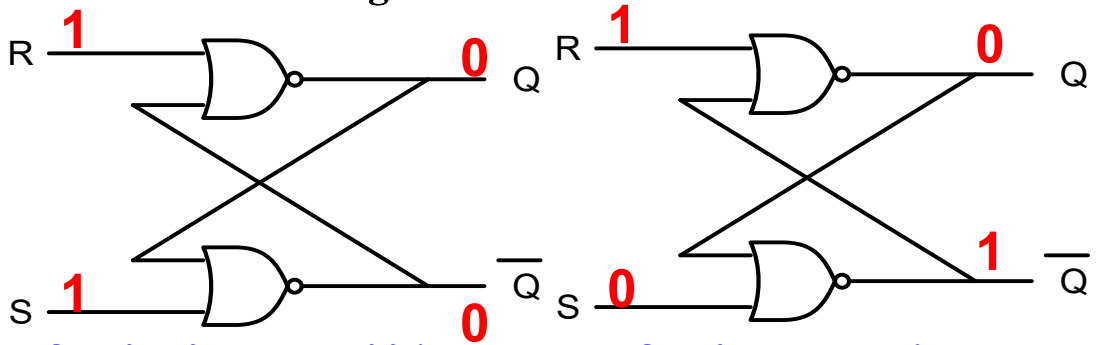
Q = 0→1 and 00 input holds Q=1, whereas it should have held 00

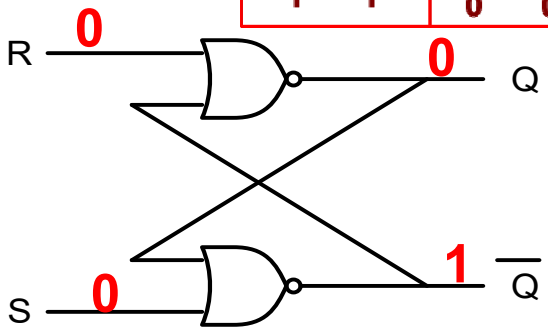




S	R	Q	$\overline{Q}$	State
1	0	1	0	SET
0	1	0	1	RESET
0	0	Q	$\overline{Q}$	HOLD
1	1	0	0	INVALID

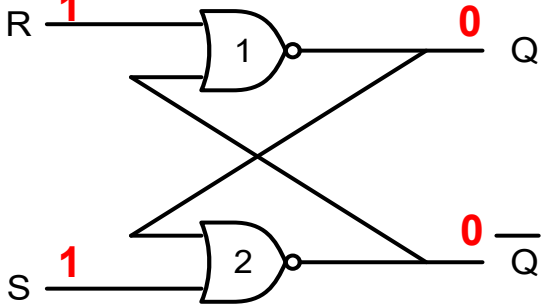
If on the other hand the inputs changed as RS = 11 → 10* → 00



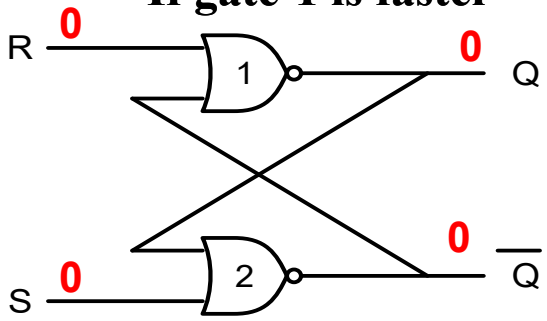


Q = 0→0 and the 00 input holds Q = 0, whereas it should have held 00.

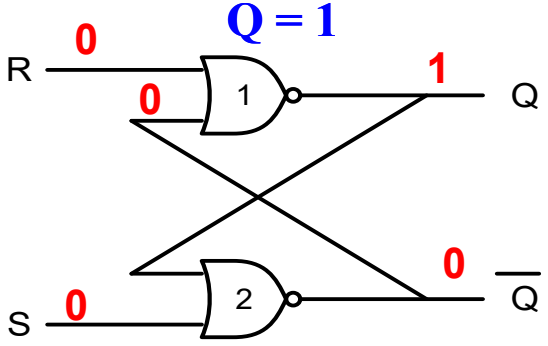
SR Latch: gate delays



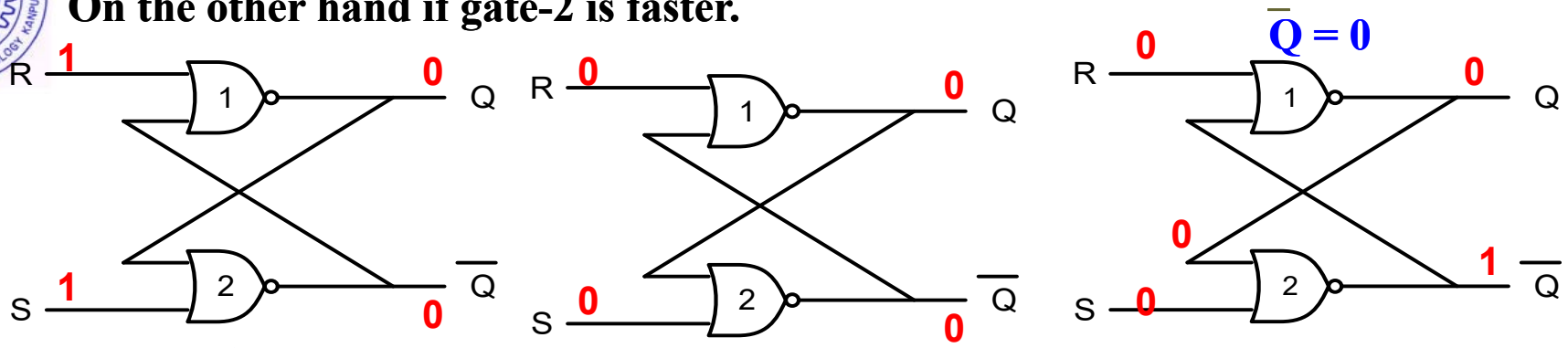
If gate-1 is faster



Q = 1

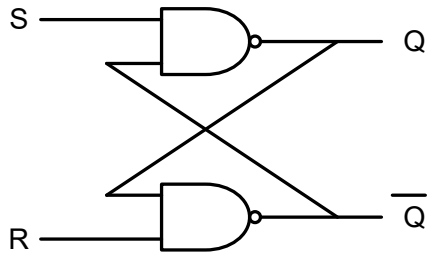


On the other hand if gate-2 is faster.

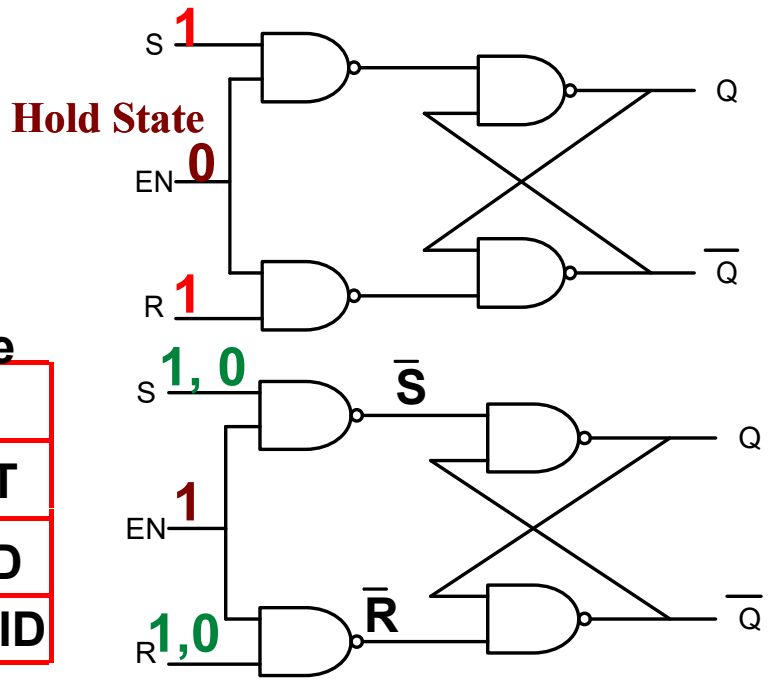


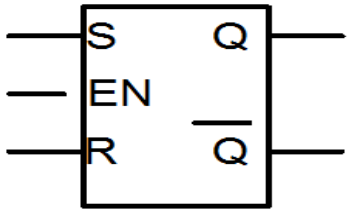
Again the output is, in general, unpredictable.

So although output is well defined when RS = 11 is applied, it becomes unpredictable once the inputs are switched to the latch-hold state by applying RS=00. That is why RS=11 is not used as an input. Use Enable Or Clock.



S	R	Q	$\bar{Q}$	State
0	1	1	0	SET
1	0	0	1	RESET
1	1	Q	$\bar{Q}$	HOLD
0	0	1	1	INVALID

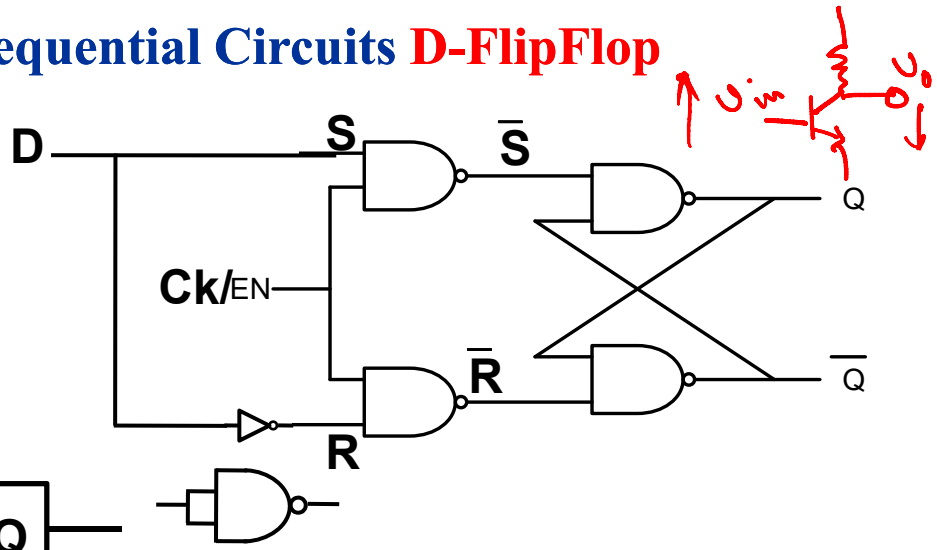




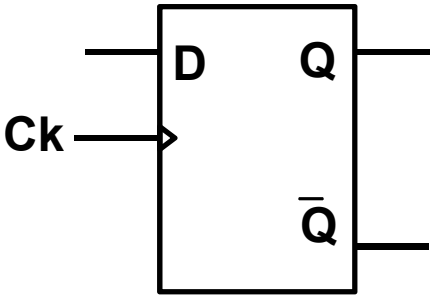
Enable	S	R	Q	$\bar{Q}$	State
0	x	x	Q	$\bar{Q}$	Hold
1	1	0	1	0	Set
1	0	1	0	1	Reset
1	0	0	Q	$\bar{Q}$	Hold
1	1	1	0	0	Invalid

ESc201, Lecture 34: (Digital) Sequential Circuits D-FlipFlop

For the inputs S and R never to show up as 1, 1 one might make sure that one input is invert of the other by using a NOT or i-input NAND gate.

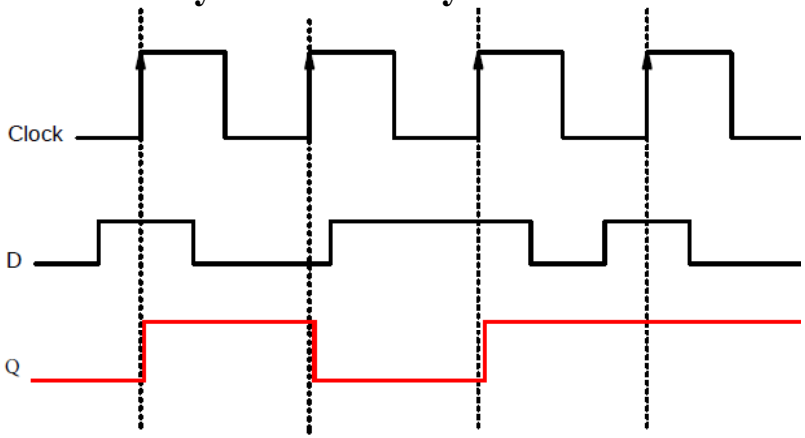


Enable	S	R	Q	$\bar{Q}$	State
0	x	x	Q	$\bar{Q}$	Hold
1	1	0	1	0	Set
1	0	1	0	1	Reset
~~1~~	~~0~~	~~0~~	~~Q~~	~~$\bar{Q}$~~	~~Hold~~
~~1~~	~~1~~	~~1~~	~~0~~	~~0~~	~~Invalid~~

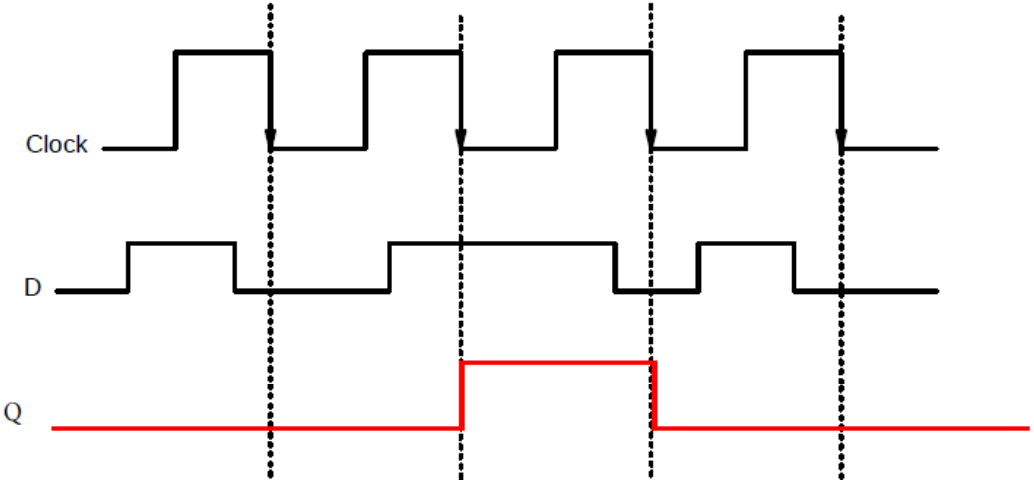


As long as Ck=0, the output Q, $\bar{Q}$ holds. The input D is only sampled at the arrival of the Ck pulse. If D=0, Q=0, $\bar{Q}$=1. If at the next Ck pulse the input has changed to D=1, then the output switches to Q=1, Q=0. Sometimes called gated D-Latch.

So the D-Flip-Flop just transfers the data for storage with a delay of one Ck cycle.



Positive edge triggered flipflop



Negative edge triggered flipflop

ESc201, Lecture 34: (Digital) Sequential Circuits JK-FlipFlop

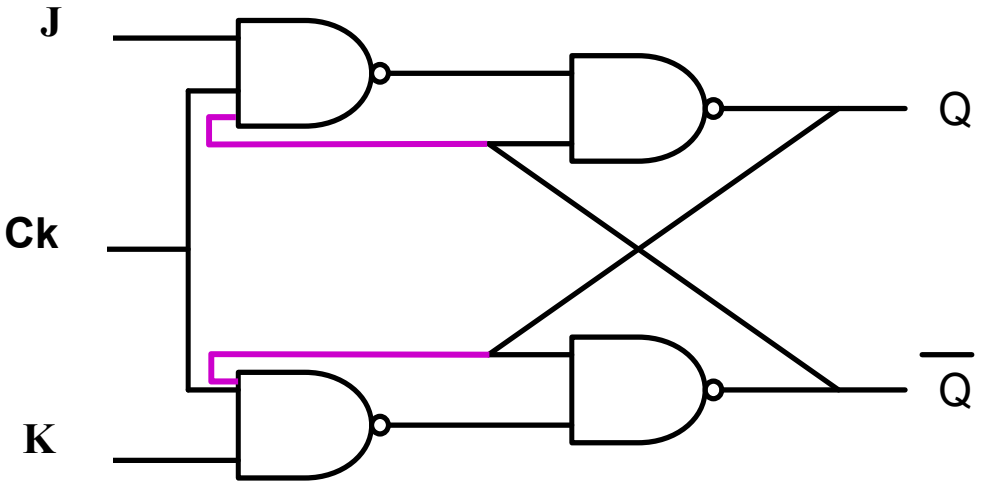
To remove the ambiguity faced in SR-flipflop a feedback is required from the complimentary output to the additional AND gate used for the clock.

J (Jack) and K (Kilby) are the input states for the JK flip-flop.

Q_n	J	K	Q_{n+1}	Q_{n+1}
0	0	0	0	Q_n
0	0	1	0	Q_n
0	1	0	1	$\bar{Q}_n$
0	1	1	1	$\bar{Q}_n$
1	0	0	1	Q_n
1	0	1	0	$\bar{Q}_n$
1	1	0	1	Q_n
1	1	1	0	$\bar{Q}_n$

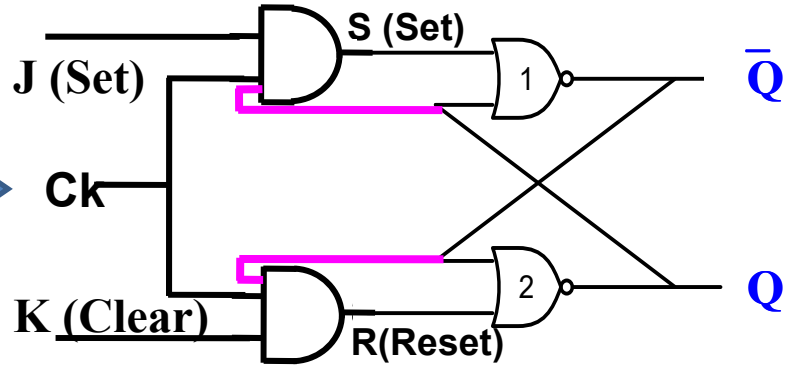
Q_n is the output at the n^{th} clock pulse.

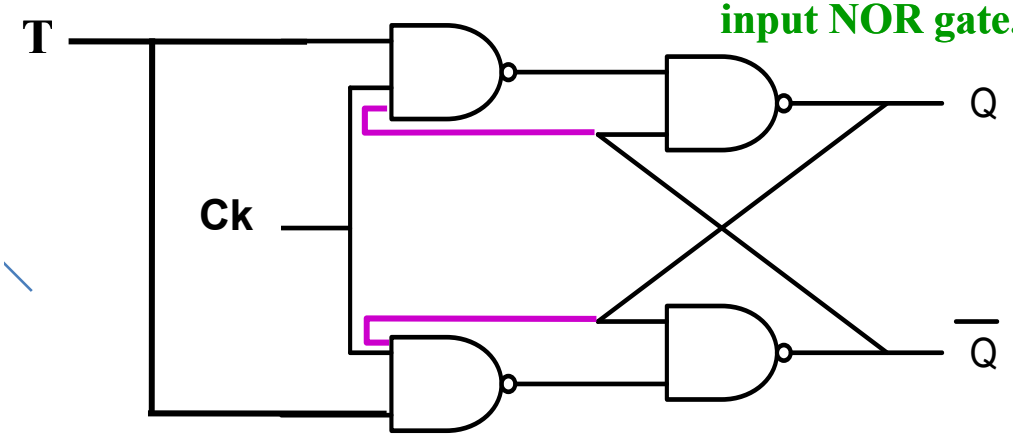
J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$



Ambiguity Removed: The last line gives a new T-flipflop.

Not a very good example where $\bar{Q}$ comes out of the 'S' input NOR gate.





T-flipflop is supposed to Toggle at each clock pulse if the input T is 1, or hold if input is 0.

$Q_{n+1} = T \oplus Q_n$

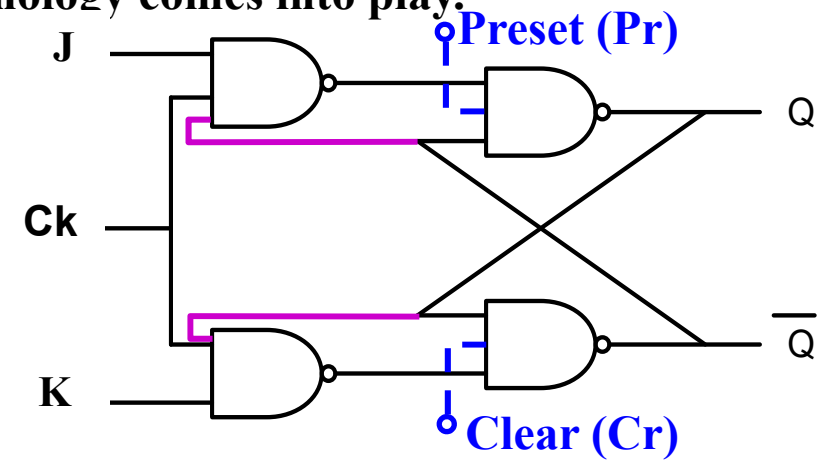
Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

ESc201, Lecture 34: (Digital) Sequential Circuits JK Master-Slave

All worries over? ---- Not quite. Technology comes into play.

Q_n	J	K	Q_{n+1}	Q_{n+1}
0	0	0	0	Q_n
0	0	1	0	Q_n
0	1	0	1	$\bar{Q}_n$
0	1	1	1	$\bar{Q}_n$
1	0	0	1	Q_n
1	0	1	0	$\bar{Q}_n$
1	1	0	1	Q_n
1	1	1	0	$\bar{Q}_n$

For J=1, K=1 if the it is positive edge triggered, as soon as the clock arrives the output state toggles after two NAND gate delays (Δt).

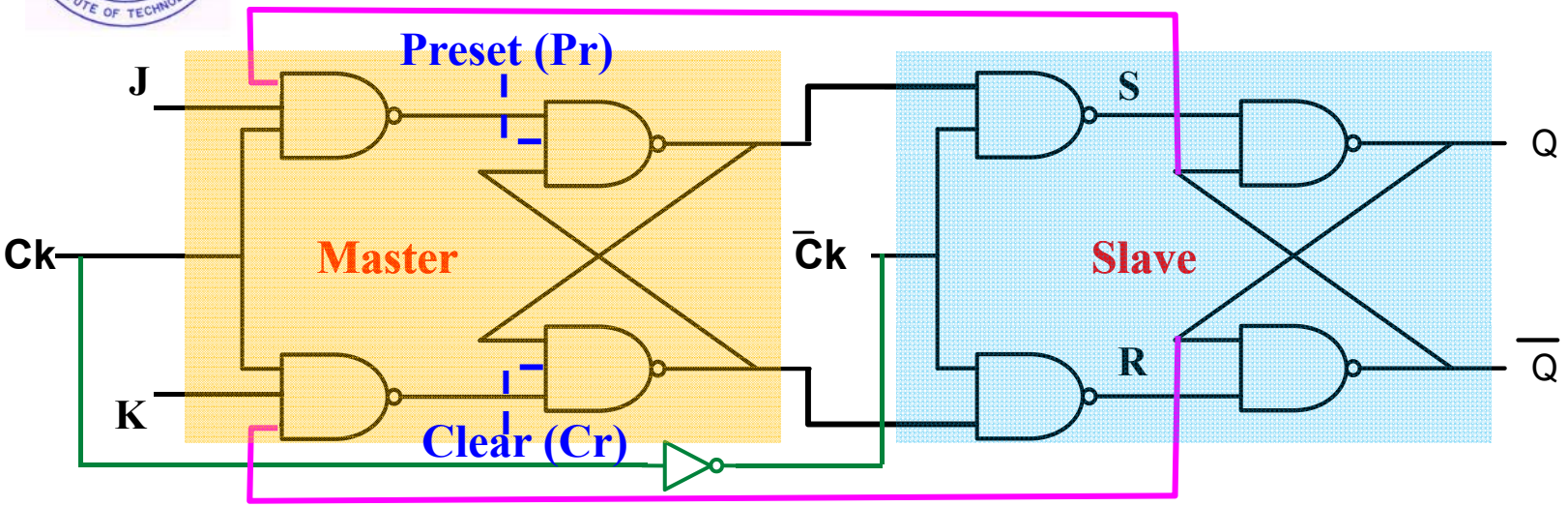


If the clock pulse is t_p and $t_p < \Delta t$, then no problem. However, if $t_p > \Delta t$, then J & K being still held at 1, the output will toggle again. This sets a race around condition. So the final state of the output after the end of the clock pulse is unknown.

CLOCK	J	K	$\overline{SET}$	$\overline{RESET}$	Q	$\overline{Q}$
-	-	-	0	1	1	0
-	-	-	1	0	0	1
⌐	0	0	1	1	Q	$\bar{Q}$
⌐	1	0	1	1	1	0
⌐	0	1	1	1	0	1
⌐	1	1	1	1	$\bar{Q}$	Q

ESc201, Lecture 34: (Digital) Sequential Circuits

Solution: JK Master-Slave

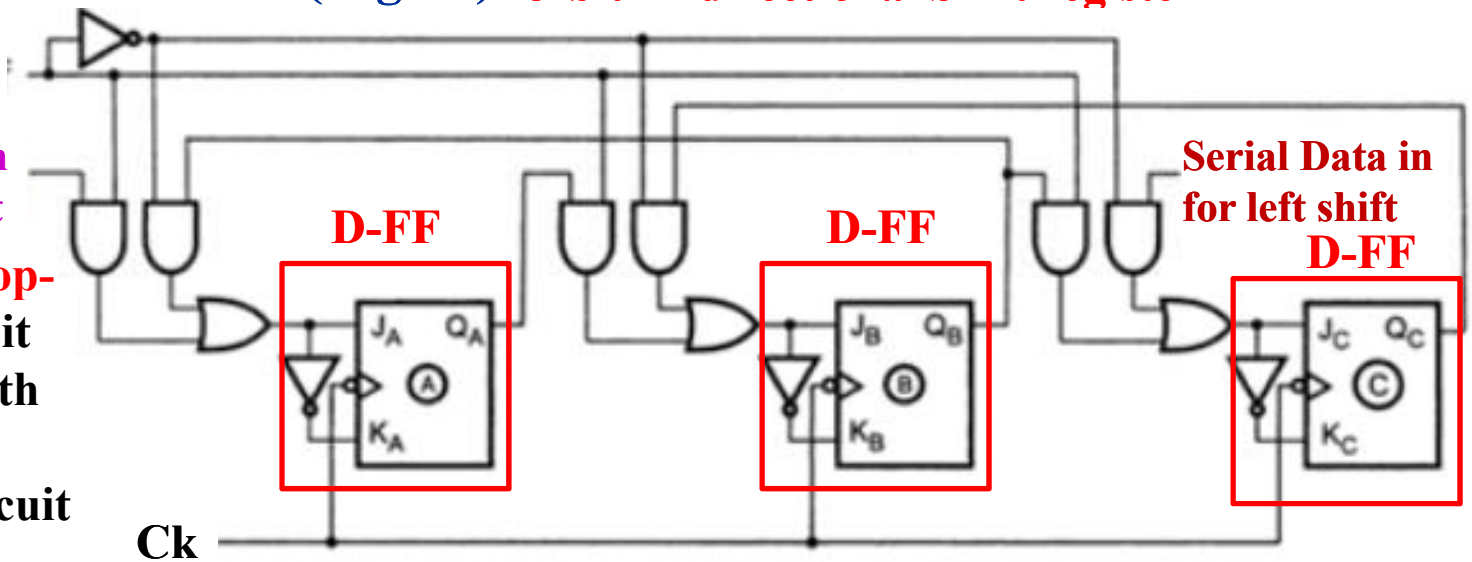


J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Analysis of clock sequential circuits-

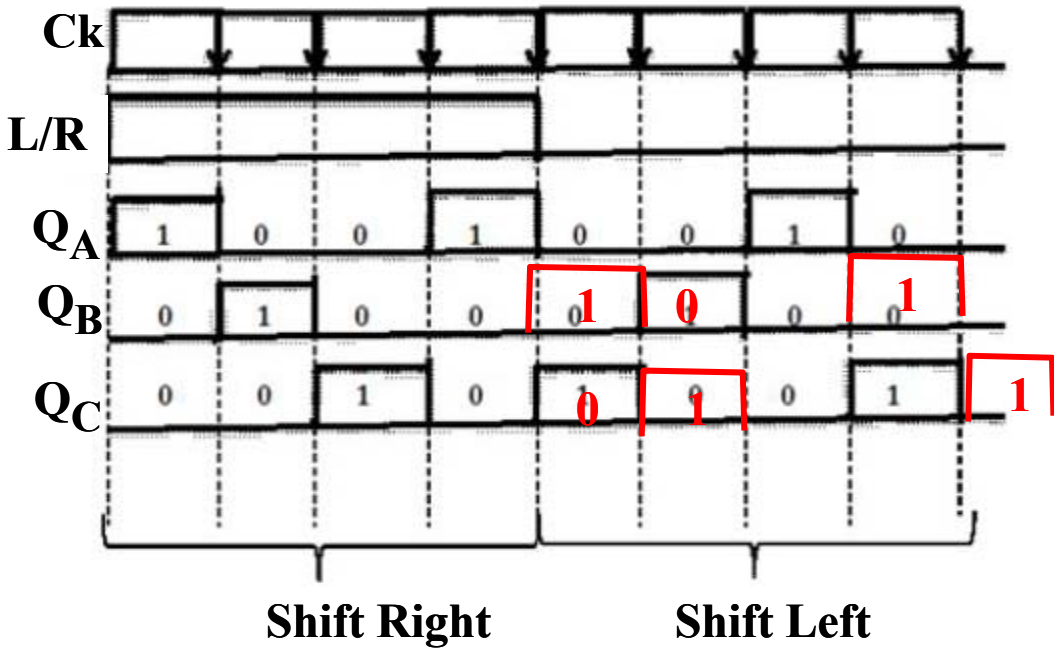
1. The behavior of sequential circuit is determined from the inputs, the outputs and the states of its flip flops. Both the outputs and the next state are the function of the inputs and the present state.
2. The Analysis of sequential circuits consists of obtaining a table or a diagram for the time sequence of inputs, outputs and the internal states. It is also possible to write Boolean expression that describe the behavior of sequential circuits. However these expressions must include the necessary time sequence .
3. A clocked sequential circuit has one input variable X, one output variable Y and two clocked RS flip flops labeled A and B.

ESc201, Lecture 33: (Digital) 3-bit Bi-directional Shift register



Triggering of flip flop-

1. A sequential circuit has a feedback path between the combinational circuit and the memory elements. This path can produced instability if the outputs of the memory elements are changing while the outputs of the combinational circuit that go to flip flop input are being sampled by the clock pulse.
2. One way of solving the feedback timing problem is to make the flip flop sensitive to the pulse 'transition' rather than the pulse duration (i.e. the negative transition of clock used).



3. Another way is to use the master slave configuration.
   Note that when the slave is activated the master is disabled and vice-versa.