INSTRUCTION MANUAL

Microprocessor
And
Assembly Language Programming Lab

(BTCS-408)

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DECLARATION

This Manual of Microprocessor and Assembly Language Programming Lab (BTCS-408) has been prepared by me as per syllabus of Microprocessor and Assembly Language Programming Lab (BTCS-408).

Signature

SYLLABUS

1. Introduction to 8085 kit.

2. Addition of two 8 bit numbers, sum 8 bit.

3. Subtraction of two 8 bit numbers.

4. Find 1’s complement of 8 bit number.

5. Find 2’s complement of 8 bit number.

6. Shift an 8 bit no. by one bit.

7. Find Largest of two 8 bit numbers.

8. Find Largest among an array of ten numbers (8 bit).

9. Sum of series of 8 bit numbers.

10. Introduction to 8086 kit.

11. Addition of two 16 bit numbers, sum 16 bit.

12. Subtraction of two 16 bit numbers.

13. Find 1’s complement of 16 bit number.

14. Find 2’s complement of 16 bit number.

INDEX

EXPERIMENT NO. 1

AIM: Introduction to 8085 kit.

A Microprocessor is a multipurpose, programmable, clock driven, register-based electronic device that reads binary instructions from a storage device called memory, accepts binary data as input and processes data according to those instructions, and provides results as output.

MPS 85-3 is an extremely powerful microprocessor trainer based on the popular 8085 CPU. It can be used as a Flexible instructional aid in academic institutions. Sophisticated features like powerful 2-pass Assembler and Text Editor allow the use of **MPS 85-3** for serious microcomputer development work in research institutions and R&D laboratories.

Following are the main features of MPS 85-3 :

- **MPS 85-3** can be operated either from on-board or from a CRT terminal through its RS 232 C interface.
- Keyboard and serial monitor programs support the entry of user programs, editing and relocation, debug facilities like breakpoints and single-stepping, direct port input/ output and full speed execution of user programs.
- 32 K Bytes of CMOS static RAM is provided with battery back-up option. Total on-board memory can be upto 64K Bytes.
- Allows multi-processor system design by supporting the HOLD and HLDA signals.
- STD bus compatible signals available on the bus connector for easy expansion.

Option Available

a. Interface Modules for training purpose (Calculator Keyboard, Elevator, Display, ADC with DAC, Dual Slope ADC, Dual DAC, Logic Controller, Traffic Lights, 8253 Demo, RTC, Tone Generator, Stepper Motor, Numerical Printer, etc.)

b. 8-bit, 16 Channel ADC

c. 26 Core Ribbon Cable Connector Set.

SPECIFICATIONS:

CPU	:8085 Operated at 3.072 MHz
Memory	:Three 28-pin JEDEC sockets offer 64K Bytes of memory as follows: 16K Bytes of firmware in one 27128 32K Bytes of static RAM Using one 62256 with optional battery backup

16K Bytes of PROM/ RAM (Optional) through Jumper selections allow this socket to accommodate 2764/ 27128/ 6264/ 62256

Firmware **:**

Serial and Keyboard Monitors.

Audio tape interface driver software.

Centronics printer interface driver software.

PROM Programming software.

Peripherals **:**

8279-5 :To control 32 keys keyboard and 6-digit, 0.5” seven segment LED display.

8253-5 :3 Programmable interval timers

Timer 0 is used for implementing single-step facility. Timer 1 is used for generating baud clock, Timer 2 is available to the user (Through jumper option, user can use Timer 1 also, if he does not use it for baud clock).

8251 A :For serial communication supporting all standard bauds from 110 to 19.200. (Baud is selected through on-board DIP switch)

8259 A : Programmable Interrupt Controller accepts 8 Interrupt signals from the auxiliary system connector.

8255-5 : (4 numbers) Two are used by the system to implement PROM Programmer, Audio Cassette Interface and Parallel Printer interface. The other two are available to user giving 48 programmable I/O Lines.

Interface Signals

CPU BUS: Demulitplexed and buffered TTL compatible signals brought-out to two 26 pin ribbon cable (spectra-strip type connectors)

Parallel I/O: 48 lines (2 X 8255-5) of TTL compatible bus brought out to two Spectra-strip type ribbon cable connectors.

Serial I/O : RS-232C with standard MODEM control signals through on-board 25 pin D-type female connector.

Cassette Interface Signals: Available on MIC and EAR sockets.

Parallel Printer Signals:

Centronics compatible Parallel Printer Interface signals available on a 25-pin D type female connector in IBM PC/ XT Compatible pin configuration.

Interrupts

All interrupts except TRAP (used for single-step implementation) are available to user.

Power Supply (Optional)

5V, (± 0.1V), 3.0A

+ 12V, (± 1.0V), 250 mA

- 12V, (± 1.0V), 250 mA

30V (± 2.0V), 100mA

Introduction to INTEL 8085

INTEL 8085 is an 8-bit, NMOS microprocessor. It is a 40 pin I.C. package fabricated on a single LSI chip. The INTEL 8085 uses a single $+5V_{d.c.}$ supply for its operation. Its clock speed is about 3MHz. The clock cycle is of 320 ns. The time for the clock cycle of the INTEL 8085AH-2, version is 200 ns. It has 80 basic instructions and 246 opcodes.

Memory

Program, data and stack memories occupy the same memory space. The total addressable memory size is 64 KB.

Program memory - program can be located anywhere in memory. Jump, branch and call instructions use 16-bit addresses, i.e. they can be used to jump/branch anywhere within 64 KB. All jump/branch instructions use absolute addressing.

Data memory - the processor always uses 16-bit addresses so that data can be placed anywhere.

Stack memory is limited only by the size of memory. Stack grows downward.

First 64 bytes in a zero memory page should be reserved for vectors used by RST instructions.

Interrupts

The processor has 5 interrupts. They are presented below in the order of their priority (from lowest to highest):

INTR is maskable 8080A compatible interrupt. When the interrupt occurs the processor fetches from the bus one instruction, usually one of these instructions:

- One of the 8 RST instructions (RST0 - RST7). The processor saves current program counter into stack and branches to memory location N * 8 (where N is a 3-bit number from 0 to 7 supplied with the RST instruction).
- CALL instruction (3 byte instruction). The processor calls the subroutine, address of which is specified in the second and third bytes of the instruction.

RST5.5 is a maskable interrupt. When this interrupt is received the processor saves the contents of the PC register into stack and branches to 2Ch (hexadecimal) address.

RST6.5 is a maskable interrupt. When this interrupt is received the processor saves the contents of the PC register into stack and branches to 34h (hexadecimal) address.

RST7.5 is a maskable interrupt. When this interrupt is received the processor saves the contents of the PC register into stack and branches to 3Ch (hexadecimal) address.

Trap is a non-maskable interrupt. When this interrupt is received the processor saves the contents of the PC register into stack and branches to 24h (hexadecimal) address.

All maskable interrupts can be enabled or disabled using EI and DI instructions. RST 5.5, RST6.5 and RST7.5 interrupts can be enabled or disabled individually using SIM instruction.

I/O ports

256 Input ports
256 Output ports

Registers

Accumulator or A register is an 8-bit register used for arithmetic, logic, I/O and load/store operations.

Flag is an 8-bit register containing 5 1-bit flags:

- Sign - set if the most significant bit of the result is set.
- Zero - set if the result is zero.
- Auxiliary carry - set if there was a carry out from bit 3 to bit 4 of the result.
- Parity - set if the parity (the number of set bits in the result) is even.
- Carry - set if there was a carry during addition, or borrow during subtraction/comparison.

General registers:

- 8-bit B and 8-bit C registers can be used as one 16-bit BC register pair. When used as a pair the C register contains low-order byte. Some instructions may use BC register as a data pointer.
- 8-bit D and 8-bit E registers can be used as one 16-bit DE register pair. When used as a pair the E register contains low-order byte. Some instructions may use DE register as a data pointer.
- 8-bit H and 8-bit L registers can be used as one 16-bit HL register pair. When used as a pair the L register contains low-order byte. HL register usually contains a data pointer used to reference memory addresses.

Stack pointer is a 16 bit register. This register is always incremented/decremented by 2.

Program counter is a 16-bit register.

Instruction Set

8085 instruction set consists of the following instructions:

- Data moving instructions.
- Arithmetic - add, subtract, increment and decrement.
- Logic - AND, OR, XOR and rotate.
- Control transfer - conditional, unconditional, call subroutine, return from subroutine and restarts.
- Input/Output instructions.
- Other - setting/clearing flag bits, enabling/disabling interrupts, stack operations, etc.

Addressing modes

Register - references the data in a register or in a register pair.
Register indirect - instruction specifies register pair containing address, where the data is located.
Direct.
Immediate - 8 or 16-bit data.

EXPERIMENT NO. 2

AIM: Write a program to add two 8 bit no's, result of 8bits.

APPARATUS: Battery, 8085 kit, power supply 220V.

INSTRUCTIONS USED:

1: The instruction MVI A, 8 bit data transfers the 8 bit number to the accumulator.

2: The instruction MVI A, 8 bit data transfers the 8 bit number to the accumulator.

3: The instruction ADD B adds the number in B to number in A.

4: This instruction ie; STA 8500 H stores the result in the memory location.

5: HLT instruction ends the program

MEMORY ADDRESS	MNEMONICS	MACHINE CODES	COMMENTS
8000	MVI A, 20H	3E 20	LOADS THE NUMBER IN ACCUMULATOR.
8002	MVI B, 30 H	06 30	LOADS THE NUMBER IN REGISTER B.
8004	ADD B	80	ADDS THE CONTENTS STORED IN B TO THE ACC
8005	STA 8503 H	32 03 85	STORES THE RESULT AT 8503 H.
8008	HLT	76	STOP.

Results:
8001-30 H

8003-20 H
8503: O/P= 50 H

EXPERIMENT NO. 3

AIM: Write a program to add two 8 bit no's, result of 16bits.

APPARATUS: Battery, 8085 kit, power supply 220V.

INSTRUCTIONS USED:

1: LXI H (LOAD REGISTER PAIR IMMEDIATELY) loads 16 bit data in register pair designated by operand.
2: MOV A, M copies the data byte into accumulator from the memory specified by the address in H-L pair
3: INX H (INCREMENT REGISTER PAIR) increments the contents of the register pair by one.
4: ADD adds the contents of memory to accumulator.
5: JNC ahead changes the program sequence to the specified 16 bit address if carry flag is set.
6: STA address (STORE ACCUMULATOR DIRECT) copies the contents of the accumulator to the memory location specified in the instruction
7: MOV A, C copies the data byte from accumulator to the memory specified by 16 bit address.
8: HLT (HALT) finishes the execution of the current instruction and stops any further execution.

MEMORY ADDRESS	MNEMONICS	MACHINE CODE	COMMENTS
8000	LXI H,8501	21,01,85	Address of first no in H-L pair
8003	MVI C,00H	0E,OO	MSB’s of sum
8005	MOV A,M	7E	First no in accumulator
8006	INX H	23	Increment address in H-L pair
8007	ADD M	86	Add first no & second no
8008	JNC AHEAD	D2,0C,80	Is carry? No, go to label ahead
800B	INR C	0C	Yes, increment C
800C(AHEAD)	STA 8503	32,03,85	LSB’s of sum in 8503
800F	MOV A,C	79	MSB’s of sum in accumulator
8010	STA 8504	32,04,85	MSB’s of sum in 8504
8013	HLT	76	Stop

Result:
8501: 98 H   8502: 80 H
8503: 18 H   8504: 01 H

EXPERIMENT NO. 4

AIM: Write a program to subtract two 8 bit numbers.

APPARATUS: Battery, 8085 kit, power supply 220V.

INSTRUCTIONS USED:

1: The instruction MVI A, 8 bit data transfers the 8 bit number to the accumulator.

2: The instruction MVI A, 8 bit data transfers the 8 bit number to the accumulator.

3: The instruction SUB B subtracts the number in B from number in A.

4: This instruction ie; STA 8500 H stores the result in the memory location.

5: HLT instruction ends the program

MEMORY ADDRESS	MNEMONICS	MACHINE CODES	COMMENTS
8000	MVI A, 30H	3E 20	LOADS THE NUMBER IN ACCUMULATOR.
8002	MVI B, 20 H	06 30	LOADS THE NUMBER IN REGISTER B.
8004	SUB B	90	ADDS THE CONTENTS STORED IN B TO THE ACC
8005	STA8503 H	32 03 85	STORES THE RESULT AT 8503 H.
8008	HLT	76	STOP.

Results:
8001-20 H
8003-30 H

8503: O/P= 10 H

EXPERIMENT NO. 5 (a)

AIM: To find one's complement of 8 bit no.

APPARATUS: 8085 kit, 220 V power supply, manual, and battery.

INSTRUCTIONS USED IN THE PROGRAM:

1: The instruction MVI a, 8 bit data transfers the 8 bit number to the accumulator.

2: Next instruction CMA takes the complement of the no.

3: This instruction ie; STA 8500 H stores the result in the memory location.

4: HLT instruction ends the program.

MEMORY ADDRESS	MNEMONICS	MACHINE CODES	COMMENTS
8000	MVI A,22H	3E 22	LOADS 8-BIT DATA IN A.
8002	CMA	2F	COMPLEMENTS THE CONTENTS IN ACCUMULATOR.
8003	STA 8500H	32 00 85	STORES THE CONTENTS OF ACC. AT 8500H.
8005	HLT	76	STOP

Result:

8001: 22 H

8500: DD H

EXPERIMENT NO. 5 (b)

AIM: To find one's complement of 16 bit no.

APPARATUS: 8085 kit, 220 V power supply, manual, and battery.

INSTRUCTIONS USED IN THE PROGRAM:

1: LDA (LOAD ACCUMULATOR DIRECT) load the contents of memory into accumulator
2: CMA complements the contents of accumulator (i.e.) lower byte of the number.
3: This instruction ie; STA 8501 H stores the result in the memory location.
4: LDA (LOAD ACCUMULATOR DIRECT) load the contents of memory into accumulator (i.e. upper byte)
5: CMA complements the contents of accumulator (i.e.) lower byte of the number.
6: This instruction ie; STA 8501 H stores the result in the memory location.
7: HLT instruction ends the program.

MEMORY ADDRESS	MNEMONICS	MACHINE CODE	COMMENTS
8000	LDA 8050 H	3A 50 80	LOAD ACC. WITH LOWER BYTE OF NUMBER
8003	CMA	2F	COMPLEMENTS THE CONTENTS IN ACCUMULATOR.
8004	STA 8501 H	32 01 85	STORES THE CONTENTS AT THE GIVEN LOCATION.
8007	LDA 8051H	3A 51 80	LOAD ACC. WITH UPPER BYTE OF NUMBER
800A	CMA	2F	COMPLEMENTS CONTENTS IN ACCUMULATOR.
800B	STA 8502 H	32 02 85	STORES THE CONTENTS AT THE GIVEN LOCATION.
800E	HLT	76	STOP

Result: 8050: 20 H
8051: 10 H
8501: DF H
8502: EF H

EXPERIMENT NO. 6 (a)

AIM: To find two's complement of 8 bit no.

APPARATUS: 8085 kit, 220 V power supply, manual, and battery.

INSTRUCTIONS USED IN THE PROGRAM:

1: The instruction MVI a, 8 bit data transfers the 8 bit number to the accumulator.

2: Next instruction CMA takes the complement of the no.

3: The instruction ADI 01H adds 1 to the complement of the number in accumulator.

3: This instruction ie; STA 8500 H stores the result in the memory location.

4: HLT instruction ends the program.

MEMORY ADDRESS	MNEMONICS	MACHINE CODES	COMMENTS
8000	MVI A,22H	3E 22	LOADS 8-BIT DATA IN A.
8002	CMA	2F	COMPLEMENTS THE CONTENTS IN ACCUMULATOR.
8003	ADI 01H	C6 01	ADDS 01H TO CONTENTS OF ACC.
8005	STA 8500	32 00 85	STORES THE CONTENTS OF ACC. AT 8500H.
8008	HLT	76	STOP

Result:

8001: 22 H
8500: DE H

EXPERIMENT NO. 6 (b)

AIM: To find two's complement of 16 bit no.

APPARATUS: 8085 kit, 220 V power supply, manual, and battery.

INSTRUCTIONS USED IN THE PROGRAM:

1: The 8 LSB's are in the memory location 8501 H.
2: The address 8501 is placed in HL pair.
3: The 8 LSB's of the no. are transferred from 8501 to the accumulator.
4: The instruction CMA takes one's complement of the LSB's.
5: The 8 LSB's of the result are stored in the memory location.
6: This result is incremented by one and stored at memory location 8503.
7: The carry resulting from the addition of one to 1’s compliment is stored in register B.
8: 8 MSB’s of the no. are taken and 1’s complement is obtained.
9: The carry is added to it.
10: 8 MSB’s of the result are stored in 2504.
11: In case of no carry, the program jumps from JNC and go to INXH and the contents of the register B is not incremented.
12: The addition of zero to one’s complement of 8 MSB’s does not affect the result.
13: HLT ends the program.

MEMORY ADDRESS	MNEMONICS	MACHINE CODE	COMMENTS
8000	LXI H,8501	21 01 85	Address of 8 LSB’S of no.
8003	MVI B,00H	06 00	Use reg. b to store carry
8005	MOV A,M	7E	8 LSB’S of the no. in acc.
8006	CMA	2F	1’s complement of 8 LSB’S of the no.
8007	ADI 01H	C6 01	2’s complement of 8 LSB’S of the no.
8009	STA 8503	32 03 85	Store 8 LSB’S of the result
800C	JNC GO	D2 10 20	Jump if carry
800F	INR B	04	Store carry

8010	INX H	23	Address of 8 MSB’S of no.
8011	MOV A,M	7E	8 MSB’S in acc.
8012	CMA	2F	1’s complement of 8 MSB’S
8013	ADD B	80	Add carry
8014	STA 8504	32 04 85	Store 8 MSB’S of the result
8017	HLT	76	Stop.

Result:

8501: 8C H	8503: 74 H
8502: 5B H	8504: A4 H

EXPERIMENT NO. 7 (a)

AIM: Write a program to shift an 8 bit no left by 1 bit.

APPARATUS: Battery, 8085 kit, power supply 220V

INSTRUCTIONS USED:

1: LDA (LOAD ACCUMULATOR DIRECT) load the contents of memory into accumulator.
2: DAD A (ADD REGISTER PAIR TO HL PAIR) shifts the contents of the accumulator to the left by one bit.
3: STA address (STORE ACCUMULATOR DIRECT) copies the contents of the accumulator to the memory location specified in the instruction.
4: HLT (HALT) finishes the execution of the current instruction and stops any further execution.

MEMORY ADDRESS	MNEMONICS	MACHINE CODE	COMMENTS
8000	LDA 8501	3A,01,85	Get data in accumulator
8003	ADD A	87	Shift in left by 1 bit
8004	STA 8502	32,02,85	Store result in address 8502
8007	HLT	76	stop

Result:

8501: 40 H

8502: 80 H

EXPERIMENT NO. 7 (b)

AIM: Write a program to shift 16 bit no left by one bit.

APPARATUS: Battery, 8085 kit, power supply 220V.

INSTRUCTIONS USED:

1: LHLD (LOAD H-L PAIR DIRECT) loads the contents of the memory location , whose address is given in the instruction.
2: DAD A (ADD REGISTER PAIR TO H-L PAIR) shifts the contents of the accumulator to the left by one bit.
3: SHLD (STORE H-L PAIR DIRECT) stores the result given in the HL pair at a specified memory location.
4: HLT (HALT) finishes the execution of the current instruction and stops any further execution.

MEMORY ADDRESS	MNEMONICS	MACHINE CODE	COMMENTS
8000	LHLD 8501	2A,01,85	Get the data in H-L pair
8003	DAD H	29	To shift left bit by 1
8004	SHLD 8503	22,03,85	Store result in 8503,8504
8007	HLT	76	stop

Result:

Input: 8501: 40 H
8502: 40 H
Output: 8503: 80 H
8504: 80 H

EXPERIMENT NO. 8

AIM: Write a program to find largest of two 8 bit numbers.

APPARATUS: Battery, 8085 kit, power supply 220V.

INSTRUCTIONS USED:
1: The instruction MVI A, 8 bit data transfers the 8 bit number to the accumulator.
2: The instruction MVI A, 8 bit data transfers the 8 bit number to the accumulator.
3: CMP B compares the contents of B with contents of A.
4: If there is no carry i.e. the number in A is greater, then the o/p is stored else the contents are interchanged with JNC and MOV A, B.
5: STA address (STORE ACCUMULATOR DIRECT) copies the contents of the accumulator to the memory location specified in the instruction.
6: HLT (HALT) finishes the execution of the current instruction and stops any further execution.

MEMORY ADDRESS	MNEMONICS	MACHINE CODE	COMMENTS
8000	MVI A, 15H	3E 15	LOADS THE NUMBER IN ACCUMULATOR
8002	MVI B,05 H	06 05	LOADS THE NUMBER IN REGISTER B.
8004	CMP B	B8	COMPARE THE CONTENTS OF B WITH A
8005	JNC(LOOP)	D2 09 80	JUMP TO LOOP IF THERE IS NO CARRY
8008	MOV A, B	78	MOVE THE CONTENTS OF B TO A.
8009(LOOP)	STA 8055 H	32 55 80	STORE THE OUTPUT AT 8055 H
800C	HLT	76	STOP THE PROGRAM

EXPERIMENT NO. 9

AIM: Write a program to find largest among an array of 10 numbers..

APPARATUS: Battery, 8085 kit, power supply 220V

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1: The instruction LXI, H transfers the address of the 1st number to H-L pair.

2: The instruction MVI C , 8 bit data transfers the 8 bit number to the C and makes C as a counter.

3: 1st number is transferred to A from memory.

4: INX H is used to get the next number in memory.

5:CMP M compares the contents of memory with A.

6: If there is no carry i.e. the number in A is greater, and then the o/p is stored else the contents are interchanged with JNC and MOV A, M.

7: counter is decremented and is checked for count to zero.

8: STA address (STORE ACCUMULATOR DIRECT) copies the contents of the accumulator to the memory location specified in the instruction.

9: HLT (HALT) finishes the execution of the current instruction and stops any further execution.

MEMORY ADDRESS	MNEMONICS	MACHINE CODE	COMMENTS
8000	LXI H, 8050 H	21 50 80	LOADS H-L PAIR WITH THE NUMBER AT 8050 H.
8003	MVI C,0AH	0E 0A	MAKE REGISTER C AS A COUNTER.
8005	MOV A, M	7E	MOVE CONTENTS OF MEMORY TO ACCUMULATOR.
8006	DCR C	0D	DECREMENT THE COUNTER.
8007(LOOP)	INX H	23	INCREMENT H-L PAIR.
8008	CMP M	BE	COMPARE THE CONTENTS OF MMEORY WITH CONTENTS OF ACCUMULATOR.
8009	JNC 800D(AHEAD)	D2 0D	JUMP IF THERE IS NO CARRY TO

		80	LOOP.
800C	MOV A, M	7E	YES, GET GREAT E R NUMBER IN ACCUMULATOR.
800D(AHEAD)	DCR C	0D	DECREMENT COUNT
800E	JNZ LOOP	C2 07 80	GO TO LOOP IF COUNT IS NOT ZERO.
8011	STA 8450 H	32 50 84	STORE RESULT AT 8450 H
8014	HLT	76	STOP THE PROGRAM

Result:

8050: 01H
8051: 02H
8052: 03H
8053: 04H
8054: 05H
8055: 06H
8056: 07H
8057: 08H
8058: 09H
8059: 20H

8450: 20 H

EXPERIMENT NO. 10

AIM: Write a program to find sum of series of 8 bit no and result is also 8 bit.

APPARATUS: Battery, 8085 kit, power supply 220V.

INSTRUCTIONS USED:

1: LXI H (LOAD REGISTER PAIR IMMEDIATELY) loads 16 bit data in register pair designated by operand.
2: MOV C M, copies the contents of the source register to the destination register.
3: MVI A (MOVE IMMEDIATE TO ACCUMULATOR) moves the data specified in the instruction to accumulator.
4: INX H (INCREMENT REGISTER PAIR) increments the contents of the register pair by one.
5: ADD adds the contents of register with the contents of the memory and stores in the same.
6: DCR C (DECREMENT REGISTER) decrements the counter by one.
7: JNZ loop (CHANGE THE SEQUENCE) changes the sequence of the program to specified 16 bit address, carry flags.
8: STA address (STORE ACCUMULATOR DIRECT) copies the contents of the accumulator to the memory location specified in the instruction.
9: HLT (HALT) finishes the execution of the current instruction and stops any further execution.

MEMORY ADDRESS	MNEMONICS	MACHINE CODE	COMMENTS
8000	LXI H,8500	21,00,85	Address for the count in H-L pair
8003	MOV C,M	4E	Move from memory to register C
8004	MVI A,00H	3E,00	Initial values of sum is 0
8006	INX H	23	Address of next data in H-L pair
8007	ADD M	86	Previous sum+ next no
8008	DCR C	0D	Decrement counter
8009	JNZ 8006	C2,06,80	Jump to 8006 if c=! 0
800C	STA 8450	32,50,84	Store sum in 8504
800F	HLT	76	stop

Result:

```
8500: 05 H    //counter
8501: 01 H
8502: 02 H
8503: 03 H
8504: 04 H
8505: 05 H

8450: 0FH
```

EXPERIMENT NO. 11

AIM: **Introduction to 8086 kit and operations on 16-bit number.**

ESA 86/88-3 is an advanced, general-purpose microcomputer system that can be operated with 8086 or 8088 CPU and provides the user a powerful and complete environment for 8086 based programming and applications development

ESA 86/88-3 can be operated in standalone mode using optional PC/AT keyboard and LCD or in serial mode with the host computer through its RS 232C/RS 485 interface.

It works with either 8086 or 8088 CPU - operating at 8 MHz in maximum mode.
The memory of ESA 86/88-3 can be configured in various ways and allows the user to realize the full 1M Byte addressing capability of the CPU.
The following DIP Switch setting selects the appropriate CPU.

DIP SW7	**Processor**
OFF	8086
ON	8088

The selection of the desired mode of operation is done as follows:

DIP SW5	**DIP SW8**	**Operational mode**
OFF	X	Stand-alone mode
ON	OFF	Serial mode with RS 485 interface
ON	ON	Serial mode with RS 232C interface

(X = Don’t care)

DIP SW6	**Printer Driver**
OFF	Disabled
ON	Enabled

The following sign-on message should appear on the console depending on the processor selected.

```
                    ESA 86 MONITOR Vx.y
```

(V x.y indicates Version x and Revision y)

The sign-on message is followed by the command prompt, "." in the next line.

ESA 86/88-3 is ready for operation in Serial mode. If an LCD interface is used, the following message appears on the Display.

```
     ESA 86 MONITOR Vx.y
     SER:9600 P:86
```

For stand-alone mode operation:

1. Connect a PC Keyboard to the DIN connector provided
2. Connect the power supply of required capacity to ESA 86/88-3 and Power ON the trainer.

Now if 8086 is installed, the following sign-on message will appear on the LCD. The sign-on message is followed by the command prompt, "." in the next line.

```
           ESA 86 MONITOR Vx.y
            KBD P:86
```

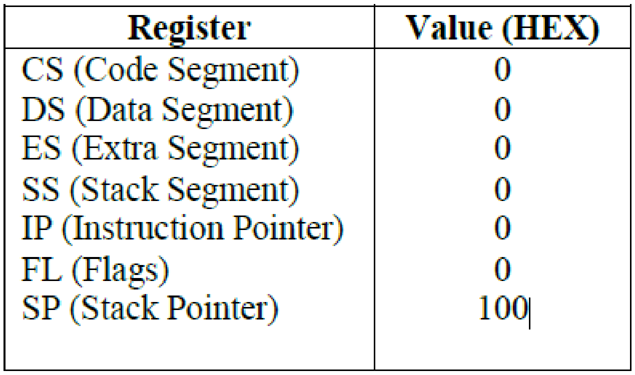
Now ESA 86/88-3 is ready for operation in the keyboard mode.

General Operation:-

On Power ON/Reset, all information about the previous user program is lost and the registers may acquire new data. However the contents of user RAM are not disturbed if onboard RESET is used.

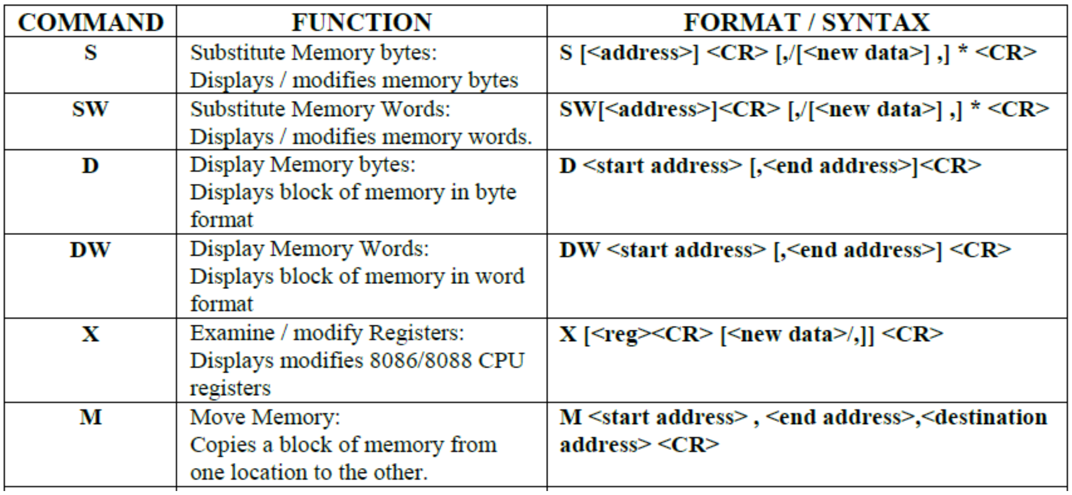
Resetting the trainer initializes the segment & status registers of the CPU as described below.

Table: Register Initialization



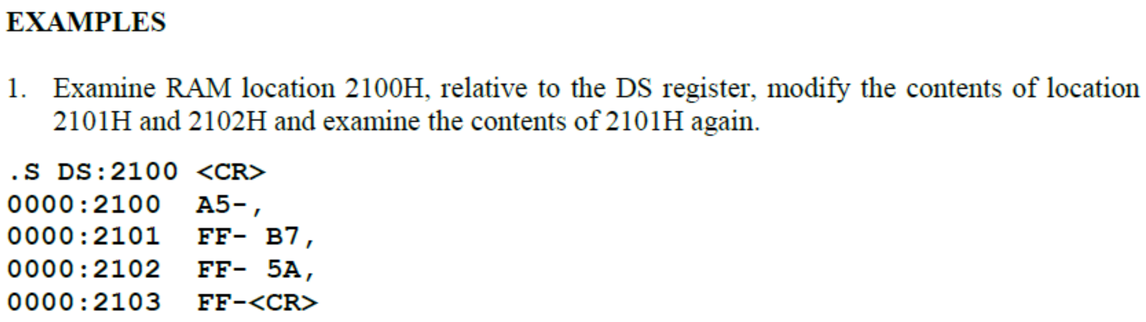
Register	Value (HEX)
CS (Code Segment)	0
DS (Data Segment)	0
ES (Extra Segment)	0
SS (Stack Segment)	0
IP (Instruction Pointer)	0
FL (Flags)	0
SP (Stack Pointer)	100

Table: ESA 86/88-3 MONITOR COMMANDS



COMMAND	FUNCTION	FORMAT / SYNTAX
S	Substitute Memory bytes: Displays / modifies memory bytes	**S [<address>] <CR> [,/[<new data>] ,] * <CR>**
SW	Substitute Memory Words: Displays / modifies memory words.	**SW[<address>]<CR> [,/[<new data>] ,] * <CR>**
D	Display Memory bytes: Displays block of memory in byte format	**D <start address> [,<end address>]<CR>**
DW	Display Memory Words: Displays block of memory in word format	**DW <start address> [,<end address>] <CR>**
X	Examine / modify Registers: Displays modifies 8086/8088 CPU registers	**X [<reg><CR> [<new data>/,]] <CR>**
M	Move Memory: Copies a block of memory from one location to the other.	**M <start address> , <end address>,<destination address> <CR>**

Substitute Commands



EXAMPLES

1. Examine RAM location 2100H, relative to the DS register, modify the contents of location 2101H and 2102H and examine the contents of 2101H again.

```
.S DS:2100 <CR>
0000:2100  A5-,
0000:2101  FF- B7,
0000:2102  FF- 5A,
0000:2103  FF-<CR>
```

```
.S DS:2101 <CR>
0000:2101  B7- <CR>
.
```

Note: Here DS is set at 0000. Hence the segment value displayed will be 0000.

2. Examine ROM location FF00:9CH and trying to modify the same.

```
.S FF00:9C<CR>
FF00:009C  FF- 44,?<CR>
.
```

3. Examine word at location 2120 H relative to DS register. Assume that DS is set to 2000

```
.SW DS:2120 <CR>
2000:2120 A1F4 <CR>
.
```

Display Command

1. Display contents of location 140H relative to DS register. Assume DS is set to 0000.

```
.D DS:140  <CR>
0000:0140 A0
.
```

Examine Command

1. Examine the contents of all the registers.

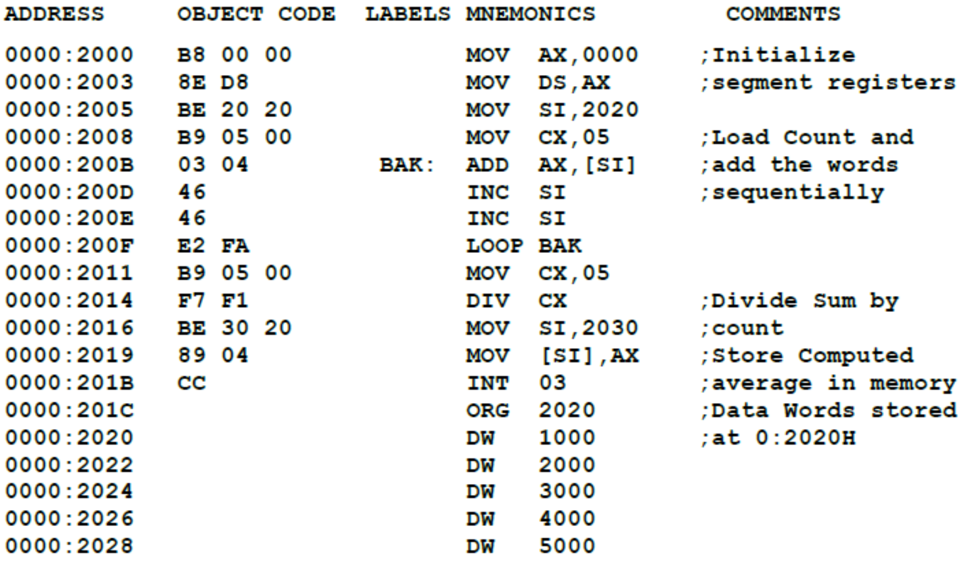
```
.X <CR>
```

```
AX=1182  BX=A113
CX=000F  DX=1242
SP=0100  BP=4020
SI=6020  DI=6F20
```

Operations on 16-bit numbers

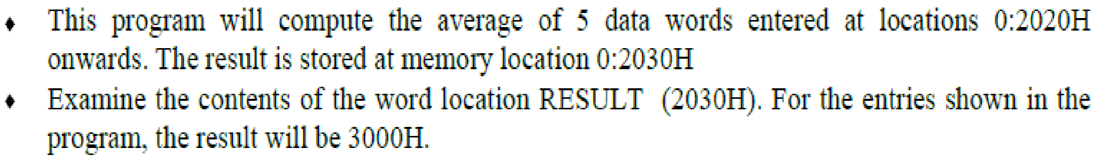
Example:-

This program computes the average of given word values stored in memory



```
ADDRESS      OBJECT CODE   LABELS MNEMONICS          COMMENTS

0000:2000    B8 00 00             MOV  AX,0000      ;Initialize
0000:2003    8E D8                MOV  DS,AX        ;segment registers
0000:2005    BE 20 20             MOV  SI,2020
0000:2008    B9 05 00             MOV  CX,05        ;Load Count and
0000:200B    03 04          BAK:  ADD  AX,[SI]      ;add the words
0000:200D    46                   INC  SI           ;sequentially
0000:200E    46                   INC  SI
0000:200F    E2 FA                LOOP BAK
0000:2011    B9 05 00             MOV  CX,05
0000:2014    F7 F1                DIV  CX           ;Divide Sum by
0000:2016    BE 30 20             MOV  SI,2030      ;count
0000:2019    89 04                MOV  [SI],AX      ;Store Computed
0000:201B    CC                   INT  03           ;average in memory
0000:201C                         ORG  2020         ;Data Words stored
0000:2020                         DW   1000         ;at 0:2020H
0000:2022                         DW   2000
0000:2024                         DW   3000
0000:2026                         DW   4000
0000:2028                         DW   5000
```



- This program will compute the average of 5 data words entered at locations 0:2020H onwards. The result is stored at memory location 0:2030H
- Examine the contents of the word location RESULT (2030H). For the entries shown in the program, the result will be 3000H.