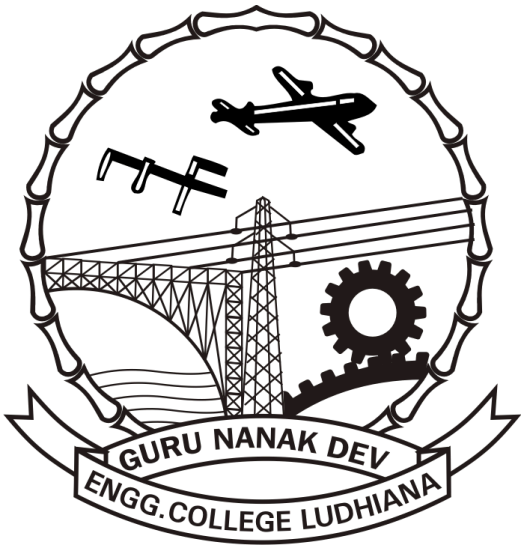
INSTRUCTION MANUAL

Digital Circuits & Logic Design Lab

(BTCS 308)



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DECLARATION

This Manual of Digital Circuits & Logic Design Lab (BTCS-308) has been prepared by me as per syllabus of Digital Circuits & Logic Design Lab (BTCS-308).

Signature

SYLLABUS

BTCS 308 Digital Circuits & Logic Design Lab

External Marks: 20 **Internal Marks: 30** **Total Marks: 50**

1. Study of Logic Gates: Truth-table verification of OR, AND, NOT, XOR, NAND and NOR gates; Realization of OR, AND, NOT and XOR functions using universal gates.
2. Half Adder / Full Adder: Realization using basic and XOR gates.
3. Half Subtractor / Full Subtractor: Realization using NAND gates.
4. 4-Bit Binary-to-Gray & Gray-to-Binary Code Converter: Realization using XOR gates.
5. 4-Bit and 8-Bit Comparator: Implementation using IC7485 magnitude comparator chips.
6. Multiplexer: Truth-table verification and realization of Half adder and Full adder using IC74153 chip.
7. Demultiplexer: Truth-table verification and realization of Half subtractor and Full subtractor using IC74139 chip.
8. Flip Flops: Truth-table verification of JK Master Slave FF, T-type and D-type FF using IC7476 chip.
9. Asynchronous Counter: Realization of 4-bit up counter and Mod-N counter using IC7490 & IC7493 chip.
10. Synchronous Counter: Realization of 4-bit up/down counter and Mod-N counter using IC74192 & IC74193 chip.
11. Shift Register: Study of shift right, SIPO, SISO, PIPO, PISO & Shift left operations using IC7495 chip.
12. DAC Operation: Study of 8-bit DAC (IC 08/0800 chip), obtain staircase waveform using IC7493 chip.
13. ADC Operations: Study of 8-bit ADC.

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EXPERIMENT NO.1

Aim: Verification of the truth tables of the logic gates.

Apparatus : Regulated power supply , trainer kit , IC's 7400,7402,7404,74098,7432,7486,tweezer,connecting leads etc.

Theory:

AND Gate (7408)

A circuit which perform an and operation is shown in figure (a).It has N inputs (N>=2) and one output. Digital signals are applied at the input terminals marked A, B……N, the other terminals being ground which is not shown in the diagram. The output is obtained at the output terminal marked Y and it is also a digital signal.

Mathematically, it is written as

Y = A AND B AND C…….AND N

Y =A.B.C……..N

Y = ABC……..N

For 2 inputs,

Y = AB

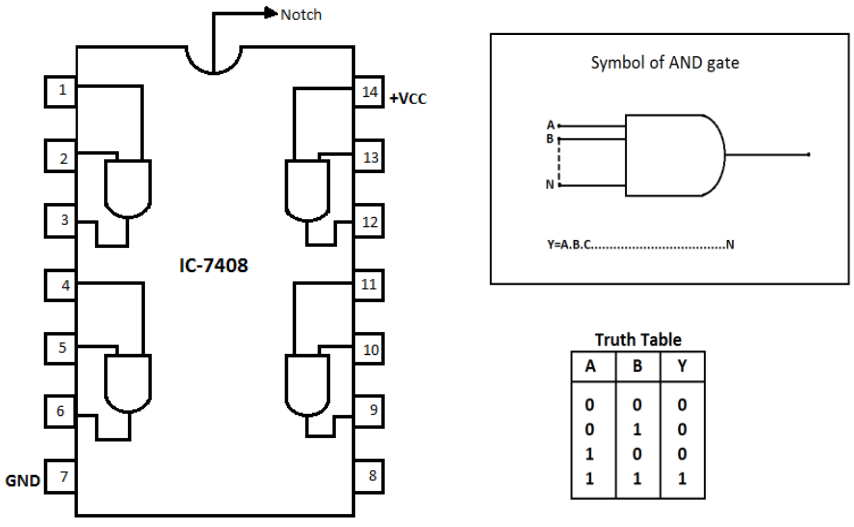


Fig. (a)

OR Gate(7432)

The adjoin Figure(b) shows a OR gate with N inputs(N>=2) and one output. The OR operation is defined as the operation in which output is 1 if one of the input is 1. Its logical equation is given by

Y= A OR B OR C……..OR N

Y= A+B+C+…….+N

For 2 inputs,

Y= A+B

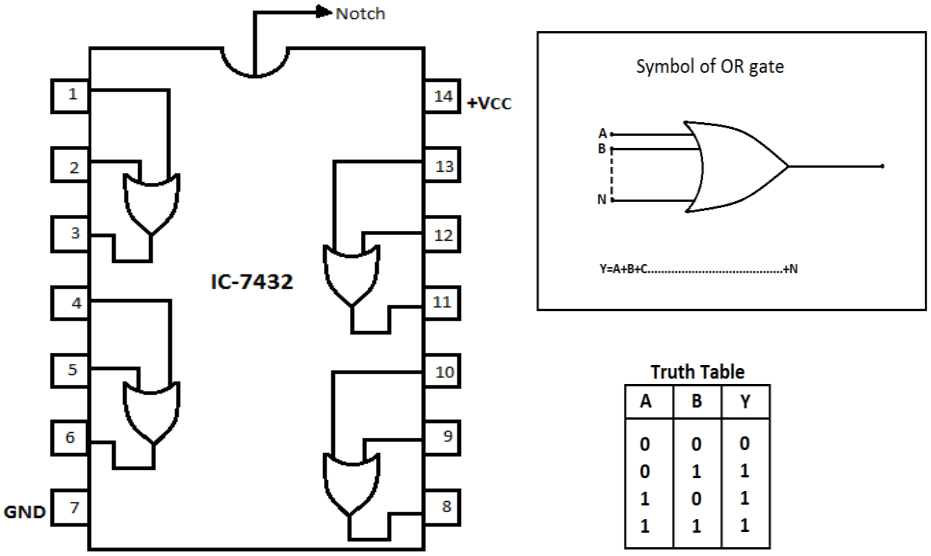


Fig. (b)

NAND Gate(7400)

The adjoining figure(c) shows a NAND gate. The NOT-AND operation is known as NAND operation.This gate is considered as an AND gate followed by a NOT gate.

The operation of this circuit (figure(b)) can be described in the following way

Output of AND gate(Y1)

$$Y1 = AB\ldots\ldots\ldots\ldots\ldots\ldots N$$

Output of NOT gate can be written as

$$Y = \overline{Y1} = \overline{(AB\ldots\ldots\ldots\ldots\ldots..N)}$$

For 2 inputs

$$Y = \overline{AB}$$

A bubble on the output side of NAND gate represents NOT operation, inversion or complementation.

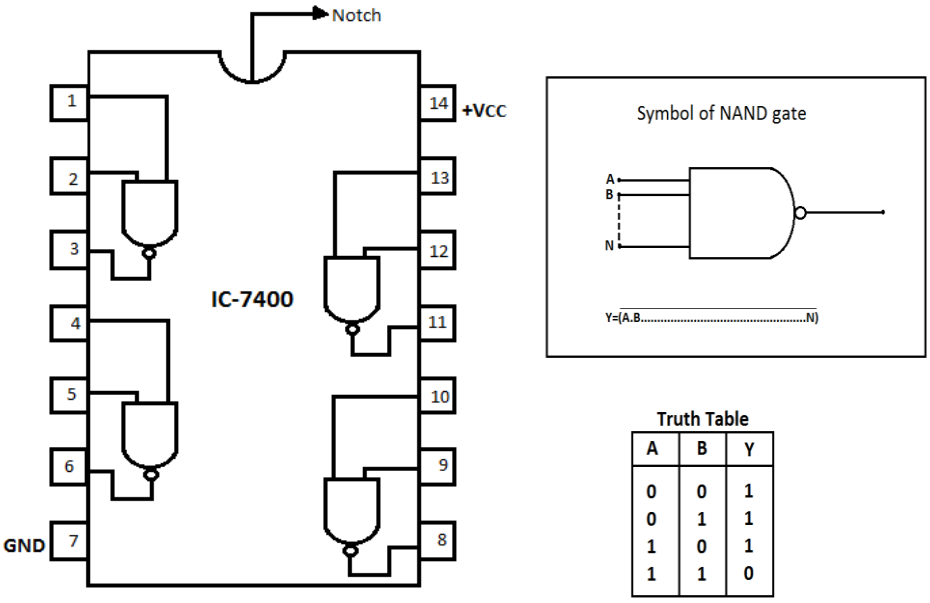


Fig. (c)

NOR Gate(7402)

The adjoining figure(d) shows a NOR gate. The OT-OR operation is known as the NOR operation. This gate is considered as an OR gate followed by a NOT gate.

The operation of this circuit (figure(d)) can be described in the following way

Output of OR gate Y1 can be written as

$$Y1 = A+B+\ldots\ldots\ldots\ldots\ldots\ldots+N$$

And the output of NOT gate Y can be written as

$$Y = \overline{Y1} = \overline{(A+B+\ldots\ldots\ldots\ldots+N)}$$

For 2 inputs

$$Y = \overline{A+B}$$

A bubble on the output side of NOR gate represents NOT operation, inversion or complementation.

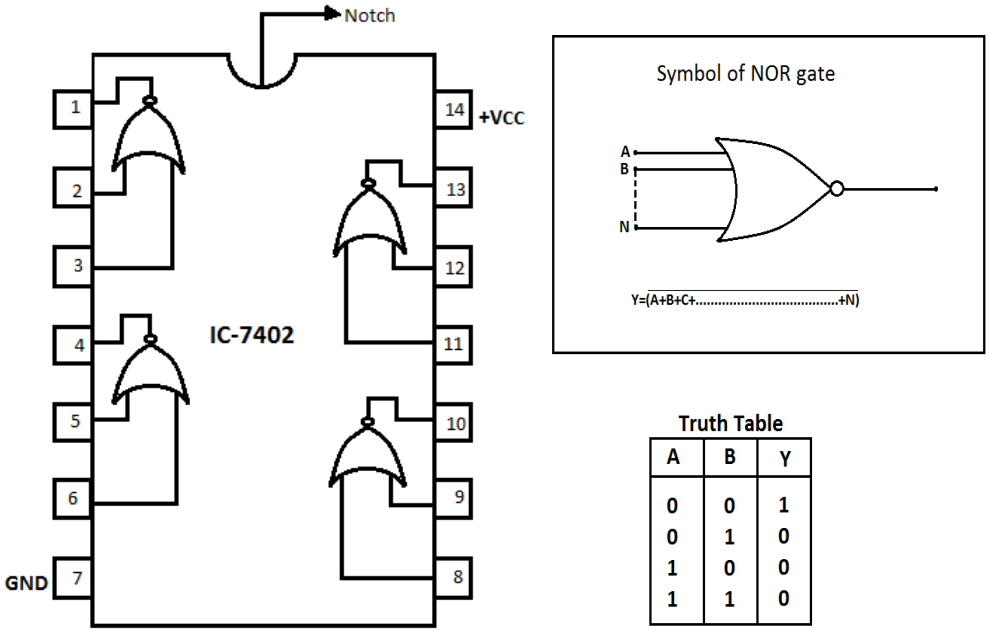


Fig. (d)

NOT Gate(7404)

The adjoining figure(e) shows a NOT gate which is also known as inverter. It has one input(A) and one output(Y) and the logical equation is written as

$$Y = \text{NOT } A$$

$$Y = \overline{A}$$

It is read as Y equals NOT A or Y equals compliments of A. It is also referred to as an inversion or complementation.

The presence of a small circle, known as the bubble always denote inversion in digital circuits.

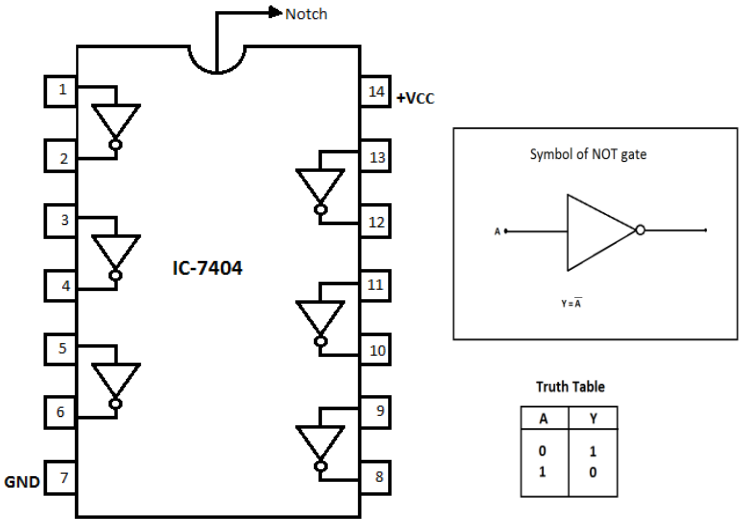


Fig. (e)

EX-OR Gate(7486)

The adjoining figure(f) shows an EX-OR gate. EX-OR operation is widely used in digital circuits. It is not a basic operation and can be performed using the basic gates ----- AND,OR and NOT. Its logic equation is

$$Y = A \text{ EX-OR } B$$

$$Y = A \oplus B$$

$$Y = \overline{A}B + A\overline{B}$$

When both inputs are same the output is 0, whereas when inputs are not same, the output is 1.

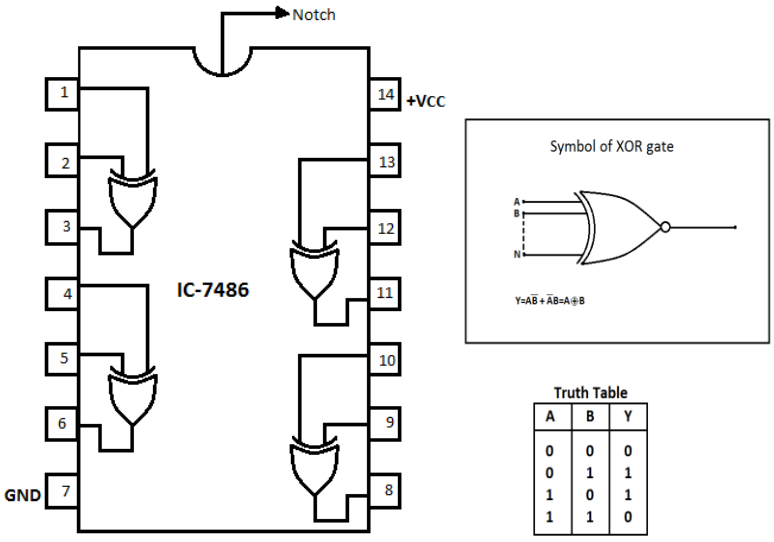


Fig. (f)

Procedure :

1. Insert the desired IC into the bread board present in the trainer kit.
2. To verify the truth table of AND,OR,NAND,EX-OR gate apply the input at 1st and 2nd pin and take the output at 3rd pin. Put GND and Vcc at pins 7 and 14 of the IC's.
3. To verify the truth table of NOR gate, apply the input at 2nd and 3rd pin and take output at 1st pin. For NOT gate input is given at 1st pin and output is taken at 2nd pin.
4. Remove the IC's with the help of tweezers.

Result : The truth table of all the logic gates has been verified.

Precautions :

1. Connections should be neat and clean.
2. Insert and remove the IC's with care.
3. Apply GND at pin no. 7 and Vcc at pin no. 14 of both the IC's.

EXPERIMENT NO. 2

AIM: - Realization of basic gates using universal NAND and NOR gates.

APPARATUS: - Power Supply, trainer kit, connecting leads, IC 7400(NAND), IC7402(NOR), tweezers.

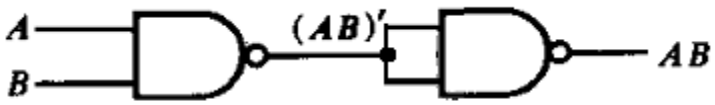
THEORY:- NAND and NOR are called as Universal gates because all the gates like AND, OR, NOT, XOR, XNOR can be realized by these gates.

NAND gate as universal gate:-

1.) Realizing AND gate using NAND gates

A NAND produces complement of AND gate. So, if the output of a NAND gate is inverted,

overall output will be that of an AND gate.



AND

Y=((A.B)')'

=A.B

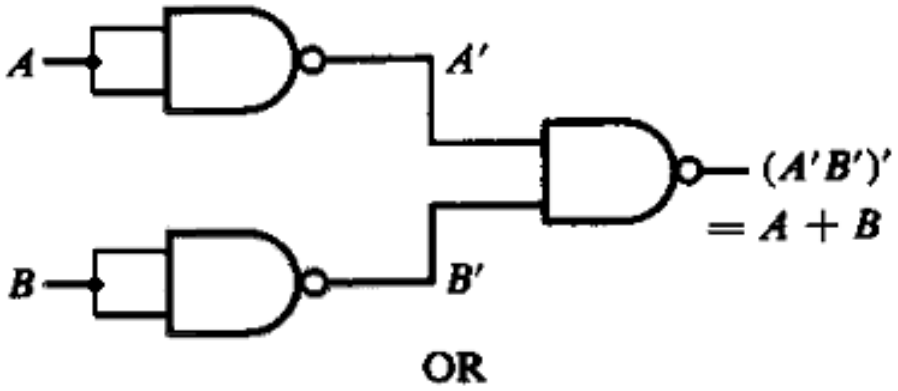
TRUTH TABLE-

A	B	(A.B)'	((A.B)')'
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

2.) Realizing OR gate using NAND gates

From DeMorgan's theorems: (A.B)' = A' + B'. Similarly, (A'.B')' = A'' + B'' = A + B

So, give the inverted inputs to a NAND gate, obtain OR operation at output.



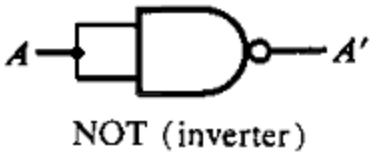
TRUTH TABLE

A	**B**	**A'**	**B'**	**(A'.B')'=A+B**
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

3.) Realizing NOT gate using NAND gates

A NOT produces complement of the input. It can have only one input, tie the inputs of a NAND

gate together. Now it will work as a NOT gate.



Y= (A.A)'

=A'

TRUTH TABLE-

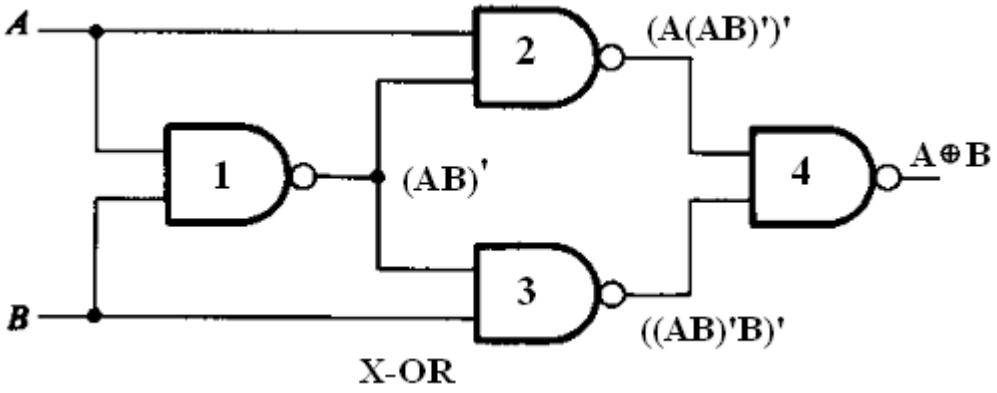
A	**A.A**	**(A.A)'**	**A'**
0	0	1	1
1	1	0	0

4.) Realizing XOR gate using NAND gates

Let A and B be the inputs and Y be the output.

Y=((A(A.B)')'.((A.B)'B)')'

=A⊕ B



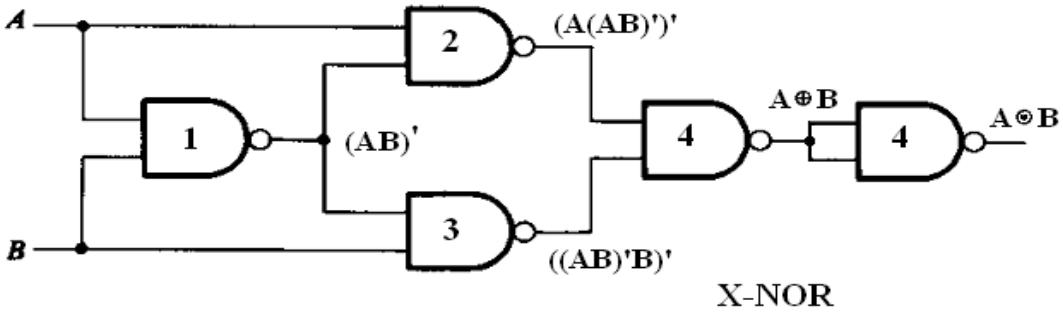
X-OR

TRUTH TABLE-

A	B	A.B	(A.B)'	(A(A.B)')	((A.B)'B)'	A⊕ B
0	0	0	1	1	1	0
0	1	0	1	1	1	1
1	0	0	1	0	1	1
1	1	1	0	1	1	0

5.) Realize X-NOR gate using NAND gates

X-NOR gate is actually X-OR gate followed by NOT gate. So give the output of X-OR gate to a NOT gate, overall ouput is that of an X-NOR gate.



X-NOR

TRUTH TABLE-

A	**B**	**(A.B)'**	**(A(A.B)')'**	**((A.B)'B)'**	**A⊕ B**	**A⊙ B**
0	0	1	1	1	0	1
0	1	1	1	1	1	0
1	0	1	1	0	1	0
1	1	0	0	1	0	1

NOR gate as universal gate-

1.) Realizing AND gate using NOR gates

From DeMorgan's theorems: (A+B)' = A'. B'. Similarly, (A'+B')' = A''. B'' = A .B

So, give the inverted inputs to a NOR gate, obtain AND operation at output.

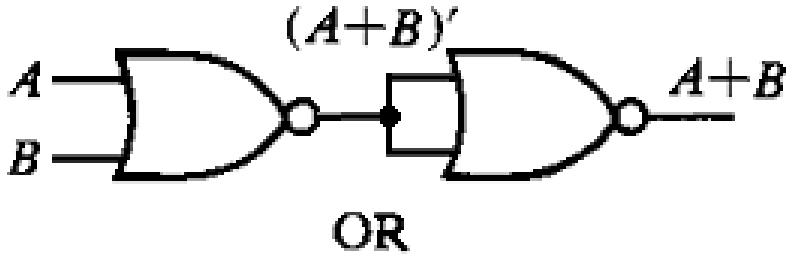
TRUTH TABLE-

A	**B**	**A'**	**B'**	**(A'+B')'**	**A.B**
0	0	1	1	0	0
0	1	1	0	0	0
1	0	0	1	0	0
1	1	0	0	1	1

2.) Realizing OR gate using Nor gates

A NOR produces complement of OR gate. So, if the output of a NOR gate is inverted, overall output will be that of an OR gate.

Y = ((A+B)')'= (A+B)



TRUTH TABLE-

A	**B**	**(A+B)'**	**((A+B)')'**
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

3.) Realizing NOT gate using NOR gates

A NOT produces complement of the input. It can have only one input, tie the inputs of a NOR gate together. Now it will work as a NOT gate. Its output is

Y = (A+A)' = (A)'

NOT

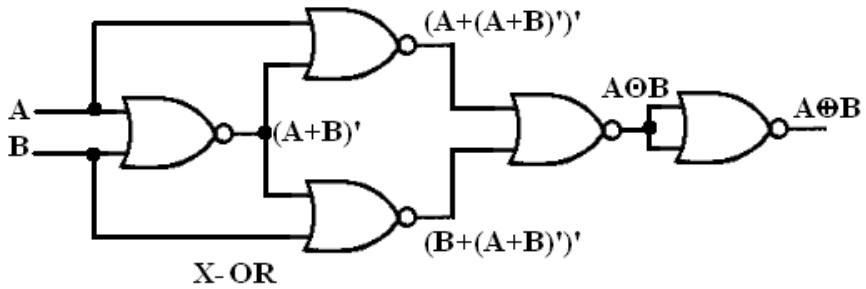
TRUTH TABLE-

A	**A+A**	**(A+A)'**	**(A)'**
0	0	1	1
1	1	0	0

4.) Realizing XOR gate using NOR gates

EX-OR gate is actually EX-NOR gate followed by NOT gate. So give the output of EX-NOR gate to a NOT gate, overall output is that of an EX-OR gate.

Y = A'.B+ A.B'



TRUTH TABLE-

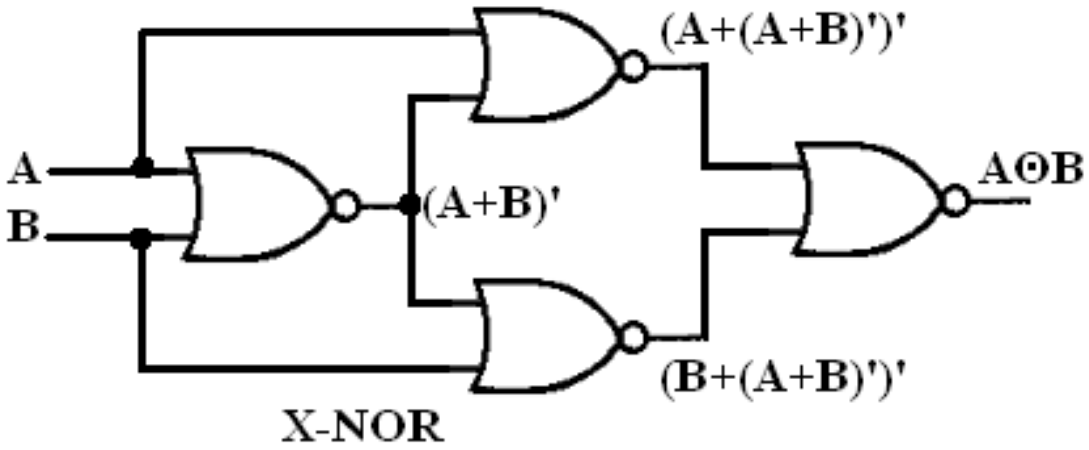
A	**B**	**A'**	**B'**	**A'.B**	**A.B'**	**(A'.B)+(A.B')**
0	0	1	1	0	0	0
0	1	1	0	1	0	1
1	0	0	1	0	1	1
1	1	0	0	0	0	0

5.) Realizing X-NOR gate using NOR gates

Let A and B are the inputs and Y be the output.

The output of a two input EX-NOR gate is given by:

Y = AB + A'B'



TRUTH TABLE-

A	B	A'	B'	A.B	A'.B'	(A.B)+(A'.B')
0	0	1	1	0	1	1
0	1	1	0	0	0	0
1	0	0	1	0	1	0
1	1	0	0	1	0	1

PROCEDURE:-

1.) Insert the desired ICs into the bread board present in the trainer kit.

2.) Apply two inputs and one output. Put GND and V_{CC} at pins 7 and 14 of the ICs.

3.) For NOT gate only one input is applied and one output.

4.) After verifying all gates remove the ICs with the help of a tweezer.

RESULT:- The truth tables of realization of all gates using NAND and NOR are verified.

PRECAUTIONS:-

1.) Connections should be neat and clean.

2.) Insert and remove all ICs with care.

3.) Apply GND at pin no. 7 and V_{CC} at pin no. 14of both the ICs.

EXPERIMENT NO. 3(a)

AIM: - To design and verify truth table of half adder using basic and XOR gates.

APPARATUS: - Regulated power supply, trainer kit, IC's 7408, 7486, tweezers, connecting leads etc.

THEORY:- A logic circuit for the addition of 2- one bit numbers is referred to as a Half Adder.

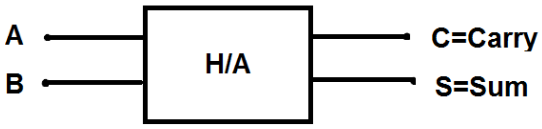
As there are two inputs A and B then according to the formula,

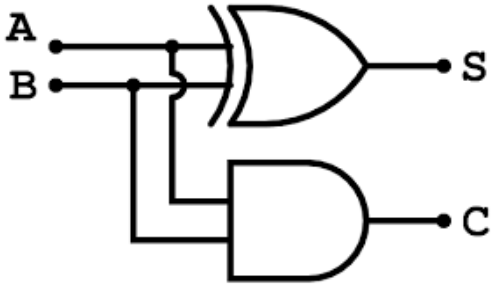
$2^n = M$

Here n=2, we get M=4

i.e No. of possible combinations are 4.

Functional block diagram of Half Adder is shown





TRUTH TABLE:-

Inputs		**Outputs**
A	B	Sum
0	0	0
0	1	1
1	0	1
1	1	0

Similarly the results can be obtained for other inputs.

PROCEDURE:-

1.) Insert the desired ICs into the bread board present in the trainer kit

2.) Make the connections as shown in circuit

3.) Apply the inputs at 1st and 2nd pin of both the ICs and take output on 3rd pin. Put GND and V_{CC} at pins 7 and 14 of ICs.

4.) Output from the IC no 7408 gives Carry and IC 7486 gives the Sum.

5.) By charging the inputs of the two ICs, truth table of half adder can be verified.

6.) Remove the ICs with the help of a tweezer.

RESULT:-

The truth table of half adder has been verified.

PRECAUTIONS:-

1.) Connections should be neat, clean and tight.

2.) Insert and remove the ICs with care.

3.) Apply GND at pin no. 7 and V_{CC} at pin no. 14 of both the ICs.

EXPERIMENT NO. 3(b)

Aim: Design and verify the truth table of Full adder.

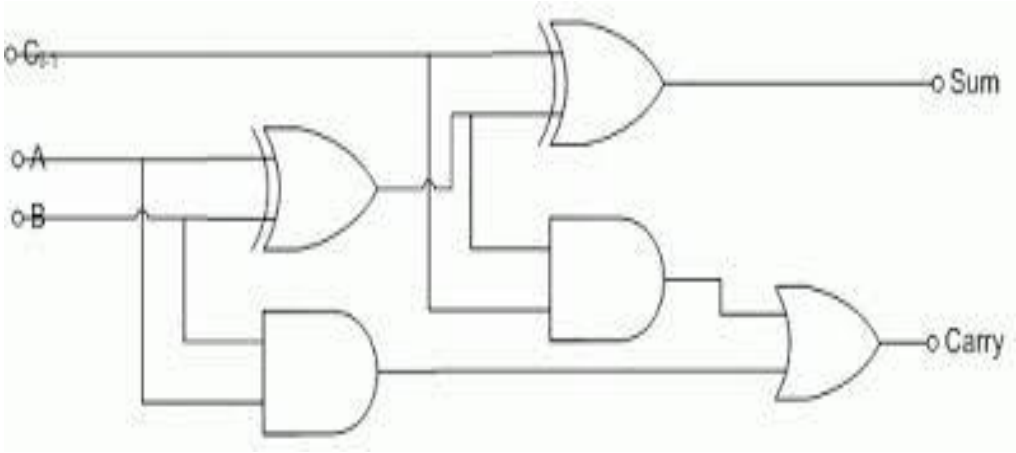
Apparatus: Regulated power supply, trainer kit, IC's 7408, 7486, 7432, tweezer, connecting leads.

Theory: A logic circuit for the addition of three one bit number is referred to as Full adder. An half adder has only two numbers and there is no provision to add carry coming from the lower order bits when multi bit addition is performed.

For this purpose, a third terminal is added and this circuit is used to add,and= where and be nth order bits of the numbers A and B respectively and = is the carry generated from the addition of (n-1)th bits. This cirucuit is referred to as full-adder.

Functional block diagram and circuit of full adder is as shown

Functional Block Diagram



Circuit Diagram of Full Adder

After the addition of three bits in full adder circuit, two outputs gets generated out of which, one is sum and other is carry out (). This circuit can also be derived by using two half adders and one OR gate. Thus, in total,it uses two XOR, two AND gates and one OR gate.

Truth table of Full adder:

Inputs			Outputs
		or	
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

=

Procedure:

1. Insert the desire IC's into the bread board present in the trainer kit.
2. Make the connection as shown in figure.
3. Apply the three inputs, two outputs are obtained from the circuit which are and .
4. By applying all the other possible combinations, verify the truth table of full adder.
5. Remove the IC with the help of tweezers.

Result:

1. The truth table of Full Adder has been verified.

Precautions:

1. Connections should be neat, clean and tight.
2. Insert and remove IC's with care.
3. Always apply GND to pin no.7 and VCC to pin 14 of IC's.

EXPERIMENT NO. 4 (a)

AIM :- Realization of Half Subtractor by using basic gates and NAND gates.

APPARATUS :- IC 7400, IC 7408,IC 7486, Patch Cords & IC Trainer Kit.

THEORY:-

HALF-SUBTRACTOR:-Subtracting a single-bit binary value B from another A (i.e. A -B) produces a difference bit D and a borrow out bit B-out. This operation is called half subtraction and the circuit to realize it is called a half subtractor.

The Boolean functions describing the half-Subtractor are:

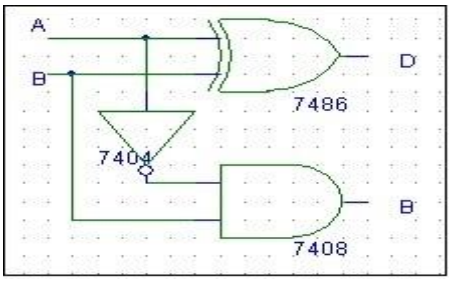
$S = A \oplus B$

BOOLEAN EXPRESSIONS:-

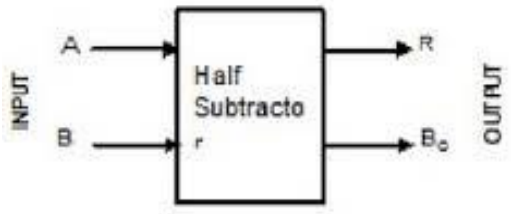
$D = A \oplus B$

$Br = A`B$

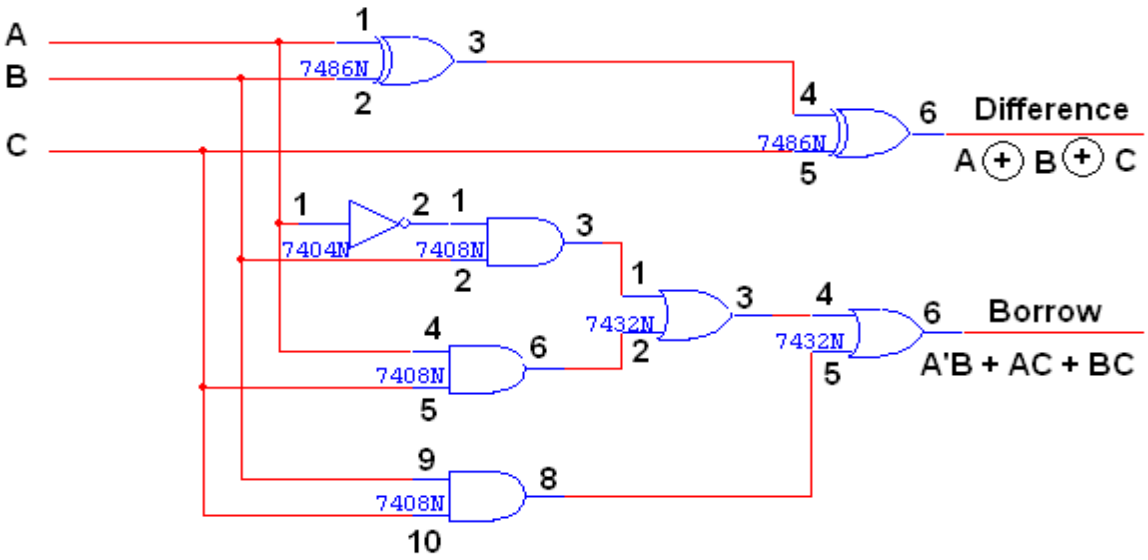
				Difference	Borrow
0	-	0	=	0	0
0	-	1	=	1	1
1	-	0	=	1	0
1	-	1	=	0	0



Logic diagram of half subtractor



Block diagram of half subtractor



Half Subtractor using NAND gate

PROCEDURE:-

1.) Check the components for their working.
2.) Insert the appropriate IC into the IC base.
3.) Make connections as shown in the circuit diagram.
4.) Verify the Truth Table and observe the outputs.

RESULT: - The truth table of the above circuit is verified.

PRECAUTIONS:-

1.) Make connections properly.

2.) Insert and remove ICs with care.

EXPERIMENT NO. 4 (b)

AIM :- Realization of full subtract or using NAND gates.

APPARATUS :-

S. No.	Particulars	Range	Quality
1	IC 7408, 7432, 7486	----	02 each
2	IC 7400	----	01 each

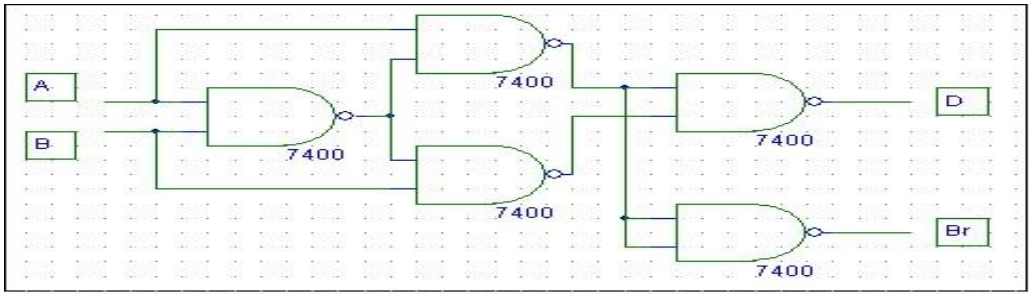
THEORY:-

Design for full subtractor:

Truth table:

Inputs			Outputs	
A	**B**	**C**	**Diff(Do)**	**Borrow(Bo)**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Full subtractor using NAND gates:



Procedure:

1. The IC is fixed on the IC trainer and VCC and GND connections are given from 5volt supply.

2. Connections are made as shown in the logic diagrams.

3. All the inputs are connected to the switches and outputs to the LEDs.

4. The truth table is verified for different combination of inputs.

Precautions:

1. Take the readings properly.

2. Make the connections properly.

EXPERIMENT NO.5

Aim: 4-Bit binary-to-gray & gray-to-Binary code converter : realization using XOR gates.

Apparatus : Regulated power supply , trainer kit , IC's 7486,tweezer,connecting leads etc.

Theory:

EX-OR Gate(7486)

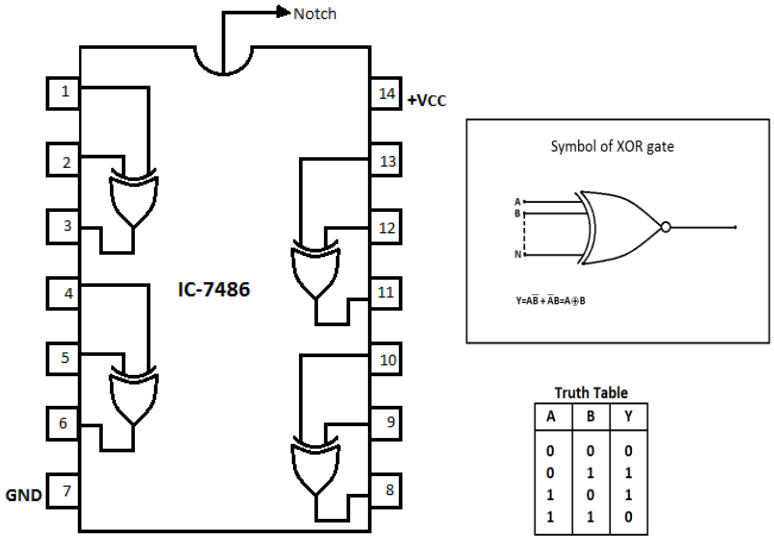
The adjoining figure(f) shows an EX-OR gate. EX-OR operation is widely used in digital circuits. It is not a basic operation and can be performed using the basic gates ----- AND,OR and NOT. Its logic equation is

$$Y = A \text{ EX-OR } B$$

$$Y = A + B$$

$$Y = AB + AB$$

When both inputs are same the output is 0, whereas when inputs are not same, the output is 1.



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Fig. (f)

Description:-

The availability of large variety of codes for the same discrete elements of information results in the use of different codes by different systems. A conversion circuit must be inserted between the two systems if

each uses different codes for same information. Thus, code converter is a circuit that makes the two systems compatible even though each uses different binary code.

The bit combination assigned to binary code to gray code. Since each code uses four bits to represent a decimal digit. There are four inputs and four outputs. Gray code is a non-weighted code. The input variable are designated as B3, B2, B1, B0 and the output variables are designated as G3, G2, G1, G0. from the truth table, combinational circuit is designed(In case of Binary to Gray converter). The input variable are designated as G3, G2, G1, G0 and the output variables are designated as B3, B2, B1, B0. from the truth table, combinational circuit is designed(In case of Gray to Binary converter).

A code converter is a circuit that makes the two systems compatible even though each uses a different binary code.

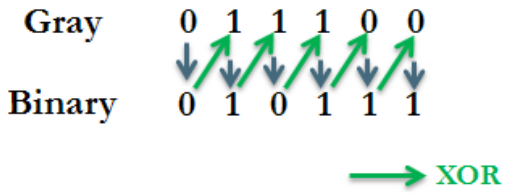
Gray To Binary Code Converter :-

Converting from Gray to Natural Binary:

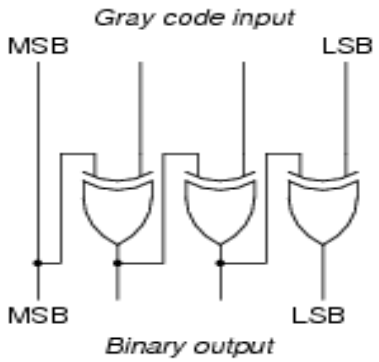
To convert a Gray code representation (Y3 Y2 Y1 Y0) to binary code (X3 X2 X1 X0), following method can be used.

$$X_3 = Y_3$$
$$X_2 = Y_2 \oplus X_3$$
$$X_1 = Y_1 \oplus X_2$$
$$X_0 = Y_0 \oplus X_1$$

That is, the MSB (X3) of binary code is same as that of gray code. The next bit (X2) is the XOR of previous result (X3) and the present bit (Y2) of the gray code and so on. Following example illustrates this concept using 6-bit code.



Logic Diagram for Gray to Binary Code Converter:-



Truth-Table :-

Gray Code Input				Binary Code Output			
G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

Procedure :

1. Insert the desired ICs into the bread board present in the trainer kit
2. Make the connections as shown in circuit
3. Put GND and V_{CC} at pins 7 and 14 respectively.
4. Now give various inputs and verify the truth table.i.e In the case of gray to binary conversion,the inputs G0,G1,G2 and G3 are giver at respective pins and outputs B0,B1,B2 and B3 are taken for all the 16 combination of inputs.
5. Remove the ICs with the help of a tweezer

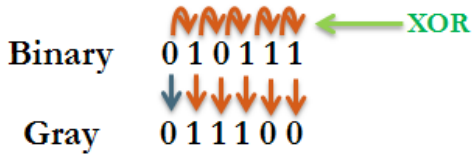
Binary To Gray Code Converter :-

Converting from Natural Binary to Gray:

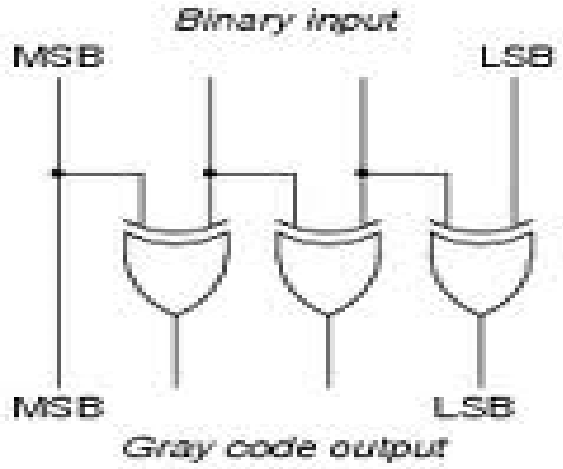
To convert a binary representation (X3 X2 X1 X0) to Gray code (Y3 Y2 Y1 Y0), following method can be used.

$$Y_3 = X_3$$
$$Y_2 = X_3 \bigoplus X_2$$
$$Y_1 = X_2 \bigoplus X_1$$
$$Y_0 = X_1 \bigoplus X_0$$

That is, the MSB (Y3) is same for both binary and Gray codes. The next bit (Y2) is the XOR of previous bit (X3) and the present bit (X2) of the binary code and so on. Following example illustrates this concept using a 6-bit code.



Logic Diagram for Gray to Binary Code Converter:-



Truth-Table:-

Decimal	Binary Code (input)	Gray Code (output)
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

Procedure :

1. Insert the desired ICs into the bread board present in the trainer kit
2. Make the connections as shown in circuit
3. Put GND and V_{CC} at pins 7 and 14 respectively.
4. Now give various inputs and verify the truth table.i.e. In the case of binary to gray conversion, the inputs B0,B1,B2 and B3 are giver at respective pins and outputs G0,G1,G2 and G3 are taken for all the 16 combination of inputs.
5. Remove the ICs with the help of a tweezer.

Result:

2. The truth table has been verified.

Precautions:

1. Connections should be neat and clean,tight and proper.
2. Insert and remove the IC's with care.
3. Apply GND at pin no. 7 and Vcc at pin no. 14 of both the IC's.
4. Check the connection once again before switching on the Digital Trainer kit.
5. Switch of the Trainer kit after performing the experiment.

EXPERIMENT NO. 6

Aim: 4 bit and 8 bit comparator Implementation using IC 7485 magnitude comparator chips

Apparatus: CONNECTING WIRES,BREAD BOARD, IC 7485 etc.

Theory:

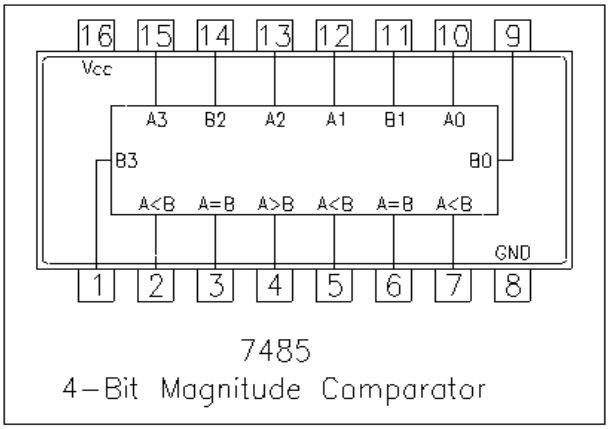
4-BIT MAGNITUDE COMPARATOR

The SN54/74LS85 is a 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A0–A3, B0–B3); A3, B3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" (OA>B), "A less than B" (OA<B), "A equal to B" (OA=B). Three Expander Inputs, IA>B, IA<B, IA=B, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: IA<B= IA>B = L, IA=B= H. For serial (ripple) expansion, the OA>B, OA<B and OA=B Outputs are connected respectively to the IA>B, IA<B, and IA=B Inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.
The Truth Table on the following page describes the operation of the SN54/74LS85 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

Easily Expandable
Binary or BCD Comparison
OA>B, OA<B, and OA=B Outputs Available

PIN NAMES

A0–A3, B0–B3
IA=B
IA<B, IA>B
OA>B
OA<B
OA=B
Parallel Inputs
A = B Expander Inputs
A < B, A > B, Expander Inputs
A Greater Than B Output (Note b)
B Greater Than A Output (Note b)
A Equal to B Output (Note b)



4-Bit Magnitude Comparator (Equality Detector)

General Description

The MM74HC688 equality detector utilizes advanced silicon-gate CMOS technology to compare bit for bit two 8-bit words and indicates whether or not they are equal. The P Q output indicates equality when it is LOW. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits. This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information. The comparator's output can drive 10 low power Schottky equivalent loads. This comparator is functionally and pin compatible to the 74LS688. All inputs are protected from damage due to static discharge by diodes to VCC and ground.

Features

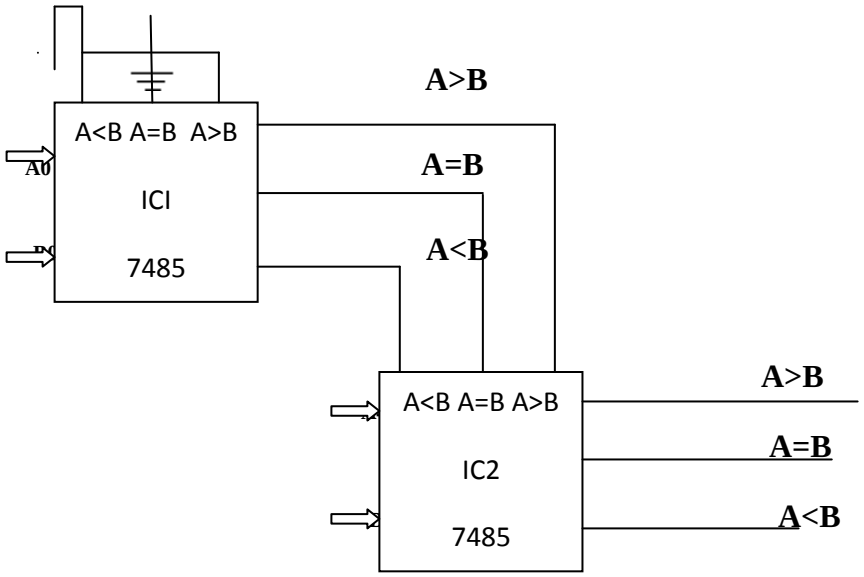
_ Typical propagation delay: 20 ns
_ Wide power supply range: 2–6V
_ Low quiescent current: 80 PA (74 Series)
_ Large output current: 4 mA (74 Series)
_ Same as HC521

Procedure :

1. Insert the desired ICs into the bread board present in the trainer kit
2. Make the connections as shown in circuit
3. An 8-bit comparator is made using two 4-bit comparators as ashown in the diagram and using the truth table for the same.
4. Remove the ICs with the help of a tweezer.

Comparing inputs A, B	Cascading inputs			Comparator outputs		
	I(A>B)	I(A=B)	I(A<B)	A>B	A=B	A<B
A>B	X	X	X	1	0	0
A=B	0	0	0	1	0	1

	0	**0**	**1**	**0**	**0**	**1**
	1	**0**	**0**	**1**	**0**	**0**
	1	**0**	**1**	**0**	**0**	**0**
	X	**1**	**X**	**0**	**1**	**0**
A<B	**X**	**X**	**X**	**0**	**0**	**1**



Result:

1. The truth table has been verified.

Precautions:

1. Connections should be neat and clean, tight and proper.
2. Insert and remove the IC's with care.
3. Apply GND at pin no. 7 and Vcc at pin no. 14 of both the IC's.
4. Check the connection once again before switching on the Digital Trainer kit.
5. Switch of the Trainer kit after performing the experiment.

EXPERIMENT NO. 7

Aim:- Multiplexer: Truth-table verification and realization of half adder and Full adder using IC74153 chip.

Apparatus: Power supply, digital trainer kit, connecting leads, IC 74153

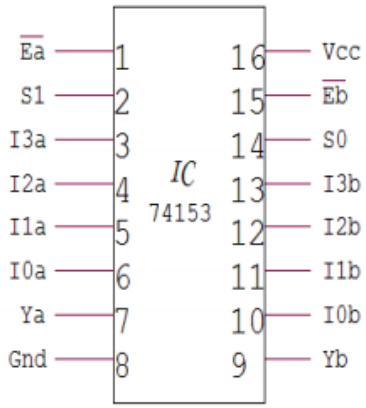
Theory: A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output lines. The selection of particular input line is controlled by a set of selection lines. Normally, there are $(2)^n$ input line and n- selection lines whose combinations determine which input is selected. 74153 is a dual 4 line-to-1 line multiplexer.

(i) **Half Adder:** A logic circuit for the addition of two bits is called half adder. After the addition of two bits, two outputs are generated one is sum and other is carry. While designing multiplexer, these two bits act as selection lines. So, two selection lines are used. Thus 2^2=4 i.e. 4:1 multiplexer is used to design a half adder. The IC used is 74153 and it is 16 pin IC.

Truth Table:

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Pin Diagram of IC 74153



The inputs A & B are provided at the selection line S1 & S0. Sum is realized on MUX A and carry is realized on MUX B.

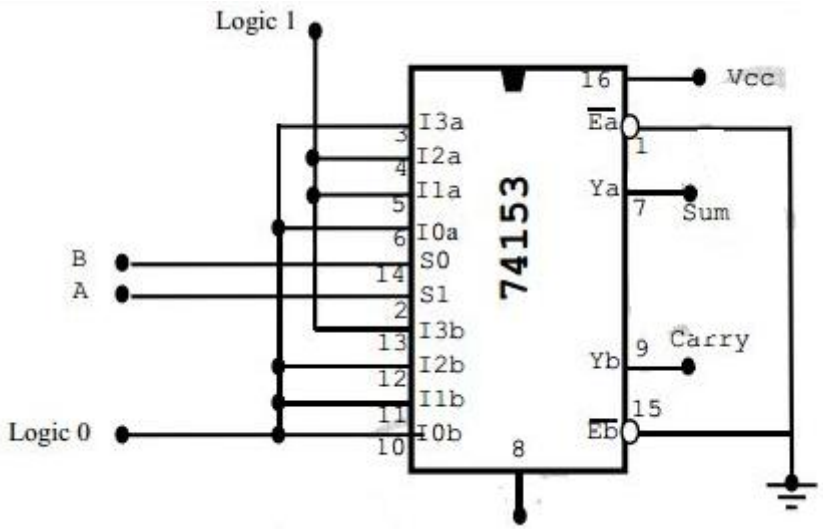
For Sum:

A=0, B=0	A=0, B=1	A=1, B=0	A=1, B=1
I0(a) = 0	I1(a) = 1	I2(a) = 1	I3(a) =0

For Carry:

A=0, B=0	A=0, B=1	A=1, B=0	A=1, B=1
I0(a) = 0	I1(a) = 0	I2(a) = 0	I3(a) =1

Half Adder using 74153 :



(ii) **Full Adder:** A logic circuit for the addition of three bits is called full adder. After the addition of three bits, two outputs are generated one is sum and other is carry. While designing multiplexer, these two bits act as selection lines and line act as input line. So, two selection lines are used and one input line is used. Thus, 2^2=4 i.e. 4:1 multiplexer is used to design a full adder.

Truth Table:

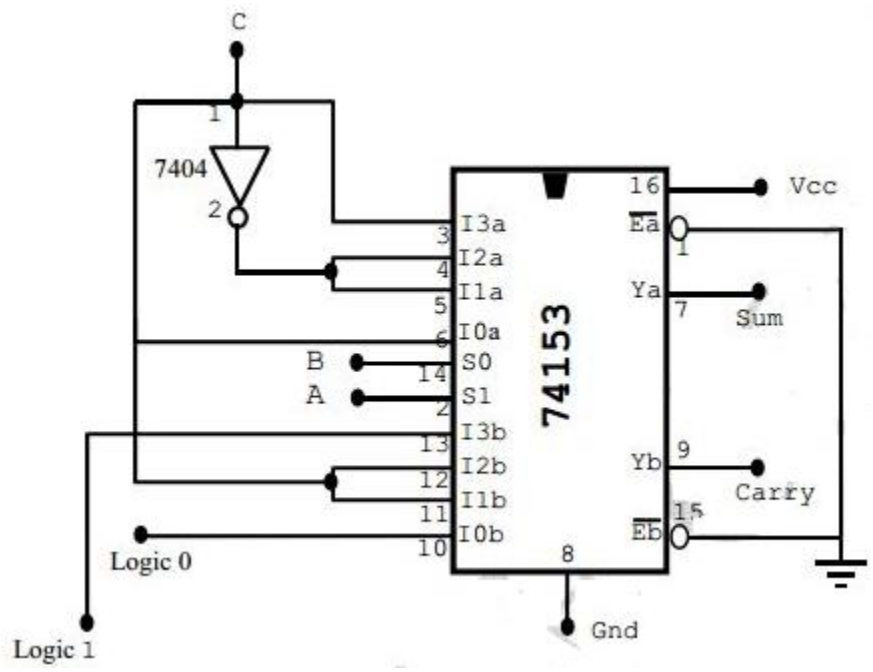
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

For Sum:

	A=0, B=0	A=0, B=1	A=1, B=0	A=1, B=1
	0	1	1	0
	1	0	0	1
	I0(a)= C	I1(a)=C’	I2(a)=C’	I3(a)=C

For Carry:

	A=0, B=0	A=0, B=1	A=1, B=0	A=1, B=1
	0	0	0	1
	0	1	1	1
	I0(a)= 0	I1(a)=C	I2(a)=C	I3(a)=1



Procedure:

1. Insert the IC into the bread board of the trainer kit.
2. The Pin [16] is connected to + Vcc.
3. Pin [8] is connected to ground.
4. The inputs are applied to S1, S0 to the multiplexer and verify the truth table of half adder & full adder circuit for both sum and carry.
5. Based on the selection lines one of the inputs will be selected at the output and thus verify the truth table.
6. Remove the IC with the help of tweezers.

Result:

The truth table of half adder and full adder circuits has been verified.

Precautions:

1. Take the readings properly.
2. Make the connections properly.

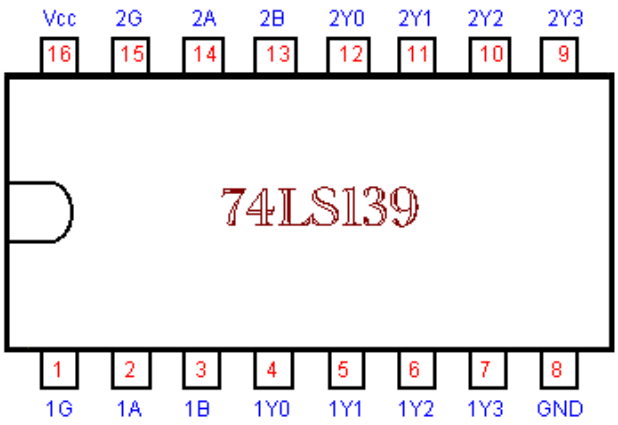
EXPERIMENT NO. 8

Aim: Demultiplexer- Truth table and verification & realization of half subtractor & full subtractor using IC 74139 chip.

Apparatus: IC 74139, connecting leading, battery supply, tweezer.

Theory : IC - 74139

IC – 74139 package contains two decoders. Each of these decoders has two address lines and four output pins. The input address lines for one of the decoders is labeled 1A and 1B.The input pins for the other decoder are labeled 2A and 2B. The output pins that are selectable because of a logic pattern on 1A and 1B are identified as $1Y_0$, $1Y_1$, $1Y_2$ and $1Y_3$.The output pins that are selectable because of a logic patten placed on the 2A and 2B input pins control the selection of the output pins identified as $2Y_0$, $2Y_1$, $2Y_2$, $2Y_3$.The integrated circuit 74LS139 contains two demultiplexers with 4 ways. Each one of them has 2 entries of selection A and B, an input G and 4 exits (Y0 with Y3). The 74139 is also useful as a learning tool to practice the use of the base 16 numbering system (HEX)to mentally represent a 16 bit binary pattern.



Pin diagram of IC-74139

Truth-table of IC-74139

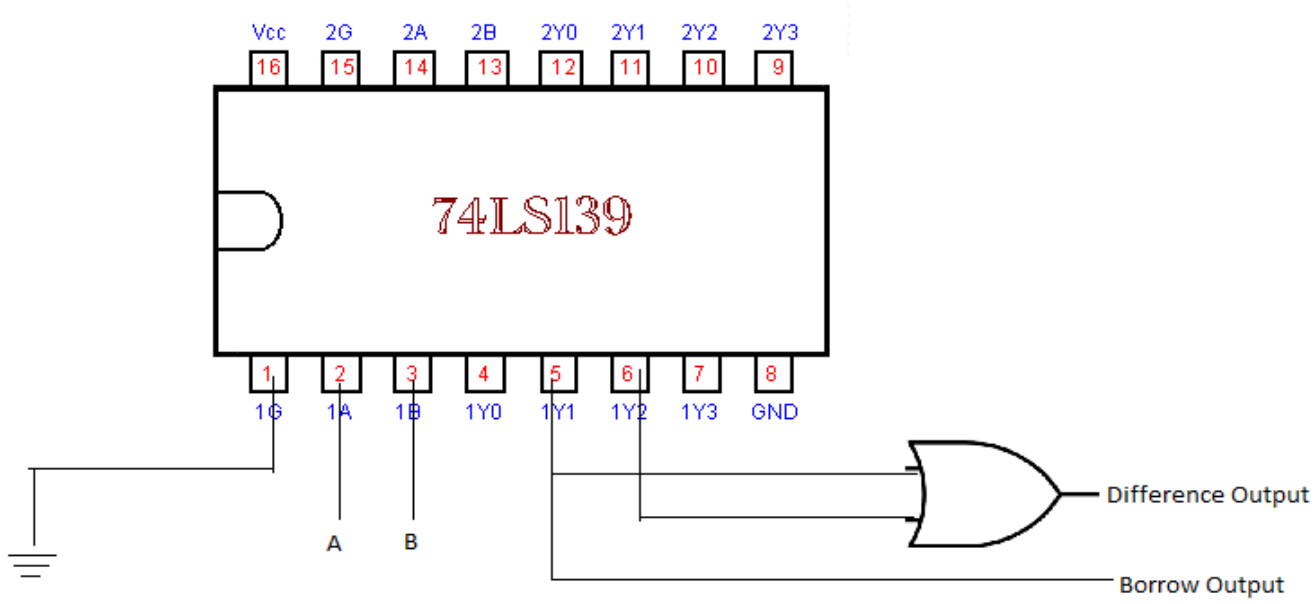
G	B	A	Y0	Y1	Y2	Y3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Half-Subtractor using IC-74139

The half-subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, X (minuend) and Y (subtrahend) and two outputs D (difference) and B (borrow).

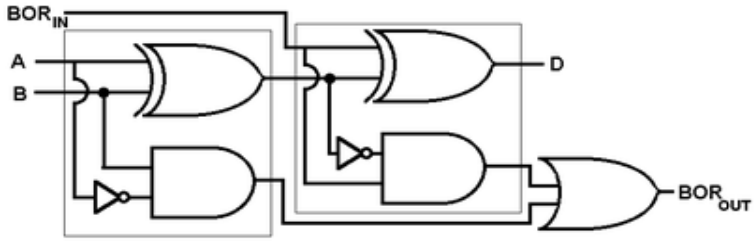
Inputs		Outputs	
A	B	D_i(Difference)	B_o(Borrow)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Half-Subtractor circuit :-



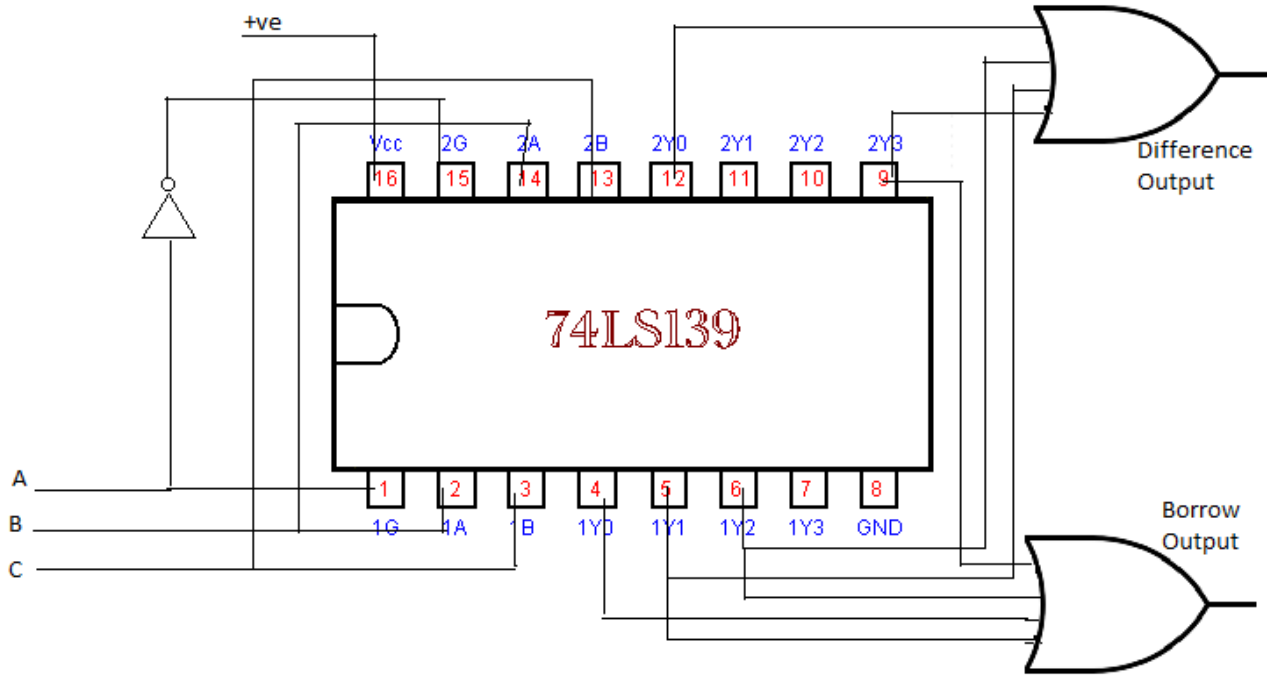
Full-Subtractor using IC-74139

a full subtractor is made by combining two half-subtractors and an additional OR-gate. A full subtractor has the borrow in capability (denoted as BORIN in the diagram below) and so allows cascadingwhich results in the possibility of multi-bit subtraction. The circuit diagram for a full subtractor is given below.



Full Subtractor-Truth Table				
Input			Output	
A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Full Subtractor Circuit :-



Procedure :

1. Insert the desied IC's into the breadboard present in the trainer kit.
2. Make the connections as shown in the theory above.
3. Pin 16 must be connected to logic high and pin 8 must be grounded.
4. The enable input must be connected to the lower level(since it is active low circuit) i.e 1G and 2G input.
5. Now give the various inputs and verify the truth table for the both half subtractor and full subtractor.
6. Remove the IC with the help of tweezer.

Result : The aim of experiment is verified.

Precautions :

1. Connections should be neat and clean.
2. Insert and remove all ICs with care
3. Apply GND at pin no. 8 and VCC at pin no. 16 of the IC-74139.

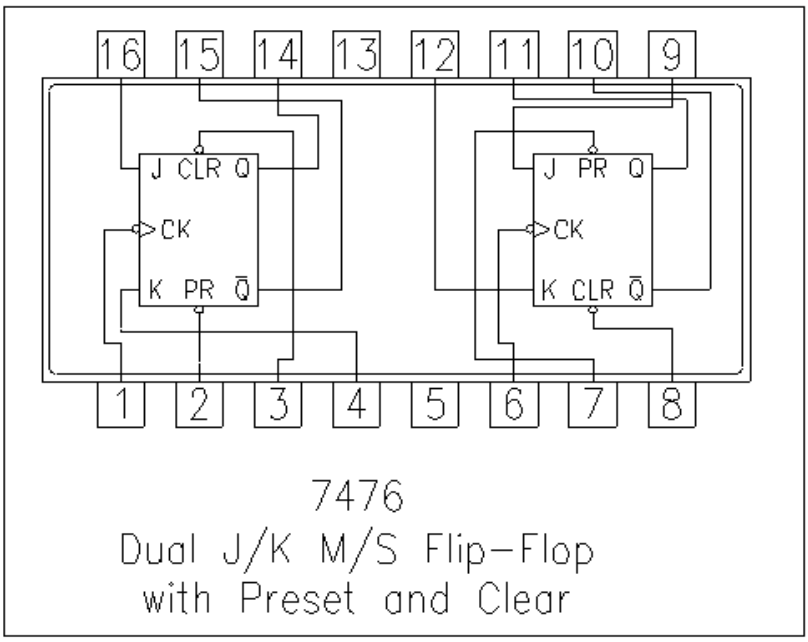
EXPERIMENT NO. 9

Aim: Truth table verification of J-K master slave F/F, T-type F/F & D-type F/F using IC-7476 chip.

Apparatus: Regulated power supply, trainer kit, tweezers, connecting leads, IC-7476.

Theory: IC-7476

IC-7476 package contain two J-K F/F. Each F/F has two outputs and two inputs along with clock, preset and clear inputs.

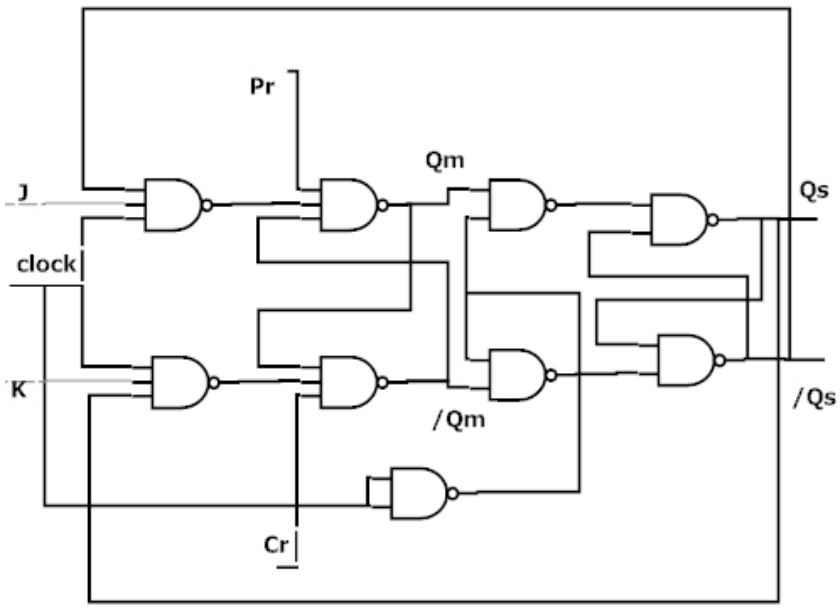


Pin Number	Description
1	Clock 1 Input
2	Preset 1 Input
3	Clear 1 Input
4	J1 Input
5	Vcc - Positive Supply
6	Clock 2 Input
7	Preset 2 Input
8	Clear 2 Input
9	J2 Input
10	Complement Q2 Output
11	Q2 Output
12	K2 Input
13	Ground
14	Complement Q1 Output
15	Q1 Output
16	K1 Input

J-K master slave flip flop:

It consists of one J-K flip flop, one slave S-R & one inverter. In fig. clock signal is connected directly to the master J-K F/F but it is connected through inverter to the slave S-R F/F. thus the master J-K flip flop is triggered on the positive clock pulse but the inverter used as the input of slave S-R flip flop force it to trigger at the negative clock pulse. Also the O/P of slave S-R F/F is connected as a third I/P for master J-K F/F. thus, overall circuit is called master-slave J-K F/F.

There are two conditions for clock either '1' or '0', when clock is 1



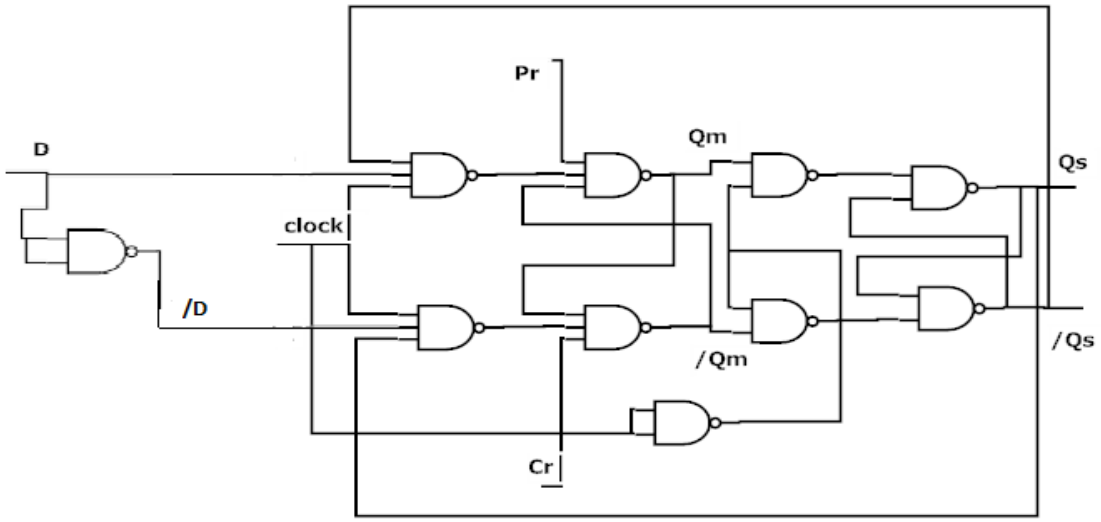
i.e. positive level, the master is active & slave is inactive. But when clock is 0, i.e. negative level, the slave is active.

Preset	Clear	J	K	Clock	Qm	/Qm	Qs	/Qs	Status
0	1	x	x	x	1	0	1	0	Set
1	0	x	x	x	0	1	0	1	Reset
1	1	0	0	-	Qm	/Qm	Qs	/Qs	No change
1	1	0	1	⎍	0	1	0	1	Reset
1	1	1	0	-	1	0	1	0	Set
1	1	1	1	⎍	/Qm	Qm	/Qs	Qs	Toggles

D type F/F:

It can be designed from SR- F/F & JK- F/F by putting an inverter or NOT gate between S & R or J & K inputs are connected together to make a single input as shown in figure.

D type F/F is used whenever S = R=0 & S=R=1 combinations are not required for particular flip flop used. This input D is called data input & thus it is named as D Flip flop. For d=0 either S=0 & r=1. For this input, output Q is always reset i.e. 0.

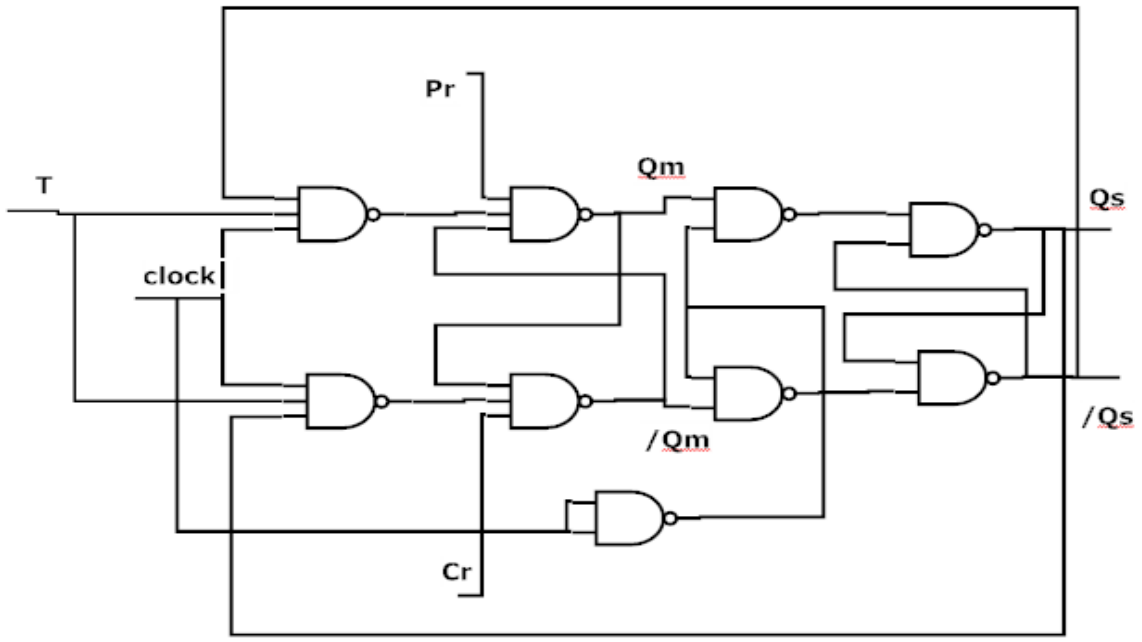


Preset	Clear	D	Clock	Q	/Q	Status
1	1	0	⌐	Q	/Q	Reset
1	1	1	⌐	/Q	Q	Set

T type Flip Flop:

It can be designed using J-K flip flop by connecting J & K inputs together to make a single input T as shown.

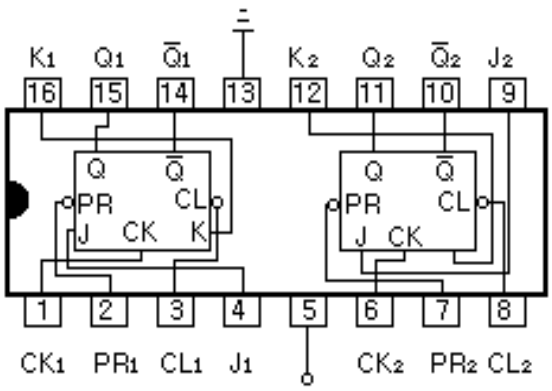
Due to toggling property it is known as toggle flip flop & are extensively used in counters to count the pulses.



Preset	Clear	T	Clock	Q	/Q	Status
1	1	0	⌐	Q	/Q	No Change
1	1	1	⌐	/Q	Q	Toggle

Procedure:

1. Insert the IC into the breadboard.
2. Make the connections as shown in the theory above in fig: 1.
3. Pin 5 must be connected to logic high and pin 13 must be grounded.
4. All combination of inputs is applied & observations are taken in table.
5. Repeat the steps from 2 to 5 for fig: 2 and fig: 3.
6. Remove the IC with the help of tweezer.



Result: The aim of experiment is verified.

Precautions:

1. Connections should be neat and clean.
2. Insert and remove all ICs with care.
3. Apply GND at pin no. 13 and VCC at pin no. 5 of the IC-7476.

EXPERIMENT NO. 10

Aim: Asynchronous Counter: Realization of 4-bit up counter and Mod-N counter using IC7490 & IC7493 chip.

Apparatus: Power supply, digital trainer kit, connecting leads, IC7490 and IC7493.

Theory: In asynchronous, events do not occur at the same time as the clock is given to the first flip flop and other successive flip flops are clocked by the output of preceding flip flop. In the every flip flop is independent of input clock.

(i) 4-bit up counter: The clock pulse fed into 1st flip-flop is rippled through other flip-flops after some propagation delay like ripple. As it is a 4-bit counter, this counter counts sequences from 0 to 15. The IC which is used for 4-bit asynchronous counter is IC 7493.

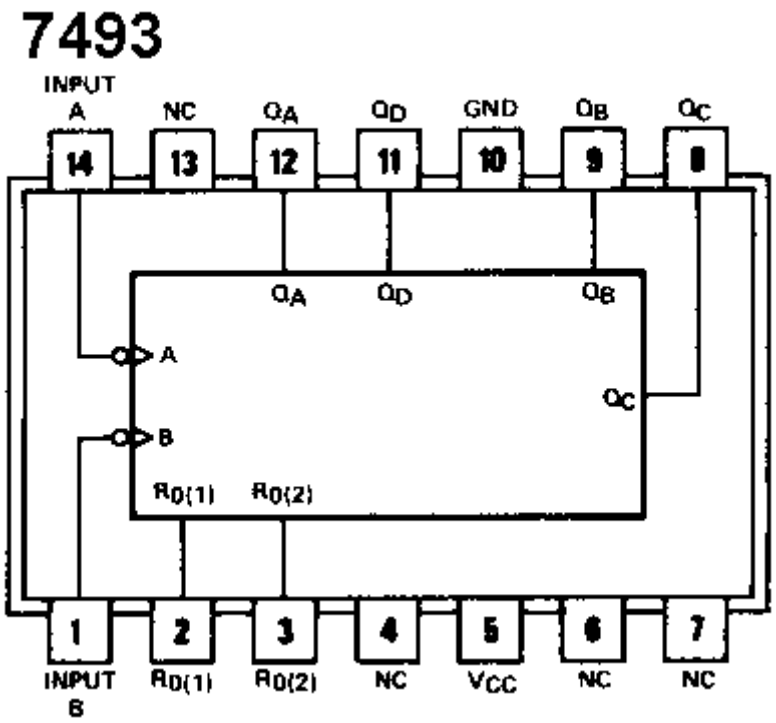
Truth Table:

Count	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Counter counts sequences from 0 to 15

The following points should be taken into consideration for its working.

1. Connect pin 1 and 12.
2. Pins R01 and R02 are provided low inputs.
3. At pin 14, clock is provided.



Pin Description:

Pin No	Function	Name
1	Clock input 2	Input2
2	Reset1	R1
3	Reset2	R2
4	Not connected	NC
5	Supply voltage; 5V (4.75V – 5.25V)	Vcc
6	Reset3	R3
7	Reset4	R4

8	Output 3, BCD Output bit 2	Q_C
9	Output 2, BCD Output bit 1	Q_B
10	Ground (0V)	Ground
11	Output 4, BCD Output bit 3	Q_D
12	Output 1, BCD Output bit 0	Q_A
13	Not connected	NC
14	Clock input 1	Input1

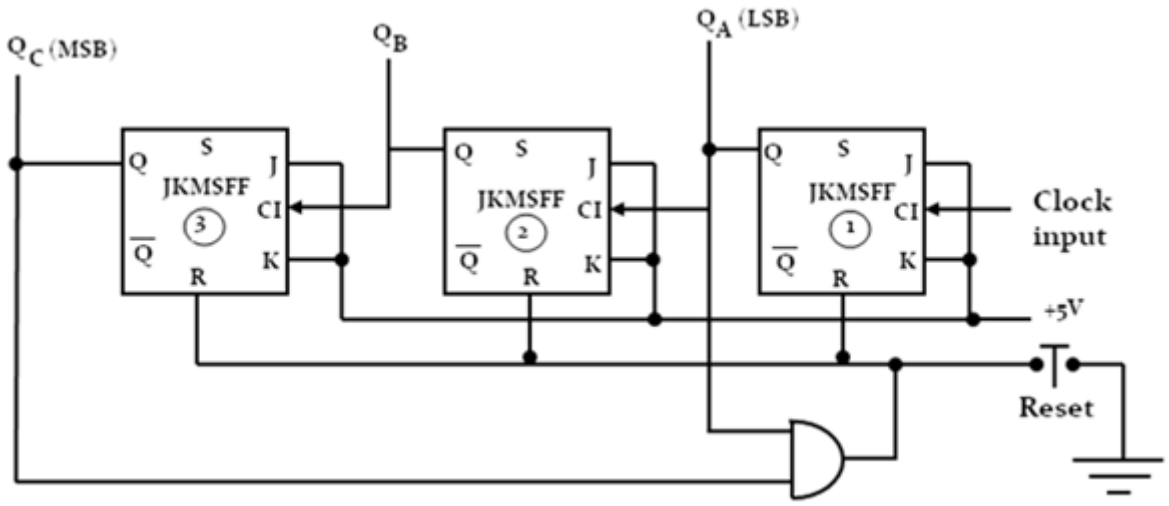
(ii) **Mod-N asynchronous counter**

Mod-5 asynchronous counter :

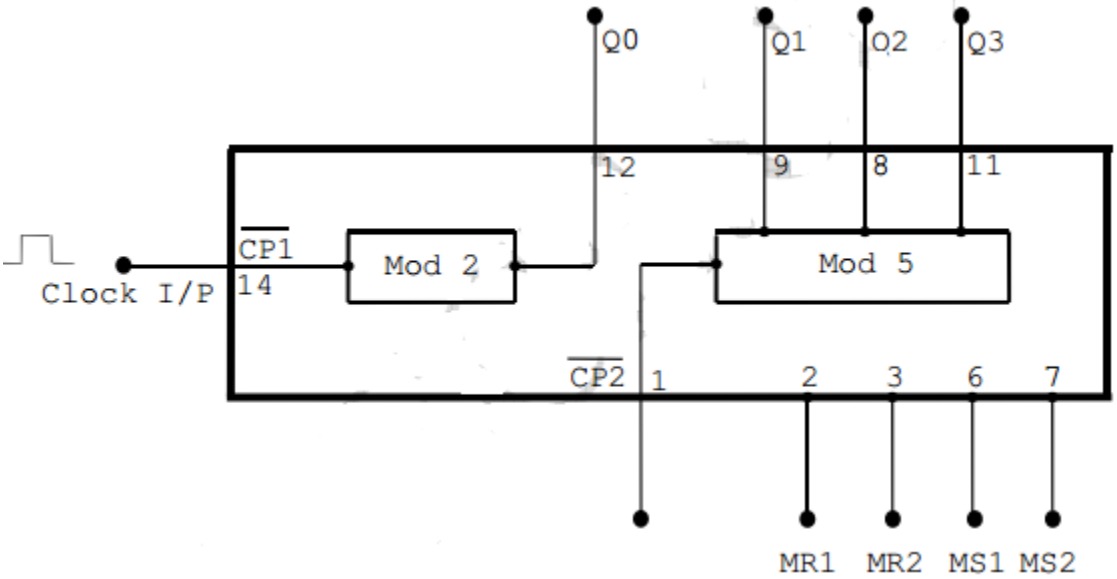
1. A 3 bit binary counter is normally counting from 000 to 111. The actual output of a 3 bit binary counter at the fifth clock pulse is 101.
2. A two input NAND gate is used to make a Mod 5 counter.
3. The outputs of the first and third flip flops (Q_A and Q_C) are connected to the input of the give NAND gate, and its output is connected to the RESET terminal of the counter,
4. Hence the counter is reset at the fifth clock pulse, which produces the output Q_C,Q_B,Q_A as 000. It is called divide by 5^{th} counter or **mod 5 counter.**

Truth Table:

Count	**Qc**	**Qb**	**Qa**
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0



Internal Diagram:



Internal diagram of IC 7490

Result: The working of 4 bit asynchronous counter & Mod-N Asynchronous counters is verified .

Procedure:

1. Insert the IC into the bread board of the trainer kit.
2. Make the connections as shown in the diagram.
3. Connect pin 1 & pin 12.
4. Pins R01 and R02 are provided low inputs.
5. On pin 14 i.e. A, a clock is provided.
6. On pin 4,6,7, 13 no connection is to be made.
7. Outputs are obtained on pin 12, 11, 9, 8.
8. Apply the inputs and clock, the output is obtained from the circuit.
9. The Pin [16] is connected to +Vcc.
10. Pin [8] is connected to ground.
11. Remove the IC with the help of tweezers.
12.

Precautions:

1. Connections should be neat & clean..
2. Insert and remove the IC's with care.
3. Handle the trainer kit with care.
4. Always apply GND to pin no. 10 and Vcc on pin no. 5 of IC
5. Take the readings properly.

EXPERIMENT NO. 11

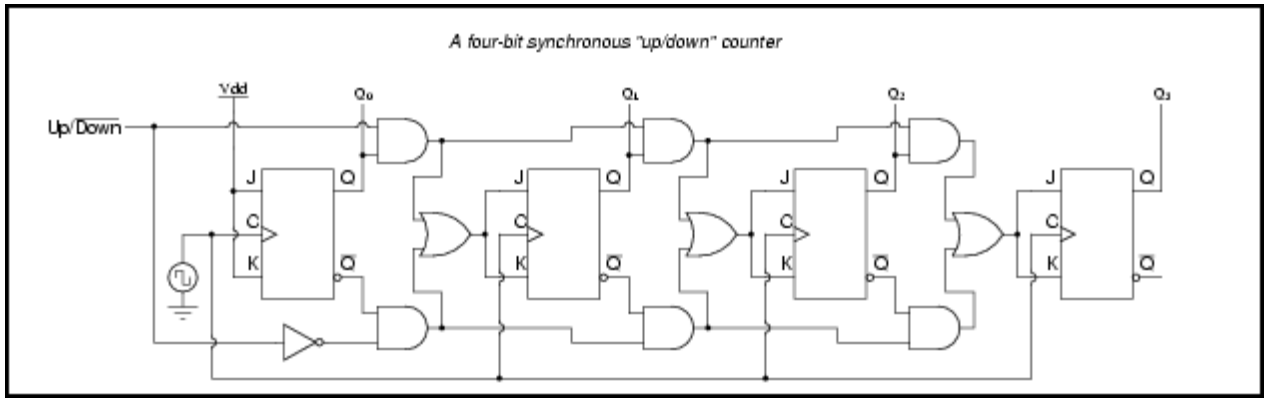
Aim: Synchronous Counter: Realization of 4-bit up/down counter and Mod-N counter using IC74192 & IC74193 chip.

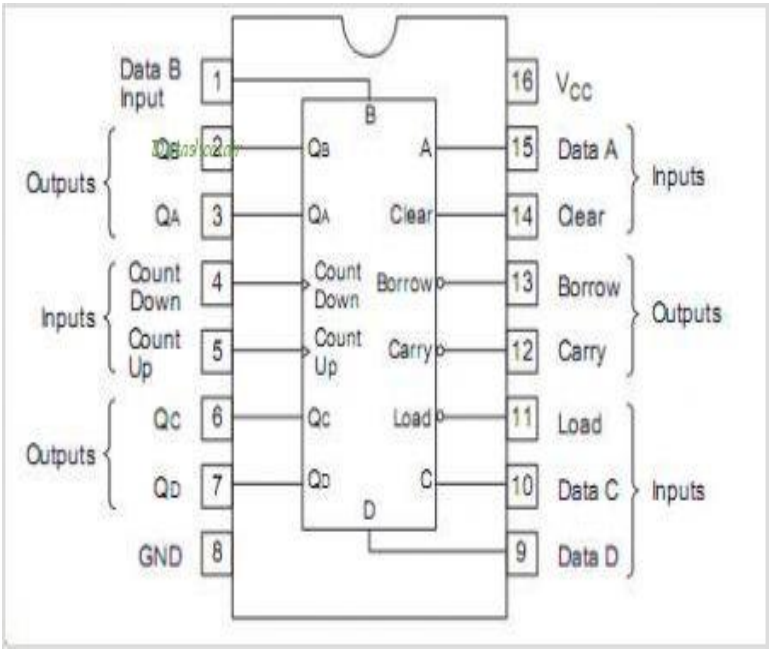
Apparatus: Power supply, digital trainer kit, connecting leads, IC74192 and IC74193.

Theory: In Synchronous Counter, the external clock signal is connected to the clock input of EVERY individual flip-flop within the Counter so that all of the flip-flops are clocked together simultaneously (in parallel) at the same time giving a fixed time relationship. In other words, changes in the output occur in "synchronization" with the clock signal. The result of this synchronization is that all the individual output bits changing state at exactly the same time in response to the common clock signal with no ripple effect and therefore, no propagation delay.

4-bit synchronous up/down counter:

Truth Table:





3-Bit Synchronous Counter :

For designing 3-bit counter following steps must be taken:

(a) Determine the filp-flop inputs which must be present for the desired next state from the present state using the excitation table of the flip-flops.

(b) Prepare k-maps for each flip-flop .Input in terms of flip-flop outputs as the input variables. Simplify the k-maps and obtain the minimized expression.

(c) Connect the circuit using flip-flops and other gates corresponding to the minimized expressions.

Procedure :

(1) Insert the IC into the bread board of the trainer kit.

(2) Make the connections as shown in figure.

(3) Apply the inputs and clock, output is obtained from the circuit.

(4) This counter so designed will count sequences from 0 to 7.

(5) Remove the IC's with the help of tweezer.

Precautions:

(1) Connections should be neat and clean.

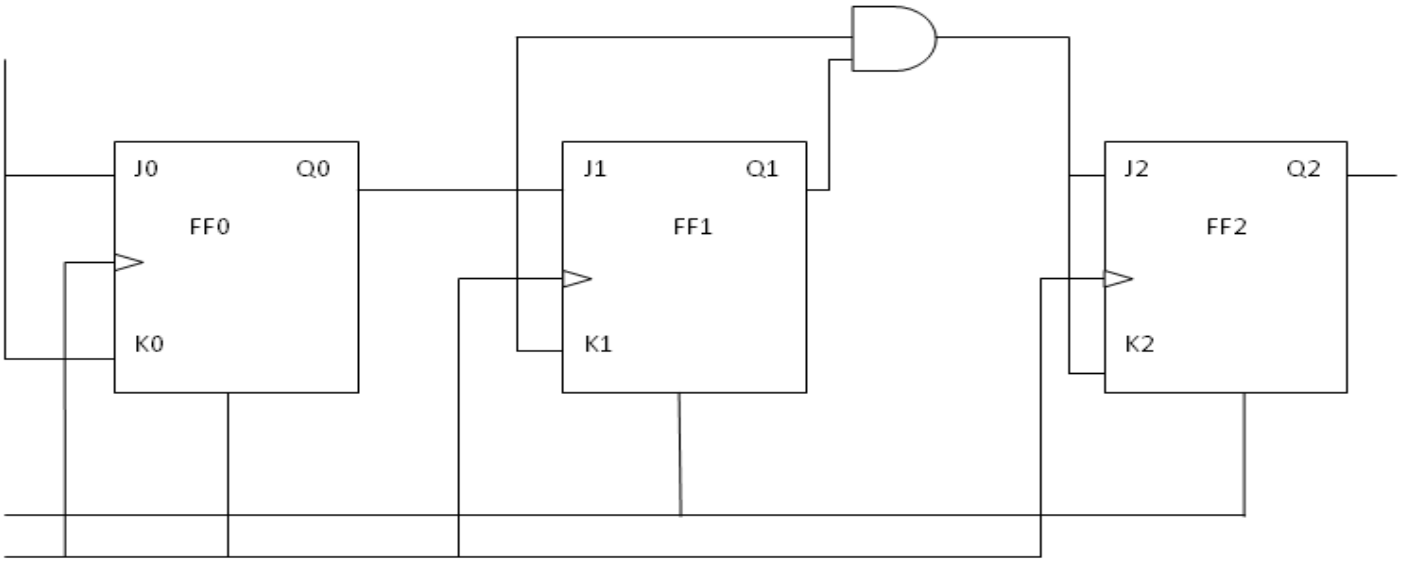
(2) Insert and remove IC's with care.

(3) Handle the trainer kit with care.

(4) Always apply GND and VCC on respective pin numbers of IC.

Number of flips used=3

Excitation table for 3-bits synchronous counter designing is as shown.



Decimal Equivalent	Present States			Next states			Flip Flop Inputs					
	Q2	Q1	Q0	Q2+1	Q1+1	Q0+1	J2	K2	J1	K1	J0	K0

0	0	0	0	0	1	0	0	X	0	X	1	X
1	0	0	1	0	0	0	1	X	1	X	X	1
2	0	1	0	0	1	0	X	X	X	0	1	X
3	0	1	1	1	0	1	X	X	X	1	X	1
4	1	0	0	1	1	X	0	0	0	X	1	X
5	1	0	1	1	0	X	1	0	1	X	X	1
6	1	1	0	1	1	X	X	0	X	0	1	X
7	1	1	1		0	X	X	1	X		X	1

EXPERIMENT NO. 12

Aim: - Study of shift right, SIPO/SISO, PISO/PIPO, shift left using IC 7495 chip.

Apparatus Required: - Power Supply, Digital trainer kit, Bread Board, IC 7495, connecting leads.

Procedure:-

Serial In Parallel Out(SIPO):-

1. Connections are made as per circuit diagram.
2. Apply the data at serial input.
3. Apply one clock pulse at clock 1 (Right Shift) observe this data at QA.
4. Apply the next data at serial input.
5. Apply one clock pulse at clock 2, observe that the data on QA will shift to QB and the new data applied will appear at QA.
6. Repeat steps 2 and 3 till all the 4 bits data are entered one by one into the shift register.

Serial In Serial Out(SISO):-

1. Connections are made as per circuit diagram.
2. Load the shift register with 4 bits of data one by one serially.
3. At the end of 4th clock pulse the first data ‘d0’ appears at QD.
4. Apply another clock pulse; the second data ‘d1’ appears at QD.
5. Apply another clock pulse; the third data appears at QD.
6. Application of next clock pulse will enable the 4th data ‘d3’ to appear at QD. Thus the data applied serially at the input comes out serially at QD

Parallel In Serial Out (PISO):-

1. Connections are made as per circuit diagram.
2. Apply the desired 4 bit data at A, B, C and D.

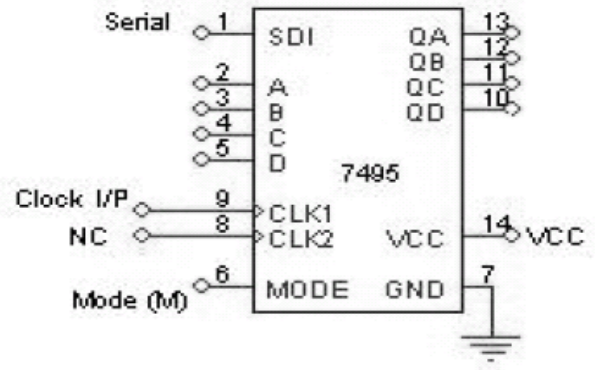
3. Keeping the mode control M=1 apply one clock pulse. The data applied at A, B, C and D will appear at QA, QB, QC and QD respectively.

4. Now mode control M=0. Apply clock pulses one by one and observe the Data coming out serially at QD.

Parallel In Parallel Out (PIPO):-

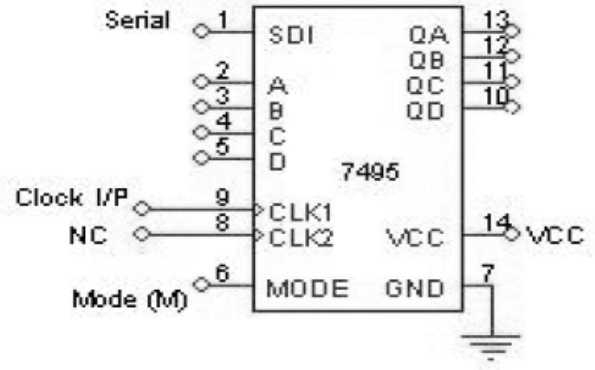
1. Connections are made as per circuit diagram.
2. Apply the 4 bit data at A, B, C and D.
3. Apply one clock pulse at Clock 2 (Note: Mode control M=1).
4. The 4 bit data at A, B, C and D appears at QA, QB, QC and QD respectively.

SIPO (Right Shift):-



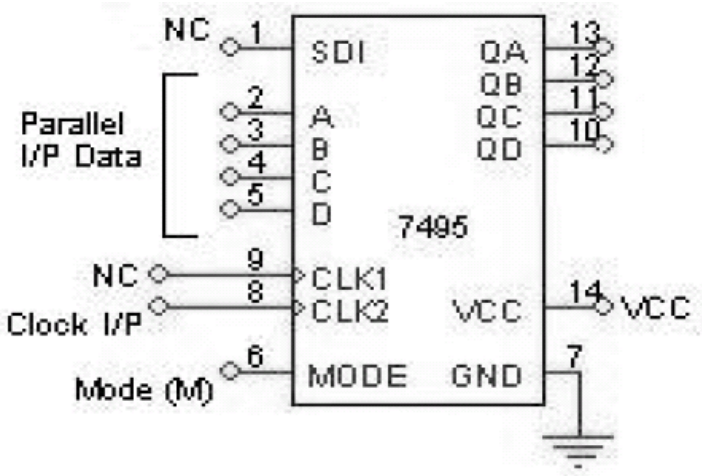
Clock	Serial i/p	QA	QB	QC	QD
1	0	0	X	X	X
2	1	1	0	X	X
3	1	1	1	0	X
4	1	1	1	1	0

SISO:-



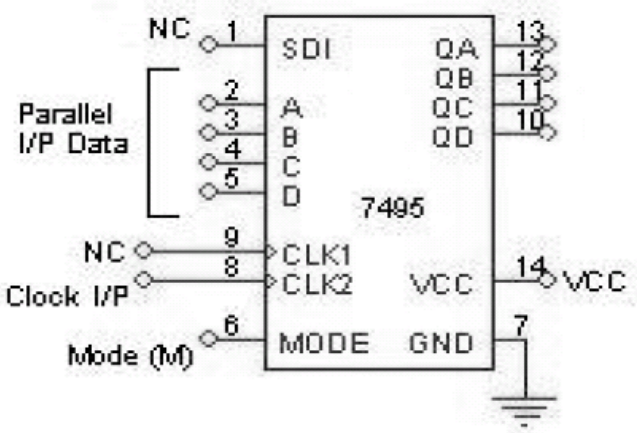
Clock	Serial i/p	QA	QB	QC	QD
1	do=0	0	X	X	X
2	d1=1	1	0	X	X
3	d2=1	1	1	0	X
4	d3=1	1	1	1	0=do
5	X	X	1	1	1=d1
6	X	X	X	1	1=d2
7	X	X	X	X	1=d3

PISO:-



Mode	Clock	Parallel i/p				Parallel o/p			
		A	B	C	D	QA	QB	QC	QD
1	1	1	0	1	1	1	0	1	1
0	2	X	X	X	X	X	1	0	1
0	3	X	X	X	X	X	X	1	0
0	4	X	X	X	X	X	X	X	1

PIPO:-



Clock	Parallel i/p				Parallel o/p			
	A	B	C	D	QA	QB	QC	QD
1	1	0	1	1	1	0	1	1

Result: The circuit for all the cases has been verified.

Precautions:

1. Take the readings properly.
2. Make the connections properly.

EXPERIMENT NO.13

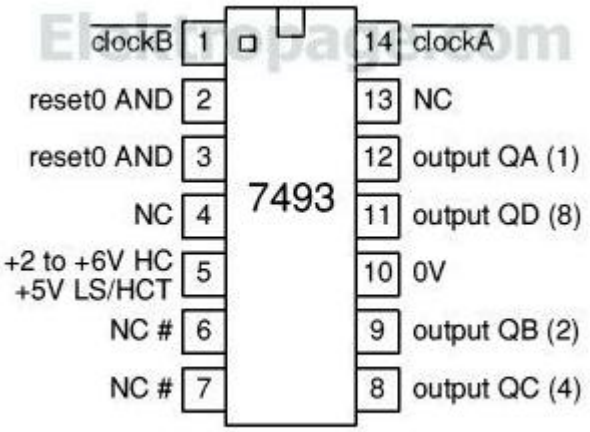
AIM: **DAC Operation : Study of 8-bit DAC (IC 08/080 chip), obtain staircase waveform using IC7493 chip.**

Apparatus Required: - Power Supply,Digital trainer kit,Bread Board, IC 7493, connecting leads,resistors and 741 op amp.

Theory:

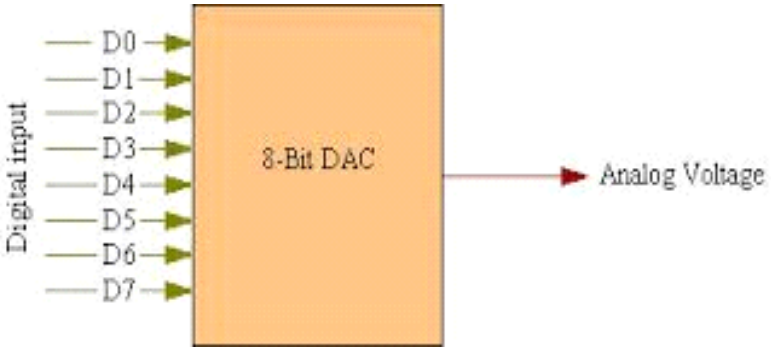
Pin Diagram of IC 79493

NC = No Connection (a pin that is not used). # on the 7490 pins 6 and 7 connect to an internal AND gate for resetting to 9. For normal use connect QA to clockB and connect the external clock signal to clockA



Digital To Analog Converters (DAC)

Digital to analog converter (DAC) is used to get analog voltage corresponding to an input digital data. Data in binary digital form can be converted to corresponding analog form by using a R-2R ladder (binary weighted resistor) network and a summing amplifier. It is more common and practical. A common example is the processing, by a modem,of computer data into audio-frequency (AF) tones that can be transmitted over a twisted pair telephone line. The circuit that performs this function is a digital-to-analog converter (DAC).



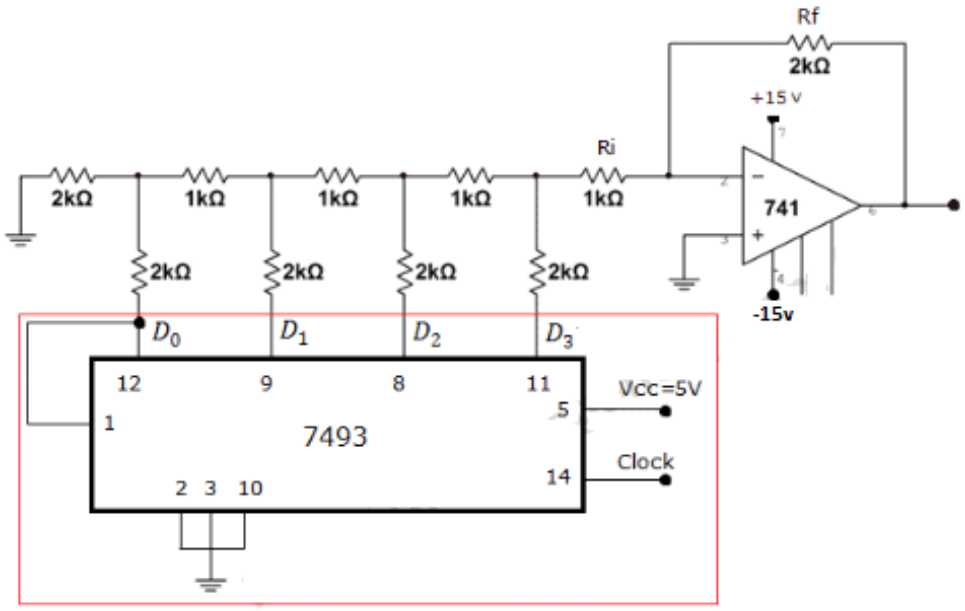


FIGURE 1-4bit DAC

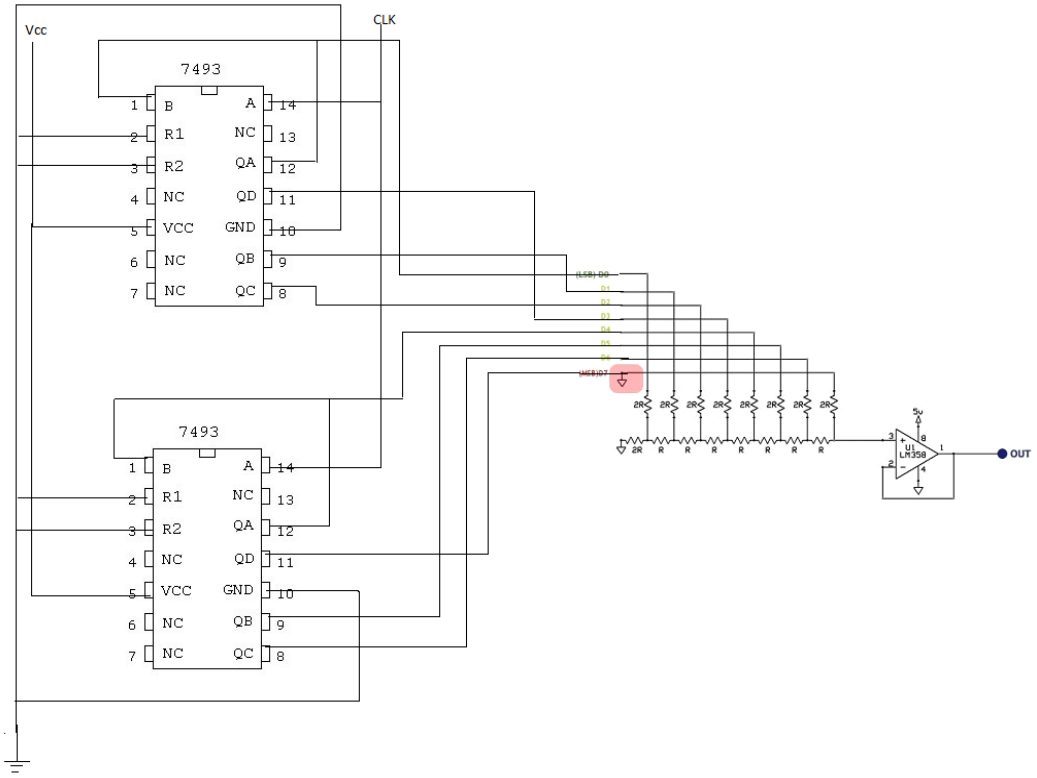


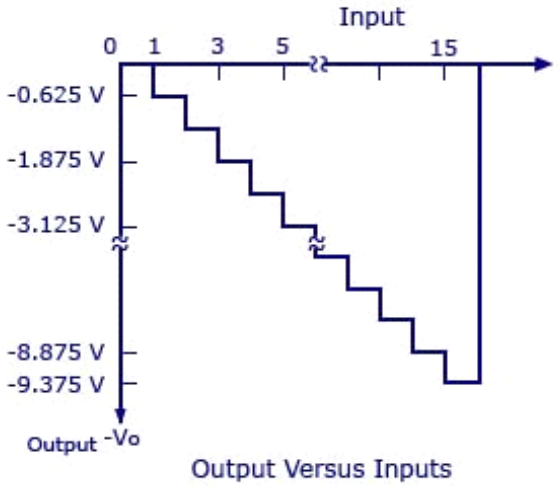
FIGURE2-8bit DAC

Procedure:

- 1 and 12of 1st IC-7493 are connected to D0of R-2R Network.

- 2,3,10 inputs of IC-7493 are grounded
- 5th pin of both ICs are connected to Vcc
- 8th and 9 pin are of ist IC are conncted to D2 and D1.
- similarly connect pins of 2nd IC according to the diagram

STAIR CASE WAVEFORM



Output Versus Inputs

Precautions :

1. Connections should be neat and clean.
2. Insert and remove the IC's with care.

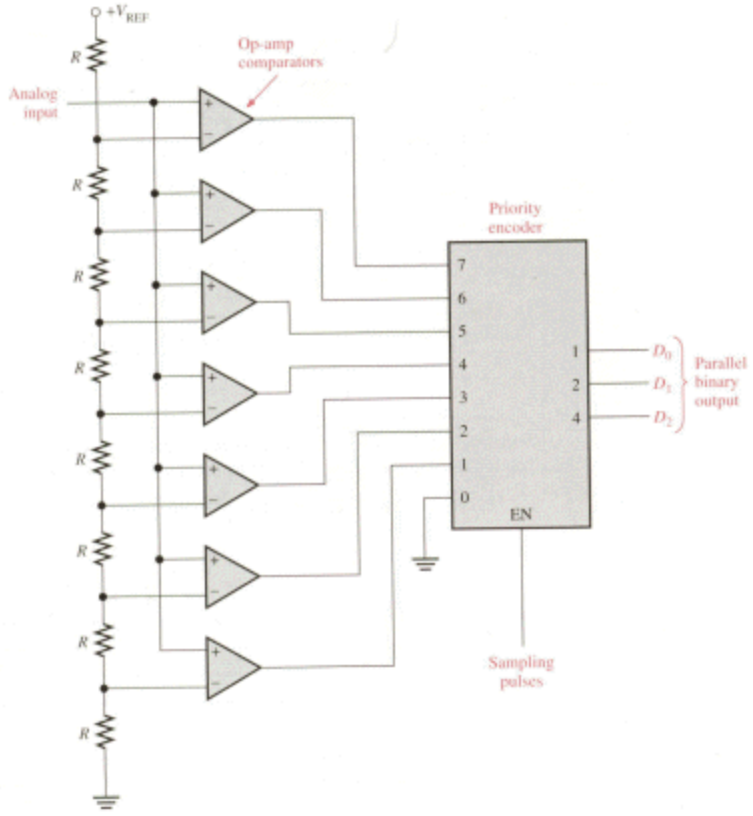
EXPERIMENT NO.14

AIM: **ADC operator: study of 8 bit ADC operator**.

Theory:

Flash (Simultaneous) ADC

The flash ADC uses comparators that compare reference voltages with the analogue input voltage. When the analogue voltage exceeds the reference voltage for a given comparator, a High is generated. In general (2^n -1) comparators are required. So for an 8-bit conversion 255 comparators are required. However the flash ADC provides a fast conversion time because of the parallel process.



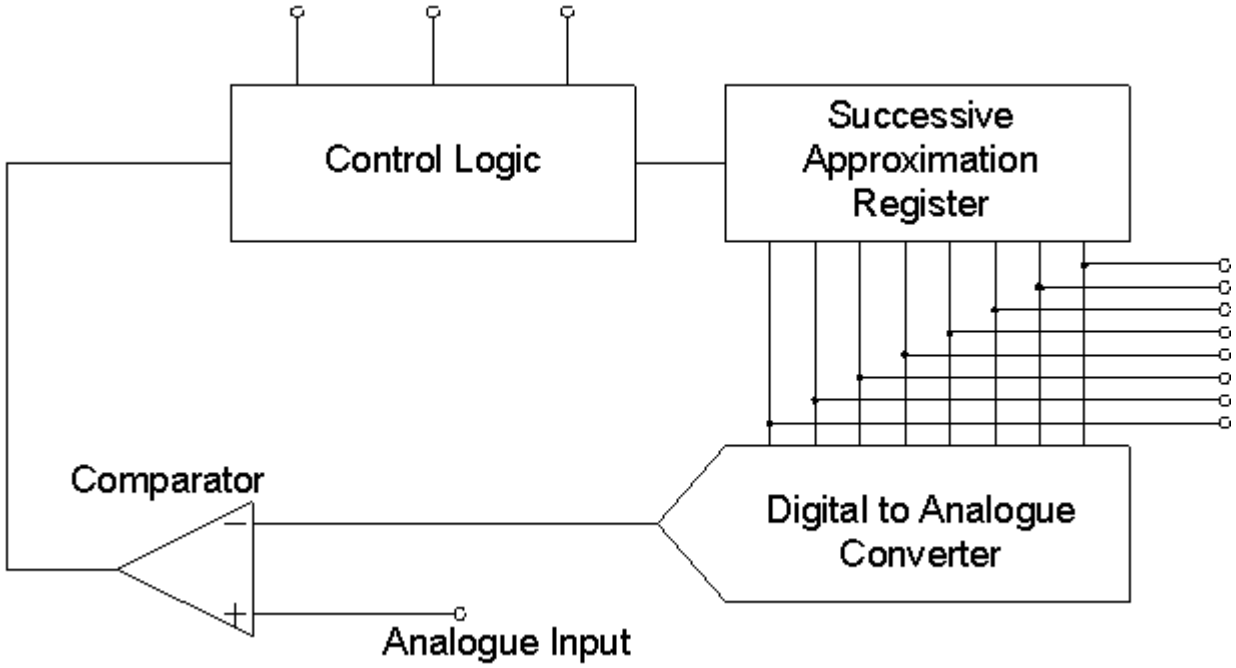
3-Bit Flash Analogue to Digital Converter (ADC)

The reference voltage for each comparator is set by the resistive voltage divider network. The output of each comparator is connected to an input of the priority encoder. The encoder is sampled by a pulse on the Enable input and a 3-bit binary code representing the analogue input appears on the encoder output. The binary code is determined by the highest order input having a High level.

Principle of Operation:

Successive Approximation ADC The flash ADC comprises an array of comparators. Each comparator is connected to a resistive voltage divider and to the analogue input voltage. The resistive voltage divider consists of equal valued resistors connected in series with the reference voltage VREF. Thus each comparator compares the analogue input voltage with a slightly different voltage from the divider. Those comparators which are connected to divider resistors where the

divider voltage is lower than the analogue input voltage will give a high output The other comparators will produce a low output. Larger analogue input voltages will result in more comparator high outputs. The pattern of comparator high/low outputs is applied to encoder circuits which convert the data into a binary output number which is proportional to the ratio of the analogue input voltage to the reference voltage.



The ADC is interfaced to a controller - usually a microprocessor. The controller decides when a conversion is to be performed and initiates the conversion by asserting the Start Convert signal line into the control logic.

The Control Logic monitors the input to determine whether the present contents of the register represent a value which is below or above the analogue input voltage. Each bit is set in turn starting with the MSB and working down to the LSB. The effect of setting each bit is noted by the control logic and if setting a particular bit results in a DAC output in excess of the analogue input voltage, the bit is cleared before moving on to the next bit otherwise the bit is left set.