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An Efficient Design of Binary to Gray Code Binary Converter using QCA

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Abstract- An upcoming Quantum Dot Cellular Automata (QCA) technology promises the incomparable compactness, high-speed operation and the features of ultralow-power utilization. In QCA, fault-tolerance is a significant feature to be considered in order to explore and manufacture quantum dots. For the reason of its high density and its inbuilt substantial properties. In this paper, the QCA based 2-bit, 3-bit, 4-bit, and 5-bit gray code converter have been proposed. The proposed converter designs reduce the number of cells (57.5% for 2-bit, 62.19% for 3-bit, 64.28% for 4-bit) and area (50% for 2-bit, 63.63% for 3-bit and 53.33% for 4bit) as compared to the earlier existing circuit, and also design a 5-bit converter. An integrated parameter, Area Utilization Factor (AUF) is also calculated for all the designs.

1. Introduction

The transistor based CMOS circuit fabrication focused is near to its physical limits [1], and there are several drawbacks to this technology at nanoscales such as high leakage, high cost of lithography and limitation of gigahertz frequency [2]. To overcome these physical limits, research in nanotechnology must be undertaken for improving the overall system efficiency by realizing Quantum dot Cellular Automata (QCA). In the year 1993, Lent *et. al* proposed a QCA based technology as a promising substitute to the CMOS technology [3]. It was further verified in the year 1997 [4]. The basic unit of this technology is a quantum cell, which includes a nanoscale square with quantum dots in its corners and two mobile electrons [5]. A quantum cell has two entirely polarized states, one being polarization (P = +1) and one polarization (P = -1) as given in Fig. 1(b & c). QCA executes logical operations and data transfer by Coulombic electron interactions inside the unit cell [5-6].
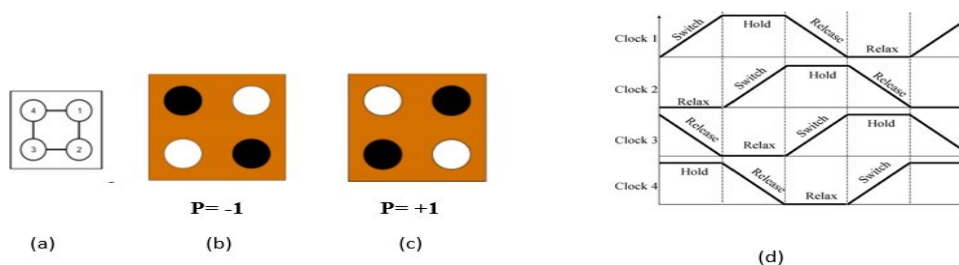

Fig. 1. (a) Unit cell (b) Polarization "-1" (binary "0") (c) Polarization "1" (binary "1") (d) Four clocks

with each one have a 90∘phase shift [9].

There is no charge movement such as in a conventional transistor. As a result, the consumption of power is lower than CMOS. The clock synchronizes and monitors the signal flow. It plays   a significant role in the QCA circuit. it has four clock zones; every clock zones are shifted by 90° [22]. Each clock zone has four states: switch, hold relax and release as shown in Fig. 1(d) [7-8].

Conventional binary data is expressed by the location of electrons in the quantum cell. The fundamental gates of QCA are three input majority voter and inverter. There are three input cells, one central cell and one output cell in the majority voter [10, 11, 12]. The output depends upon the majority of the input cell states. A logical expression is given in eq. (1). Fig. 2 (a) shows the majority voter [21].

$$OUT\ (A, B, C) = A.B + B.C + C.A \tag{1}$$

(a)

(b)
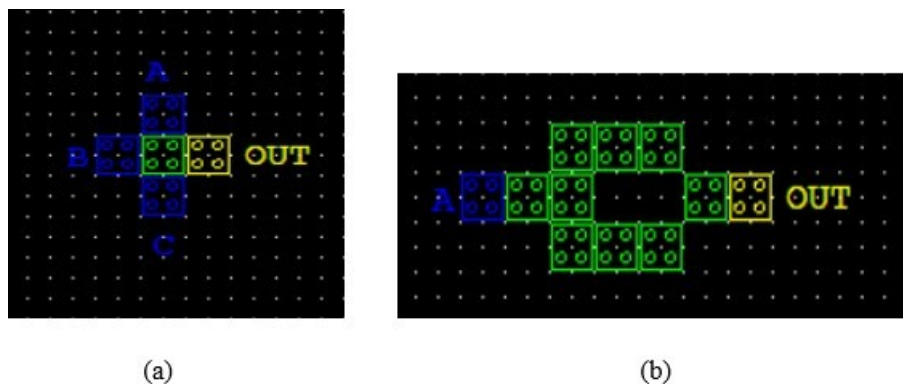
Fig. 2. (a) Majority voter gate (b) Inverter gate

In Fig. 2 (b) inverter gate is shown which has one input and one output. The output of the inverter is the complement of the input signal. Similarly, several QCA based logic gates are implemented and proposed in literature. The work presented in this paper is focused on gray code binary converter.

2. Related Work
Many researchers did lots of work in the field of QCA in past years. In [13], the authors designed a new 2-bit, 3-bit, 4-bit gray code converter. The circuit was analysed in terms of power analysis, number of cells, area and switching speed. Majeed *et. al* designed QCA based 3-bit, and 4-bit gray code converter, with fewer cells [14]. These designs are effective where the number of cells is smaller, the minimum clock phases are used and the interconnect length was significantly reduced. Islam *et al.* gave an effective and detailed approach to implement the QCA-based binary to gray code converter. The proposed designs required fewer cells, less phases of clock, and small area. The circuit working was verified by simulation result [15]. Guleria *et. al* designed a 4-bit gray code converter using fewer cells and less latency. The results of the designed were also verified with the truth table [16].

3. Methodology
Proposed circuits are designed with "QCADesigner 2.0.1". It is a modeling and simulation tool for a circuit based on QCA. The circuit's efficiency is tested by QCADesigner 2.0.1 which encompasses default values such as cell size, number of samples, the radius of effect, convergence tolerance, relative permittivity, clock amplitude factor, relaxation time which are given below [17]. In this

article, for the simulation of the circuits Bistable-Approximation Engine is used. Details of this engine is given in table 1.

Table 1. Simulation Engine Set-up details:

| Number of Samples	12800
Convergence Tolerance	0.001000
Radius of Effect [nm]	65.000000
Relative Permittivity	12.900000
Clock High	9.800000e-022
Clock Low	3.800000e-023
Clock shift	0.000000e+000
Clock Amplitude Factor	2.000000
Layer Separation	11.500000
Maximum Iterations Per Sample	100

4. Proposed Circuits and Analysis

At present lots of schemes are being used for data manipulation. In many cases, distinct codes use distinct schemes and it is required sometimes to use the contribution from one system to another system. Code converters are the circuits that convert the binary code into gray code [18].

4.1 Gray code

Gray codes are commonly used in digital communication to detect errors [19, 20]. Fig. 3(a) illustrates the QCA based 2-bit binary to gray code converter circuit [22]. The logical expression for the 2-bit binary to gray code converter is given in eq. (2) and (3) [24, 25] and the truth table is shown in Table 2.

$$g1 = b1 \tag{2}$$

$$g0 = b1 \oplus b0 \tag{3}$$
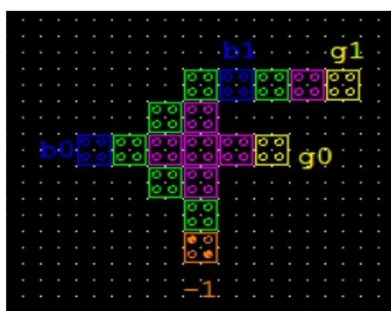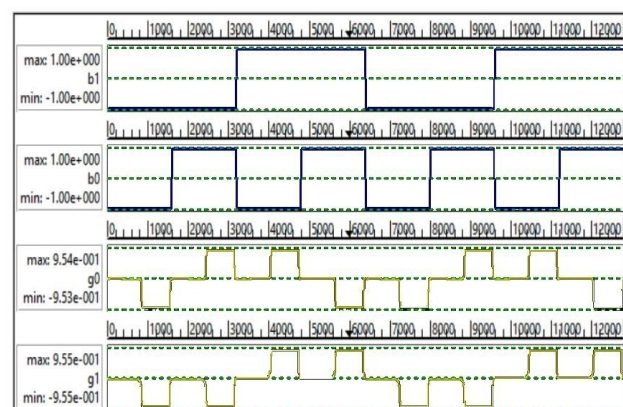
(a)   (b)

Fig 3. (a) QCA based 2-bit Gray code converter (b) Output of 2-bit Gray code converter

Table 2. The truth table for the 2-bit gray code converter

Binary Code		Gray Code	
b1	**b0**	**g 1**	**g0**
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 4. The truth table for the 4-bit gray code converter

Binary Code				Gray Code			
b3	**b2**	**b1**	**b0**	**g3**	**g2**	**g 1**	**g0**
0	0	0	0	0	0	0	0
1	0	0	0	1	1	0	0
0	0	0	1	0	0	0	1
1	0	0	1	1	1	0	1
0	1	0	0	0	1	1	0
1	1	0	0	1	0	1	0
0	1	0	1	0	1	1	1
1	1	0	1	1	0	1	1
0	0	1	0	0	0	1	1
1	0	1	0	1	1	1	1
0	0	1	1	0	1	1	0
1	0	1	1	1	1	1	0
0	1	1	0	0	1	0	1
1	1	1	0	1	0	0	1
0	1	1	1	0	1	0	0
1	1	1	1	1	0	0	0

Table 3. The truth table for the 3-bit gray code converter

Binary Code			Gray Code		
b2	**b1**	**b0**	**g2**	**g 1**	**g0**
0	0	0	0	0	0
0	0	1	0	0	1
1	0	0	1	1	0
1	0	1	1	1	1
0	1	0	0	1	1
0	1	1	0	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Fig. 4(a) illustrates QCA based 3-bit gray code converter circuit. Logical expression for the 3-bit binary to gray code converter is given in eq. (4), (5) & (6) and the truth table is displayed in Table 3.
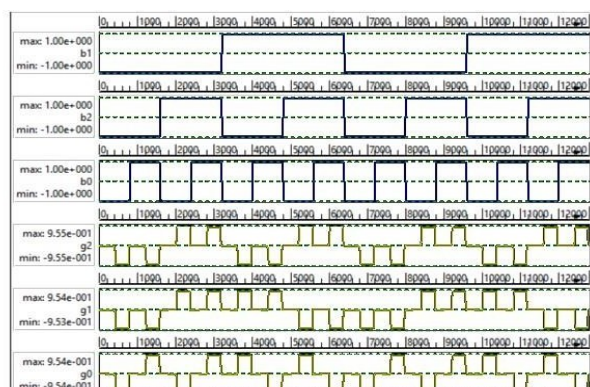
$$g2 = b2 \tag{4}$$

$$g1 = b2 \oplus b1 \tag{5}$$

$$g0 = b1 \oplus b0 \tag{6}$$
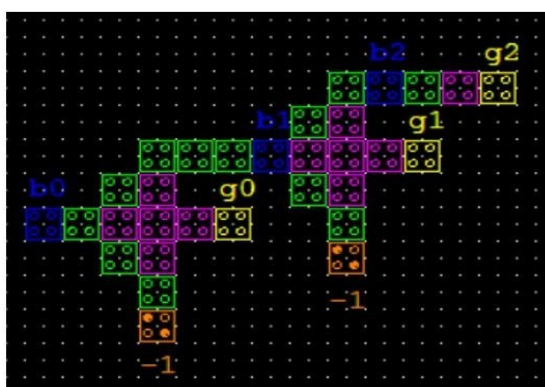
(a)   (b)

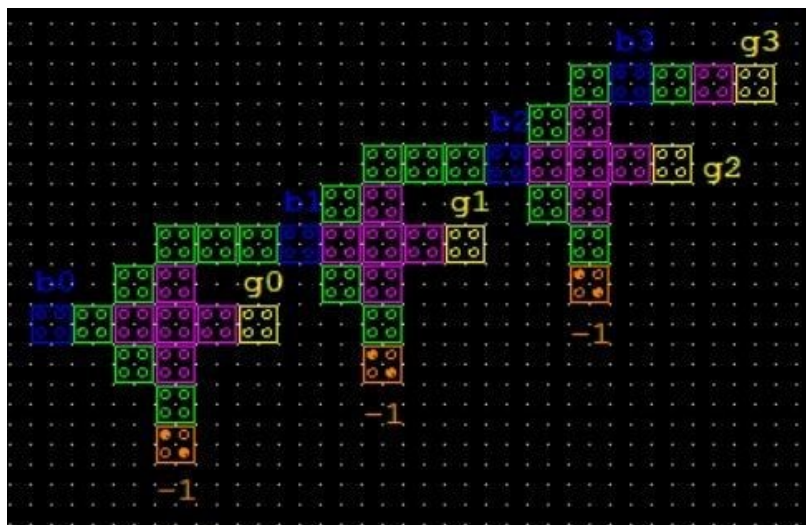**Fig 4.** (a) QCA based 3-bit converter (b) Output of 3-bit converter

Fig. 5(a) displays the QCA based 4-bit binary to gray code converter circuit. The logical expression for the 4-bit binary to gray code converter is given in eq. (7), (8), (9) & (10) and the truth table is presented in Table 4.
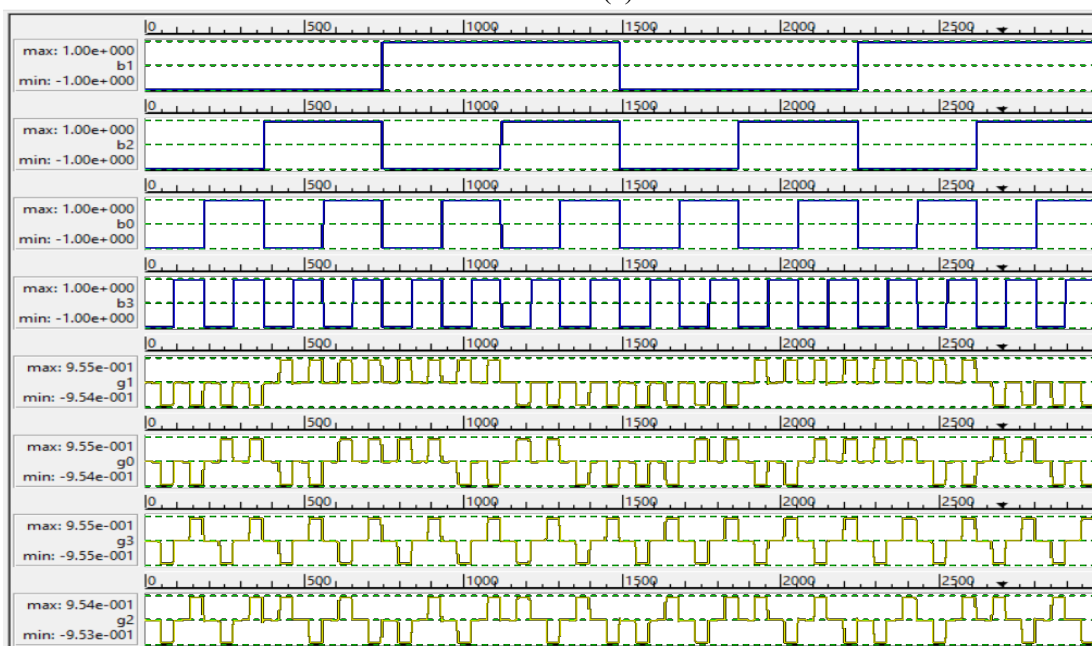
$$g3 = b3 \tag{7}$$

$$g2 = b3 \oplus b2 \tag{8}$$

$$g1 = b2 \oplus b1 \tag{9}$$

$$g0 = b1 \oplus b0 \tag{10}$$

(a)

(b)

Fig. 5. (a) QCA based 4-bit converter (b) Output of 4-bit converter

Fig. 6(a) shows the QCA based 5-bit gray code converter circuit. The logical expression for the 5-bit binary to gray code converter is given in eq. (11), (12), (13), (14) & (15) and the truth table is given in Table 5.

Table 5. The truth table of 5-bit gray code converter

| Binary Code					Gray Code				
b4	b3	b2	b1	b0	g4	g3	g2	g 1	g0
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	1	0	0	0
0	1	0	0	0	0	1	1	0	0
1	1	0	0	0	1	0	1	0	0
0	0	0	0	1	0	0	0	0	1
1	0	0	0	1	1	1	0	0	1
0	1	0	0	1	0	1	1	0	1
1	1	0	0	1	1	0	1	0	1
0	0	1	0	0	0	0	1	1	0
1	0	1	0	0	1	1	1	1	0
0	1	1	0	0	0	1	0	1	0
1	1	1	0	0	1	0	0	1	0
0	0	1	0	1	0	0	1	1	1
1	0	1	0	1	1	1	1	1	1
0	1	1	0	1	0	1	0	1	1
1	1	1	0	1	1	0	0	1	1
0	0	0	1	0	0	0	0	1	1
1	0	0	1	0	1	1	0	1	1
0	1	0	1	0	0	1	1	1	1
1	1	0	1	0	1	0	1	1	1
0	0	0	1	1	0	0	0	1	0
1	0	0	1	1	1	1	0	1	0
0	1	0	1	1	0	1	1	1	0
1	1	0	1	1	1	0	1	1	0
0	0	1	1	0	0	0	1	0	1
1	0	1	1	0	1	1	1	0	1
0	1	1	1	0	0	1	0	0	1
1	1	1	1	0	1	0	0	0	1
0	0	1	1	1	0	0	1	0	0
1	0	1	1	1	1	1	1	0	0
0	1	1	1	1	0	1	0	0	0
1	1	1	1	1	1	0	0	0	0

$$g4 = b4 \qquad (11)$$

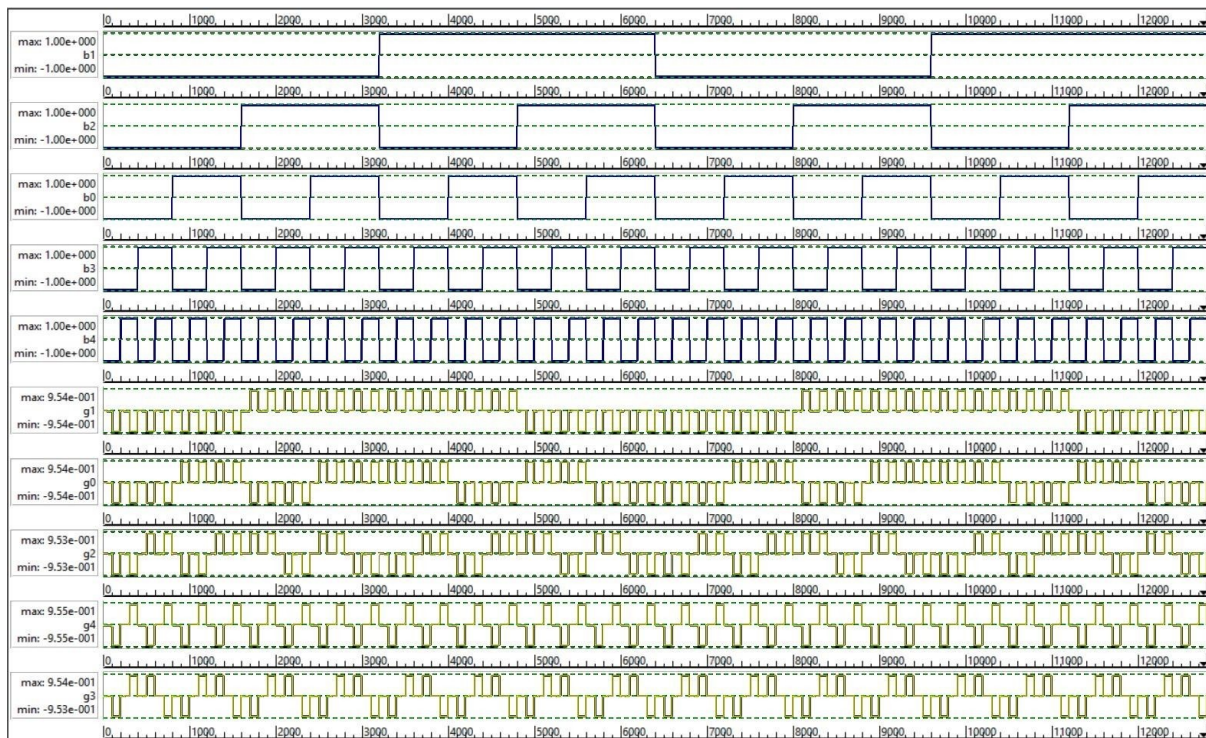$$g3 = b4 \oplus b3 \qquad (12)$$

$$g2 = b3 \oplus b2 \qquad (13)$$

$$g1 = b2 \oplus b1 \qquad (14)$$

$$g0 = b1 \oplus b0 \qquad (15)$$
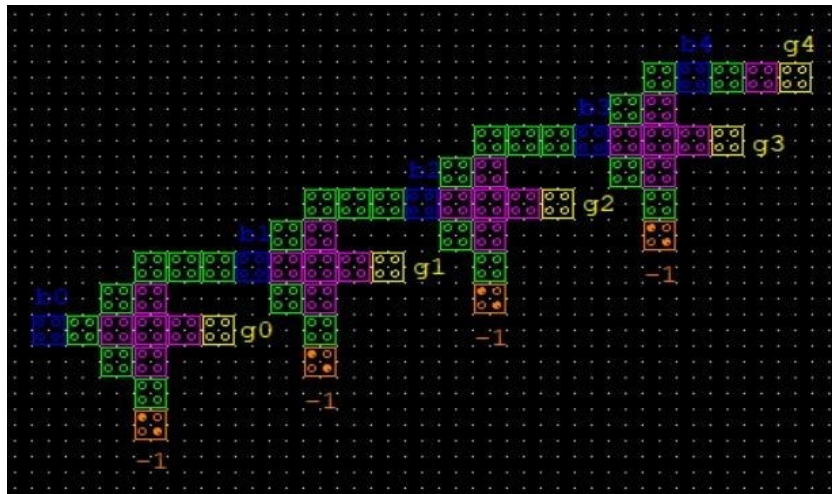
(a)

(b)

Fig. 6. (a) QCA based 5-bit converter (b) Output of 5-bit gray code converter

5. Result and Discussion

Fig. 7(a) illustrates the examination of required cells between proposed designs and existing designs. The proposed designs of 2-bit, 3-bit, 4-bit, 5-bit gray code converters take 17, 31, 45 and 59 number of cells respectively and whereas the existing designs in literature of 2-bit, 3-bit and 4-bit gray code converters took 40, 82 and 126 number of cells, respectively. This article also proposes a 5-bit gray code converter which is an advancement of the previous designs.
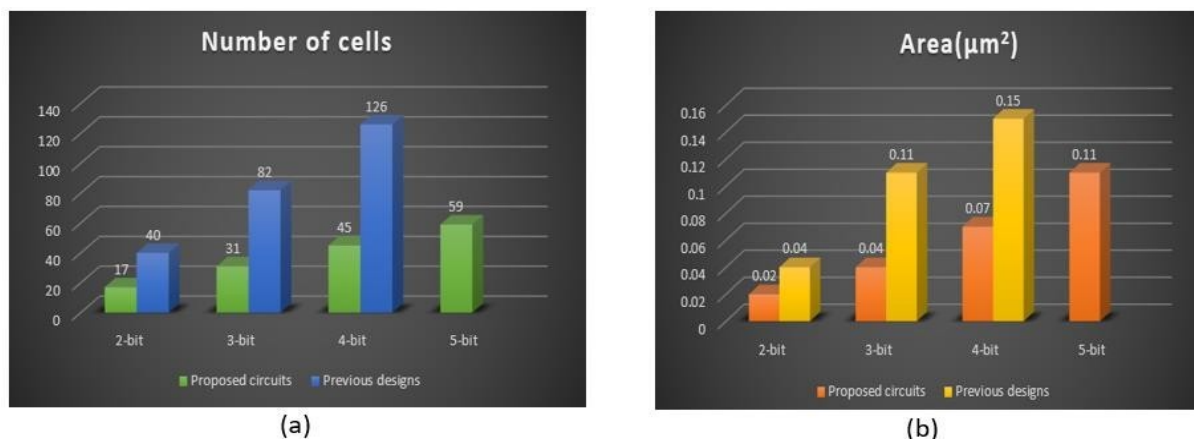
Fig. 7 (a) Comparison of required cells between proposed designs and previous existing designs
(b) Represent the area (μm^2) of basic gates and circuits.

Fig. 7(b) shows an analysis of the area between proposed designs and existing designs. The proposed designs of 2-bit, 3-bit, 4-bit, and 5-bit gray code converters take 0.02 μm^2, 0.04 μm^2, 0.07 μm^2 and 0.11 μm^2, respectively and previous existing designs of 2-bit, 3-bit, and 4-bit gray code converters take 0.04 μm^2, 0.11 μm^2 and 0.15 μm^2, respectively.

Fig. 8 shows the Area Utilization Factor (AUF) of 2-bit, 3-bit, 4-bit, and 5-bit binary to gray code converter which are 3.38, 4.05, 4.86 and 5.70, respectively.

Fig. 8. Area utilization factor (AUF)

6. Conclusion

This paper proposes a QCA based binary to gray code converter circuit. These converters' operations are explored using bistable vector simulation using QCA designer. The proposed designs are well organized with fewer cells and area. The designs proposed for the converter have an advantage in terms of cell count reduction by 57.5% for 2-bit, 62.17% for 3-bit and 64.28% for 4-bit and the area reduction of 50% for 2-bit, 63.63% for 3-bit and 53.33% for 4-bit, when compared to the existing circuits proposed in literature. The AUF of each design is also calculated.

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