Design and simulation of QCA-based 3-bit binary to gray and vice versa code converter in reversible and non-reversible mode

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ABSTRACT

The current Very Large-Scale Integration (VLSI) technology has reached its peak due to the fundamental physical limits of Complementary Metal-Oxide-Semiconductor (CMOS). Quantum-dot Cellular Automata (QCA) is considered a proper alternative to CMOS technology in digital circuit design. QCA has features like low power, small area, and high speed in nanoscale digital circuit design. A code converter is a circuit that converts a determined code to another one. Code converters such as Binary to Gray, Gray to Binary, and Binary to BCD converters have a crucial role in fast signal processing in digital systems. Also, code converters are used as a base unit for data transmission into the Arithmetic Logic Unit (ALU) to perform processes. A Binary-to-Gray converter converts the input data to a Gray number. In this paper, we propose a 3-bit Binary to Gray and vice versa code converter in QCA. Previous proposed designs could only convert Binary to Gray code or vice versa, but the proposed design convert both B2G and G2B codes into a circuit. We design our circuit in both reversible and non-reversible modes. The simulation of the proposed design is done using the QCADesigner 2.0.3 tools. The simulation results show that the proposed design is superior to the existing designs in terms of evaluation parameters such as cell count, area, latency, and quantum cost.

1. Introduction

With the growth of the digital industry, new challenges have emerged in using complementary Metal-Oxide-Semiconductor (CMOS) technology in nanoscale circuits' design [1]. CMOS technology has significant weakness, like power dissipation [2]. Reversible and non-reversible gates are commonly utilized in digital circuit design [3]. The number of inputs and outputs on a reversible logic gate should be equal. In a reversible gate, there is a separate output for each distinct input. The input and output vectors, on the other hand, have a one-to-one correlation. In irreversible logic gates, inputs cannot be calculated using outputs. In 1960, Landauer proved that performing reversible computations would result in KTLn2 Joules of energy dissipation for every bit of information loss. K is the Boltzmann constant, and T is the environmental temperature for performing computations [4]. The reversible gates are used to build reversible logic circuits [5]. CMOS technology challenges have raised motivation for researchers to work on

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designing alternative technologies like Quantum-dot Cellular Automata (QCA). The main components of QCA are quantum cells, which contain four quantum dots and two extra mobile electrons. The positions of these electrons define the binary states [4,6]. The QCA wire, QCA inverter, and QCA majority gate are regarded as the main elements in QCA logic devices. A QCA wire is a bundle of QCA cells. A QCA majority gate shows a three-input logic function. If the majority of inputs are "1", the output of the majority function will be in logic "1". If the majority of inputs are "0", the output of a majority function will be in logic "0" In QCA-based designs, there are two types of crossovers: coplanar and multilayer. Storing and clearing information in the QCA cells are controlled by the clock. In recent years, logic circuits such as adders, shift registers, multiplexers, increments, multipliers, subtractors, fault-tolerance circuits, and Arithmetic Logic Units (ALU) have been designed in QCA-based [6–24].

In order to perform calculations on information by a computer, it must first be converted into acceptable code and then processed. Therefore, designing and manufacturing different converters is very important. In digital systems, code converters have a significant role in fast signal processing. For performing processing, code converters are base units for data transfer to arithmetic units. Some of the crucial converters are Binary to Gray (B2G), Gray to Binary (G2B), Binary to BCD, and BCD to Binary. In Gray code, two consecutive numbers have just a one-bit difference. In recent years, there has been too much research into B2G code and G2B code converters based on reversible and non-reversible in QCA [16]. Previously proposed designs could only convert B2G codes or vice versa, but the proposed design in this paper can convert both B2G and G2B codes into a circuit. This paper follows the following contributions:

- The design of a reversible 3-bit B2G and vice versa converter in QCA is suggested.
- The design of a non-reversible 3-bit B2G and vice versa converter in QCA is proposed.
- The simulations of the proposed designs are done using QCADesigner 2.0.3 tools [25].
- Calculating evaluation parameters such as the number of cells, quantum cost, latency, and occupied area
- Comparing the proposed designs to related research

This paper is organized as follows: the basic concepts of QCA cell, QCA wire, QCA clocking, majority and inverter gates, RMUX1 block, and Feynman gate used in the proposed designs are described in Section 2. In Section 3, we discuss the previous studies. In Section 4, the logical schematic of proposed designs such as reversible and non-reversible converters is described in detail. In Section 5, the simulation results and the evaluation parameters such as quantum cost, the number of cells, the consumed area, and the delay are shown. Section 6 discusses the conclusion and future work.

2. Background

In this section, we explore the basic concepts of QCA technology, like the QCA cell, the QCA wire, the QCA clock, the majority gate, and the inverter gate. Also, we provide the block diagrams of the Feynman and the RMUX1 gates used in the proposed designs in subsections 2.4 and 2.5.

2.1. QCA Cell

The QCA cell is the basic unit of QCA. A QCA cell has a square structure. Each QCA cell has four quantum dots in the corners and two free electrons that can move freely between them. The electron locations for $p = 1$ and $p = -1$ polarizations are shown in Fig. 1 [10,26].

The QCA wire could be built by connecting cells side by side. Within a QCA circuit, the QCA wire is essential for transmitting information from one point to another. There are two varieties of QCA wire: 90° and 45°. The polarization of the whole array of QCA cells in a 90° QCA wire is the same. In a 45° QCA wire, each subsequent cell has alternating polarization. Fig. 2 shows two QCA-based wires with 90-degree (Fig. 2.a) and 45-degree (Fig. 2.b) cells [22,24,26].

2.2. QCA clocking

QCA requires a clocking mechanism. QCA circuits employ a different clocking mechanism than CMOS circuits. This mechanism divides the clock into four phases. They are: Switch, Hold, Release, and Relax. During the Switch phase, electrons begin to tunnel between dots. The state of a cell is fixed during the Hold phase. The state of the cell is unpolarized during the Release phase. The cells
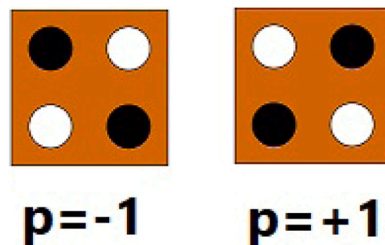

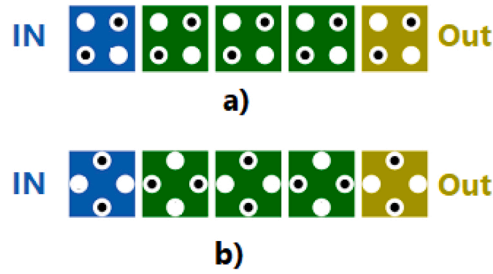**Fig. 1.** QCA cell polarization [26].

Fig. 2. QCA wire types [24,26].

remain unpolarized during the Relax phase [24,26].

2.3. Majority gate and QCA inverter

In this section, we will describe the majority and the inverter gates in QCA. In QCA-based designs, the majority gate is frequently employed. There are three or five inputs and just one output on them. The output value is calculated based on the input values. Setting one of the inputs of a three-input majority gate to the logic value "0" or "1", respectively, creates a logical AND-gate or OR-gate. Fig. 3 shows the AND-gate and OR-gate QCA schematics and layouts. The inverter gate is another proper gate in the QCA. Fig. 4 shows two examples of this gate. The And-gate, OR-gate, and inverter gate could be used to design and implement each of the combinational circuits [15,17,26].

2.4. Feynman Gate

The Feynman gate is a reversible gate with two inputs and two outputs. Fig. 5 depicts the schematic diagram of this gate. Its inputs are A and B. Its outputs, P and Q are described by the equations: $P = A, Q = A \oplus B$. The quantum cost of this gate is one. This gate may duplicate the input signal (if the input B is 0). It can also be used to complement the input signal (if the input B is 1).

2.5. RMUX1 Gate

RMUX1 is a reversible logic gate with three inputs and three outputs [28]. A, B, and C are inputs, and P, Q, and R are outputs of this gate. The relation between the inputs and outputs is described by Eq. (1). This gate's quantum cost is four. Fig. 6 depicts the block diagram for this gate.

$$\begin{cases} P = A \\ Q = \overline{A}B + AC \\ R = \overline{A}C + A\overline{B} \end{cases} \tag{1}$$

3. Previous works

In recent years, many researchers have conducted lots of research about digital converters in the QCA. Some of the presented articles have examined the aspects of fault-tolerance and testing [29–32], but we will not examine this aspect in this article. Saravanan et al. [33] suggested new reversible logic designs for B2G, G2B, and BCD to Excess-3 code, and Excess-3 to BCD code conversions. Karkaj et al. [34] proposed a two-input XOR gate. They designed and simulated reversible and non-reversible structures for 4-bit B2G and vice versa converters in QCA. Ahmed et al. [35] offered effective designs of B2G and G2B converters for 4, 8, and 16 bits, and these designs were scalable to N-bit. Al-Shafi et al. [36] proposed a 2-bit B2G, a 3-bit B2G, and a 4-bit B2G converter in QCA. Their proposed designs reduced the number of cells and the occupied area and increased the switching speed. Das et al. [37] Suggested reversible B2G and G2B code converters using the Feynman gate. Their design is suitable for low-power computer communications. Gassoumi et al. [26] presented a B2G code converter based on the Feynman gate. Their suggested converter comprises 29 cells and covers an occupied area of about of $0.04\mu m^2$. Xiao et al. [38] offered a QCA-based B2G code converter. The simulation results reveal that their proposed
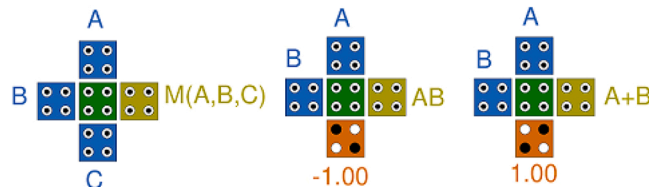

Fig. 3. QCA layout of the majority, The AND-gate and OR-gate [26].

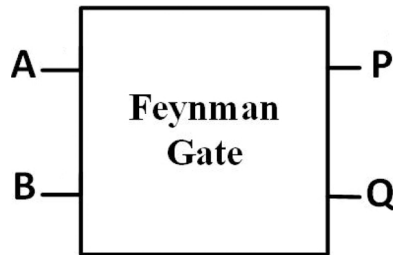**Fig. 4.** Two examples of inverter gate [26].

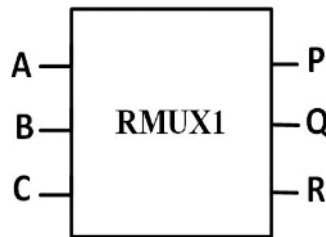**Fig. 5.** The block diagram of Feynman [27].

Fig. 6. The block diagram of RMUX1 [28].

design has a considerable improvement in terms of latency, complexity, and occupied space compared to existing work. Seyedi et al. [39] proposed a fault-tolerance nanoscale design for B2G converter based on QCA. They evaluated four parameters, namely, single-cell missing, displacement, misalignment, and extra single-cell by the simulation tools.

4. The proposed designs

A code converter is a combinational circuit that is put between two systems to make them compatible, as one of them may utilize different coding for the same data. The primary purpose of code converters is to increase the performance of information processing systems. QCA-based designed code converters are circuits for changing information from one format to another. Gray code converters have a wide range of applications in error detection and information transmission via computer networks. In existing designs, most converters have just the ability to perform B2G or G2B code conversion. In this paper, we suggest our designs that can convert B2G and G2B codes. In Sections 4.1, 4.2, and 4.3, we will examine each of them in detail.
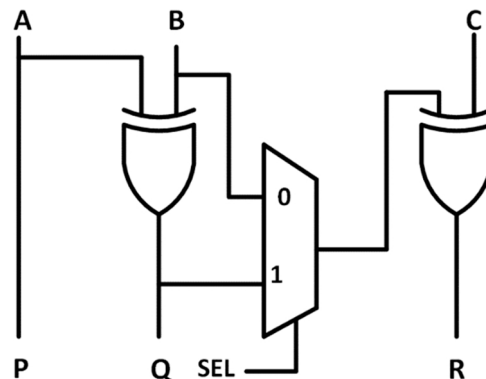

Fig. 7. The logical schematic of proposed 3-bit B2G converter and vice versa.

4.1. The logical schematic of proposed designs

In this section, the logical schematic of the proposed designs is presented. Fig. 7 depicts the logical structure of the proposed 3-bit B2G code converter and vice versa. The inputs are A, B, and C, whereas the outputs are P, Q, and R.

In the circuit, SEL serves as a selector. If SEL is equal to 0, the circuit acts as a B2G code converter, and if SEL is equal to 1, the circuit acts as a G2B code converter. In Eqs. (2) and (3), the output values are shown based on the SEL selection value.

$$
If \quad SEL == 0 \quad \Rightarrow \quad \left\{ \begin{array}{c} P = A \\ Q = A \oplus B \\ R = B \oplus C \end{array} \right\} \tag{2}
$$

$$
If \quad SEL == 1 \quad \Rightarrow \quad \left\{ \begin{array}{c} P = A \\ Q = A \oplus B \\ R = A \oplus B \oplus C \end{array} \right\} \tag{3}
$$

Table 1 shows the truth table for the suggested design. A, B, and C indicate converter inputs in this table; SEL is used as a selector. Also, P, Q, and R indicate converter outputs. The word "Converter" is used to specify the type of converter in Table 1.

4.2. Simulation of the proposed non-reversible B2G and vice versa code converter

Fig. 8 depicts a simulation of the proposed non-reversible B2G and vice versa code converter using the QCADesigner 2.0.3 tools. The QCADesigner is a precise tool for modeling and simulating QCA-based circuits [18]. The suggested circuit has 44 cells, 0.058 μm^2 area, and a one-clock delay. In this figure, the output functions for P, Q, and R, are according to Eq. (4). If the SEL is equal to 0, then the B2G code converter is shown in the output. If the SEL is equal to 1, then the G2B code converter is shown in the output.

$$
\left\{ \begin{array}{c} P = A \\ Q = A \oplus B \\ R = C \oplus (SEL.Q + \overline{SEL}.B) \end{array} \right\} \tag{4}
$$

4.3. Simulation of the proposed reversible 3-bit B2G and vice versa code converter

We employ Feynman and RMUX1 gates to create reversible 3-bit B2G and vice versa code converters in this article. Fig. 9 shows the logical design of the 3-bit reversible B2G and vice versa code converter. This design includes two Feynman gates and one RMUX1 gate. The RMUX1 gate is utilized to create the reversible selector. A, B, and C are inputs, and P, Q, and R are outputs. $Gr_1 and Gr_2$ are garbage outputs.

Fig. 10 depicts a simulation of this design using the QCADesigner 2.0.3 tools. This simulation includes 104 cells, an area of 0.133 μm^2, and a latency of 2 clocks. Its quantum cost is six.

4.4. Discussion

In recent years, related papers have suggested separate circuits for B2G and G2B code converters in the QCA. There was a need for a single circuit design which could integrate both capabilities in one circuit. As a result, we designed a circuit that can perform both conversions. We simulated the proposed design using the QCA designer tool and verified the accuracy of its operation according to

Table 1
Truth table for the proposed 3-bit B2G and G2B code converter.

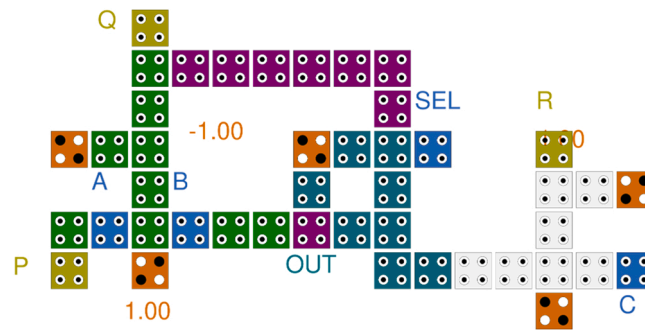| Selector	Inputs			Outputs			Converter
SEL	**A**	**B**	**C**	**P**	**Q**	**R**	**B2G**
0	0	0	0	0	0	0	
0	0	0	1	0	0	1	
0	0	1	0	0	1	1	
0	0	1	1	0	1	0	
0	1	0	0	1	1	0	
0	1	0	1	1	1	1	
0	1	1	0	1	0	1	
0	1	1	1	1	0	0	
1	0	0	0	0	0	0	**G2B**
1	0	0	1	0	0	1	
1	0	1	0	0	1	1	
1	0	1	1	0	1	0	
1	1	0	0	1	1	1	
1	1	0	1	1	1	0	
1	1	1	0	1	0	0	
1	1	1	1	1	0	1	

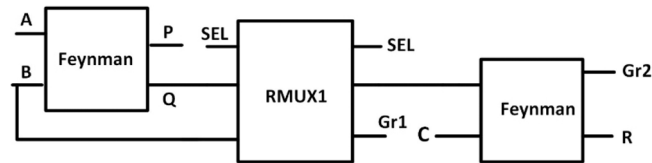Fig. 8. The proposed B2G and vice versa code converter in QCA.

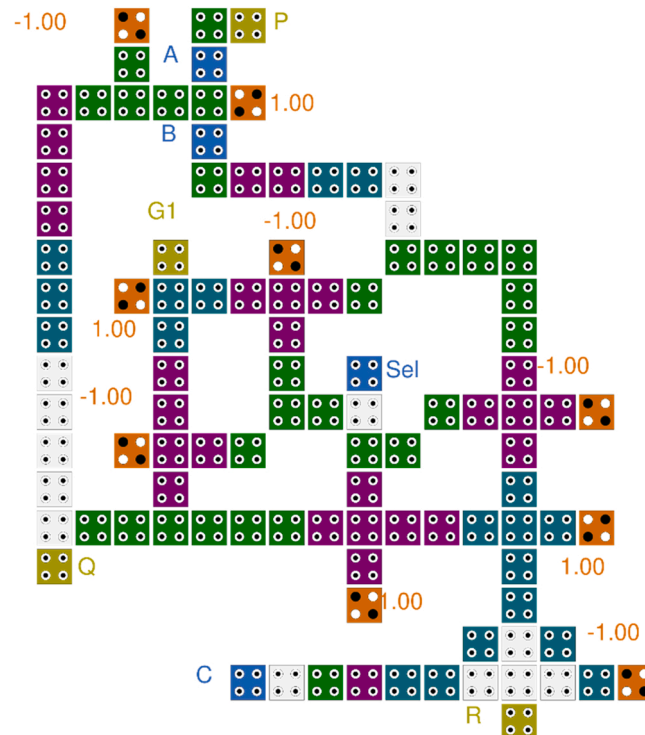Fig. 9. The block diagram of the proposed design of reversible 3-bit B2G and vice versa code converter.

Fig. 10. The proposed reversible B2G and vice versa code converter in QCA.

Table 1.

5. Simulation results and comparison of evaluation parameters

In this section, we will show the simulation results and compare them with the previous works. To evaluate the proposed design's precision, we used the QCA Designer 2.0.3 tool. Fig. 11 illustrates the results of both proposed designs. The inputs are A, B, and C. In the proposed design, SEL is employed as a selector. The outputs are P, Q, and R. The outputs of the reversible proposed design and the non-

reversible proposed design are appeared after 1 and 2 clock cycles, respectively. As stated in Section 4.1, if SEL = 0, the circuit acts as a 3-bit B2G code converter, and if SEL = 1, the circuit acts as a G2B code converter. All values shown in the output (Fig. 11) can be matched to the actual values specified in truth table (Table 1). For example, if ABC = 101 and SEL = 0, the circuit is a 3-bit B2G code converter, and the output becomes PQR = 111 (we marked the red box in Fig. 11). As another example, if ABC = 101 and SEL = 1, the circuit is a G2B code converter, and the output is PQR = 110 (we marked the blue box in Fig. 11).

The results of the proposed designs are evaluated, then compared to recent research in terms of the number of cells, latency, occupied area, quantum cost, and functionality. The functionality of a circuit means the kind of conversion that is done by the circuit. Is the circuit a B2G code converter? Or is it a G2B code converter? Alternately, it carries out both operations. The proposed design can convert B2G code and vice versa. Previous research could only do one type of conversion, but our proposed design can achieve both types of conversion. The comparisons of proposed designs for non-reversible and non-reversible designs are shown in two separate tables. In Table 2, comparisons of the proposed non-reversible designs to existing reversible designs are shown. As it is clear, the proposed design can perform both conversions, and at the same time it has been improved in terms of the number of cells and occupied area over the existing research.

Comparisons of the proposed reversible 3-bit B2G and vice versa code converters to existing reversible designs are shown in Table 3. This design can perform both functional conversions, which is a unique characteristic of the suggested design. In terms of the number of cells, it has improvements compared to some existing designs. In terms of latency, it is better than some available designs and worse than a few. The proposed design has the worst quantum cost of any other design. The reason for being worse in terms of quantum cost or other parameters compared to some existing designs is that we have used the selector to select between B2G and G2B code conversion. To perform this operation, we need to use a 3 * 3 reversible block. So, the best block that we can use for this operation has a minimum quantum cost of four, and the final quantum cost of this design is at least six. Our proposed design has the best possible value, too. Also, implementation of this design increases the number of cells as well as latency and area.

6. Conclusion and the future works

In this paper, we have proposed a unique design for a QCA-based B2G and vice versa code converter in both reversible and non-reversible modes. Its block diagram, the simulation, and the results were presented. The proposed design has a selector. If the value of the selector is equal to zero, it can perform QCA-based B2G. If the value of the selector is equal to one, it can perform a QCA-based G2B code converter. The proposed design was simulated in both reversible and non-reversible manners. The main advantage of the proposed design is that it can perform two types of converters. Previous designs could only perform one conversion, whereas the proposed design can perform both B2G and vice versa code converters. The simulation was performed using QCADesigner 2.0.3. The simulation results revealed that the suggested non-reversible design has a substantial advantage over existing designs regarding cell count and occupied area. Also, the reversible proposed design is better than some of the related work regarding cell count and latency. In future work, the proposed circuit could be scaled up to N-bit, the multiplexer's simulation could be improved, and the testing aspect of the proposed design could be completed.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to
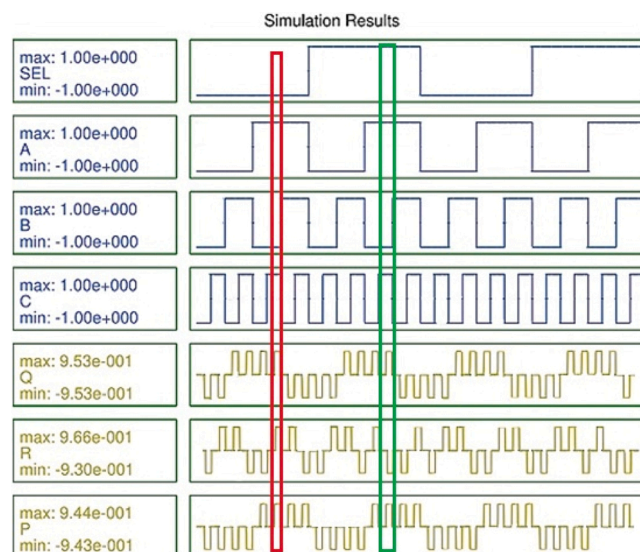

Fig. 11. Simulation results of the proposed designs.

Table 2

Comparisons of the proposed non-reversible 3-bit B2G and vice versa code converter.

Ref.	Cell Count	Area	Latency	Functionality
3-bit B2G converter[36]	82	$0.11\mu m^2$	0.75	Only B2G
3-bit B2G converter[40]	69	$0.08\mu m^2$	0.5	Only B2G
3-bit B2G converter[41]	59	$0.056\mu m^2$	0.75	Only B2G
Proposed Design	**44**	*0.058 μm^2*	**1**	**G2B and B2G**

Table 3

Comparisons of the proposed reversible 3-bit B2G and vice versa code converter.

Ref.	Cell Count	Area	Latency	Quantum Cost	Functionality
3-bit B2G converter[38]	29	$0.04\mu m^2$	0.5	2	Only B2G
3-bit B2G converter[37]	118	$0.0926\mu m^2$	3	2	Only B2G
3-bit G2B converter[37]	112	$0.1399\mu m^2$	4	2	Only G2B
3-bit G2B converter[10]	194	$0.2801\mu m^2$	4.25	2	Only G2B
3-bit B2G converter[10]	117	$0.0953\mu m^2$	2.25	2	Only B2G
3-bit B2G converter[12]	75	$0.0554\mu m^2$	1	2	Only B2G
3-bit G2B converter[12]	114	$0.10693\mu m^2$	2	2	Only G2B
3-bit B2G converter[42]	69	$0.0521\mu m^2$	0.75	2	Only B2G
3-bit G2B converter[42]	82	$0.0661\mu m^2$	1.5	2	Only G2B
Proposed Design of 3-bit B2G	**104**	*0.133μm^2*	**2**	**6**	**B2G and G2B**

influence the work reported in this paper.

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