Homework 3: Synthesis

In synthesis, we generate a logic circuit from a behavioral description. The behavioral description is in the form of Verilog code. The logic circuit is generated using logic gates from a specified standard cell library. This logic circuit, also called a gate-level netlist, is also in Verilog format.

In this homework assignment, you will create behavioral Verilog code for an ultra-simple combinational function, and manually generate the logic circuit with simple gates. In a subsequent assignment, you will run your behavioral code through a synthesis tool to generate the logic circuit automatically.

sel_sense

"sel_sense" is a simple combinational circuit with two inputs and one output. A plain-English behavioral description of the logic is as follows:

1. The circuit has one output, B, and two inputs, A and S
2. The output B is equal to the input A if S = 0 or is equal to the inverse of input A if S = 1.

Submissions:

(i) Write a simple behavioral Verilog code for sel_sense

(ii) Draw a schematic of a circuit that implements sel_sense. Your schematic must involve gates like NAND2, NOR2, MUX, INVERTER, XOR, NAND, etc. Choose whichever gates you like to implement the logic. Do not make a truth-table; draw a schematic based only on your understanding of the logic. Use standard symbols for the gates in your schematic.

(iii) Now write a truth table for the circuit. Based on your truth-table, if you would like to make an alternative schematic for the circuit, please do so, and you can submit that schematic as well.