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Part - A)

1) Compute the switching power consumption in the clock tree in the schematic given :

Soln:

Power =
$$C_L * V_{dd}^2 * f$$

$$V_{dd} = 0.8 \text{ v}$$

$$f = 750 \text{ MHz}$$

Total capacitance is
$$(C_L): C_{B1} + C_{nck1} + C_{B2} + C_{nck2} + C_{B3} + C_{nck3} + C_{B4} + C_{nck4} + C_{B4} + C_{FF1} + C_{nck5} + C_{B5} + C_{FF2} + C_{nck6} + C_{B6} + C_{FF3} + C_{nck7} + C_{B7} + C_{FF4}$$

$$C_L = 5 + (8 * 0.2) + 2(5 + (10 * 0.2)) + 4(7 + (16 * 0.2) + 2)$$

$$C_L = 69.4 \text{ fF}$$

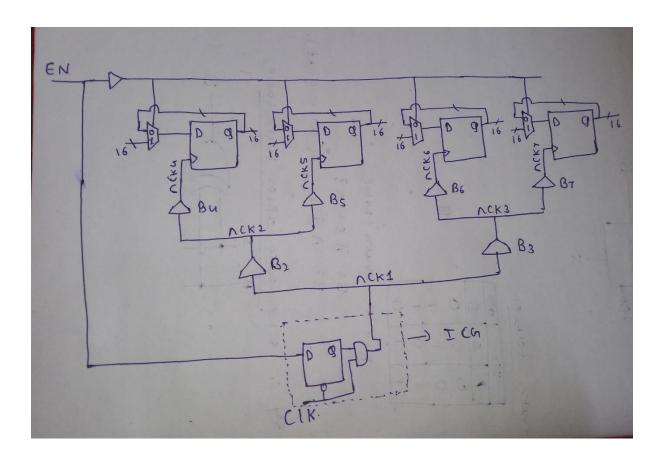
Power =
$$C_L * V_{dd}^2 * f$$

Power =
$$69.4 * (0.8)^2 * 750 * 10^{-9}$$

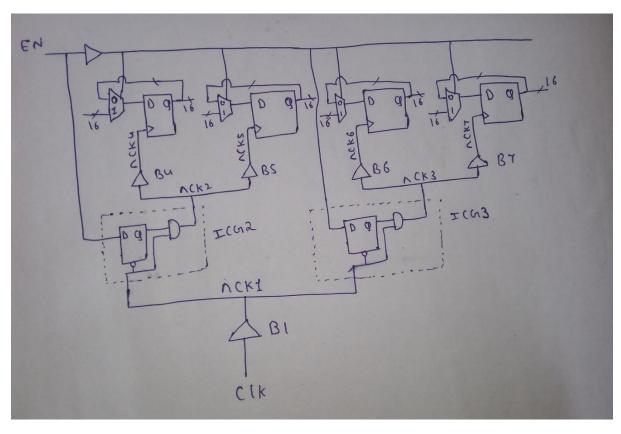
Power =
$$33.312 * 10^{-6}$$
 watt

Power = 33.312 micro watt

- 2) i)
- a) For the 64-bit register with enable, draw schematic when the buffer B1 is replaced with an ICG.



b) For the 64-bit register with enable, draw schematic when the buffer B3 and buffer B4 is replaced with ICGs.



ii) Compute the power in the clock tree for case (a) and case (b).

Case a)

Total capacitance is
$$(C_L): C_{ICG} + C_{nck1} + C_{B2} + C_{nck2} + C_{B3} + C_{nck3} + C_{B4} + C_{nck4} + C_{B4} + C_{FF1} + C_{nck5} + C_{B5} + C_{FF2} + C_{nck6} + C_{B6} + C_{FF3} + C_{nck7} + C_{B7} + C_{FF4}$$

$$C_L = 3 + (8 * 0.2) + 2(5 + (10 * 0.2)) + 4(7 + (16 * 0.2) + 2)$$

$$C_L = 67.4 \text{ Ff}$$

Power=
$$C_L * V_{dd}^2 * f$$

Power = 67.4 * $(0.8)^2 * 750 * 10^{-9}$
Power = 32.352 micro watt

Case b)

Total capacitance is
$$(C_L): C_{B1} + C_{nck1} + C_{ICG} + C_{nck2} + C_{ICG} + C_{nck3} + C_{B4} + C_{nck4} + C_{B4} + C_{FF1} + C_{nck5} + C_{B5} + C_{FF2} + C_{nck6} + C_{B6} + C_{FF3} + C_{nck7} + C_{B7} + C_{FF4}$$

$$C_L = 5 + (8*0.2) + 2(3 + (10*0.2)) + 4(7 + (16*0.2) + 2)$$

$$C_L = 65.4 \text{ Ff}$$

Power=
$$C_L * V_{dd}^2 * f$$

Power = 23.8 * $(0.8)^2 * 750 * 10^{-9}$

Power = 31.392 micro watt

Part - B)

ICGs in Standard Cell Libraries

Determine the number and type of ICGs in the four libraries listed below, and tabulate the information in the tables that follow:

- 1) Cadence RAK
- 2) Nangate
- 3) Nangate 15nm
- 4) Skywater

CMOS ASIC DESIGN

Solutions_Assignment2

	Cadence RAK	Nangate	Nangate 15nm	Skywater
Total no. of ICGs	16	8	1	6
ICGs with no test input	16	8	0	0
ICGs with test input	0	0	1	0
ICG max drive strength	X20	X8	X1	X4
ICG min drive strength	X2	X1	X1	X1