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Part – A: Sel_sense

1] Synthesize sel_sense with the SkyWater HS and MS libraries. Submit the resulting netlists.

sel_sense with the SkyWater HS library:

```
                          Total  Weighted
Operation                  Area  Neg Slk Worst Path
-------------------------------------------------------------------------------
 global_incr                 11        0  N/A

    Cost Group            Target    Slack    Clock
-------------------------------------------------
       default          unconst. unconst.     N.A.

Info    : Done mapping. [SYNTH-5]
        : Done mapping 'sel_sense'.
     flow.cputime  flow.realtime  timing.setup.tns  timing.setup.wns  snapshot
UM:             0            193             -0 ps       infinity ps  syn_map
legacy_genus:/> write_hdl

// Generated by Cadence Genus(TM) Synthesis Solution GENUS15.22 - 15.20-s024_1
// Generated on: Oct 11 2020 23:46:32

// Verification Directory fv/sel_sense

module sel_sense(A, S, B);
  input A, S;
  output B;
  wire A, S;
  wire B;
  sky130_fd_sc_hs__xnor2_1 g12(.A (S), .B (A), .Y (B));
endmodule

legacy_genus:/>
```

sel_sense with the SkyWater MS library:

```
                          Total  Weighted
Operation                  Area  Neg Slk Worst Path
-------------------------------------------------------------------------------
 global_incr                 11        0  N/A

    Cost Group            Target    Slack    Clock
-----------------------------------------------------
       default          unconst. unconst.     N.A.

Info    : Done mapping. [SYNTH-5]
        : Done mapping 'sel_sense'.
     flow.cputime  flow.realtime  timing.setup.tns  timing.setup.wns  snapshot
UM:             0             16             -0 ps       infinity ps  syn_map
legacy_genus:/> write_hdl

// Generated by Cadence Genus(TM) Synthesis Solution GENUS15.22 - 15.20-s024_1
// Generated on: Oct 12 2020 00:44:25

// Verification Directory fv/sel_sense

module sel_sense(A, S, B);
  input A, S;
  output B;
  wire A, S;
  wire B;
  sky130_fd_sc_ms__xnor2_1 g12(.A (S), .B (A), .Y (B));
endmodule

legacy_genus:/>
```

adlv30@VLSI18:~ adlv30@VLSI18:/cad_a...

2] Put a “don’t use” on all XOR and XNOR gates, resynthesize, and submit the resulting netlists.

For skywater HS library:

After using set_dont_use skywater_fd_sc_hs__xnor2_2 we got this further on doing the same for xnor2_4 in the netlist found no changes

```
        plc_star         0  (        0 /        0 )  0.00
        drc_bufs         0  (        0 /        0 )  0.00
        drc_fopt         0  (        0 /        0 )  0.00
        drc_bufb         0  (        0 /        0 )  0.00
             dup         0  (        0 /        0 )  0.00
       crit_dnsz         0  (        0 /        0 )  0.00
       crit_upsz         0  (        0 /        0 )  0.00

Info    : Done incrementally optimizing. [SYNTH-8]
        : Done incrementally optimizing 'sel_sense'.
     flow.cputime  flow.realtime  timing.setup.tns  timing.setup.wns  snapshot
UM:             0             18             -0 ps       infinity ps  syn_opt_7
legacy_genus:/> write_hdl

// Generated by Cadence Genus(TM) Synthesis Solution GENUS15.22 - 15.20-s024_1
// Generated on: Oct 12 2020 00:04:47

// Verification Directory fv/sel_sense

module sel_sense(A, S, B);
  input A, S;
  output B;
  wire A, S;
  wire B;
  sky130_fd_sc_hs__xnor2_4 g12(.A (S), .B (A), .Y (B));
endmodule

legacy_genus:/> set_dont_use sky130_fd_sc_hs__xnor2_4
legacy_genus:/> syn_opt
```

For skywater MS library:
After using set_dont_use skywater_fd_sc_ms__xnor2_2 we got this further on doing the same for xnor2_4 in the netlist found no changes

```
          plc_st         0  (        0 /        0 )  0.00
        plc_star         0  (        0 /        0 )  0.00
        drc_bufs         0  (        0 /        0 )  0.00
        drc_fopt         0  (        0 /        0 )  0.00
        drc_bufb         0  (        0 /        0 )  0.00
             dup         0  (        0 /        0 )  0.00
       crit_dnsz         0  (        0 /        0 )  0.00
       crit_upsz         0  (        0 /        0 )  0.00

Info    : Done incrementally optimizing. [SYNTH-8]
        : Done incrementally optimizing 'sel_sense'.
     flow.cputime  flow.realtime  timing.setup.tns  timing.setup.wns  snapshot
UM:             0             35             -0 ps       infinity ps  syn_opt_2
legacy_genus:/> write_hdl

// Generated by Cadence Genus(TM) Synthesis Solution GENUS15.22 - 15.20-s024_1
// Generated on: Oct 12 2020 00:47:39

// Verification Directory fv/sel_sense

module sel_sense(A, S, B);
  input A, S;
  output B;
  wire A, S;
  wire B;
  sky130_fd_sc_ms__xnor2_4 g12(.A (S), .B (A), .Y (B));
endmodule

legacy_genus:/>
```

3] For the HS and MS netlists with no “don’t use” directives, plot A->B delay as a function of load capacitance at B. Let the capacitance vary from 0.005 to 0.1 pF. Create plots for S = 0 and for S = 1. Let transition time at A be 0.04 ns. Note that for timing to be reported from A to B, you will need to specify a max delay constraint for that path.

For Skywater HS library:

A] For 0.005pf as a load capacitance

```
  Generated on:           Oct 12 2020  12:22:29 am
  Module:                 sel_sense
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


Path 1: VIOLATED (-29 ps) Path Delay Check
     Startpoint: (R) A
       Endpoint: (R) B

                 Capture    Launch
     Path Delay:+      50         -
        Arrival:=      50

  Required Time:=      50
      Data Path:-      79
          Slack:=     -29

#-------------------------------------------------------------------------------------------------
# Timing Point   Flags   Arc   Edge           Cell            Fanout Load Trans Delay Arrival
#                                                               (fF)  (ps)  (ps)   (ps)
#-------------------------------------------------------------------------------------------------
  A              <<<     -     R     (arrival)                    1 14.8    40     0       0
  g12/Y          -       B->Y  R     sky130_fd_sc_hs__xnor2_4     1  5.0    74    79      79
  B              <<<     -     R     (port)                       -    -     -     0      79
#-------------------------------------------------------------------------------------------------

legacy_genus:/>
```

B] For 0.1pf as a load capacitance

```
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================


Path 1: VIOLATED (-105 ps) Path Delay Check
     Startpoint: (F) A
       Endpoint: (R) B

                  Capture    Launch
     Path Delay:+      50         -
        Arrival:=      50

  Required Time:=      50
      Data Path:-     155
          Slack:=    -105

#-------------------------------------------------------------------------------------------------
# Timing Point   Flags   Arc   Edge           Cell             Fanout  Load Trans Delay Arrival
#                                                                      (fF)  (ps)  (ps)   (ps)
#-------------------------------------------------------------------------------------------------
  A              <<<     -     F     (arrival)                      2  65.4    40     0       0
  g18/Y          -       A->Y  R     sky130_fd_sc_hs__clkinv_16     1  16.1    18    15      15
  g22/Y          -       A->Y  F     sky130_fd_sc_hs__nand2_8       1  16.0    25    24      40
  g21/Y          -       B->Y  R     sky130_fd_sc_hs__nand2_8       1 100.0   172   116     155
  B              <<<     -     R     (port)                         -     -     -     0     155
#-------------------------------------------------------------------------------------------------

legacy_genus:/> 
```

For Skywater MS library:

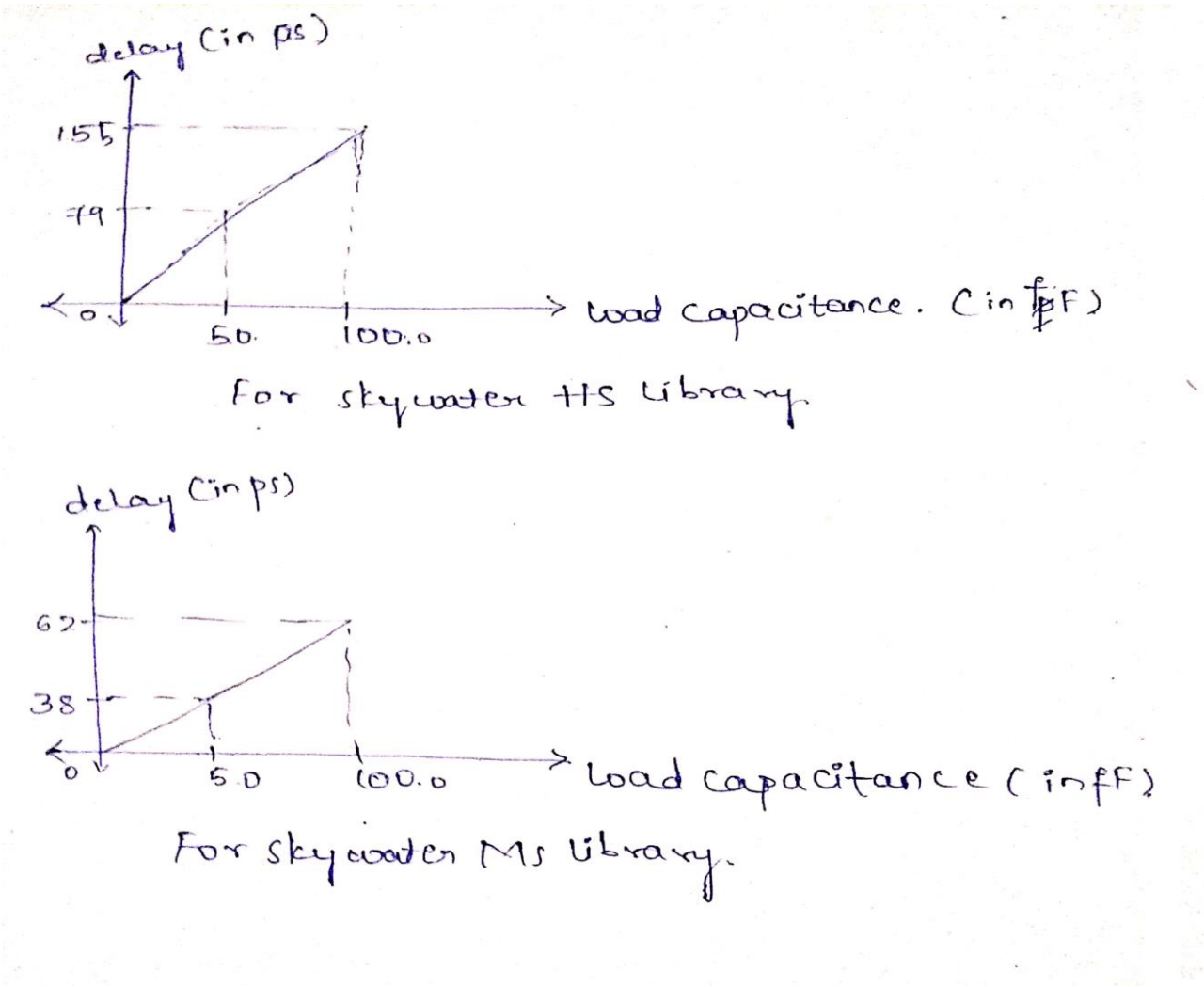
A] For 0.005pf as a load capacitance

```
  Module:                 sel_sense
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================


Path 1: MET (72 ps) Path Delay Check
     Startpoint: (F) A
       Endpoint: (R) B

                  Capture    Launch
     Path Delay:+     200         -
        Arrival:=     200

  Required Time:=     200
      Data Path:-     128
          Slack:=      72

#-------------------------------------------------------------------------------------------------
# Timing Point   Flags   Arc   Edge          Cell            Fanout Load Trans Delay Arrival
#                                                                 (fF)  (ps)  (ps)   (ps)
#-------------------------------------------------------------------------------------------------
  A              <<<     -     F     (arrival)                   1  5.8    40     0       0
  g2/X           -       A->X  F     sky130_fd_sc_ms__xor2_1     1  3.2    38    90      90
  g3/Y           -       A->Y  R     sky130_fd_sc_ms__inv_1      1  5.0    39    38     128
  B              <<<     -     R     (port)                      -    -     -     0     128
#-------------------------------------------------------------------------------------------------

legacy_genus:/> 
```

B] For 0.1pf as a load capacitance

```
  Area mode:              timing library
============================================================


Path 1: MET (2 ps) Path Delay Check
     Startpoint: (F) A
       Endpoint: (F) B

                  Capture    Launch
     Path Delay:+     200         -
        Arrival:=     200

  Required Time:=     200
      Data Path:-     198
          Slack:=       2

#-------------------------------------------------------------------------------------------------------
# Timing Point   Flags   Arc   Edge           Cell             Fanout  Load Trans Delay Arrival
#                                                               (fF)  (ps)  (ps)   (ps)
#-------------------------------------------------------------------------------------------------------
  A              <<<     -     F     (arrival)                     2  60.8    40     0       0
  g2/Y           -       A->Y  R     sky130_fd_sc_ms__clkinv_16    1   5.9    16    17      17
  g4/Y           -       A->Y  F     sky130_fd_sc_ms__nand2_2      1   8.8    35    34      51
  g6/Y           -       A->Y  R     sky130_fd_sc_ms__nand2_4      1  23.5   112    84     136
  g21/Y          -       A->Y  F     sky130_fd_sc_ms__inv_8        1 100.0    66    62     198
  B              <<<     -     F     (port)                        -     -     -     0     198
#-------------------------------------------------------------------------------------------------------

legacy_genus:/>
```

Plots:



Part – B: Mux Comparator

1] Write behavioral Verilog code for a combinational logic function called “mux_comparator” that compares two three-bit numbers x and y, and outputs whichever one of the two numbers is numerically less. Output should be called z.

```
Module mux_comparator(x,y,z);

Input [2:0] x,y;

Output [2:0] z;

always@(*)

if(x>y) z = y; else z = a;

endmodule
```