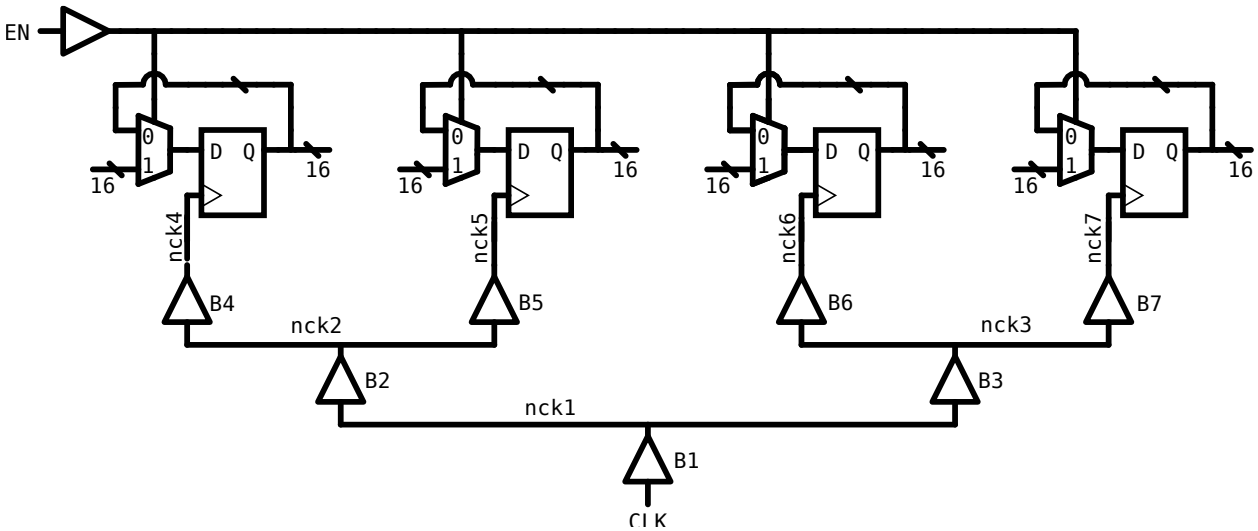
Homework 2: Clock Gating

(A) Clock Power

The following is a schematic of a 64-bit register with enable:



Net lengths and pin capacitances

- The following table lists the input pin capacitances of the clock buffers:

Instance Names	Input Pin Capacitance (fF)
B1, B2, B3	5
B4, B5, B6, B7	7

- The capacitance of the clock pin of flip-flops is 2 fF.
- The capacitance of nets is 0.2 fF/μm. The following table lists the lengths of the nets in the clock tree:

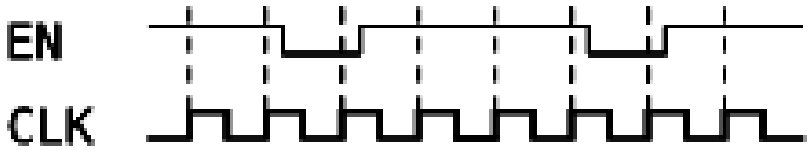
Net Names	Length (μm)
nck1	8
nck2, nck3	10
nck4, nc5, nck6, nck7	16

Operating Conditions and Clock Frequency

- The power supply voltage is 0.8V.
- The clock frequency is 750 MHz.

Questions

(1) Compute the switching power consumption in the clock tree in the schematic above
(2) The EN has the following periodic waveform:



The circuit is reimplemented with clock gating with ICGs. The capacitance of the C input pin of the ICG is 3 fF. Two implementations are done:

a) the buffer B1 is replaced with an ICG.
b) the buffer B1 is retained, but B2 and B3 are each replaced with an ICG.

i) Draw circuit schematics for case (a) and case (b)
ii) Compute the power in the clock tree for case (a) and case (b).

(B) ICGs in Standard Cell Libraries

Determine the number and type of ICGs in the four libraries listed below, and tabulate the information in the tables that follow:

1) Cadence RAK
2) Nangate
3) Nangate 15nm
4) Skywater

	Cadence RAK	Nangate	Nangate 15	Skywater
Total no. of ICGs				
ICGs with no test input				
ICGs with test input				
ICG max drive strength				
ICG min drive strength				