Homework 4: Synthesis

(A) sel_sense

You can use the behavioral code that you wrote for sel_sense in Homework Assignment #3 for the questions that follow, or you can use the behavioral code in /cad_area/vlsi/design/selsense/sel_sense.v.

Submissions:

(i) Synthesize sel_sense with the SkyWater HS and MS libraries. Submit the resulting netlists.

(ii) Put a "don't use" on all XOR and XNOR gates, resynthesize, and submit the resulting netlists.

(iii) For the HS and MS netlists with no "don't use" directives, plot A->B delay as a function of load capacitance at B. Let the capacitance vary from 0.005 to 0.1 pF. Create plots for S = 0 and for S = 1. Let transition time at A be 0.04 ns. Note that for timing to be reported from A to B, you will need to specify a max delay constraint for that path.

(B) mux_comparator

Submissions:

(i) Write behavioral Verilog code for a combinational logic function called "mux_comparator" that compares two three-bit numbers x and y, and outputs whichever one of the two numbers is numerically less. Output should be called z.

(ii) Synthesize this function with the libraries Cadence RAK, NangateOpenCellLibrary and Nangate_15nm_OCL (see Homework #1 for paths). Submit the three netlists that result.

(iii) In each case, identify the critical path from input to output, listing the max_delay from input to output. List the number of standard cells in the critical path.

(iv) In each case, identify the min_delay path and tabulate the min delay. List the number of standard cells in the min_delay path.

(v) Change the three-bit numbers x and y to eight-bit numbers. Resynthesize, and report the number of standard cells in the critical (max_delay) path.