Name – Manjunath Veeraiah Kalmath

USN - 01FE17BEC240

Roll No – 175

School of ECE

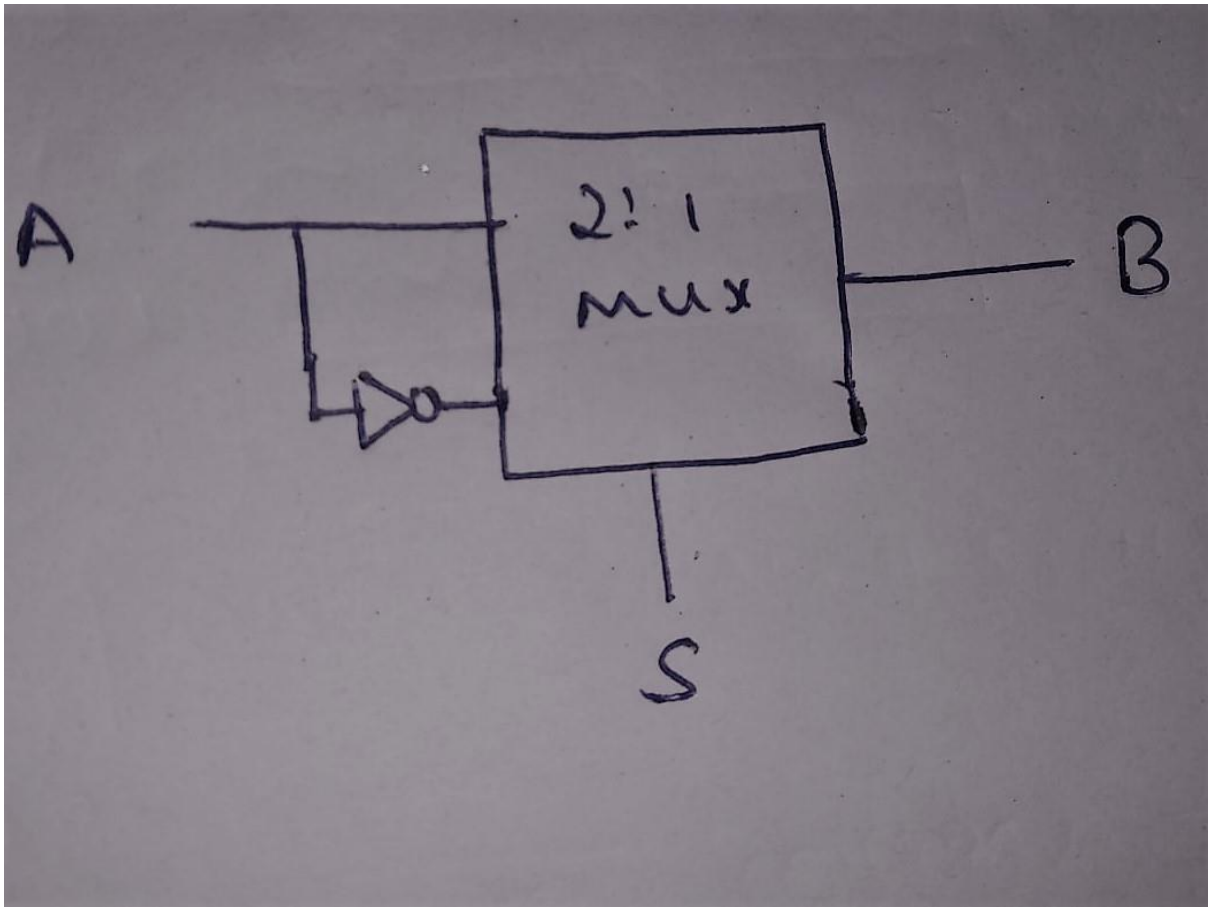
Q1. Write a simple behavioral Verilog code for sel_sense

*****Verilog Code*****

```
Module sel_sense(A,S,B);
Input A,S;
Output B;
always@(*)
begin
        if(S==0)
                B=A;
        else
                B=!A;
end
endmodule
```

****

Q2. Draw a schematic of a circuit that implements sel_sense. Your schematic must involve gates like NAND2, NOR2, MUX, INVERTER, XOR, NAND, etc. Choose whichever gates you like to implement the logic. Do not make a truth-table; draw a schematic based only on your understanding of the logic. Use standard symbols for the gates in your schematic.



Q3. Now write a truth table for the circuit. Based on your truth-table, if you would like to make an alternative schematic for the circuit, please do so, and you can submit that schematic as well.

→ Truth Table:

I/p		O/p
A	S	B
0	0	0
0	1	1
1	0	1
1	1	0

From Truth Table,

$B = A \oplus S$.

⟹ Use of "XOR Gate"

→ Schematic After writing Truth Table: