Homework 1: Standard Cell Libraries

For the exercises below, you will use the following standard cell libraries:

1. RAK (from Cadence's Rapid Adoption Kit)
   You will find the dotlib and LEF files under
   /cad_area/vlsi/libraries/cadence_RAK/LIBS/lib/max
   /cad_area/vlsi/libraries/cadence_RAK/LIBS/lef
2. NangateOpenCellLibrary
   You will find the dotlib under:
   /cad_area/vlsi/libraries/Nangate_OCL
   You will find the LEF under
   /home/anandb/ultralite/tech/NangateOpenCellLibrary_PDKv1_3_v2010_12/Back_End
3. Nangate_15nm_OCL
   You will find the dotlib under:
   /cad_area/vlsi/libraries/NanGate_15nm_OCL_v0.1_2014_06_Apache.A/front_end/timing_power_noise/NLDM
   You will find the LEF under:
   /cad_area/vlsi/libraries/NanGate_15nm_OCL_v0.1_2014_06_Apache.A/back_end/lef
4. Skywater
   You will find the dotlib for the high-speed (HS) library under:
   /cad_area/vlsi/libraries/skywater/sky130_fd_sc_hs/Liberty
   You will find the dotlib for the medium-speed (MS) library under:
   /cad_area/vlsi/libraries/skywater/sky130_fd_sc_ms/Liberty

Create Links to the Library Files

First, from your home directory, set up *links* to all the files or directories listed above. This saves you the trouble of having to specify the whole path each time to access those files or directories. You can even use simpler names to reduce typing. A link is essentially a shortcut. It is a type of file in unix that points to another file or a folder on your computer.

To create a link, you use the unix "ln -s" command:

```
unix> ln -s <path to the file/folder to be linked> <name of link to be created>
```

For example:

```
unix> link -s /home/anandb/ultralite/tech/NangateOpenCellLibrary_PDKv1_3_v2010_12/Front_End/Liberty nangate_lib
```

When you run "ls -l" at your unix prompt, links will be listed with an "l" in the first field: lrwxrwxrwx

Using pipelined unix commands like grep, determine and tabulate the data requested below. When using grep, you will likely need to use the -A and -B options to get the lines you need.

(A) Cell counts and types

	RAK	Nangate_OCL	Nangate_15nm	Skywater HS
Total No. of Cells				
DFFs				
Total no. of DFFs				
No. of DFFs with reset				
No. of DFFs with set				
No. of negative edge-triggered DFFs				
NAND gates				
Count of 2-input NAND gates				
Count of 3-input NAND gates				
Count of 4-input NAND gates				
Muxes				
Count of 2-input muxes*				
Count of 3-input muxes*				
Count of 4-input muxes*				

*Note that a "2-input" mux actually has a third input, which is the "select" input. Similarly, 3-input and 4-input muxes will have two select inputs, which are in addition.

(B) Cell Drive Strengths

	RAK	Nangate_OCL	Nangate_15nm	Skywater HS
Inverter				
Total count				
Max drive strength				
Min drive strength				
Buffer				
Total count				
Max drive strength				
Min drive strength				
NAND2				
Total count				
Max drive strength				
Min drive strength				
DFFs				
Total count				
Max drive strength				
Min drive strength				

(C) Cell pin capacitances and area

For any gate with more than one input, the input pin capacitance will be different for different inputs. Select any one input, but be consistent and use the same input when you report capacitance vs. drive strength in the table below.

Cell	Input Pin	Cadence_RAK	Nangate_OCL	Nangate_15nm	Skywater HS
Inverter					
Buffer					
NAND2					

(D) Operating Conditions (P-V-T)

In the skywater HS and MS libraries, for what P-V-T conditions are dotlibs available? Report this in a table like the following:

dotlib file name	P	V (volts)	T (^oC)

You will likely need to use a series of pipelined grep commands with and without the "-v" option.

(E) Physical Design

Extract data from the LEF files, including techlef, to fill out the following table:

	RAK	NangateOpenCellLibrary	Nangate_15nm
Cell height			
No. of metal layers			
Routing pitch			
Cell height in routing tracks			