

Experiment #6 Analog to Digital Convertor

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1. Clarify objective

In this lab we will:

- Construct an analog to digital convertor using various logic devices such as the NAND gates, Schmitt Triggers, NOT gates, transistors, etc.
- Construct the ADC which will take in an analog input and convert it to a digital (binary) output
- Explore how to digitize clock pulses using trigger and stop pulses and counting the number of clock pulses with a counter
- Construct and demonstrate the workings of the following components:

- - Trigger Pulse Generator (TPG)
- - Clock Pulse Generator (CPG)
- - Counter
- - Analog to Time Convertor (ATC)
- - Control Logic (CL)
- Improve our circuit construction skills by incorporating each component of this lab in an organized manner

2. Background

Most signals in nature (voices, power levels, etc.) are analog in nature. It is very important to read/load data from these signals however we need to convert these to digital first. This can be achieved using an Analog-to-Digital Convertor. In this lab we will construct this convertor using the various logic devices (NAND gates, NOT gates, transistors, etc.) and the Analog Discovery 2 device.

In this lab, we will construct this convertor utilizing the Analog-to-Time convertor method which works as follows:

- On receipt of an appropriate trigger pulse, a second stop pulse is generated at time t , where t represents the span of time lapsed between the trigger pulse and the second stop pulse. This t is proportional to the voltage being digitized.
- By gating a free running clock pulse train with this trigger pulse (whose time period is equal to t) and counting the number of clock pulses this ADC is obtained.

In this lab we will build five components and independently test their operation to ensure that it produces the desired output. As a final step, all these five components will be integrated together to form the convertor.

These are the five components we will be implementing in this lab:

- Trigger Pulse Generator (TPG)
- Clock Pulse Generator (CPG)
- Counter
- Analog to Time Convertor (ATC)
- Control Logic (CL)

Below is the circuit diagram of the final integrated circuit with all the five components incorporated together to achieve the convertor:

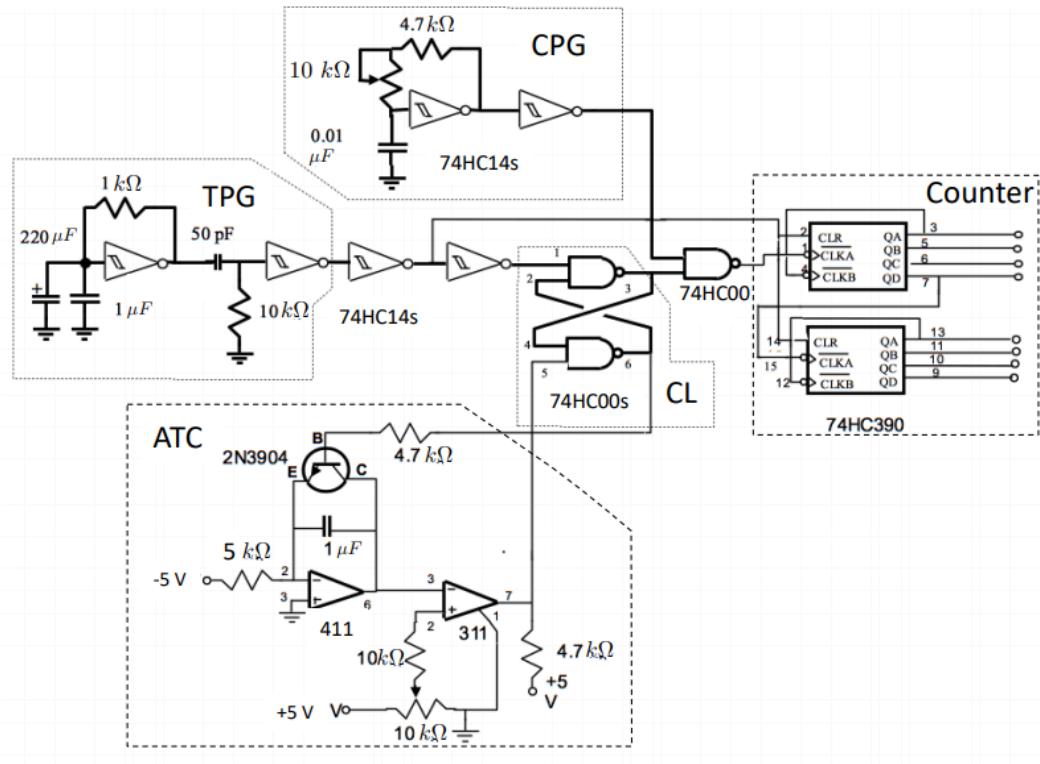


Figure 1 : The final circuit integrating all the five different components to achieve the ADC (from Dr. Jones' Experiment 6a description)

2.1 Trigger Pulse Generator (TPG)

The first step is understanding a schmitt trigger and how it incorporated hysteresis. In a schmitt trigger hysteresis is implemented by applying positive feedback to the non-inverting input of the differential amplifier. This circuit is named trigger because the output retains its value until the input changed sufficiently for it to change states. The circuit diagram of the two different circuits we will use to study these triggers are as follows:

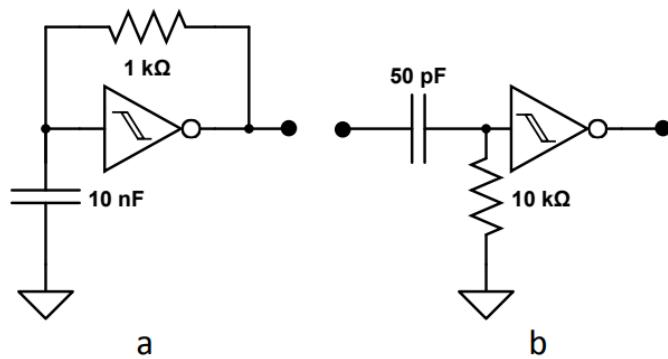


Figure2 : a) Square wave oscillator b) Short pulse rectifier. The output of the square wave oscillator is connected to the short pulse rectifier in order to complete the Trigger Pulse Generator (from Dr. Jones' Experiment 6a description)

As we can see in the image above, there are two components which integrate together to produce the TPG. A square wave oscillator is achieved using a single RC integrating circuit between the output and input of the

inverting Schmitt Trigger. This will produce a square wave whose frequency value will depend on the value of R and C used since these two values determine the time constant. As shown in the image below, the output automatically oscillates from V_{SS} to V_{DD} as the capacitor charges from one Schmitt trigger threshold to the other.

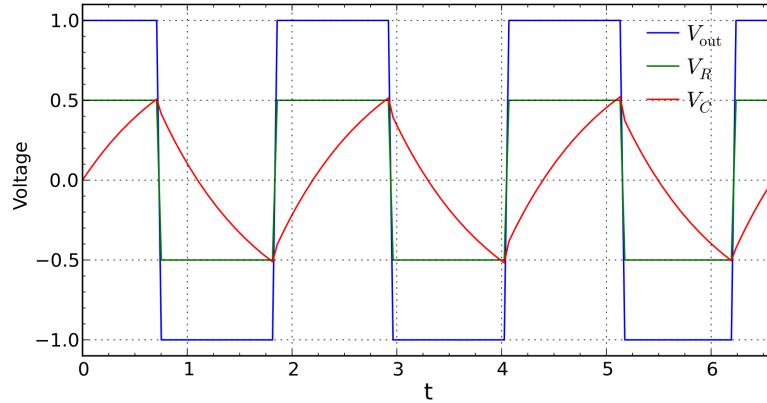


Figure 3 : Output and capacitor waveforms of the comparator-based square wave oscillator (Source: Wikipedia)

Second of the two components to make a TPG is the short-pulse rectifier as shown in Figure 2b. A rectifier is an electronic device which takes in an alternating current, which reverses direction, and transforms it to a direct current. The reversing operation is performed by an inverter (the Schmitt Trigger in our case). The short pulse rectifier is connected in series with the square wave oscillator where the square wave input contributes to the periodicity of the rectifier. This rectifier transforms the square wave into a series of pulses with the same frequency.

2.2 Clock Pulse Generator (CPG)

A clock pulse generator produces clock pulse signals which are used in synchronizing a circuit's oscillation. It produces pulses with frequency which is tunable by the potentiometer in the circuit. The frequency ranges from 6kHz to 19kHz and unless changed by tuning the potentiometer, should remain the same. The oscillations are produced by the capacitor in the circuit which essentially feeds these oscillations into the trigger as an input which are then produced as pulses as an output. The circuit diagram of the CPG component of the ADC is as follows:

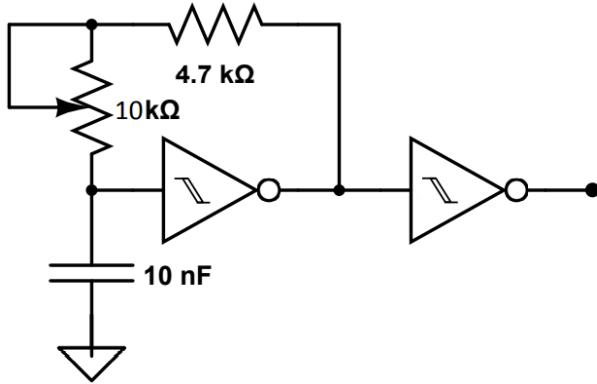


Figure4 : Circuit diagram of the CPG (from Dr. Jones' Experiment 6a description)

2.3 Counter

In order to be able to quantify our results, we need a counting device and that's where the counter comes in. To construct this counter, we need to connect two decade counters with each other as shown in the figure below. This component of the circuit will essentially have a negative pulse train feeding into the clock input. These incrementing values can be visually inspected when the 7-segment LED display is connected to the counter. These values will be shown in the base 10 fashion (counting from 0 to 99). This counter has the reset/clear functionality as well which will be utilized in clearing the output at later points in the lab.

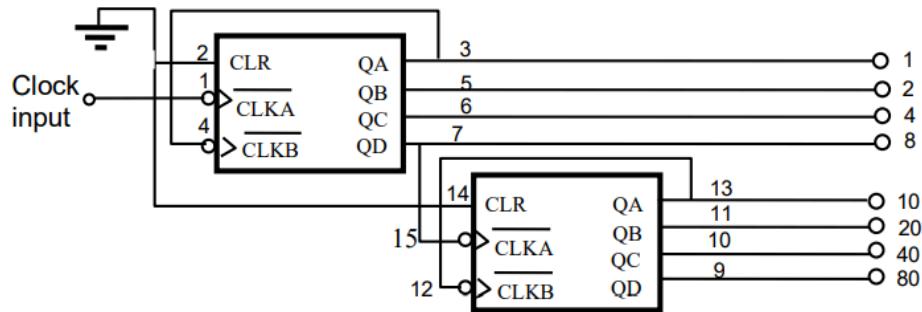


Figure5 : The $\div 100$ counter created using two decade counters (Source: Dr. Jones' Experiment 6a description)

2.4 Analog to Time Convertor (ATC)

The Analog to Time Convertor (ATC) has two components, namely: an Integrator and a Comparator. The output of the integrator is a ramp generator signal (showing the linear relationship between voltage and time) whereas the output of the comparator is a "stop" signal to represent when the voltage ramp exceeds the input voltage. The comparator essentially performs this by comparing the DC signal (whose value is to be determined) and the ramp generator voltage signal.

In addition to comparing the ramp to the input voltage and "stopping it", the comparator also resets the control flip-flop, hence cutting off the clock pulses from the decade counter. The circuit diagram of this component of the lab is shown below:

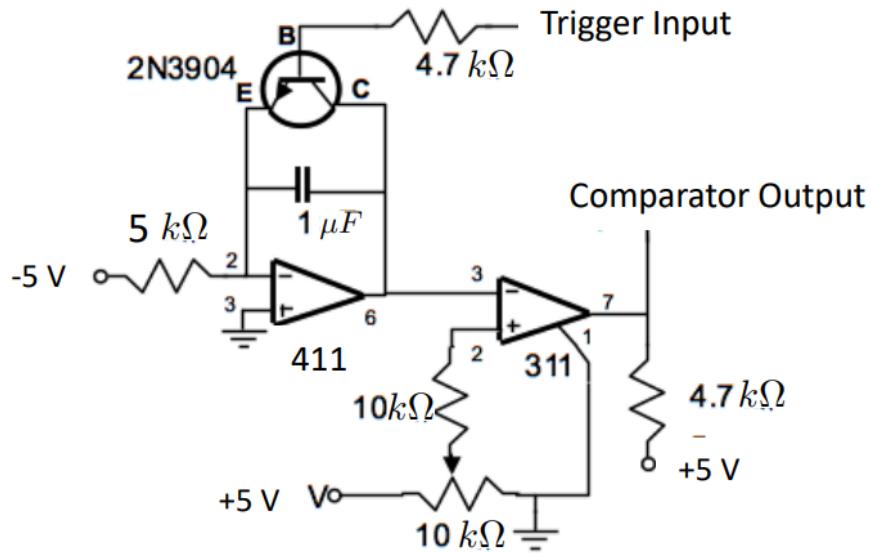


Figure6 : Analog to Time Convertor with the Integrator and the Comparator integrated together (Source: Dr. Jones' Experiment 6a ATC)

2.5 Control Logic

Now that we have set up all our components, we need a way for them to communicate with each other. This is enabled by a flip flop device. The flip flop that we'll construct in this lab will be made from NAND gates. In order to better understand its operation, let's look at the circuit diagram of a flip flop. The corresponding truth table for the flip flop will be explained in detail in section 3.5. Here is the circuit diagram:

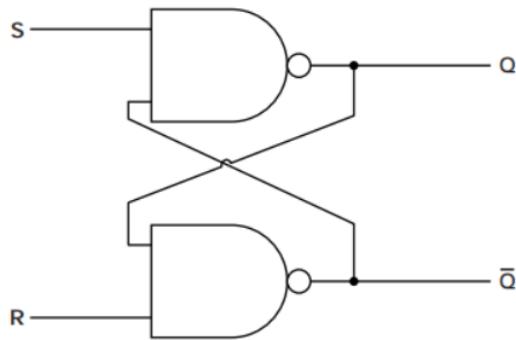


Figure7 : Circuit diagram of a flip flop constructed from two NAND gates (Source: Electronics StackExchange)

As we can see in the figure above, there are "SET" (output HI) and "RESET" (output LO) pins namely S and R labelled in the diagram above. There is also a third input for the circuit and that is the previous restored state of the device before "RESET" was pressed. Details of this will be included in section 3.5.

3. Components

3.1 Trigger Pulse Generator (TPG)

3.1.1 Measuring Hysteresis of the Schmitt Trigger

Before we build the components mentioned in section 2.1, we need to understand how a Schmitt Trigger works and how it utilizes hysteresis to provide noise immunity. To perform the above measurements, the circuit construction is as follows.

The circuit construction of the above component is as follows:

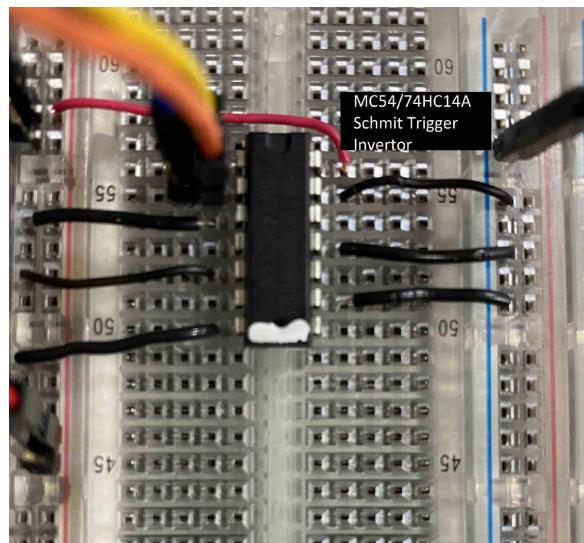


Figure8 : Construction of the square wave oscillator where the components are labelled in the circuit and all the black wires represent the ground connections

Note: As shown in the above circuit, it is very important to ground the unused inputs otherwise they will be in an unstable state and through cross talk can influence other inverter inputs. Using the triangle wave input, to calculate the hysteresis:

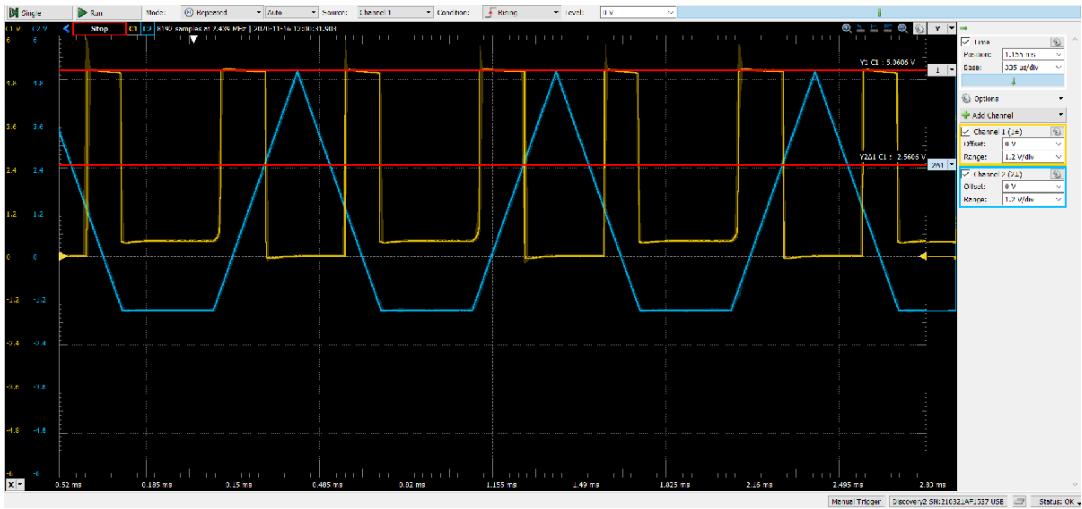


Figure 9 : Showing the input and output of the scope when triangle wave was used to measure the hysteresis of the schmitt trigger. The yellow graph represents the input signal (clipped) and the blue graph represents the square wave output.

Hysteresis measurements:

Following measurements were taken using the y-cursors and the quick measurements tool in scope of the waveforms software. It was assumed that the uncertainty of the scope was negligible hence only the observational uncertainties contributed to the uncertainties in this case. Note that there are two threshold values namely the LoToHi and HiToLo. These two threshold values contribute to the excellent noise immunity that Schmitt triggers provide. How they do that is explained below. Measurements are;

Final **LoToHi** value with uncertainties is: 1.64 ± 0.03 V

Final **HiToLo** value with uncertainties is: 3.03 ± 0.03 V

These measurements were taken when triangle wave with 1kHz frequency used as the input.

How does Schmitt Triggers deploy the use of hysteresis to provide noise immunity?

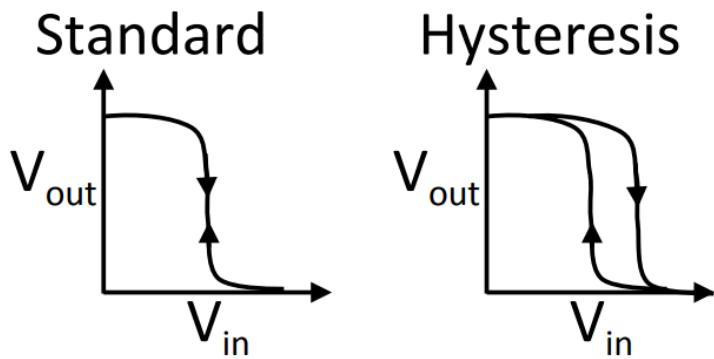


Figure 10 : This image shows the difference between a standard signal and the hysteresis property of the invertors (from Dr. Jones' Experiment 6a description)

Schmitt triggers utilize hysteresis by making use of positive feedback. Due to this property of hysteresis, schmitt triggers have two threshold values. A noisy input can cause the output to switch back and forth from noise. This noise signal when used as an input for the Schmitt trigger can cause only one switch in the output, after which it would have to move beyond the other threshold in order to cause change in the other switch. This is how Schmitt Triggers provide noise immunity.

3.1.2 Square Wave Oscillator

After measuring the hysteresis of the trigger, we will now construct the following circuit to perform as the square wave oscillator.

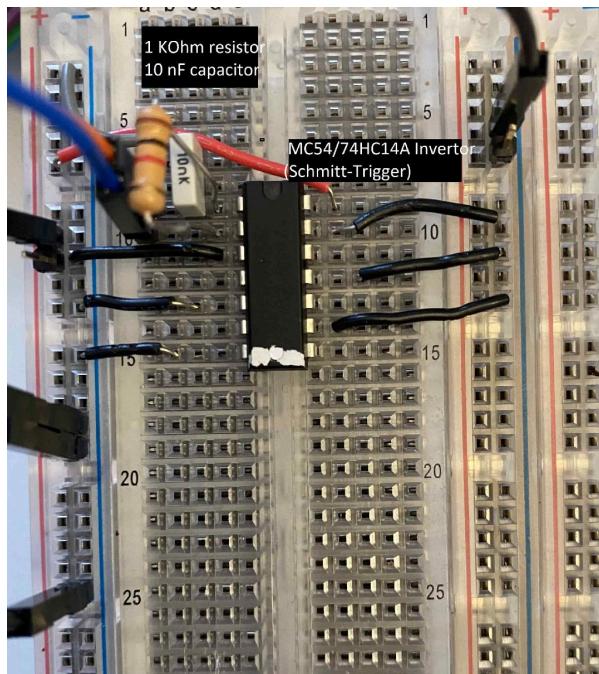


Figure 11 : A square wave oscillator using an RC integrating circuit with a schmitt trigger

Explanation:

To achieve a square wave oscillator we connect an integrating RC circuit between the input and output points of an inverting Schmitt Trigger. The output of this circuit will be a square wave whose oscillation frequency will be dependent on the R and C values. It works as follows:

At time 0, the voltage of the capacitor (V_C) is 0. This means that the input voltage of the Schmitt Trigger is 0 which means that the V_{output} of the trigger goes to HI (4.76V) and it starts charging the capacitor through the resistor. After sometime when V_C crosses the HI threshold voltage of the trigger, V_{output} goes to LO and this in turn initiates the discharge of the capacitor through the resistor. This step continues until V_C crosses the LO threshold and V_{output} goes to HI again. This step continues producing the square wave form of the oscillator.

In the image below, we can see the input discharging and charging waveforms of the RC (yellow) circuit in comparison to the output square wave oscillations (blue).

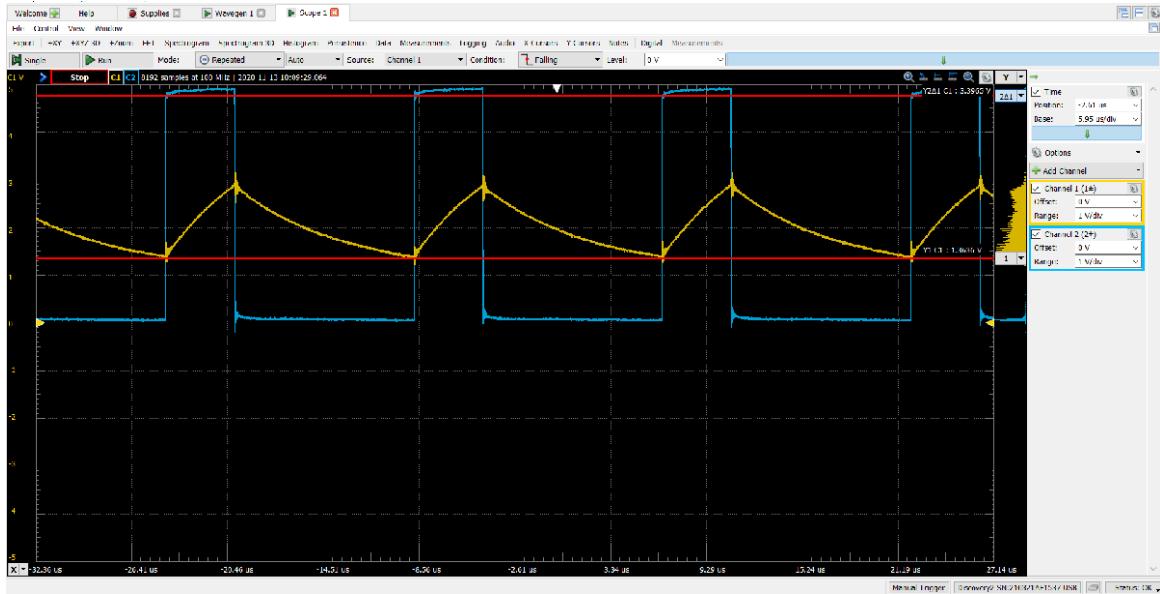


Figure 12 : This image shows the square wave output of the above circuit using an integrating RC circuit with an inverting Schmitt Trigger

The voltage measurements of the above circuit are as follows. The voltage values were taken in order to get a better sense of the circuit and how it works. One could also compare the values to the previous hysteresis values found in section 3.1.1. Same method of measurement was deployed as in section 3.1.1.

Final value of the **IoToHi threshold** is: 1.843 ± 0.03 V

Similarly we can have:

Final **hiToLo** threshold value comes out to be: 3.358 ± 0.02 V

Note: Schmitt triggers are asymmetric devices hence the IoToHi and the hiToLo delays are not symmetric.

3.1.3 Short-pulse Rectifier

3.1.3.1 Short-pulse rectifier with the larger frequency

To perform the measurements of the analog input repetitively, we need the above circuit to produce short pulses instead of square waves. This can be achieved using the circuit in Figure 2b.

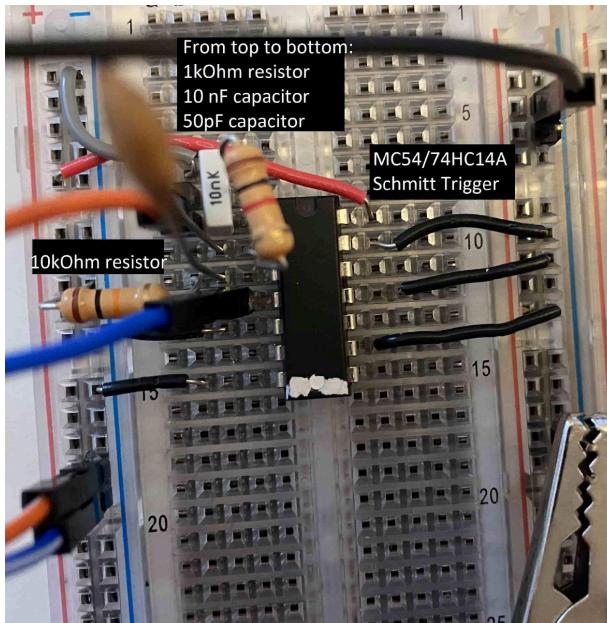


Figure 13 : Circuit construction of the short pulse rectifier incorporated into the square wave oscillator. The output of the square wave oscillator is the input of the short pulse rectifier

In order to get a better sense of the circuit and some of the components, some of the calculations are as follows:

$$R = 998.2 \pm 0.3 \Omega$$

$$C = 10 \text{ nF}$$

```
resistor = 998.2; %Ohms
resistor_uncert = 0.3 %Digital uncertainty in Ohms
```

$$\text{resistor_uncert} = 0.3000$$

```
capacitor = 10*10^(-9); %Farads
capacitor_uncert = (0.2*capacitor); % 20% of the manufacturer's uncertainty also measured in Farads
```

```
time_constant = resistor * capacitor; %seconds
oscillation_freq = 1/time_constant; %Hertz
```

The oscillation frequency of the above circuit is: 100kHz

The uncertainty calculations for the above frequency value are as follows:

$$f = \frac{1}{\tau} = \frac{1}{RC}, \text{ from this relationship we have: } \sigma_f = \sqrt{\left(\frac{-1}{R^2 C}\right)^2 (\sigma R)^2 + \left(\frac{1}{RC^2}\right)^2 (\sigma C)^2} = 30 \text{ kHz}$$

Explain the operation of the short pulse rectifier:

A rectifier is an electronic device which takes in an alternating current, which reverses direction, and transforms it to a direct current. The reversing operation is performed by an inverter (the Schmitt Trigger in our case).

The short pulse rectifier is connected in series with the square wave oscillator where the square wave input contributes to the periodicity of the rectifier. This rectifier transforms the square wave into a series of pulses with the same frequency. For this lab, we will be performing a full-wave rectification where the phase, which mathematically, represents the absolute value of a function.

To explain this process further, following are the exports from the scope to show how the rectification is done:

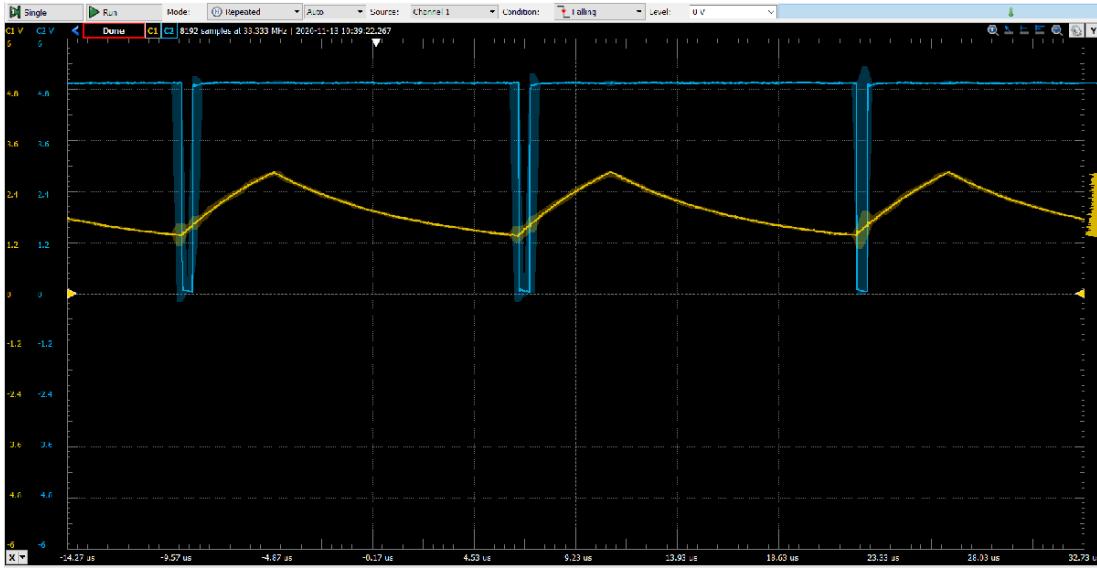


Figure 14 : This image shows the operation of the short pulse rectifier where the yellow represents the analog input signal from the RC circuit and the blue represents the corresponding DC output produced in short pulses.

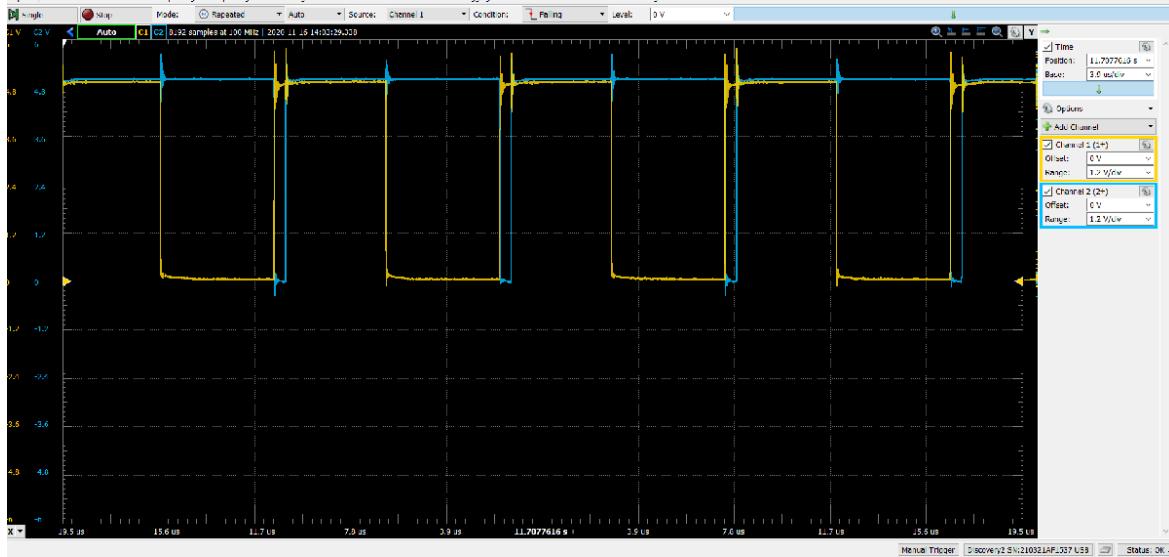


Figure 15 : The image above shows the comparison between the square wave output from the inverter (yellow) and the short pulse rectifier output (in blue)

The voltage measurements of the above circuit are as follows. A different method was used to measure the values and calculate uncertainties for the measurements. Upon consultation with peers and the TAs, it was established that two values can be measured for a single threshold: one maximum possible value and one minimum possible value. Then one could calculate the threshold values and uncertainty as follows:

```

hiToLoMax_2 = 3.376; %Volts
hiToLoMin_2 = 3.326; %Volts
hiToLo_2 = (hiToLoMax_2 + hiToLoMin_2) /2; %Volts
hiToLoUncert_2 = (hiToLoMax_2 - hiToLoMin_2)/2; %Volts

```

Hence final value for the **hiToLo** threshold is: $3.35 \pm 0.03 V$

Similarly, we can perform the same computation for the loToHi threshold for this circuit:

```

loToHiMax_2 = 3.318; %Volts
loToHiMin_2 = 3.258; %Volts
loToHi_2 = (loToHiMax_2 + loToHiMin_2)/2; %Volts
loToHiUncert_2 = (loToHiMax_2 - loToHiMin_2)/2; %Volts

```

Hence, the final **loToHi** threshold value fort this circuit is: $3.288 \pm 0.03 V$

From Figure 14, it can be noticed that the short pulse rectifier produces a DC signal representing HI for the entirety of the of the analog input signal however it changes to LO briefly when the capacitor discharges fully. This is because the voltage across the capacitor maintains a status quo and doesn't change immediately with any fluctuations in the circuit. To maintain this status quo, the two plates of the capacitor have to compliment each other's voltages. Therefore, when the input voltage changes from LO to HI the output changes to HI instantly as well so that the overall voltage across the capacitor is maintained at LO. This is why for the entire wave of the RC signal, the short pulse rectifier is at HI. The same reasoning can be applied to when the voltage of the input changes from HI to LO and we can see that for that brief period the short pulse rectifier is at LO.

3.1.3.2 Changing the oscillation frequency of the RC circuit and verifying the corresponding operation of the short pulse recitifier:

To change the oscillation frequency of the RC signal, we replace the $10nF$ capacitor with $220\mu F$ and $1.0\mu F$ capacitors. Since the frequency of the circuit is dependent on the time constant of the circuit which in turns depends on the R and C values. Hence using capacitors with larger values will extend the time constant and decrease the oscilalton frequency. The new circuit with the changes is as follows:

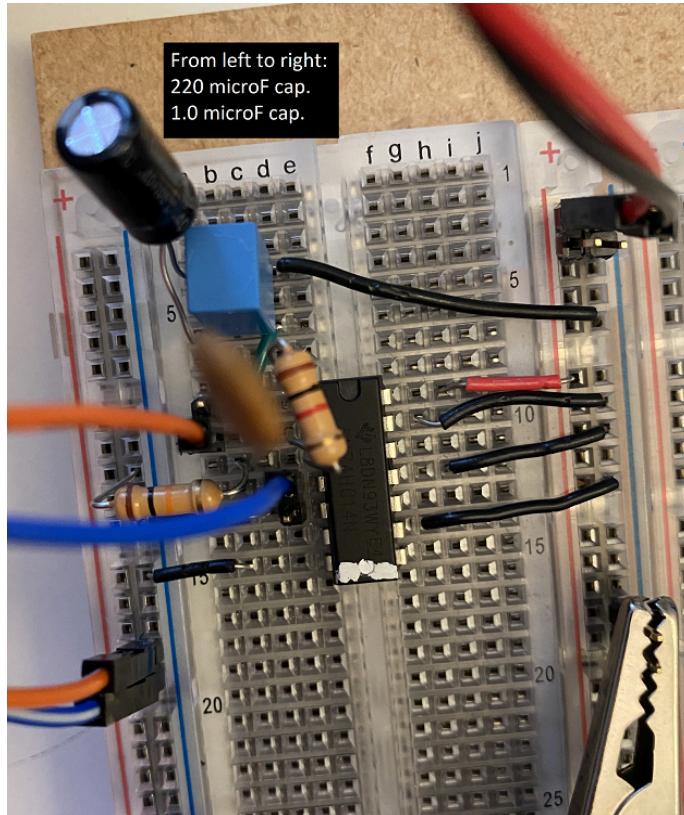


Figure 16 : Updated circuit with the 220microF and the 1.0microF capacitors in parallel with each other replacing the previous 10nF capacitor

Frequency measurements of the updated circuit:

```
cap_1 = 220 *10^(-6) %Farads
```

```
cap_1 = 2.2000e-04
```

```
cap_2 = 1*10^(-6) %Farads
```

```
cap_2 = 1.0000e-06
```

```
cap_eq = cap_1 + cap_2; % equivalent capacitance of two capacitors in parallel (measured in Farads)
timeC = resistor * cap_eq; % seconds
newOscillationFreq = 1/timeC; %Hertz
ratio = newOscillationFreq/ oscillation_freq;
```

The uncertainty calculations for the above frequency value are as follows:

$$f = \frac{1}{\tau} = \frac{1}{RC}, \text{ from this relationship we have: } \sigma f = \sqrt{\left(\frac{-1}{R^2 C}\right)^2 (\sigma R)^2 + \left(\frac{1}{RC^2}\right)^2 (\sigma C)^2} = 0.9066 \text{ kHz}$$

$$f = 4.53 \pm 0.91 \text{ Hz}$$

From the above calculations, we see that the new oscillation frequency is 4.53Hz which is $4.53 * 10^{-5}$ times smaller than the oscillation frequency measured in section 3.1.3.1. Our results and calculations prove that the

oscillation frequency has decreased drastically which is supported by the square wave graph as well. In the figure below, we see that the time scale is in seconds in comparison to the time scale in 3.1.3.1 where the time scale was in microseconds.

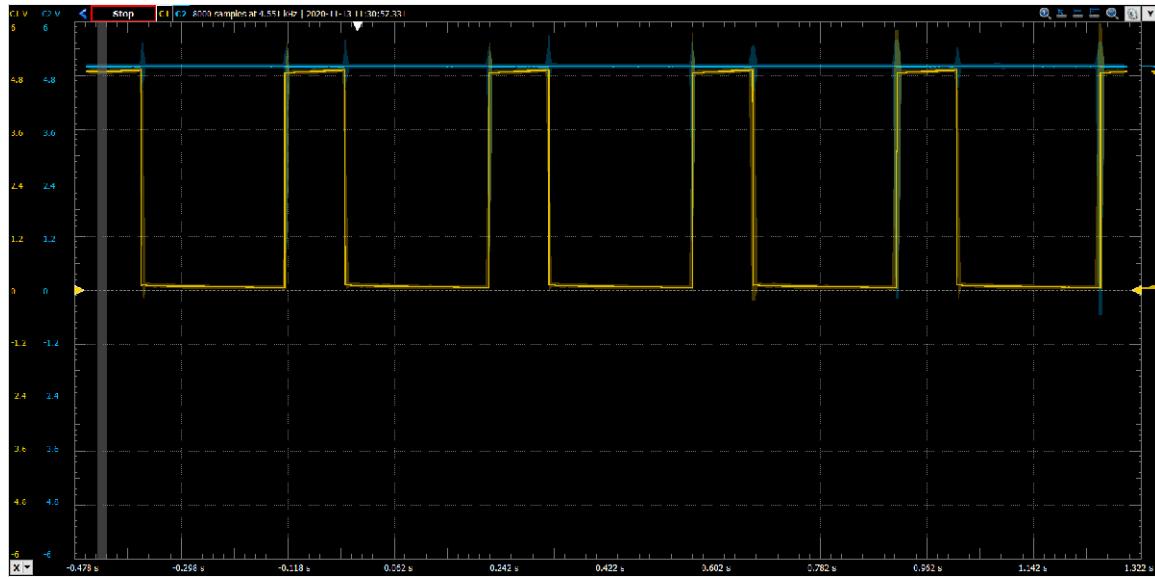


Figure 17 : The above image shows the updated short pulse rectifier with the decreased frequency. This is evident from the larger time period of the blue signal (short pulse rectifier output) vs. the yellow signal (square wave oscillator) which is the same as before.

3.2 Clock Pulse Generator (CPG)

The explanation of how this component of the ADC works, please refer to section 2.2. For convenience, I included the circuit diagram of CPG below alongside the circuit that I constructed:

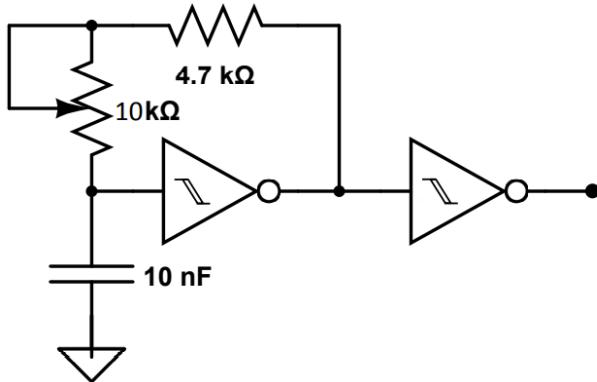


Figure 18: Circuit diagram of CPG

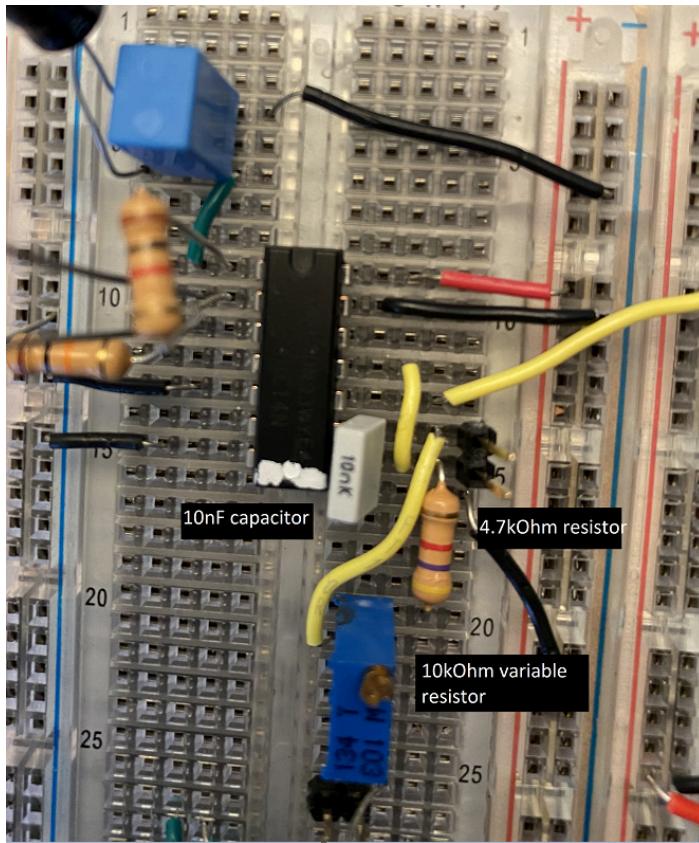


Figure 19 : The circuit construction of CPG

Note that the 10kOhm variable resistor in the circuit above is the potentiometer in the circuit which is used to tune the oscillation frequency of the circuit.

After the construction of the circuit, the operation of the circuit was verified. The circuit produced square waves with oscillation frequency ranging from 6kHz to 19kHz. The following exports from the oscilloscope verify this operation as well. To obtain the frequency of these oscillations, quick measurement tool in waveforms was used with the uncertainties only being the last fluctuating digit of the measurement.

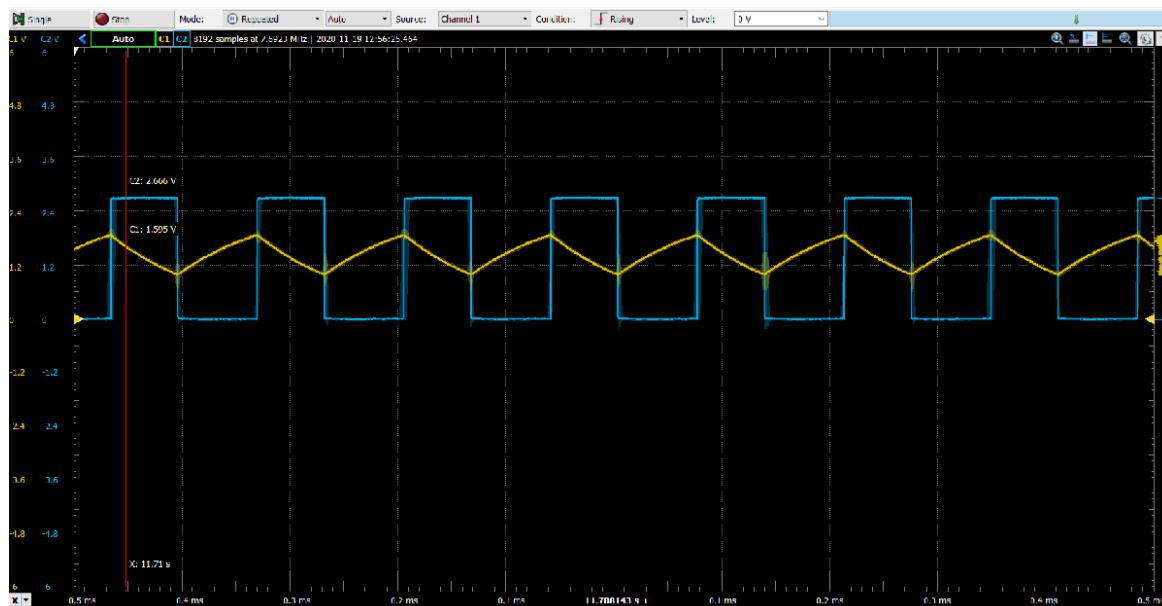


Figure20 : Export of the CPG with the oscillation frequency of 6kHz

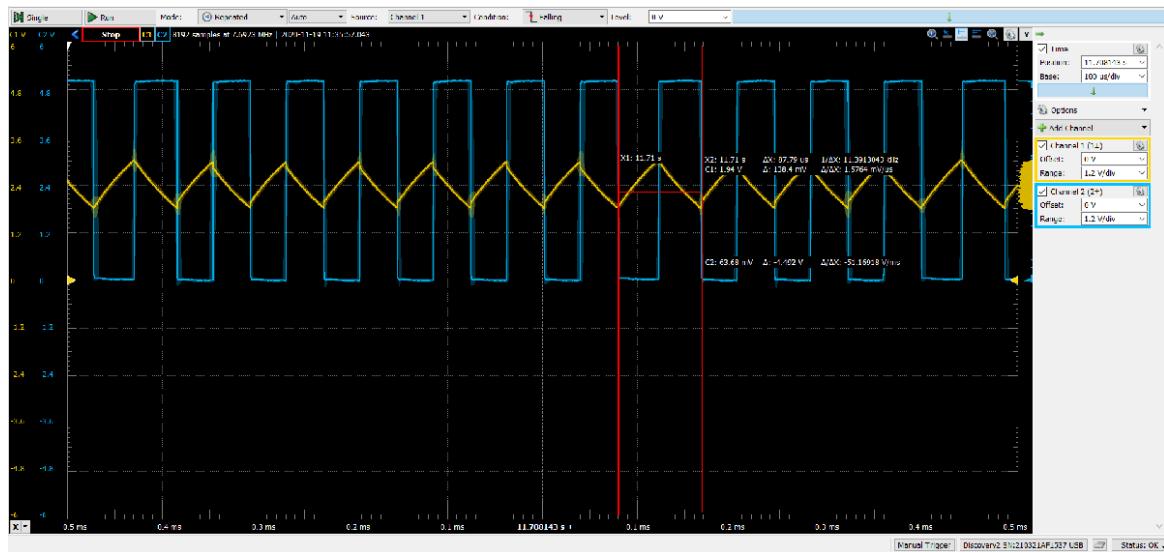


Figure21 : Export of the CPG with the oscillation frequency of 14kHz

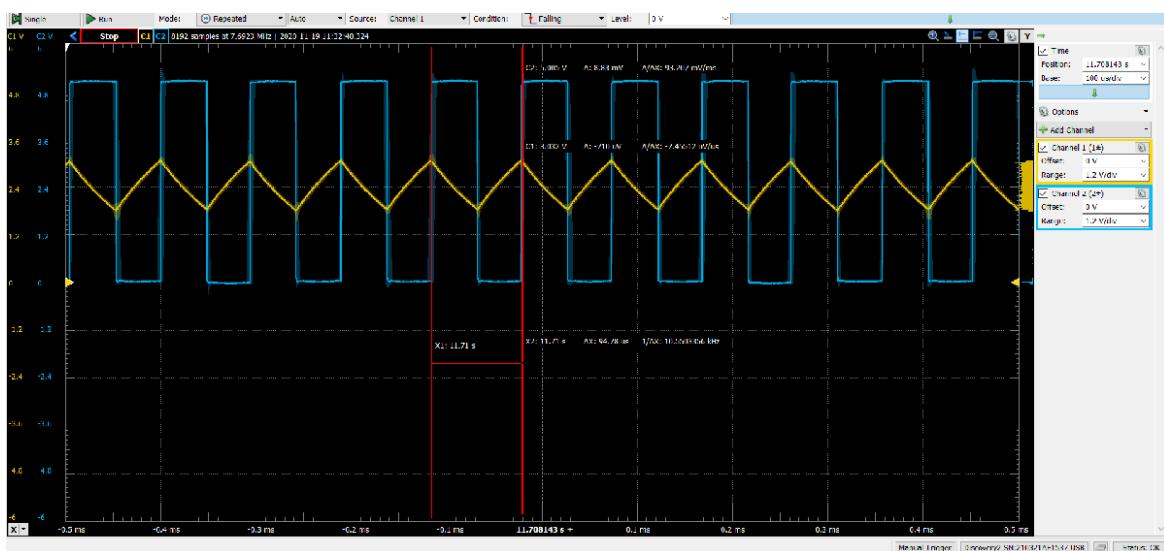


Figure22 : Export of the CPG with the oscillation frequency of 10kHz

CPG essentially works the same as the square wave oscillator in section 3.1 the only difference being the addition of the variable resistor (potentiometer) to tune the frequency of oscillation. This circuit also has an inverting effect on the output square waves produced.

3.3 Counter

The detailed explanation about the workings of this component are included in section 2.3 and here is the circuit diagram of the respective component:

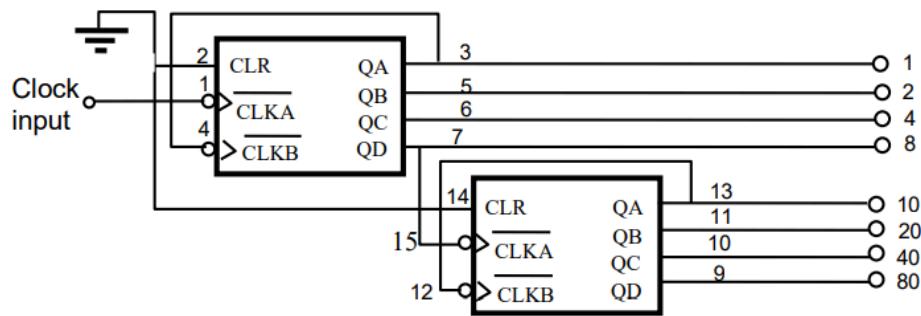


Figure23 : The $\div 100$ counter created using to decade counters (Source: Dr. Jones' Experiment 6a description)

I constructed the physical circuit following the guidelines from the circuit diagram above and here is the physical circuit of the counter:

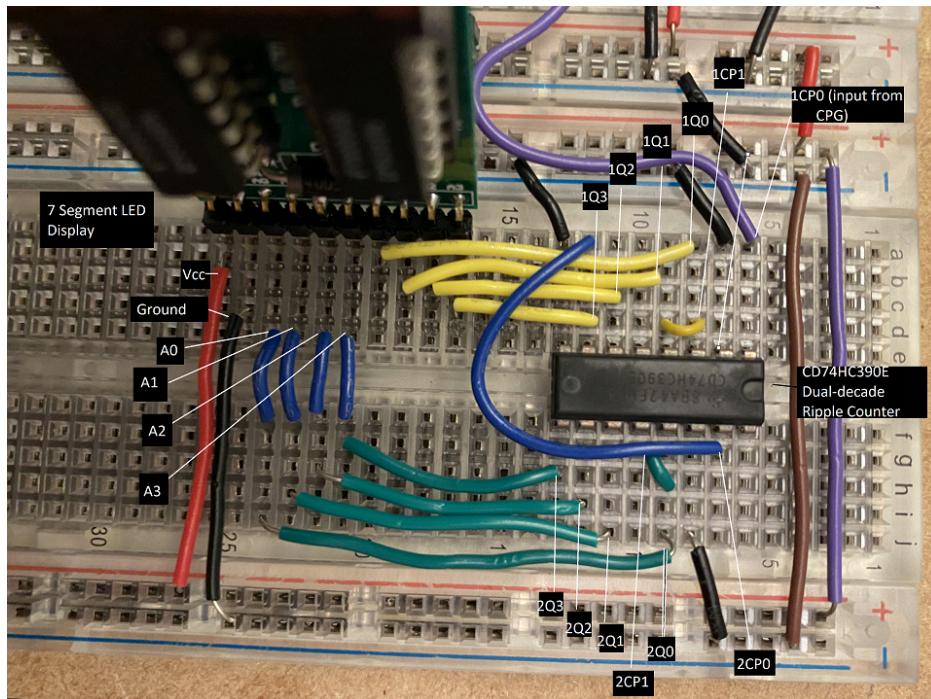


Figure24 : Circuit construction of the $\div 100$ counter. The voltage supply to the counter was disconnected at the time this image was taken hence, it is not labelled in the diagram

Another note: In the above figure, the circuit image is taken after the components were integrated together. In the chaos of doing this lab, I unfortunately, forgot to take a picture of the circuit when I used STATIC IO pins to provide the input clock pulse of frequency of 100Hz. However, the workings of this components can be seen in this [video](#) (which I did remember to take).

Connections in the above circuit are as follows:

Since each Q pin represents a storage unit of one bit, to display a tens digit on the 7segment LED display, we need to connect the components as follows so that the bits add up to the required digit we want to display.

- Rightmost A0 was connected to 1Q0, A1 to 1Q1 , A2 to 1Q2 and A3 to 1Q3. These connections represent the least significant digit on as displayed on the 7Segment LED display.
- 1Q3 is connected to 2CP0 so that the bits add up to show the digit in the seconds place on the 7 Segment LED display
- Leftmost A0 is connected to 2Q0, A1 to 2Q1, A2 to 2Q2 and finally A3 to 2Q3

3.4 Analog to Time Convertor (ATC)

An explanation of how this component works is provided in section 2.4 but a detailed description of both the comparator and the integrator follows:

3.4.1 Description of the Integrator Circuit

An Op-Amp integrating circuit produces an output voltage which is proportional to the area contained under the wave form. If the input voltage is a continuous square wave, this results in the charging and discharging of the capacitor (feedback loop). This results in a triangular wave output (ramp generator signal) whose frequency is dependent on the RC constants. The rate of change of output voltage is proportional to the value of the applied voltage signal. This can be achieved using a capacitor, resistor, negative feedback, and two golden rules of Op-Amps. To get a better understanding of how the golden rules are applied, let's look at the circuit diagram of an integrator:

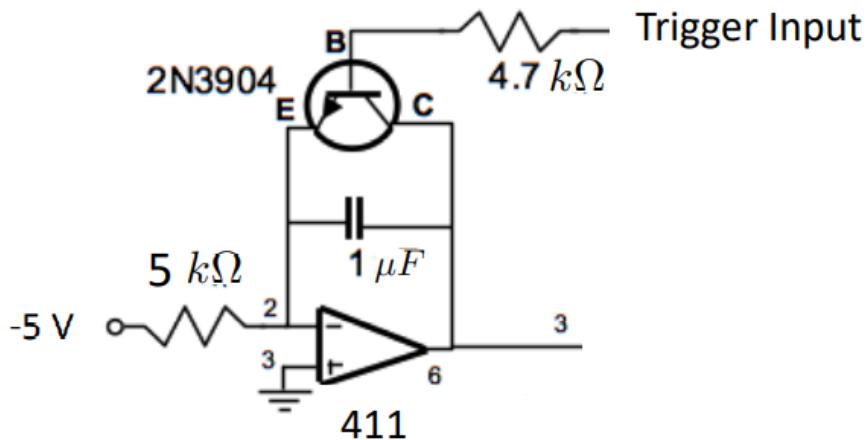


Figure25 : The integrator component of the ATC utilizing Op-Amp with resistor and capacitor to produce the desired outcome (Source: Dr. Jones' Experiment 6a)

In the above diagram, using the golden rules of Op-Amps, we know that voltage at node 2 = 0V. Detailed calculations and numerical proof of the circuit follows:

Note that for brevity, $5k\Omega$ and $1\mu F$ are written as R and C in the following equations.

$$V_2 = V_3 = 0 \text{ V}$$

Using KCL at node 2, we have the following result :

$$I_{\text{in}} = \frac{(V_{\text{in}} - V_2)}{R} = \frac{V_{\text{in}}}{R} A, \quad I_{\text{out}} = (C) \frac{d(V_2 - V_{\text{out}})}{dt} = (-C) \frac{d(V_{\text{out}})}{dt}$$

Equating the above two equations for I_{out} and I_{in} , we have the following result :

$$\begin{aligned} \frac{V_{\text{in}}}{R} &= (-C) \frac{d(V_{\text{out}})}{dt} \\ \int \frac{V_{\text{in}}}{R} dt &= (-C) \int d \frac{(V_{\text{out}})}{dt} dt \\ \int_0^t \frac{V_{\text{in}}}{R} dt &= (-C)V_{\text{out}} \\ V_{\text{out}} &= \frac{-1}{RC} \int_0^t V_{\text{in}} dt \quad \text{eq. (1)} \end{aligned}$$

From eq.(1), we can see the numerical integration that occurs in this circuit. The comparison between the input square wave pulses and the output ramp generator can be done based on the following images:

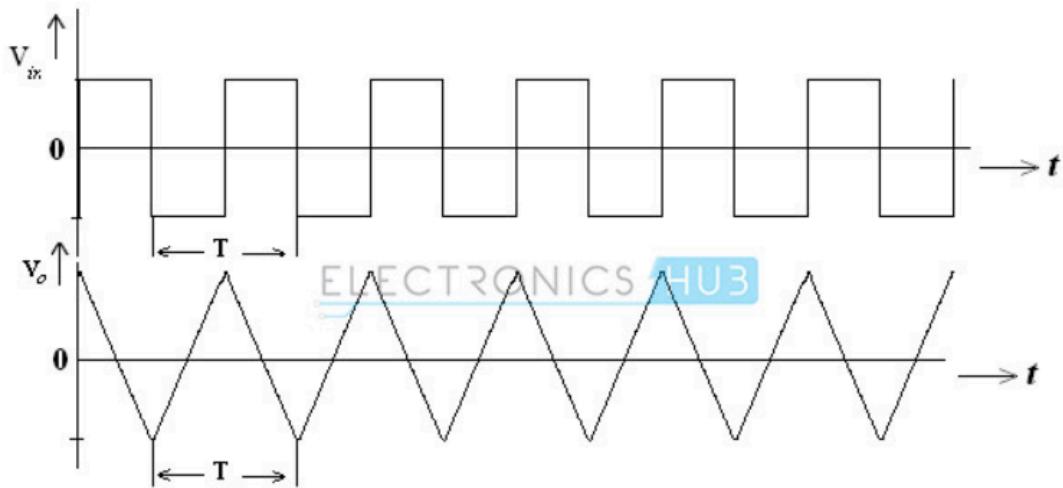


Figure 26 : Comparison between the input square wave pulses and the output ramp generator of an Integrator circuit (Source: [Electronic's Hub](#))

In the above figure Figure26, we can see that there is a transistor in parallel with the circuit. This transistor acts as an electronic switch and is controlled by the logic circuit. When the switch is open (LO), the integrator works as described above. However, when the switch closes (HI), the feedback capacitor is shorted and this results in a zero potential drop being produced at the output of the 411 OpAmp.

3.4.2 Description of the Comparator circuit

The comparator component of ATC uses a difference amplifier (311). This comparator is an electronic decision making circuit that makes use of an operational amplifiers very high gain in its open-loop state, meaning that there is no feedback resistor, as can be seen in the circuit diagram below. The comparator essentially generates HI or LO voltage signals depending on whether the input ramp voltage is less than or greater than

the DC voltage as tuned by the $10k\Omega$ variable resistor (potentiometer). When the input of the comparator (ramp signal) moves past the DC voltage threshold, a sudden change of state occurs for the output of the comparator and it switches from HI to LO state.

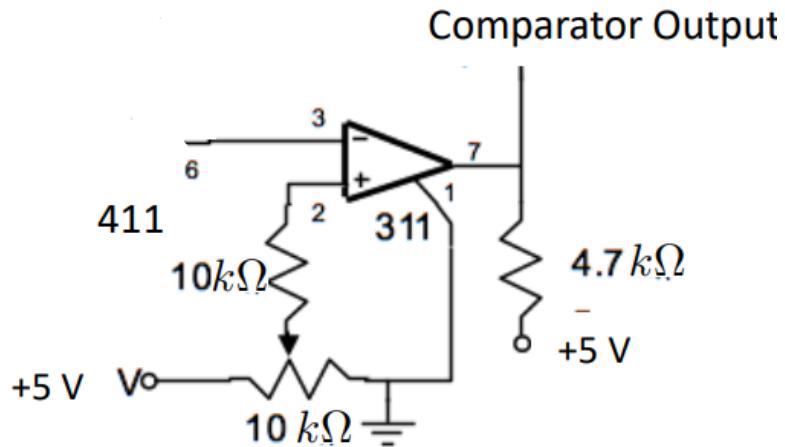


Figure27 : Circuit diagram of the comparator circuit of the ATC as described in the Experiment

6a description. Note that pin 6 is the input pin receiving the ramp generator signal as an input from the integrator. How these components interact can be seen in section 4.

3.4.3 Circuit construction of ATC

Using the circuit diagram in section 2.4 and the individual component diagrams in section 3.4.1 and 3.4.2, I constructed the following circuit.

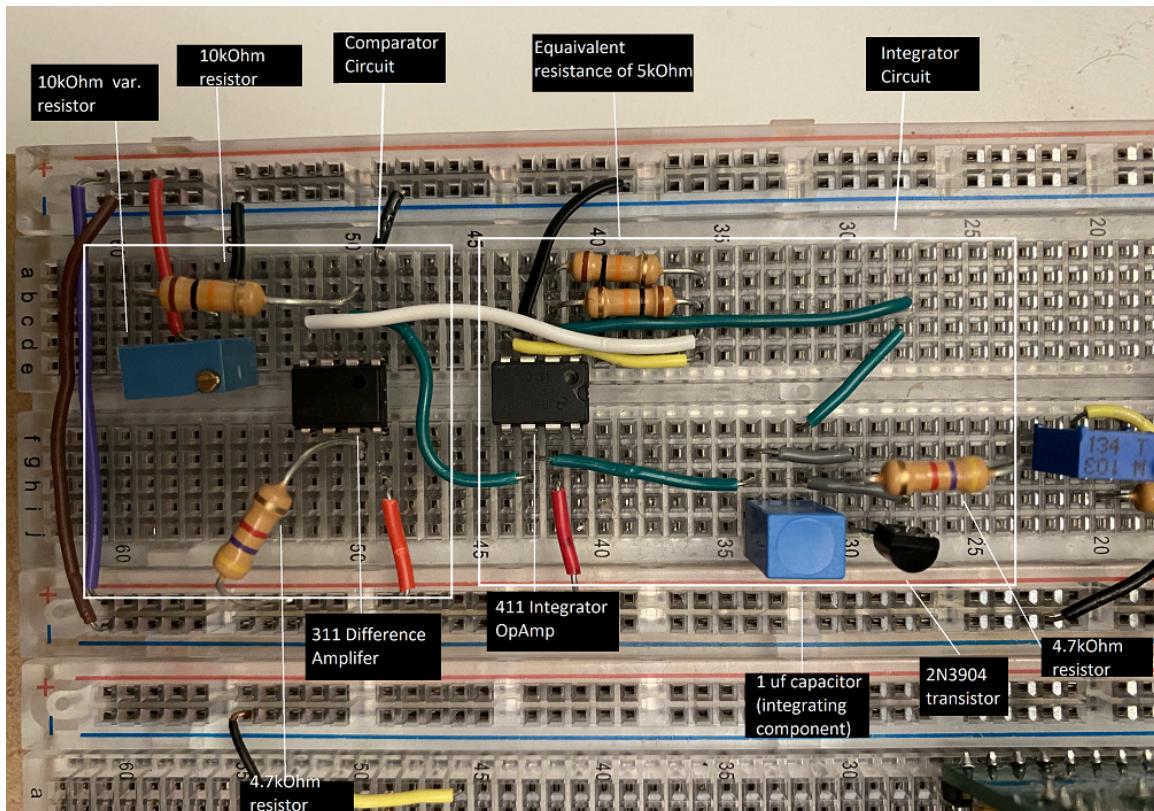


Figure28 : Circuit construction of the Integrator and Comparator components of ATC

To test the operation of the above circuit, I used the Analog discovery 2 scope and wavegen features. Wavegen was used to provide a square wave signal to the transistor switch in the integrator circuit using the pulse signal. The input and output voltage levels were measured and the following export from scope was taken.

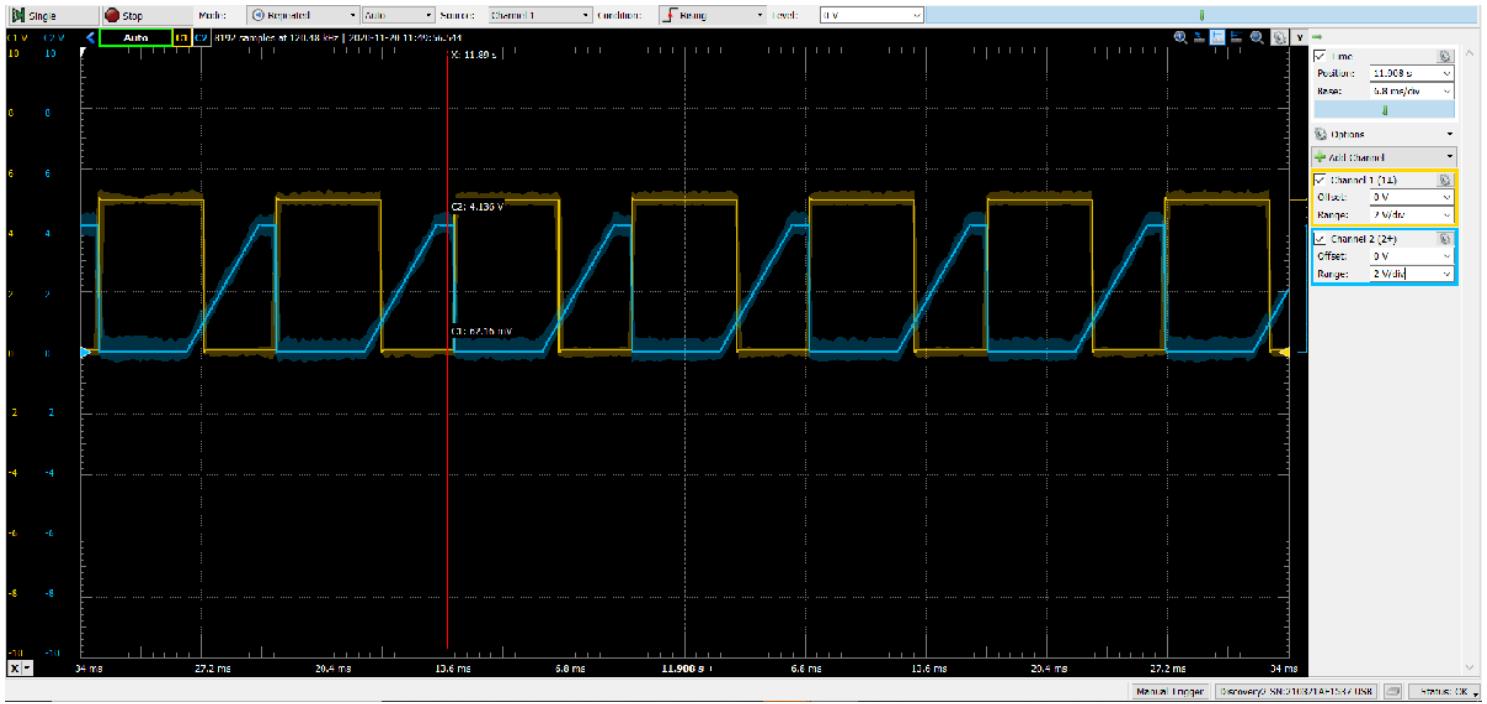


Figure29 : The graphs of integrator (blue) and comparator (yellow) outputs taken using the single shot feature in scope in Analog Discovery 2

As we can in the abve screen export, we can see that the circuit performs as desired by producing a ramp signal for the integrator and square wave signal for the comparator. It is interesting to note that the our prediction about the change of state of the comparator from HI to LO are true. We see that when the input ramp signal reaches the higher DC voltage threshold (as tuned by the variable potentiometer), the signal changes abruptly from HI to LO state. When the ramp is turned off by the trigger, the input voltage reaches the lower DC voltage threshold and the signal changes abruptly from LO to HI. In the figure above, we can also see that the voltage signal is also clipped. This is due to the fact that this open-loop of the OpAmp (explained in section 3.4.2) means infinte gain. However, since the voltage is limited by the supply voltage amplitude (input), this results in the clipping of the circuit.

3.5 Control Logic

3.5.1 Understanding the truth table and detailed explanation

Let's re-visit our circuit diagram for this component:

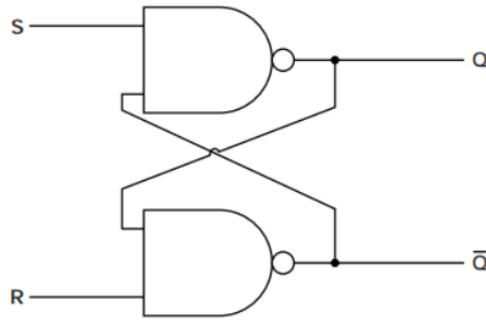


Figure30 : Circuit diagram of a flip flop constructed from two NAND gates (Source: [Electronics StackExchange](#))

In the above circuit diagram we see how there are three inputs for the component (also explained in section 2.5). These three input values determine the current state of the logic device. This device works by saving a single bit of data. The simplest way to make any basic single bit set-reset SR flip-flop is to connect together a pair of cross-coupled 2-input NAND gates as shown above. Following is the truth table for the device which will provide us with better understanding of how the devie behaves when certain input values are supplied:

S	R	Q	\bar{Q}
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1

Figure31 : Truth table of a flip flop device constructed using two NAND gates (Source: [Electronics StackExchange](#))

From the above table we can infer that when Q and \bar{Q} represent opposite values. When the "RESET" is set to HI and "SET" is set to LO, that is when the flip flop stores its current state and remembers it for the next variation of inputs until the same combination is repeated. Note that a state of LO for both "SET" and "RESET" is invalid since it violates our statement above that Q and \bar{Q} are inverse states of each other. In the above truth table we can see that when this invalid state is reached, both the outputs are set to HI which, as I mentioned before, is wrong.

3.5.2 Circuit construction and verifying the truth table

After understanding how the counter logic works, I constructed my circuit by following the guidelines in section 3.5.1 and section 2.5. The circuit construction was as follows:

Note: The following image was taken after all the components were integrated together. Hence, there are connection such as "output for the counter" and "from CPG". To conduct the preliminary analysis, I utilized the

STATIC IO to act as input and output pins. The screen exports from the STATIC IO will be included to validate this statement as well.

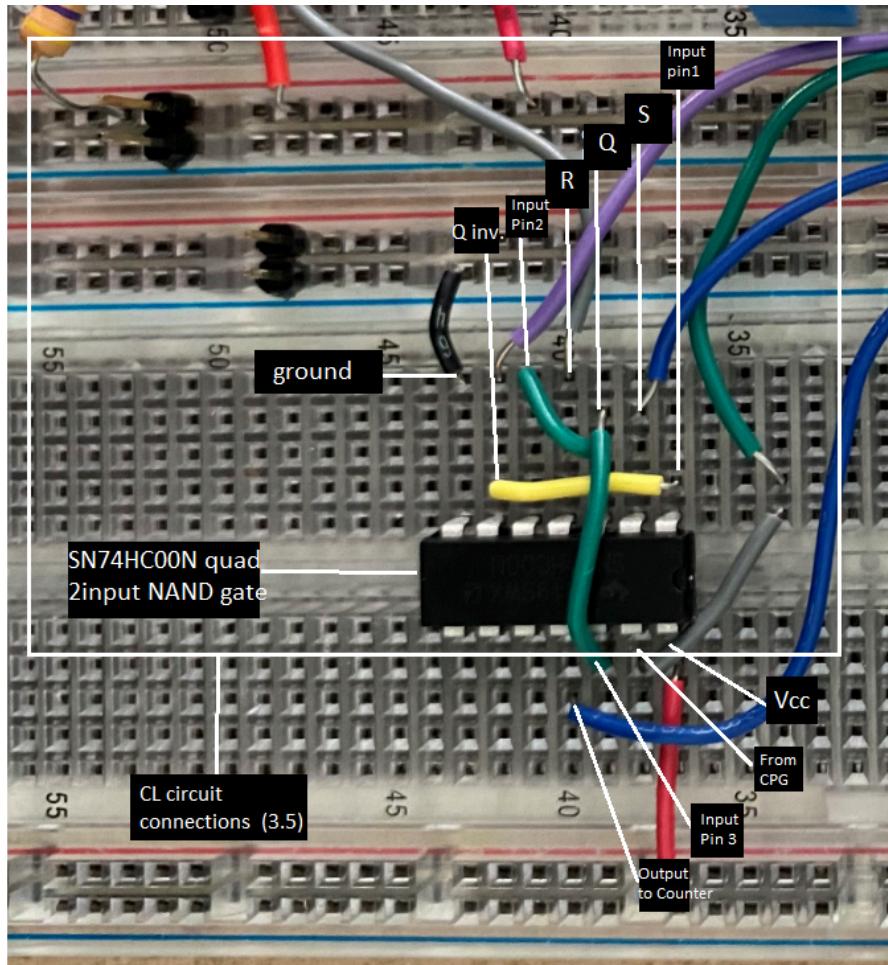


Figure32 : Circuit construction of a flipflop device using two NAND gates. Note that only the components in the "CL circuit connections (3.5)" are relevant for this section.

The other components come in when we integrate all the components together.

After constructing my circuit, I verified that the output of this circuit agreed with the truth table provided above. I have included the screen exports from STATIC IO to prove this claim. Description of how the output relates to the table will be included in the figure description. The pin configurations are as follows: S = Pin 1, R = Pin 3, Q = Pin 2 and \bar{Q} = Pin 5.

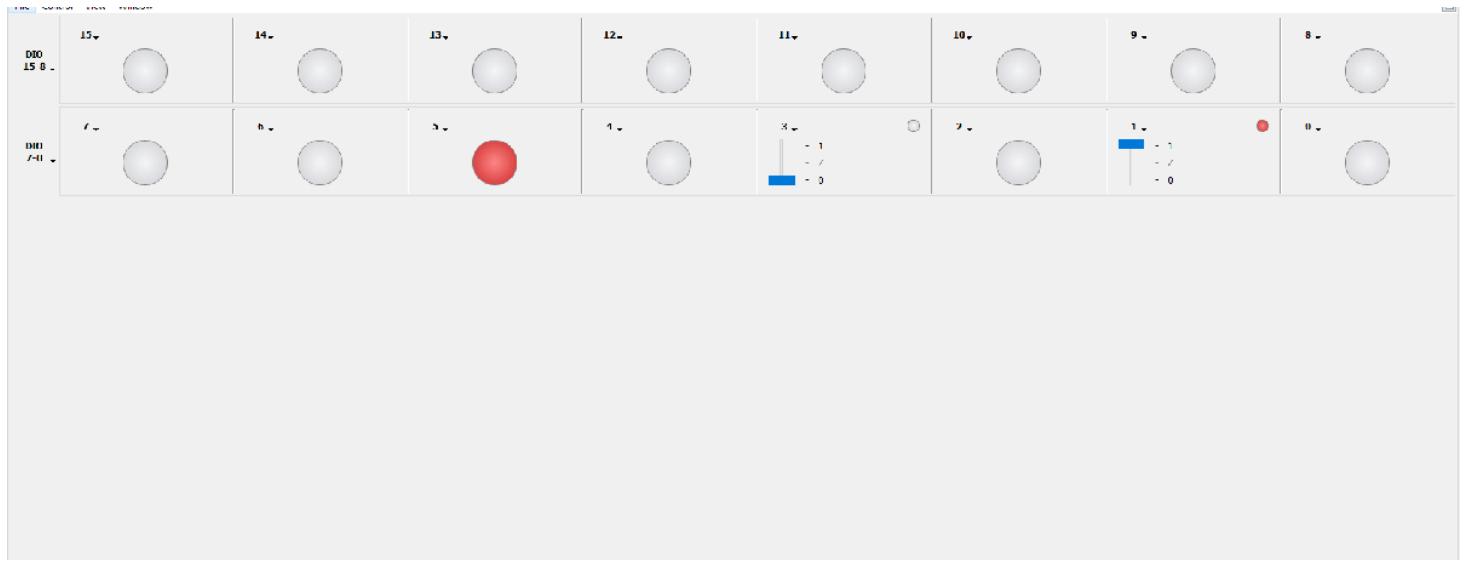


Figure33 : State 1 when $S = HI$, $R = LO$ so consequently $\bar{Q} = HI$ and, $Q = LO$.

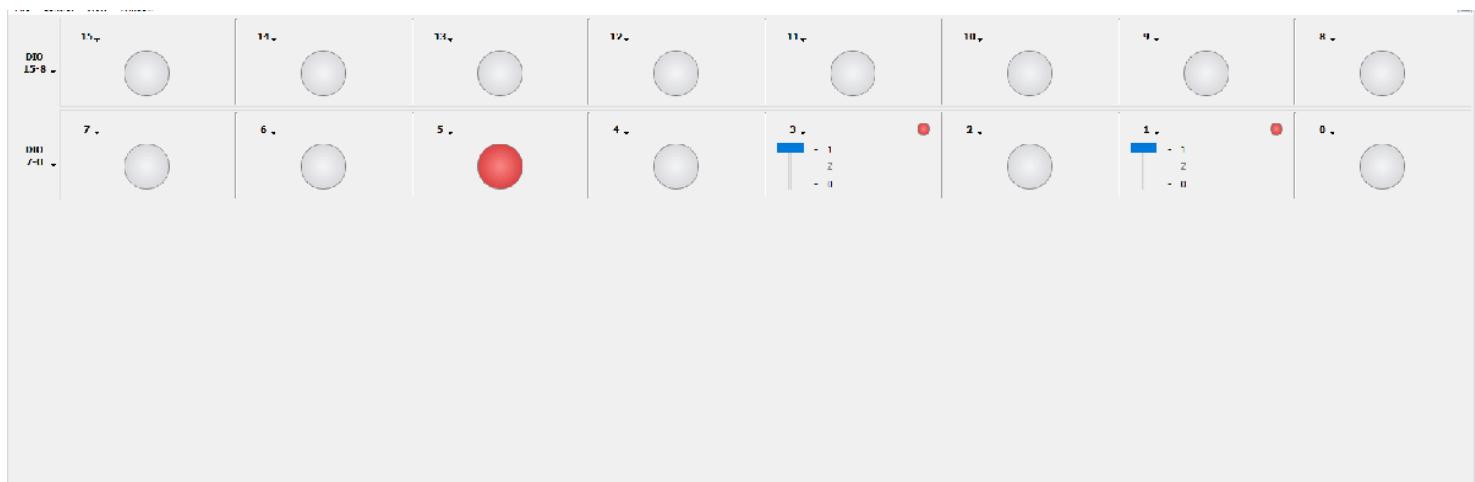


Figure34 : State 2 when $S = HI$, $R = HI$ so consequently $\bar{Q} = HI$ and, $Q = LO$

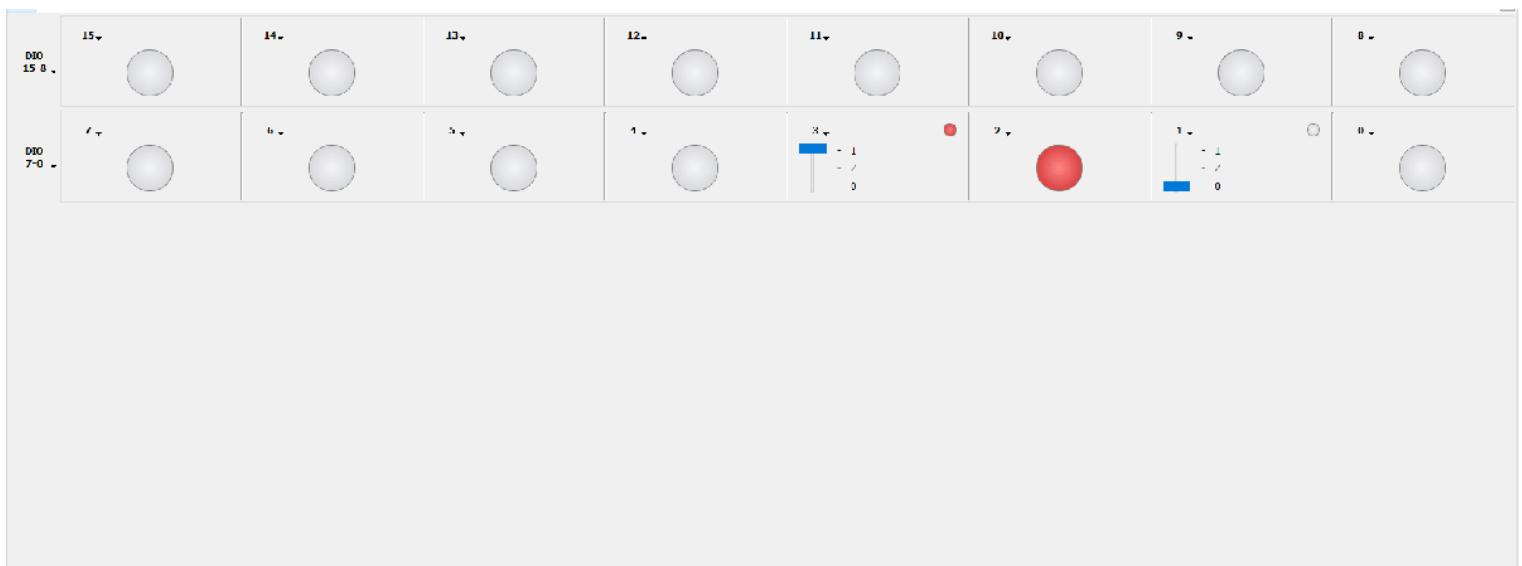


Figure35 : State 3 when $S = LO$, $R = HI$ so consequently $\bar{Q} = LO$ and, $Q = HI$

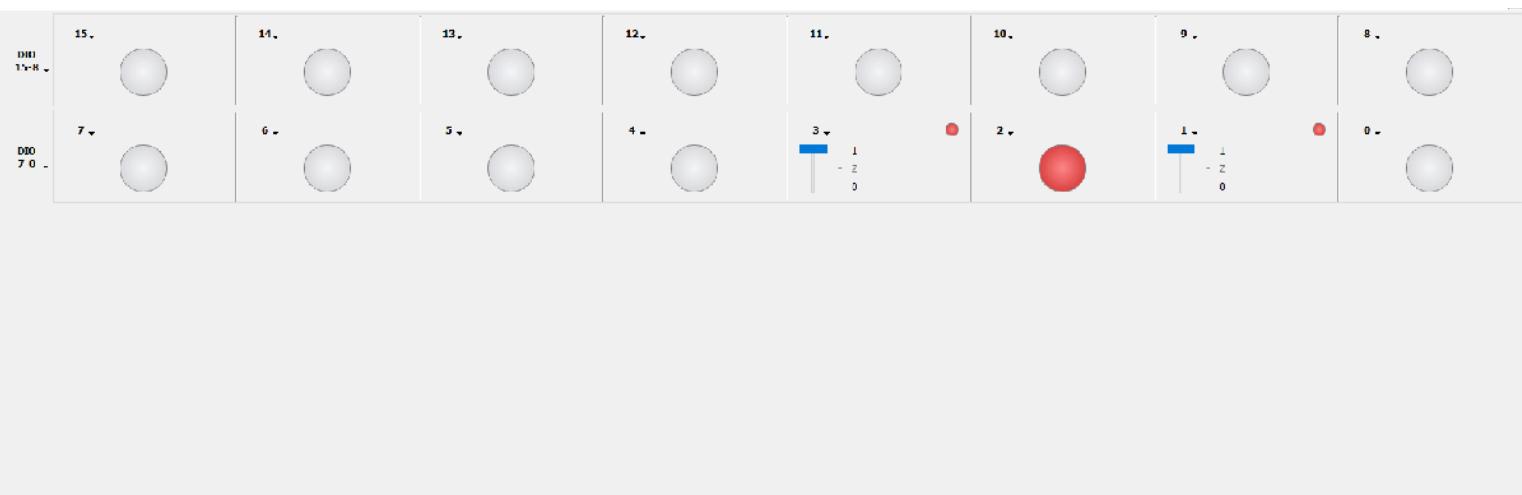


Figure36 : State 4 when $S = HI$, $R = HI$ so consequently $\bar{Q} = LO$ and, $Q = HI$

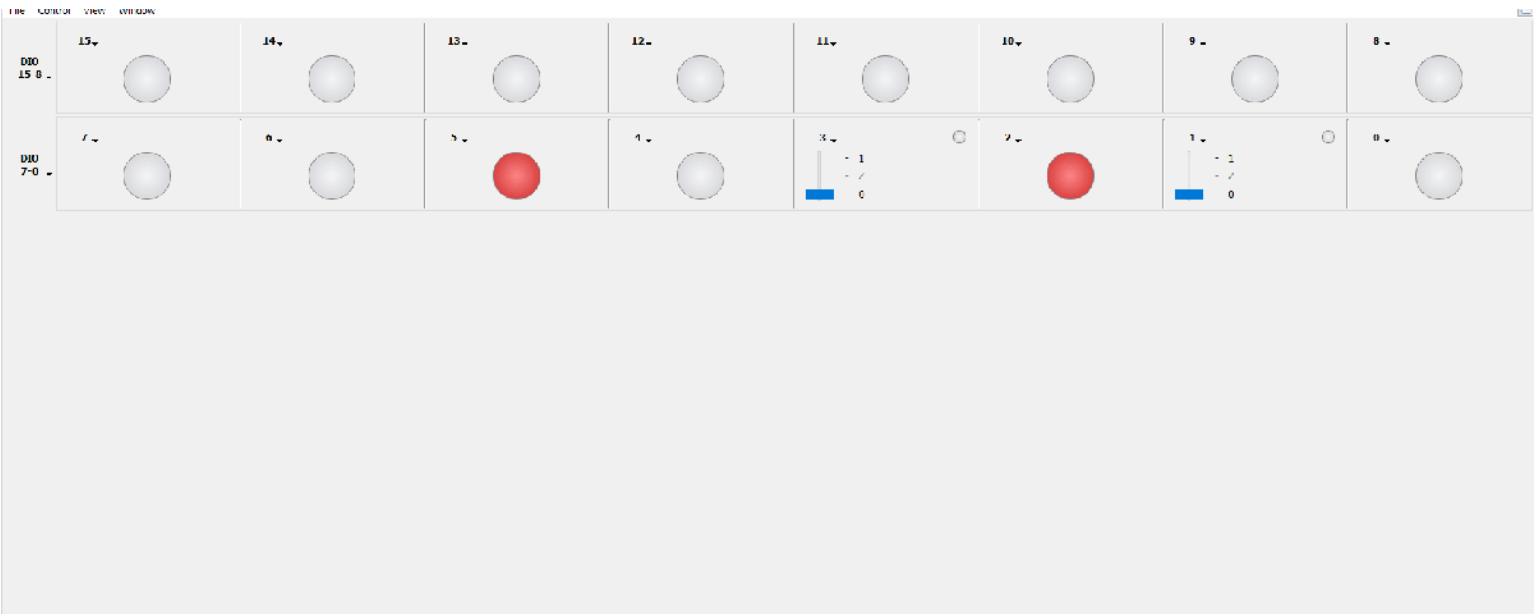


Figure37 : State 5 (invalid state) when $S = LO$, $R = LO$ so consequently $\bar{Q} = HI$ and, $Q = HI$

From the above screen exports of the STATIC IO, I verified that my circuit functioned as desired. We can also see that our predictions about the invalid state and such were proved true as well. State 5 should be omitted since it violates the pre-condition however for demonstration purposes, it was included in the exports included.

After verifying all the states of this flip flop and the functionality of each of the individual components, we now move on to section 4 of this lab: the most interesting and nerve-racking component. I crossed my fingers and moved on the integration component.

4. Integration of components

Before we start integrating all the components together, let's revisit all the background information and fully understand how all the components integrate together. This will enable us to not only have a deeper understanding of the ADC itself but also help troubleshoot when something doesn't work as desired.

Here is the circuit diagram of the complete ADC device again, but with labels included for all the important connections that will be crucial in our explanations of the circuit:

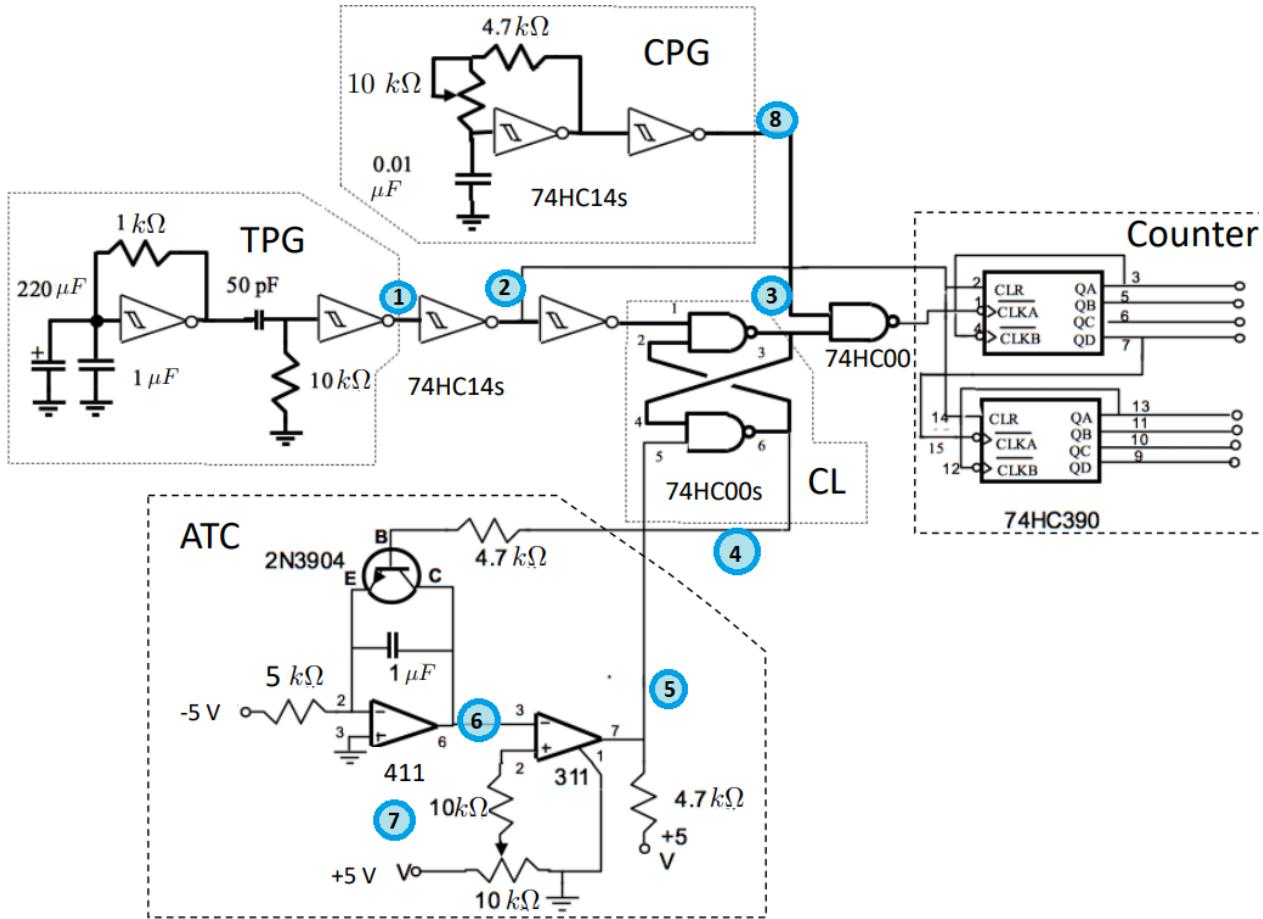


Figure 38 : Final integration of all the components together to work together as Analog to Digital Convertor with labels (Source: Dr. Jones' Description of Experiment 6a)

Now to understand the functionality of ADC, let's look at each component individually and in integration with other:

- TPG is what determines the frequency of the circuit. It produces a negative going output at **1** whereas the decade counter requires a positive input. Hence, we add another inverter at **2** to flip the negative output of the TPG to positive pulses and to provide extra time delay.
- CL or control logic (acting as the logic gate for the circuit) is what allows the pulses from CPG at **8** to pass to the decade counter. Now to ensure that no gated clock pulses can arrive at the counter before the counter has been cleared, we need to provide a slight time delay. This is accomplished by another inverter is added to the circuit (connected in series with **2**).
- The inverter mentioned in the above step, alongside providing more time delay for the input to the decade counter, inverts back the short positive pulse to negative since the flip flop requires a short input negative pulse.
- CL (control logic) then opens the transistor switch on the ramp generator to initiate the ATC (at **4**).
- Then we have the integrator ramp generator signal at **6** (which is determined by the DC input voltage of the comparator) which depends on the DC input voltage at **7**.
- The output of the comparator at **5** feeds into the CL to determine when to stop feeding clock pulses into the ramp signal, which in turn turns the ramp signal off.

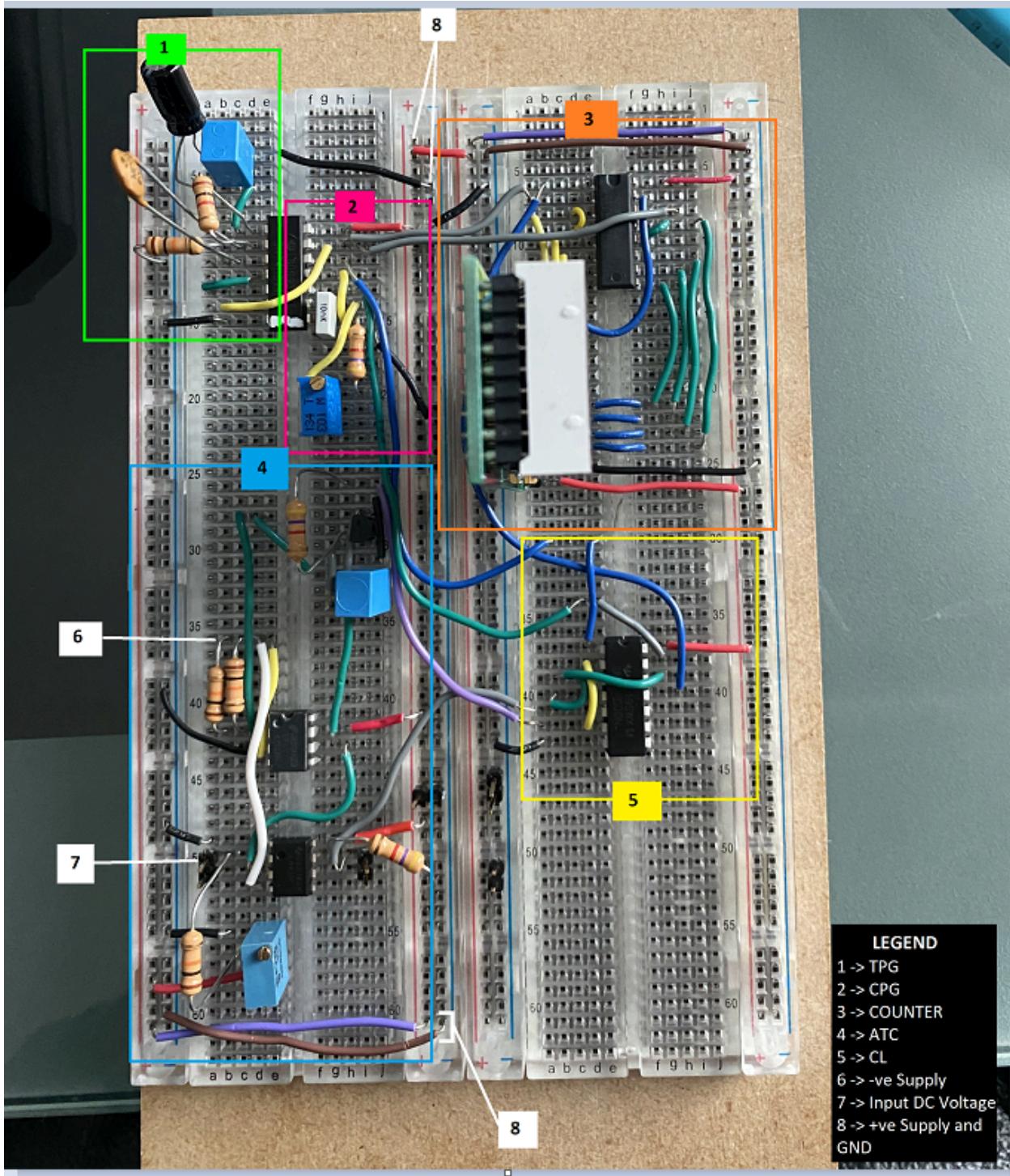


Figure39 : Final Circuit construction with all the components integrated together. The image above includes the legend on how the different components were labelled. Also note that red wires were only used for +ve Supply and black wires were only used for Ground. White was used for -ve supply, green and the purple and brown wires used in the bottom left row and top right of the breadboard were to extend supply to other rails on the breadboard. Detailed description of all the components and connections is done in each component's respective section.

Now onto the details of integration of each of the components. I will try to break it down into steps:

1. First the operator of the circuit adjusts the value of the potentiometer to set the threshold value for the DC input voltage to the comparator at **7**.
2. Next, this voltage determines when the ramp generator signal will turn on (when the voltage at **6** is lower than DC input voltage) or off (when the output at **6** crosses the threshold DC voltage).
3. Now whenever the output at **6** exceeds the threshold voltage, the comparator will produce an output received as LO for the flip flop at **5**. Note that this also means that at PIN 5 of the NAND gate, there will be an input signal of LO.
4. The input at PIN 1 of the NAND gate will be high at this point in time of the circuit operation and so these combined output will result in a HI being at PIN 6 of the NAND gate.
5. This HI value at **4** will in turn close the transistor switch shorting the capacitor and this will terminate the production of the ramp. Now the output at comparator is set back to HI resulting in a LO output at **4** hence steps 1-5 are repeated.

After gaining the information about the ATC's functionality, let's look at the integration of the other components together. As explained above, whenever the output at PIN 6 of the NAND gate is LO, the capacitor connection will be restored and the ramp generator will start producing signals. Output from TPG is what determines the time at which this happens. When the output at **1** is LO, input at PIN 1 of the NAND gate will also be LOW (after a time delay though, as explained above). This will restore the capacitor connection and the ramp generator will start generating signal again. We also see that whenever the input at PIN 3 of the NAND gate is LO, no matter what the input at **8** is, the output to the decade counter will be HI.

Another crazy cool fact about this circuit is that LED display to us seems like it refreshes right away to produce the right output when we tune the DC input voltage at **7** however it's just counting that fast that it gives the illusion of a smooth transition.

To understand this explanation about the integration of components together, we can take a look at the timing diagram where all the components come together to produce the final visual output of each component's output (pretty cool stuff!). The timing window is included below:

Note: To visually see each of the outputs better, me and my peers decided to add a shift to the y-values of the graph so that all the components could be stacked on top of each other for better comparison.

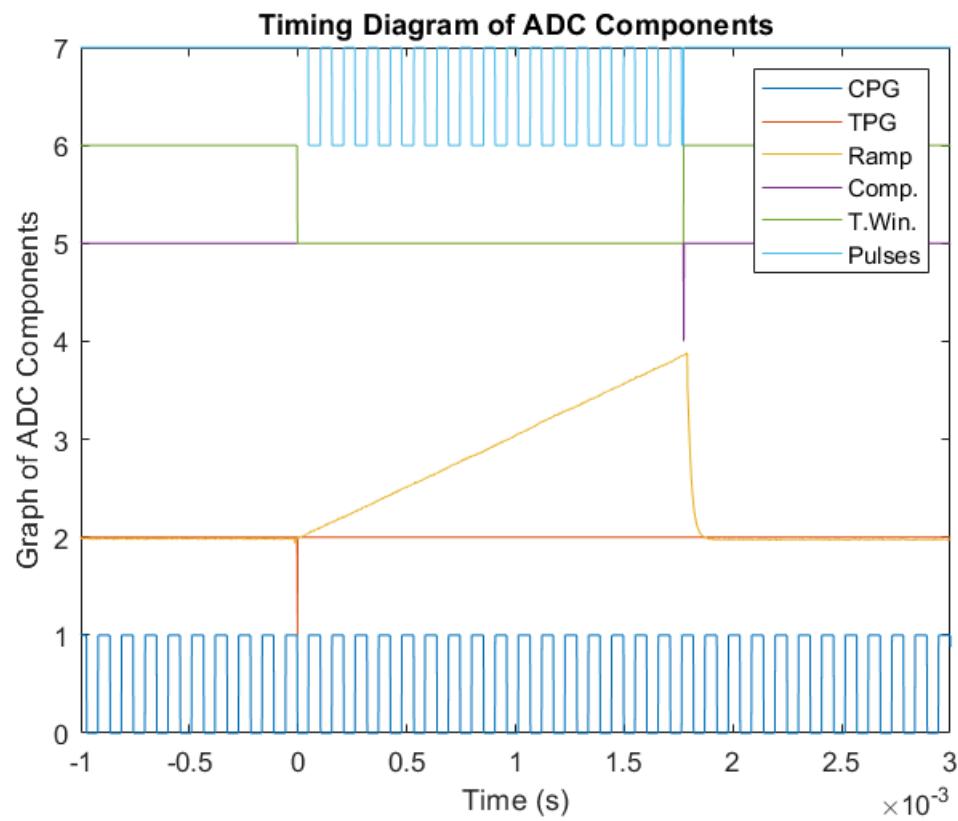
```
clear legend
plot(Times, CPG);
hold on;
plot(Times, TPG + 1);
plot(times + 0.580*10^-3, integrator + 2); %the phase shift in time was necessary to ensure
% that the integrator ramp started at 0 as well even
%the collection of the data points started earlier
plot(Times, Comp + 4);
plot(Times, timingWin + 5);
plot(Times, noOfPulses + 6);
xlim([-1*10^-3,3*10^-3]);
hold off

xlabel('Time (s)')
```

```

ylabel('Graph of ADC Components');
legend({'CPG', 'TPG', 'Ramp', 'Comp.', 'T.Win.', 'Pulses'})
title('Timing Diagram of ADC Components')

```



Another quick note: For the above timing diagram measurements, I was able to capture the outputs with the $220\mu F$ capacitor in the circuit and didn't need to take it out.

Here's a revised legend for the above timing diagram:

CPG: Clock Pulse Generator

TPG: Trigger Pulse Generator

Ramp: Ramp generator signal

Comp. : Output of the Comparator

T. Win.: Timing Window of the circuit

Pulses: Number of Pulses being counted in the time period determined by the timing window

From the above timing diagram we can see that the time at which TPG produces the short pulse is exactly when the ramp generator starts producing the signal. The ramp generator stops the signal exactly at the instant when the comparator produces a HI signal (indicating that the ramp generator voltage was exceeded the threshold DC input voltage). This same concept of time (the amount of time the ramp stays in the circuit) is captured by the timing window as well. The timing window is LO for exactly the amount of time equal to the time period of

the ramp signal. We can also see the number of pulses counted in that amount of time to produce the output signal at LED (the illusion of refreshing right away). Lastly, we have the CPG continuously producing clock pulses for the circuit.

Note: The time window is affected by the comparator since the comparator determines the end point of the time window. This can be changed using the variable resistor in the comparator circuit using the 10 kΩ

To further solidify that the ADC works as desired, here's a conversion table between the input voltage values as measured by the DMM vs. what was shown on the LED display:

DMM Voltage Measurements	LED Display Values
0.30 ± 0.3 V	0.3
1.31 ± 0.3 V	1.3
2.11 ± 0.3 V	2.1
3.30 ± 0.3 V	3.3
3.70 ± 0.3 V	3.7

As we can see from the above table, conversion is one to one. However, you might ask why is the largest voltage value only 3.7? Well, that's because the voltage signal gets clipped at 3.7-3.8 range and the LED display is maxed out at that value. When tested with such values, the LED display shows 88 (unknown).

I have also included the image of the images from some of the voltage measurements done for the table above:

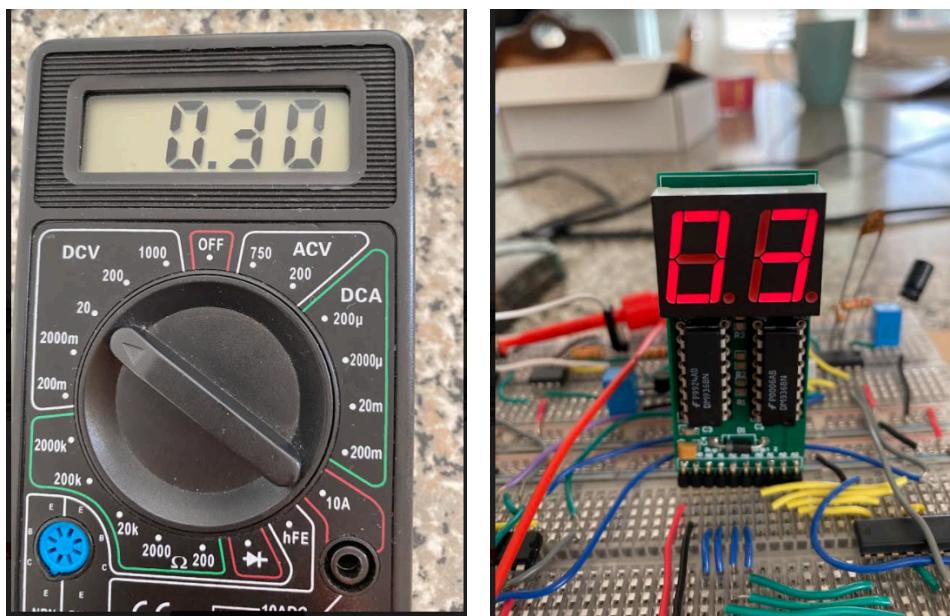
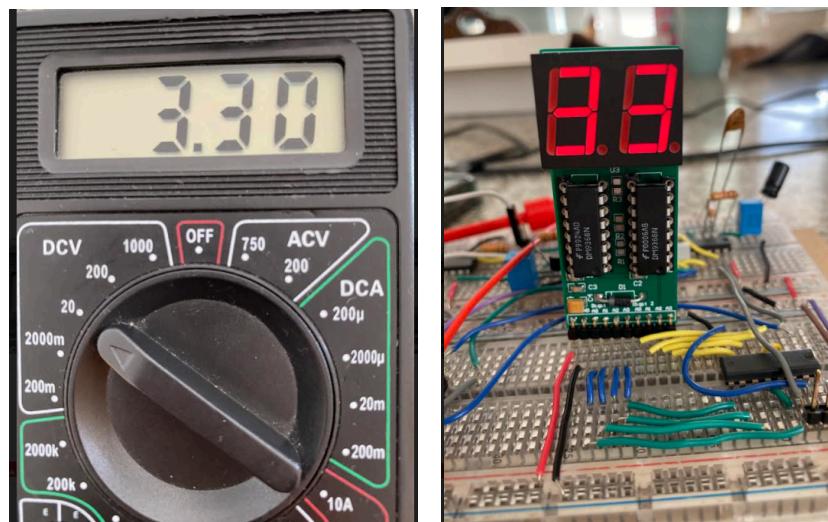
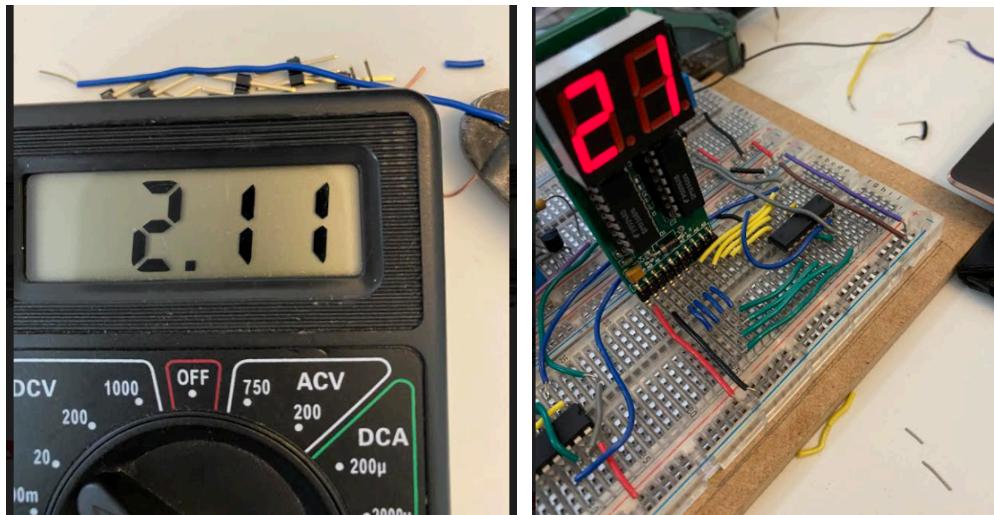


Figure40 : Some of the voltage measurements from experiment

5. Troubleshooting Section

Yes! I have a whole section dedicated to all the hours I spent debugging my circuit :)

- One of the biggest situations that repeatedly happened to me and wasted a lot of time trying to debug the circuit was that oscilloscope kept showing current overflow. I would check all my connections, make sure every component was grounded properly and that the supplies were in the right power rail. After all this troubleshooting, I would eventually find out that I had not connected the wall-supply to the analog discovery which causes a current overflow sign to occur. Although tedious, this problem at least assured me that I wasn't shorting components together in my circuit.
- Another thing that I had trouble with throughout the lab was with my analog discovery 2 device. The pins that attach to the analog discovery 2 were very loose for me and I had to hold them in place for every single experiment. For this lab, especially, it was difficult since due to the loose connections the output on scope was not what I expected 50% of the time which resulted in me debugging my circuit. I would eventually find out that the problem was with the wires and not the specific components on the breadboard.
- When I implemented my ATC, the output it produced was very wrong. I then checked the individual output of the integrator and the comparator to make sure that those were correct. Upon further analysis, I realized that I had not connected the -5V supply required in the integrator circuit which was problematic for the other components and invalidated my output at the comparator.

Below are some of the techniques I used to debug and troubleshoot my circuit and I would advise my future self to take these into consideration when having trouble with a circuit:

- Draw out the connections that you think are in the circuit and reason them out with the actual connections on the breadboard: This tip was mentioned by Prof. Jones when he was giving us insights on how to troubleshoot and waste less time. I personally found it very helpful since after drawing a 2D circuit drawing of the components I was having trouble with and thoroughly going through the connections on the breadboard, I usually found the problem--loose wires, not connected to supply, not grounded properly etc.
- Check the voltage output with a DMM of the component that isn't working properly: Measuring voltage of different segments within the same circuit usually helps identify which connection is causing the problem. When the output of my CPG wasn't correct during one of the first times in the experiment, I used this approach and measured the voltage at each connection. I, then, discovered that the potentiometer wasn't connected to the capacitor properly hence it didn't affect the circuit at all. This was the reason as to why the frequency of the output signal was not changing when I was tuning the potentiometer in the CPG. After measuring the voltage at each instance, I figured it out.
- Check that all the components are connected to the supply and other specific components are grounded properly: I know this is one of the elementary things to do when you try to debug the circuit but usually what caused a faulty output was that, for example in the Schmitt Trigger, unused inputs were not grounded properly hence they were affecting the output of the other pins.
- If you are certain about all the above steps, try pushing in the wires! If that doesn't work then as a last resort, follow the next tip.

- Ask for help! Sometimes, when I had gone through all the steps above and my circuit component would still not work, I asked the TAs or even my labmates. I usually had missed something in my circuit that they helped me realize which saved a lot of my debugging time.

6. Conclusion

This lab, pointing out the obvious, was the most interesting project in this course. As excruciating and frustrating it was to debug and troubleshoot and still not have some of the components work well, the outcome was worth it. If I think back now, having all the regular circuit components such as capacitors, resistors, transistor, etc. come together and produce something such as converting an Analog signal to digital, is almost magic. I know that this is a fundamental device which is used everywhere since as we saw in the background section, analog signals are everywhere and to process information from them, we need to transform them into digital. This course set the foundation of electronics, integrated circuits, and a lot of other skill set which I won't mention (because there are a lot of them). Through this lab, I refined my troubleshooting, debugging and circuit construction skills. I realized the importance of making neat circuits (so much easier for debugging!), different debugging techniques, operation and functionality of Schmitt Triggers, logic gates, decade counter, OpAmps, and much more. I am very grateful for having a great team of instructors and TAs for this course and I feel much more confident in my circuit construction skills than what I started with at the beginning of the course. Now, to finish conclude my personal experience with this lab, I will provide a very brief summary of the components and their results:

TPG: The output was a short-time pulse which would be used an input in the control logic of the circuit.

CPG: The output was a clock pulse with a tunable frequency which could be varied using the potentiometer. The output from this is used an input to the decade counter (determined by the CL)

Counter: Counts the pulses and displays the result on the LED display

ATC: Comparator output determines when to stop feeding pulses into the decade counter

CL: Essentially what allows all the other components to communicate with each other

The timing window essentially represents the time taken by one period of the signal to take place. This is determined by the TPG and ATC (comparator) which initialize the starting and ending point of the signal. If we measure the time window, the value can be found to be: 1.5 ± 0.05 ms using the scope (one can also measure this using the timing diagram included above).

To conclude, I am still amazed by how all the components come together to produce such a device and I am very grateful for having the opportunity to conduct this experiment this term. Thank you for a great term!