NATIONAL INSTITUTE OF TECHNOLOGY ROURKELA
END SEMESTER EXAMINATION, 2018
BTech 3rd Semester

SUBJECT: Digital System Design **DEPT. CODE: CS 2001**
FULL MARKS: 50 **Duration of Examination: 3Hours**
Number of pages: 1

Answer **Any FIVE.** Figures at the right hand margin indicate marks
All parts of a question should be answered at one place

Q.No.	Question	Marks
1	**(a)** Design a **mod 10** asynchronous counter using **T** flip flops. **(b)** Convert a **SR** flip flop to **D** flip flop. **(c)** Find the **15's** and **16's** complement of following hexadecimal numbers. *(i)* **76** *(ii)* **7B.A**	[5+3+2]
2	**(a)** Differentiate between Ring counter and Johnson counter. Write the sequence of stages for a **5** bit Johnson counter. **(b)** Analyze the sequential circuit with two **T** type flip flops, which is specified by the following state equations. **Z = A** **A (t+1) = x′ y + xB** **B (t+1) = xB + Ax′** **(c)** Implement a half subtractor using multiplexer. Use block diagram of multiplexer.	[4+4+2]
3	**(a)** Design a serial binary adder logic circuit. **(b)** Draw the logic diagram of a 1:16 DEMUX using 1:4 DEMUXes. Use block diagrams. **(c)** In a number system, if **41/ 3 = 13**, find its base.	[5+3+2]
4.	**(a)** Design a sequence detector with **D** flip flops to detect the sequence **101011**. (b) Design a **2** bit comparator with suitable **decoder**. (c)Find the Gray codes for $(15)_{10}$ and $(14)_{10}$	[5+3+2]
5	**(a)** Design a synchronous counter with JK flip flops that goes through states **3**, **4**, **6**, **7**, **3** and so on. Check whether the counter is self-starting? Modify the circuit such that whenever the counter goes to an invalid state, it comes back to state **3**. **(b)** Design a full subtractor using two half subtractors and an **OR** gate. (c) What is the range of signed decimal values that can be represented in a byte? Justify your answer.	[5+3+2]
6.	**(a)** Design a sequence generator using shift register to generates the sequence **1101011.** Use **D** flip flops**.** **(b)** Design a combinational logic circuit with four input variables that will produce logic 1 output when the number of 1's in the inputs is even. **(c)** Perform the following subtractions using excess-3 code *(i)* **276 – 175** *(ii)* **57.6 – 27.8**	[5+3+2]