End Semester Examination, Autumn–2021-22

Part-B Full marks: **20** Exam duration: **1 Hours**

Answer **all** questions. Figures next to each question in square bracket indicate marks.
All Parts of a question should be answered at one place.
This question paper contains ONE page.

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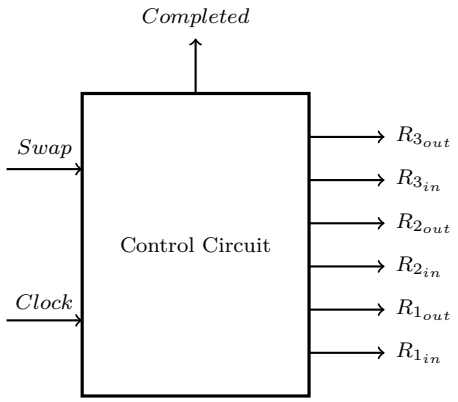
1. Your roll number has the pattern `1yyCSabcd`. Count all unique digits in `{a, b, c, d}`. If the number of unique digits are less than 4, take any digit of your choice to make 4 unique digits. Consider the final 4 unique digits as your minterms and let it be `{p, q, r, s}`.

   Use T-Flip-Flops to design a 4-bit counter that has a control input called $\overline{F}/R$. The functionality of the control input is given below. [10]

   $$\overline{F}/R = \begin{cases} 0, & \text{the circuit counts in Forward sequence as } \texttt{p} \rightarrow \texttt{q} \rightarrow \texttt{r} \rightarrow \texttt{s} \rightarrow \texttt{p} \cdots \\ 1, & \text{the circuit counts in Reverse sequence as } \texttt{s} \rightarrow \texttt{r} \rightarrow \texttt{q} \rightarrow \texttt{p} \rightarrow \texttt{s} \cdots \end{cases}$$

2. Design the control circuit to swap the contents of two n-bit registers R_1 and R_2. Let there be a temporary n-bit register R_3. The following figure indicates the external signals involved in the control circuit.



   The swap procedure begins when $Swap = 1$. The swap procedure has the following sequence along with the control signals —

   $$\begin{aligned} [R_3] \leftarrow [R_2] \quad & R_{3_{in}} = 1,\ R_{2_{out}} = 1 \\ [R_2] \leftarrow [R_1] \quad & R_{2_{in}} = 1,\ R_{1_{out}} = 1 \\ [R_1] \leftarrow [R_3] \quad & R_{1_{in}} = 1,\ R_{3_{out}} = 1 \end{aligned}$$

   Once the *Swap* signal has been asserted, the above three steps are executed irrespective of subsequent *Swap* signals, and finally *Completed* signal becomes high to indicate that the swap procedure has been completed. In your design, include state diagram, state table, logic diagram along with excitation equations. [10]

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