Department of Computer Science & Engineering,
National Institute of Technology Rourkela

End-Semester Examination (Autumn), 2019

Subject:**Digital System Design** Subject Code:**CS-2001**

Full Marks:**50** Duration:**3 Hours**

Answer all questions.

Figures at the right margin indicate marks. All parts of a question must be answered at one place.

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1. (a) Implement a full subtractor using two 4:1 multiplexers. [3]

   (b) Design a Mod-8 ripple counter using T flip-flops. [3]

   (c) Implement a full subtractor using two 4:1 multiplexers. [3]

   (d) State the difference between a Mealy and Moore machine. [1]

2. (a) Design a synchronous counter using JK flip-flops that goes through states 3, 4, 6, 7, and 3 .... [5] Check whether the counter is self starting? Modify the circuit such that whenever it goes to invalid state, it comes back to state 3.

   (b) Draw the sequence table, state diagram and logic diagram of a 4 bit twisted ring counter using D flip-flop. [3]

   (c) Explain how the race around condition can be avoided in J-K Flip Flops. [2]

3. (a) Design a 4-bit shift register with parallel load using D flip-flops. These are two control inputs: shift and load. When shift = 1, the content of the register is shifted by one position. New data is transferred into the register when load = 1 and shift = 0. If both control inputs are equal to 0, the content of the register does not change. [4]

   (b) Design a POS circuit that will generate an even parity for a 4 bit input . [3]

   (c) Draw and explain the logic diagram of 2's complement 4 bit binary subtraction. [3]

4. (a) Design a sequence detector using D flip-flop to detect the sequence 1011. One bit overlapping is permitted. [5]

   (b) Design a 5 to 32 line decoder using 3 to 8 line decoders and 2 to 4 line decoders. [3]

   (c) Let $f(A, B) = A' + B$. Find the Simplified expression for function $f(f(x + y, y), z)$. [2]

5. (a) Carry out the following flip-flop conversions. [4]

      i. D to SR

      ii. JK to D.

   (b) Synthesize a serial binary adder. [4]

   (c) Draw the timing diagram for a 4 bit SISO shift register for an input string of 1101. [2]

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