#### Counters

Reference
Chapter 7
Registers and Register Transfers
Moris Mano 4<sup>th</sup> Edition

#### Counter

- A register that goes through a prescribed sequence of distinct states upon the application of a sequence of input pulses
- Input pulses may be
  - Clock pulses
  - Originate from some other source
  - May occur at regular or irregular interval of time

# **Binary Counter**

- Counter that follows the binary number sequence is called binary counter
- An n-bit binary counter consists of n flip-flops and can count in binary from 0 through 2<sup>n</sup>-1

# **Types of Counters**

#### 1. Asynchronous Counters

In which C input of some of the flip-flops are triggered not by common pulse but rather by the transitions that occur on other flip-flop outputs

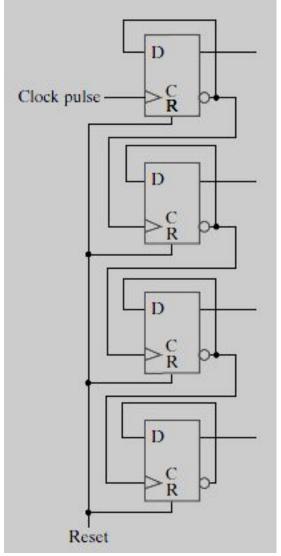
e.g. Ripple counters

#### 2. Synchronous Counters

In which the C inputs of all flip-flops receive common pulse

# **Asynchronous Counters**

# 4-bit Ripple Counter



Q <sub>3</sub>	Q <sub>2</sub>	Q,	Q <sub>0</sub>
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

What will be the state of counter on positive edge after 1111?

# 4-bit Ripple Counter

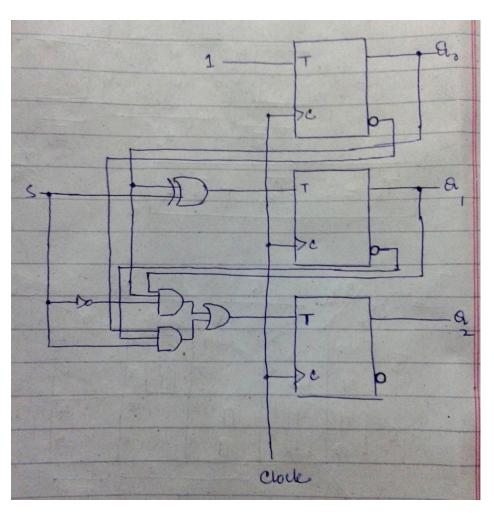
 Design a 4-bit ripple counter for downward counting

Can you design an asynchronous Up-Down Counter with Selection Input?

Downward Counting Seque				
Q <sub>3</sub>	$\mathbf{Q}_2$	Q,	Q <sub>o</sub>	
1	1	1	1	
1	1	1	0	
1	1	0	1	
1	1	0	0	
1	0	1	1	
1	0	1	0	
1	0	0	1	
1	0	0	0	
0	1	1	1	
0	1	1	0	
0	1	0	1	
0	1	0	0	
0	0	1	1	
0	0	1	0	
0	0	0	1	
0	0	0	0	

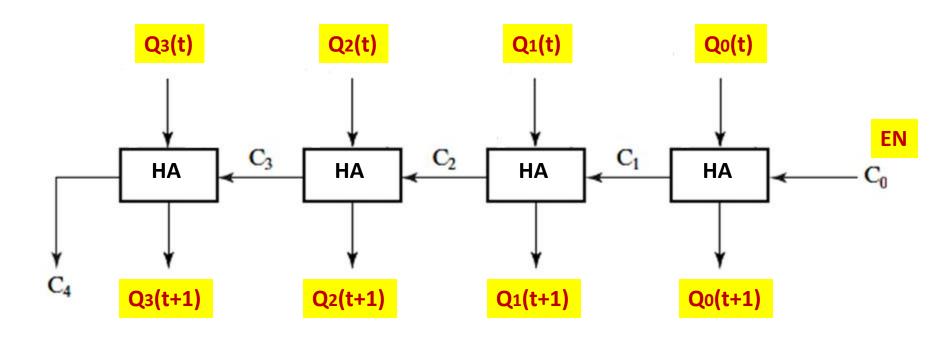
# **Synchronous Counters**

## Synchronous 3-bit Up-Down Counter

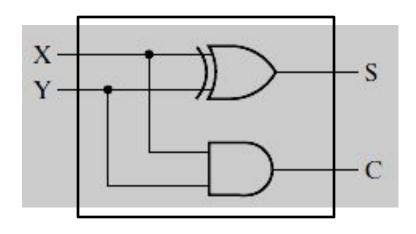


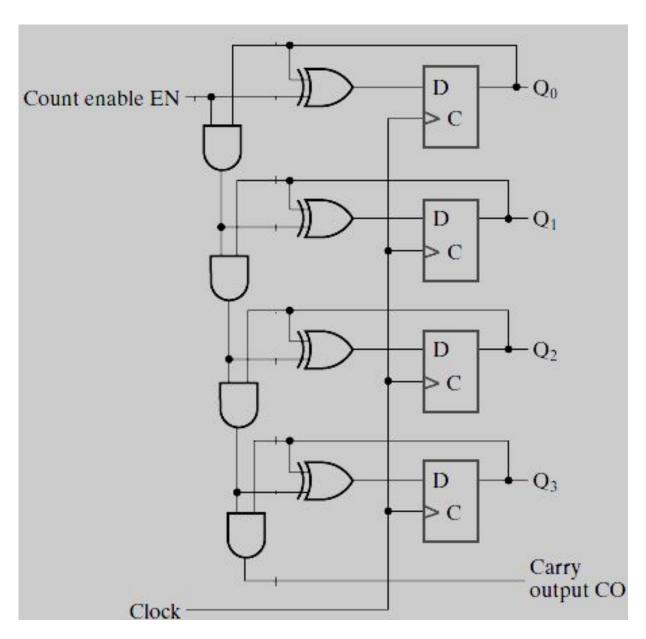
For S=0
Count Upward

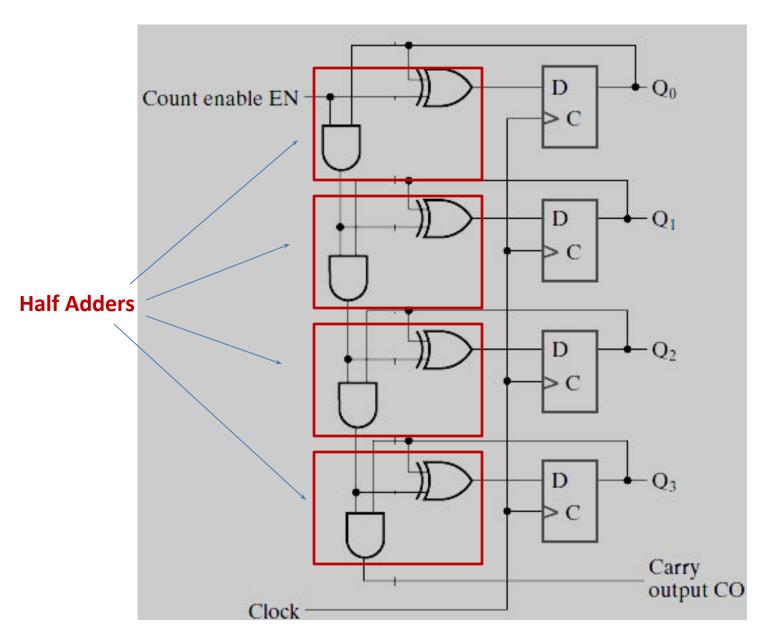
For S=1
Count Downward

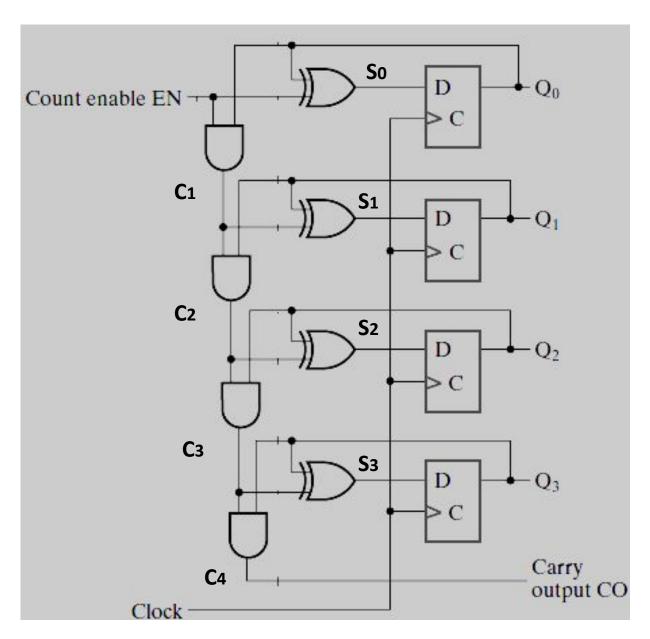


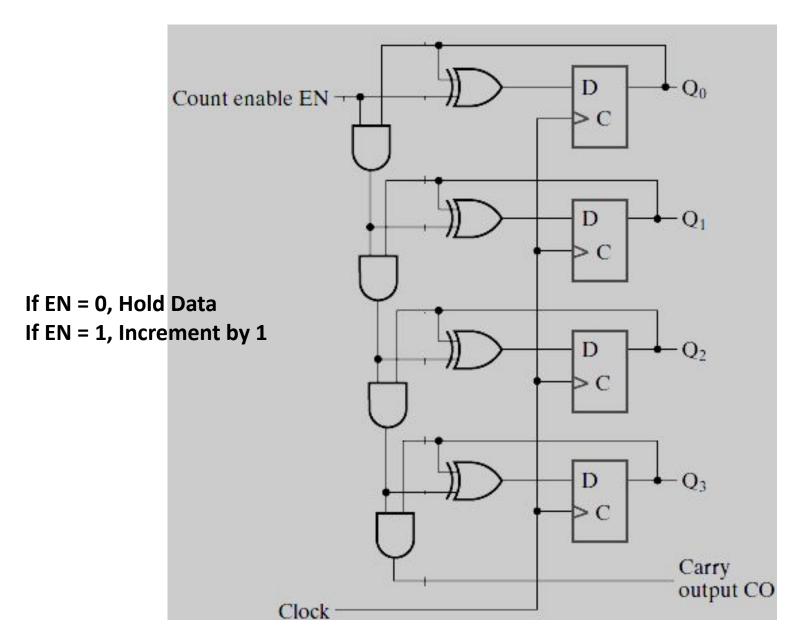
## Half Adder

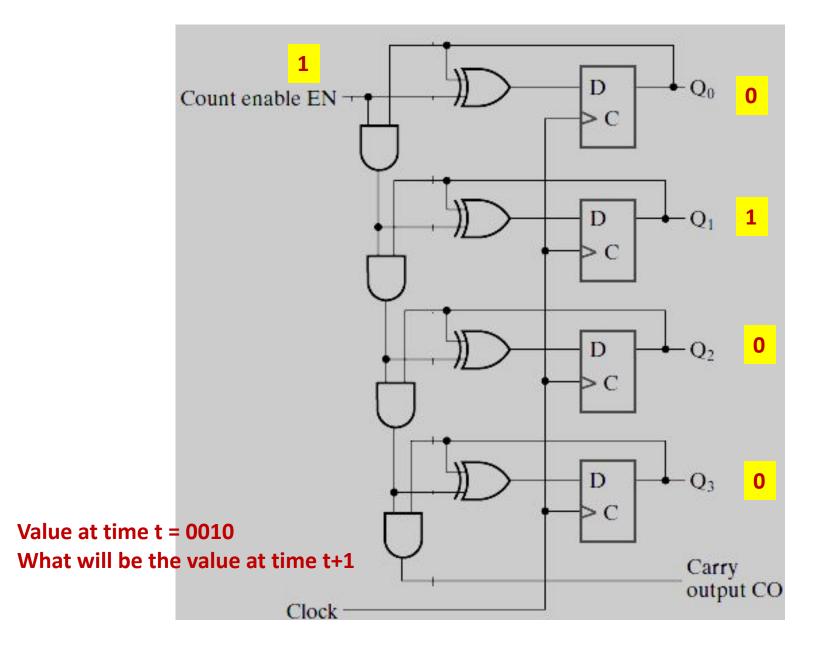


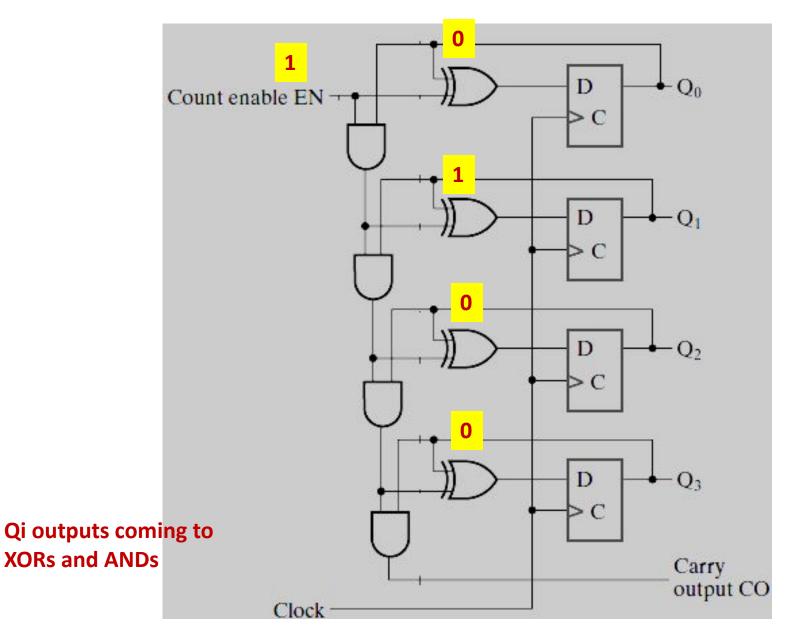


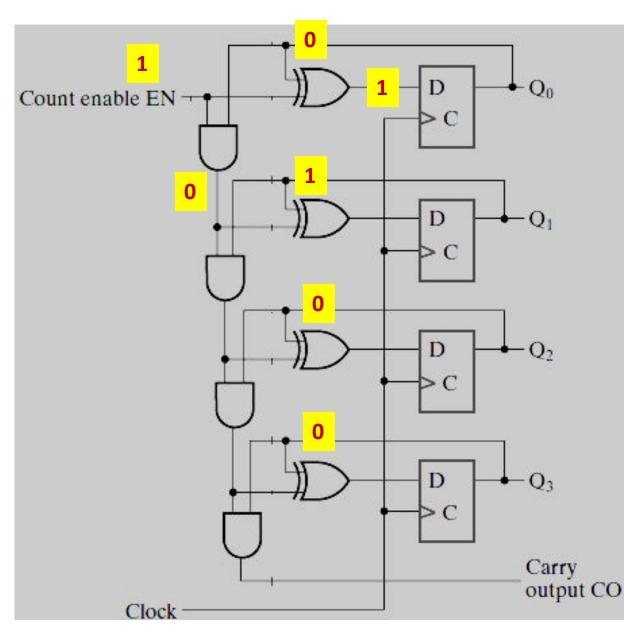


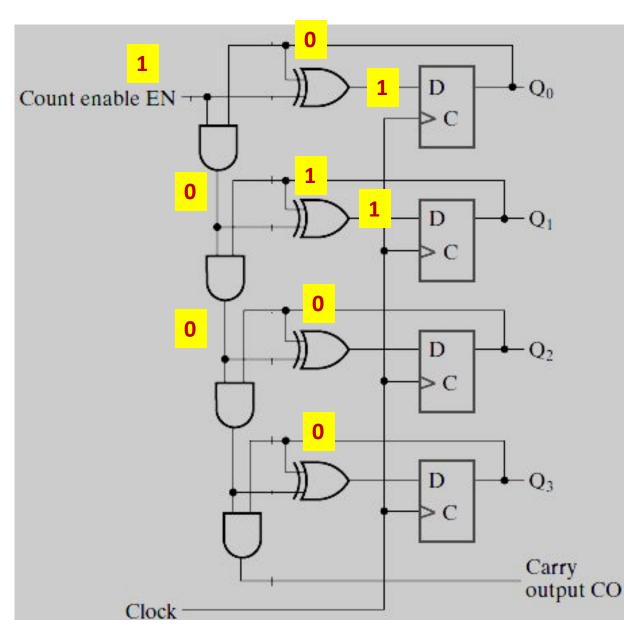


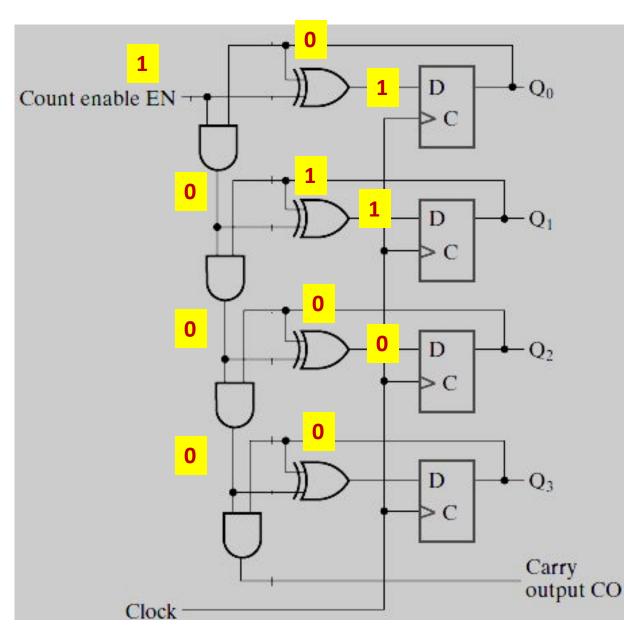


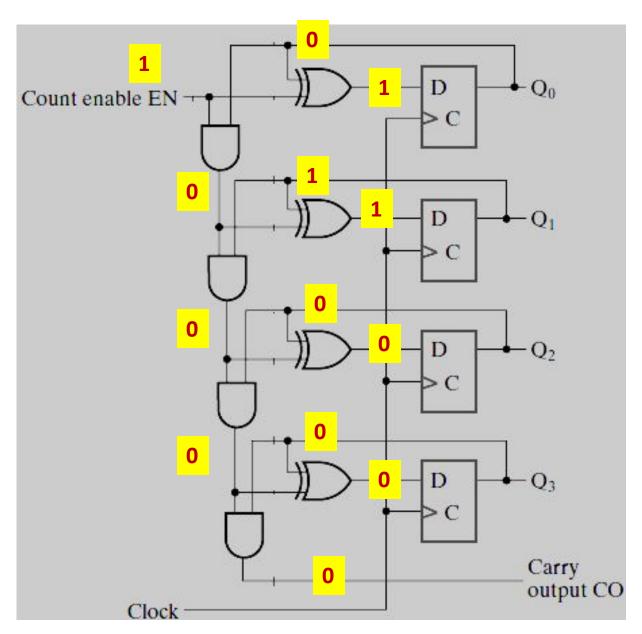


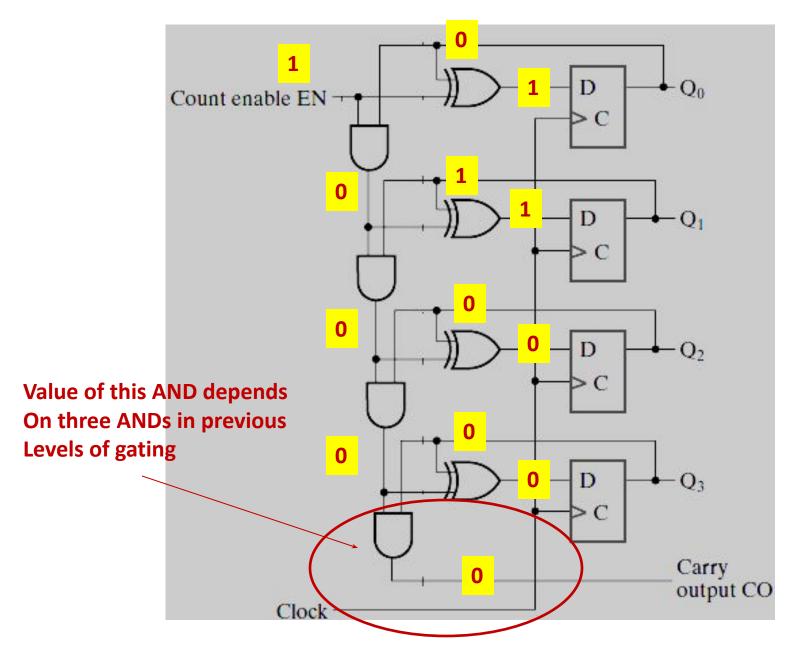


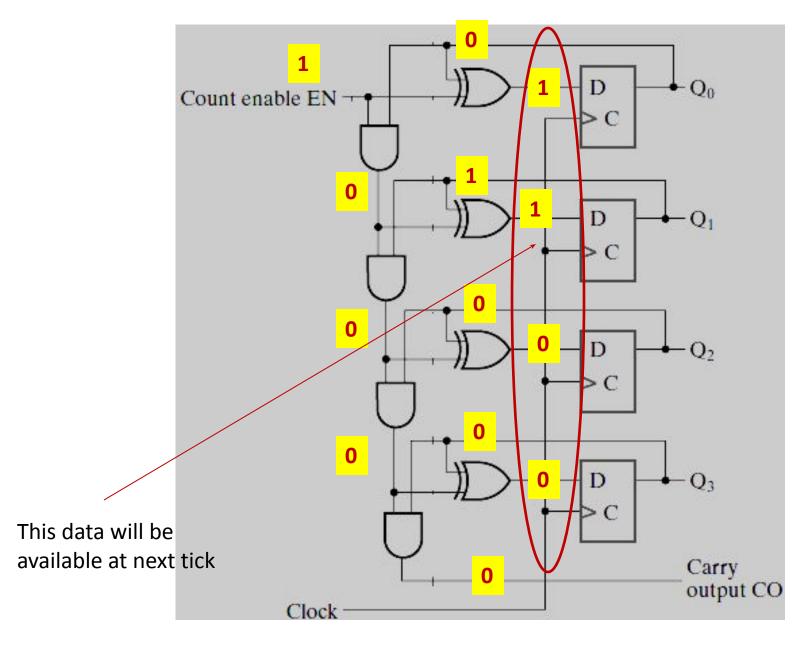


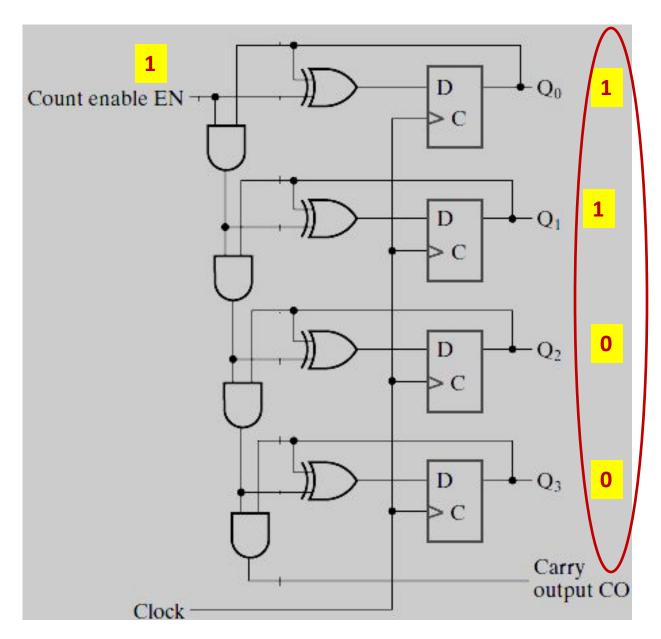




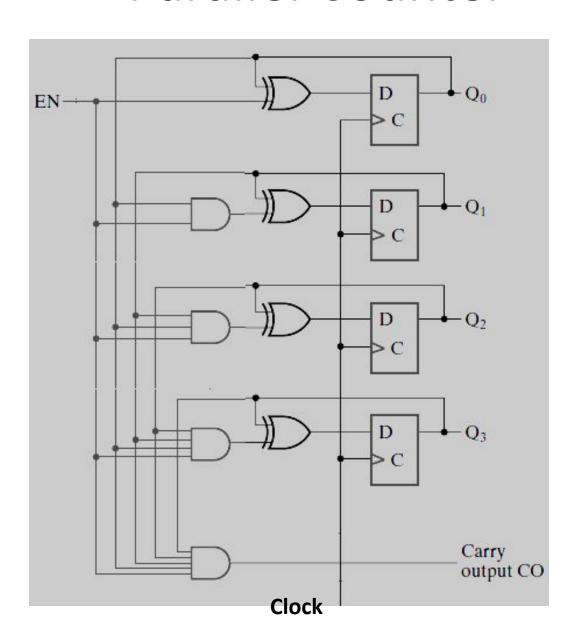


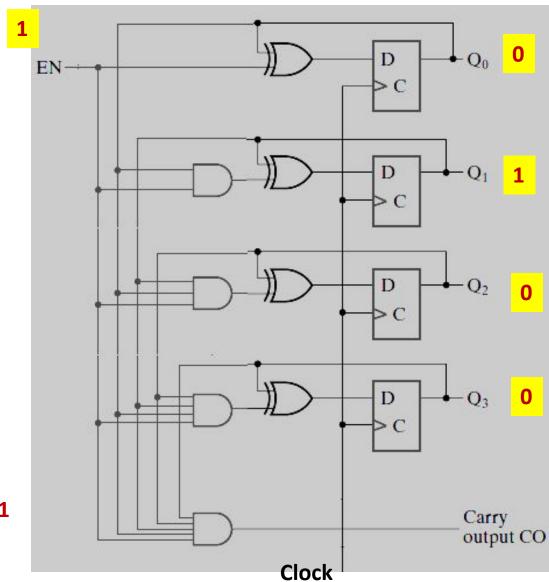




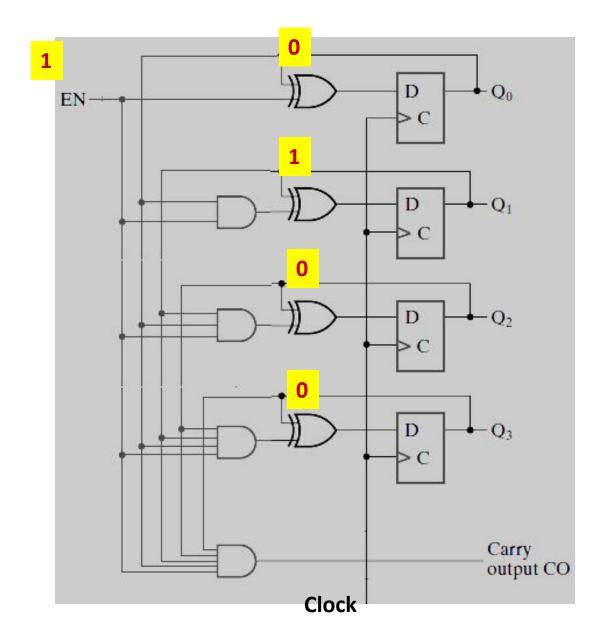


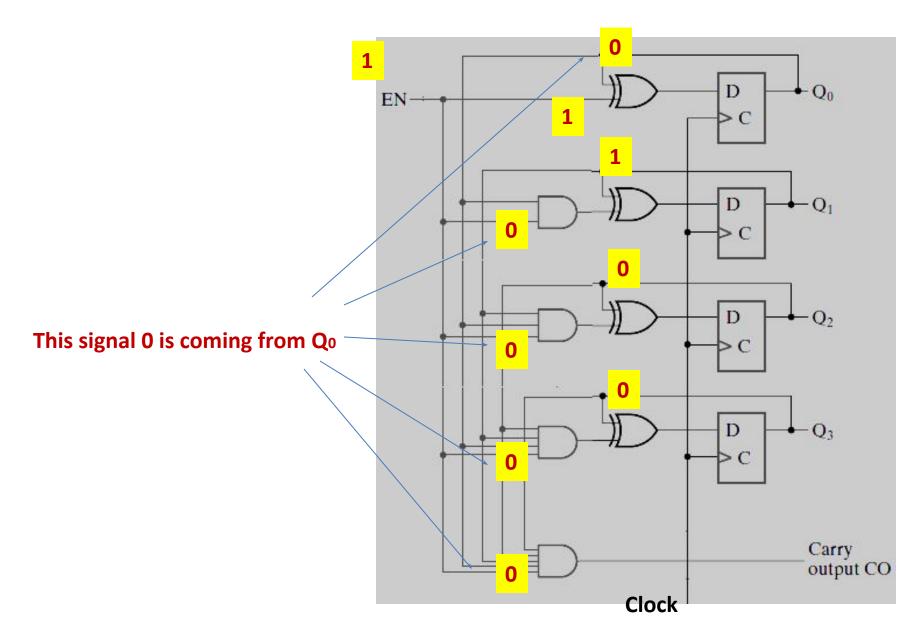
# Parallel Counter

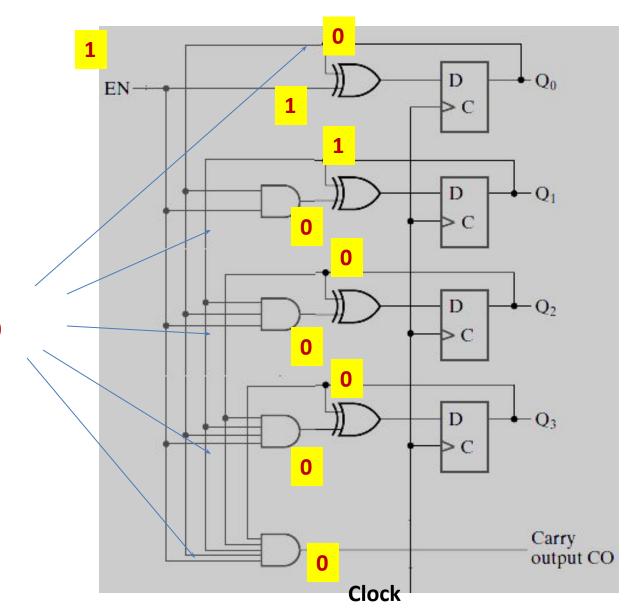




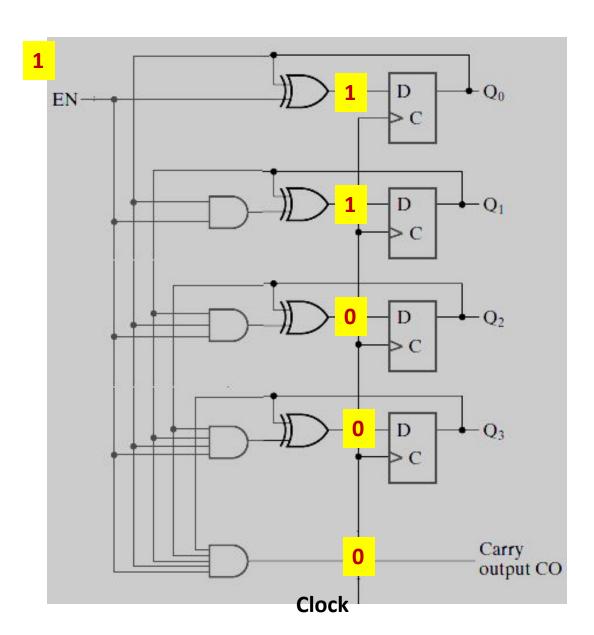
Value at time t = 0010
What will be the value at time t+1



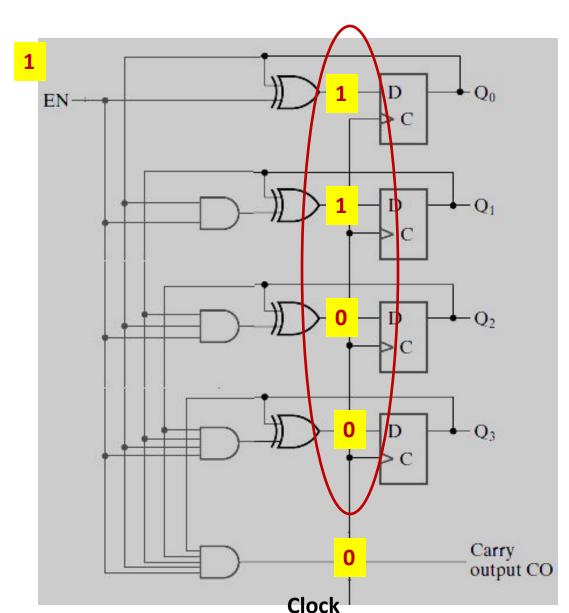




All the ANDs which got 0 Gave output 0



X XOR 1 = X' X XOR 0 = X

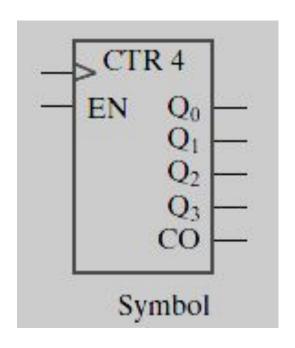


This data will be available
On counter output at time t+1

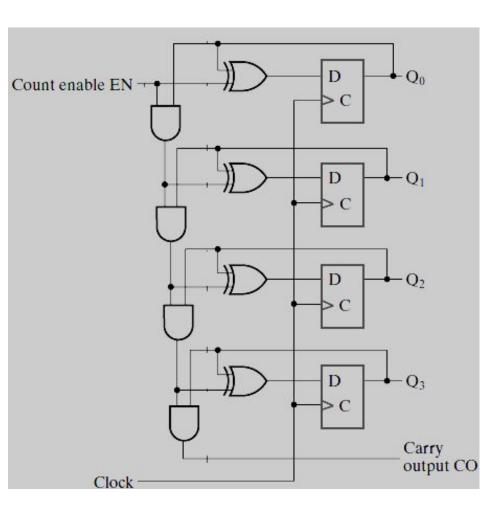
 $Q_0$ EN -Q<sub>3</sub> Carry output CO Clock

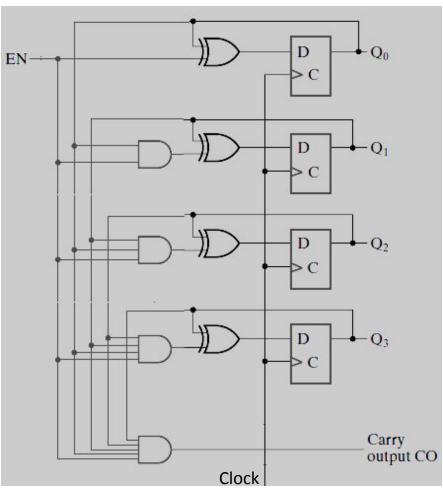
Counter at time t+1

# 4-Bit Synchronous Binary Counter



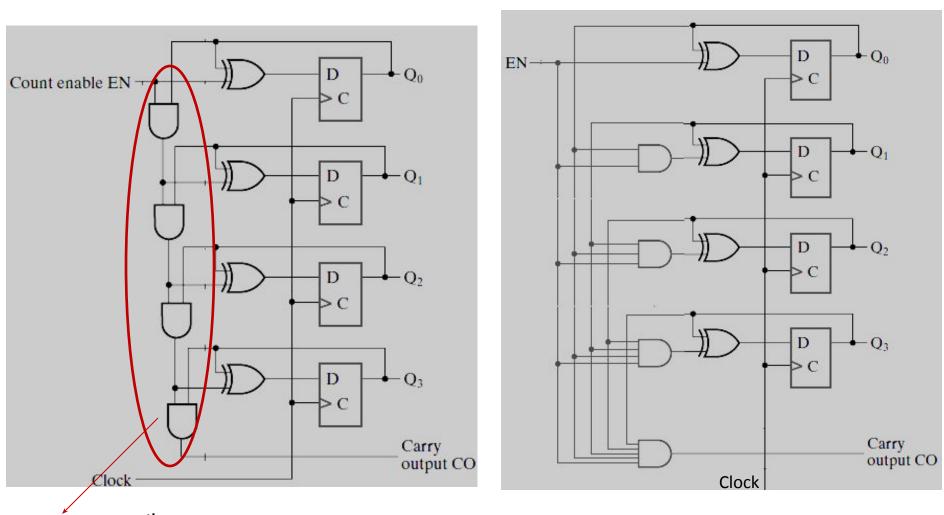
#### Serial VS Parallel Counter





Gate delay being accumulated in Serial Counter as last AND is at level 4 of gating. For example, going from state 1111 to state 0000.

### Serial VS Parallel Counter



Output of 4<sup>th</sup> AND gate depends on the outputs of all previous AND gates. i.e. Delay of four AND Gates being accumulated.

**1.** <u>Arbitrary Count Sequence:</u> Design a synchronous counter which follows sequence given below:

0, 2, 4, 6, 8, 0, 2, ...

2. <u>BCD Counter:</u> Design a BCD synchronous counter which follows the sequence given below:

0,1,2,3,4,5,6,7,8,9,0,1,2,...

**3.** <u>Modulo-7 Counter:</u> Which follows the sequence 0,1,2,3,4,5,6,0,1,2,...

#### 4. Digital Watch

For your convenience consider we have 64 seconds in one minute, 64 minutes in one hour and total 32 hours in a day.

#### 5. Automatic Parking Control

Take Carln and CarOut signals from sensors at Entry and Exit Gates respectively. Parking area has total capacity of 32 cars, when total count of cars in the plaza reaches 32 lock the Entry Door otherwise the door will remain unlocked.

#### 6. Counter with Parallel Load

Register composed of **D Flip-Flops** which loads the data if Load = 1 otherwise behaves like a binary counter.

**7.** Counter composed of **D Flip-Flops** which takes X and Y selection inputs and performs following operations:

X	Y	Operation
0	0	Count
0	1	Shift Right
1	0	Shift Left
1	1	Parallel Load