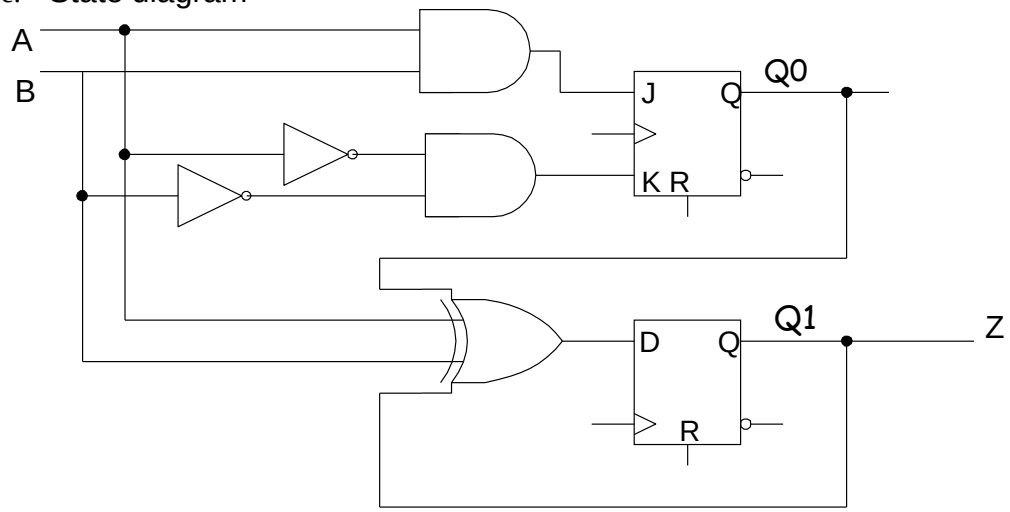
LAB - 10

Objective: Student should understand how to design a sequential circuit given its specifications in sentence structure or state diagram or state table form. Furthermore understand the use of shift registers.

TASK #1: Analyze the given sequential circuit. Fill the table given below and mention the following:

a. Input equations
b. Output equations
c. Excitation equations
d. Next state equations
e. State diagram



Current States		Inputs		Next States		Output
Q0	Q1	A	B	Q0 (t+1)	Q1 (t+1)	Z

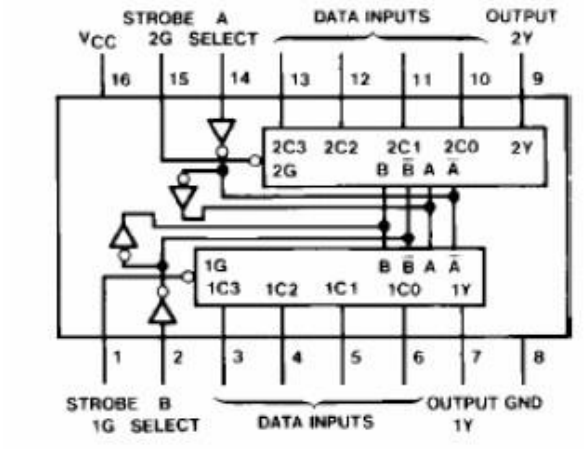
Task #2: Implement a synchronous up-down counter using flip flop on logic trainer.

Task #3: Draw the logic diagram of a shift register with D flip flops with mode selection inputs S1 and S0 and implement the circuit on the breadboard. The shift register is to be operated according to the following function table. One stage of this register should contain a 4-to-1 line MUX and a D-type flip-flop.

Mode Selection		**Register Operations**
S1	**S0**	
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load data

4 to 1 Mux:

Connection Diagram

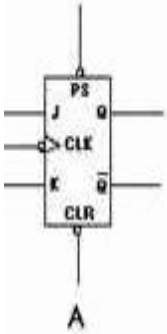


Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = HIGH Level
L = LOW Level
X = Don't Care

JK FLIP FLOP

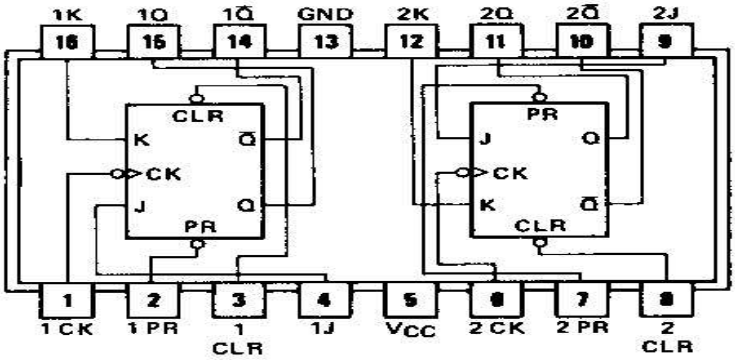


	INPUTS					OUTPUTS	
	PRESET	CLEAR	CLOCK	J	K	Q	Q̄
1	0	0	X	X	X	1	1
2	0	1	X	X	X	1	0
3	1	0	X	X	X	0	1
4	1	1	↓	0	0	0	Q̄
5	1	1	↓	1	0	1	0
6	1	1	↓	0	1	0	1
7	1	1	↓	1	1	TOGGLE	
8	1	1	0	X	X	Q	Q̄

X = IRRELEVANT

B

7476



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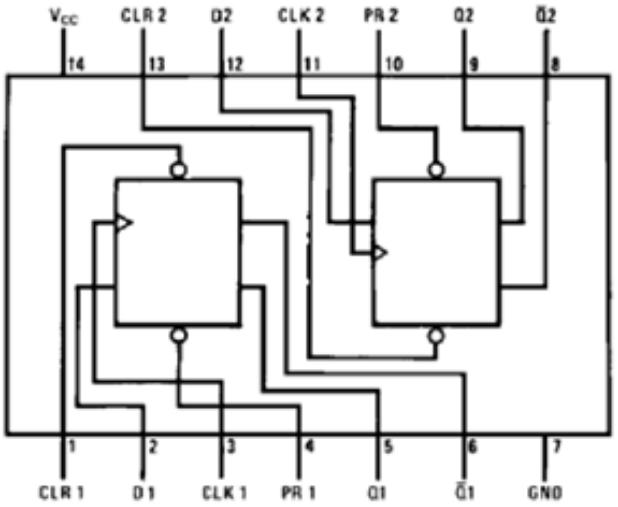
Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

Connection Diagram



Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Logic Level

X = Either LOW or HIGH Logic Level

L = LOW Logic Level

↑ = Positive-going Transition

Q_0 = The output logic level of Q before the indicated input conditions were established.

Note 1: This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (HIGH) level.