National University of Computer and Emerging Sciences, Lahore Campus

Course:	Digital Logic Design	Course Code:	EE1005
Program:	BS(Computer Science/ Data Science/Robotics except BSR-2E)	Semester:	Spring 2023
Duration:	60 Minutes	Total Marks:	50
Paper Date:	10/04/2023	Weight	15%
Section:	ALL	Page(s):	6
Exam:	Midterm-2 Solution	Roll No.	_____
		Section:	

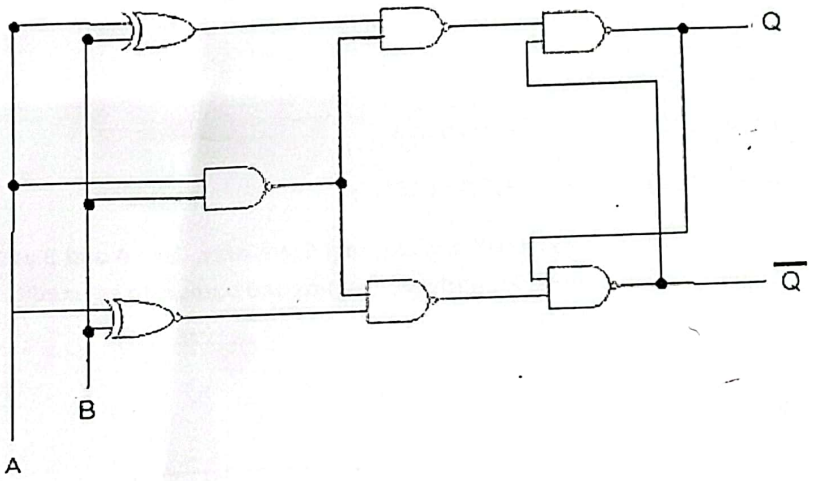
Instruction/Notes:
- *Attempt all the questions in the space provided to you in this answer booklet.*
- *Extra rough sheets are NOT ALLOWED.*
- *Draw neat circuits.*

Question 1 [8 + 8= 16 Marks]: Latches [CLO 5]

Marks	
CLO 4 (34)	CLO 5 (16)

a) Fill in the characteristic table of A-B Latch circuit given below.

Q(t)	A	B	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



b) Fill in the reduced characteristic table of A-B Latch.

A	B	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	Q(t), Mem

Roll #

Question 2 [10+10 = 20 Marks]: Decoders and Multiplexers [CLO 4]

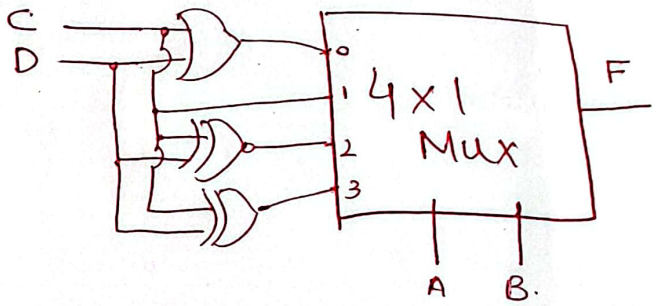
Input				Output
A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Implement the function given below

F (A, B, C, D) = ∑m(1,2,3,6,7,8,11,13,14)

(a) **Using a 4x1 MUX and external Gates only. Take A and B as Selection Inputs and C and D a Data Inputs. Properly label inputs and outputs to get credit.**

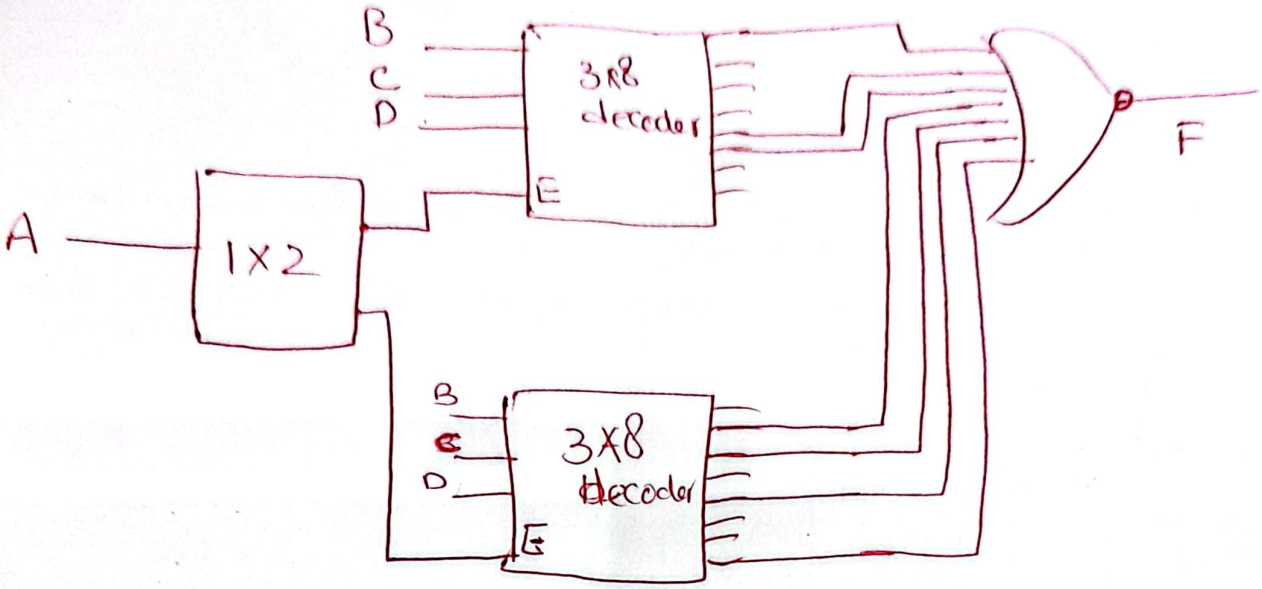
$I_0 = C + D$, $I_1 = C$, ~~$I_2 = C \odot D$~~ $I_2 = C \odot D$, $I_3 = C \oplus D$



Course:
Program

Roll #_____

(b) Using 3-to-8-line decoders, 1-to-2 line decoder and one NOR gate. Properly label inputs and outputs to get credit.



[CLO 4]

Question 3 [14 Marks]: Design

We have to design a machine that takes two 2-bit numbers A(A_1A_0) and B(B_1B_0) and two selection signals M_1M_0 as inputs and produces result R as the output according to the following functionality:

M1	M0	Operation	Description
0	0	R= A + B	Adds A and B
0	1	R= A – B	Subtract B from A
1	X	R= A * 2	Doubles A

Your task is to make a fully functional machine. Properly show the flow of data and label all blocks and inputs/outputs to get credit.

You have to design the machine using Decoder(s) block, Adder-Subtractor(s) block and additional gates required (Detailed gate implementation of Decoder(s) blocks and Adder-Subtractor(s) blocks are not required. Also mention the sizes of decoder block and Adder/Subtractor block used).