Department of Computer Science
National University of Computer and Emerging Sciences
Lahore Campus

Course Outline Digital Logic Design EE1005
Spring 2023

Instructor Name: Tazeem Haider
Email address: tazeem.haider@nu.edu.pk
Program: BS
Credit Hours: 3+1
Type: Core
Course Group: DLD-Spring 2023
Class Code:
TA:
Office Hours: Tuesday 11:30 to 12:30, Wednesday 2:00 – 3:00pm
Class timings: Monday & Wednesday 10:00-11:30 (Section A)
Tuesday & Thursday 01:00-2:30 (Section B)
Monday & Wednesday 11:30-01:00 (Section C)

Course Description/Objectives/Goals:

This course introduces the fundamentals of digital computers. It covers the design and analysis techniques for digital circuits – combinational as well as sequential.

Course Learning Outcomes (CLOs):
1. Understand different number systems and their conversion.
2. Recognize and use basic gates to implement logic circuits
3. Constructs optimized logic circuit design
4. Construct and utilize the basic functional blocks to design combinational circuits
5. Design and demonstrate synchronous/ asynchronous

Textbook Name: M. Morris Mano & Charles R. Kime, *Logic and Computer Design Fundamentals* Edition: (5th Edition Updated, Prentice Hall)

Additional Reference Material Used (if any):

1. John F. Wakerly, *Digital Design: Principles and Practices* (5th Edition, Pearson Education, 2001)
2. Thomas L. Floyd, Digital Fundamentals (7th Edition, Prentice Hall, 2000)

Percentage Grade Distribution:

QUIZZES	**15%**
MIDTERMS	**30%**
FINAL	**45%**
ASSIGNMENTS	**10%**

Lec.No.	Course Contents Covered
1	1. Information Representation, Digital Computer 2. Number Systems (Binary, Octal, Hex) and Conversions 3. Data Ranges, Conventions (KB, MB, GB)
2	1. BCD 2. ASCII Code 3. Parity Bit 4. Arithmetic Operations (Addition, Subtraction using borrow method, Multiplication)
3	1. Signed Unsiged Binary Numbers 2. Signed Magnitude Representation 3. 2's Complement Representation 4. 1's Complement 5. Subtraction using 2's Complement
4	1. Logic Gates 2. Timing Diagram 3. Gate Delay 4. Boolean Equation, Logic Circuit, Truth Table 5. Boolean Identities and Laws (Commutative etc.) 6. Dual and Duality Principle 7. Proof of Distributive Law and Consensus Theorem 8. Complementing Function using DE Morgan's Law and Dual
5	1. Boolean Functions and their implementation • Definition of Combinational logic circuit. • Examples of making truth table and circuit diagram from Boolean equation. 2. Dual of a function 3. Complement of a function 4. Dual vs complement 5. Practice of questions reducing to particular number of literals. 6. Implementing functions with only OR and NOT gates. 7. Implementing functions with only AND and NOT gates.
6	1. Canonical and Standard Forms (Minterms, Maxterms, Conversions) • How to write minterms/maxterms from truth table • Writing a function in terms of its minterms/maxterms • Properties of minterms /maxterms. 2. Literal cost 3. Gate input cost
7	1. Minimization of Boolean functions using K-Map • How to build table and why there should be a difference of 1 between 2 cells? • 2 variables • 3 variables
8	1. Minimization of Boolean functions using K-Map 2. Implicants, prime implicants, essential prime implicants, Non essential Prime implicants (just introduction)

	3. 4 variables 4. 5 variables (just table) 5. Don't Care States
9	Universal gates, XOR, XNOR, Parity Generators/ Checkers
10	1. Implementation of Boolean functions using universal gates 2. Combinational circuits 3. Design Procedure • a circuit that accepts 3-bit number and generates a 6 bit binary number equal to square of the given number • Code convertors • 2 bit multiplier • BCD numbers • BCD to 7 segment display
11	Mid I
12	1. Decoders + Examples • 1-to -2 line decoder • 2-to -4 line decoder • 3-to -8 line decoder 2. Decoders with enable input 3. Encoders 4. Priority encoder • BCD to decimal example. 5. Decoders and combinational circuits
13	• Forming larger size decoder from smaller one (3-to-8 line decoder from 1-to -2 line decoders and 2-to -4 line decoders)
14	1. Multiplexers + Examples • 2x1 Mux • 4x1 Mux • 8x1 Mux 2. Dual and Quad MUX 3. Forming functions using decoders and multiplexer. 4. Demultiplexer + Examples
15	1. Forming larger size MUX from smaller one
16	1. Binary Adders • Half Adder • Full Adders • Binary Ripple Carry Adder • Binary Multipliers
17	1. 1's and 2's Complements 2. Binary Adder/Subtractor 3. BCD Adder 4. 2-bit magnitude comparator
18	1. Introduction to Sequential Circuits 2. Introduction to Latches • SR Latch

	• S'R' Latch • SR Latch with a control • Timing Diagram with Latches
19	• Introduction to Flip Flops • how flip flops are different from latches • why we use flip flops • D Flip flop
20	1. Types of flip flop • Edge triggered Flip flop • JK flip flop • Characteristic table and equations of D and JK flip flop.
21	1. Flip-Flops with Direct Inputs 2. Sequential Analysis With examples 3. Given the circuit generate the state diagram
22	Mid II
23	Some more examples of Sequential Design (given the circuit generate the state diagram)
24	1. Given description form state diagram and design the circuit 2. Excitation tables for flip flops, D and JK.
25	Sequential circuit design practice problems. 4.13, 4.14, 4.15
26	1. Registers implementation with flip flops 2. 4 bit register with parallel load
27	1. Shift register 2. Serial addition with registers 3. Shift register with parallel load 4. Bidirectional Shift Register 5. Serial In/Parallel Out
28	1. Microoperations, Register Transfers (briefly) 2. Counters (synchronous and asynchronous) 3. 4 bit Ripple counter
29	1. Serial and Parallel Counters 2. Parallel gating counter 3. upward and downward counters
30	1. RAM, ROM 2. Memory Access • Random Access • Sequential Access 3. RAM Operation • Read • Write 4. Chip select option in RAMS.

Grading Scheme: Absolute

Absolute Grading Scher

Total Marks (%)	Gra
≥ 90	A+
86-89	A
82-85	A-
78-81	B+
74-77	B
70-73	B-
66-69	C+
62-65	C
58-61	C-

Rules:

1. Plagiarism is not tolerable in any form. Cheating in any respect will be treated as a big crime and your cases will be forwarded to DC. It is the responsibility of the student to protect their assignments from being copied. In case of cheating, both parties will be considered equally responsible.
2. Eligibility to pass this course, students should have to get at least 50% marks and 80% attendance.
3. Assignments should be submitted in due time.
4. Quizzes can be unannounced, covering contents of last two lectures. There will be no makeup of missed quiz.
5. Students can contest their grades on quizzes and assignments ONLY within a week of the release of grades. Exams will be available for review according to university policies.