

# National University of Computer and Emerging sciences

# **Objectives:**

- To learn and understand the working of Universal gates and XOR and XNOR gates
- SOP and POS expressions from K-map with don't care condition

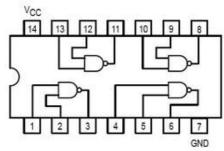
# **Introduction to NAND Gate**

74LS00 IC contains four 2-input NAND gates. The function table and connection diagram for this IC are shown below:

### **Function Table**

### **Connection Diagram:**

Inputs		Output
A	В	Y
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L



H= Logic High, L= Logic Low

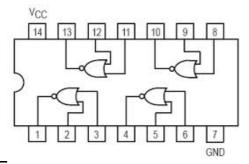
### **Introduction to NOR Gate**

74LS02 IC contains four 2-input NOR gates. The function table and connection diagram for this IC are shown below:

# **Function Table:**

#### **Connection Diagram:**

Inp	outs	Output
A	В	Y
L	L	Н
L	Н	L
Н	L	L
Н	Н	L



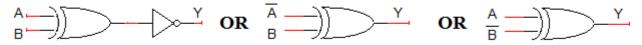
H= Logic High, L= Logic Low

### **Exclusive-OR & Exclusive-NOR gates:**

The figure given below shows the symbol of Exclusive-OR (XOR) and Exclusive-NOR (XNOR) gates.



Boolean expression of XNOR gate is  $AB + \bar{A}\bar{B}$  and Boolean expression of XOR is  $\bar{A}B + A\bar{B}$ . Boolean expression of XNOR gate can be implemented using XOR gate as shown in figure below:



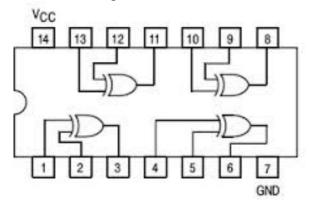
### **Function Table:**

Inputs		Output
A	В	Y
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

H= Logic High, L= Logic Low

#### **Connection Diagram:**

**74LS86 IC** will be used for implementation of XOR gate function. **74LS86 IC** contains four 2-input XOR gates. The function table and connection diagram for this IC are shown below:



### **LAB TASK#1:**

The light bulb is ON, if switch A is OFF and switch B is ON and either switch B is OFF or switch C is ON, or if switch A is ON and switch D is ON and either switch D is OFF or switch C is OFF

- a) Draw the truth table for the light bulb.
- b) Write Boolean function for the light bulb in canonical form using minterms.
- c) Write Boolean function for the light bulb in canonical form using maxterms.
- d) Find minimal SOP expression for the light bulb using K-map. Draw K-map in the space given below:
- e) Fill the following table 4-1 in order to determine the gate cost for the implementation of Boolean function for the light bulb found in part (d).

IC type	Required No. of Gates	Gates per IC	Required No. of ICs

- f) Find minimal POS expression for the light bulb using K-map. Draw K-map in the space
- g) Fill the following table 4-2 in order to determine the gate cost for the implementation of Boolean function for the light bulb found in part (f)

IC type	Required No. of Gates	Gates per IC	Required No. of ICs

- h) Find Boolean expression (mixed form) for the light bulb which is neither SOP nor POS expression
- i) Fill the following table 4-3 in order to determine the gate cost for the implementation of Boolean function for the light bulb found in part (h).

IC type	Required No. of Gates	Gates per IC	Required No. of ICs

j) Implement the cost effective expression. Write the Boolean expression you have chosen to be cost effective in the space given below along with its logic diagram. Give proper reasoning for the chosen expression.

#### LAB TASK#2:

For t	the Boolean functi	on $F1(w, x, y, z) = \sum_{i=1}^{n} f(x_i, x_i, y_i, z_i)$	$\sum m(0,1,2)$	2,3,7,8	, 10) wi	th don't	care	condition
	$(x, y, z) = \sum (5,6,11,1)$	5) do the following:						
a)	Find truth table							
b)	Find minimal <b>SOP</b> e	vnraggion for Poolagn	function	F1 115	ing V ma	n Drovy V	moni	in the space
U)	given below	xpression for boolean	Tunction	r i us	ilig K-ilia	p. Diaw K	-map i	in the space
	given below							
	Fill the following to	ble in order to detern	aina tha d	roto oo	est for the	imploman	tation	of Poolson
c)	function $F1$ found in	ble in order to detern	illie tile §	gate co	st for the	impiemen	tation	oi boolean
	Tunction 7 1 found in	part (0)						
						1		
		IC type	Required No. of	Gates	Required			
		31	Gates	per IC	No. of ICs			
		Total no. of	IC <sub>a</sub>					
		Total no. of	ics					
d)	Find minimal <b>POS</b> e	xpression for Boolean	function	<i>F</i> 1 us	ing K-ma	n. Draw K	-map i	n the space
/	given below	r			<b>8</b>	r		· · · · · · · · · · · · · · · · · · ·
e)	Fill the following tal	ble in order to detern	nine the g	gate co	st for the	implemen	tation	of Boolean
	function for $F1$ found	in part (d)						
			Required			1		
		IC type	Required No. of	Gates per IC	Required No. of ICs			
			Gates					

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### **LAB TASK#3:**

For the Boolean function  $F2(A, B, C, D) = \prod M(9,13,15)$  do the following:

- a) Draw the truth table
- b) Find minimal SOP expression for Boolean function F2 using K-map. Draw K-map. Implement it using NAND gate.
- c) Fill the following table 4-7 in order to determine the gate cost for the implementation of Boolean function F2 found in part (b)

IC type	Required No. of Gates	Gates per IC	Required No. of ICs

- d) Find minimal POS expression for Boolean function F2 using K-map. Draw K-map.
- e) Fill the following table 4-8 in order to determine the gate cost for the implementation of Boolean function for F2 found in part (d).

IC type	Required No. of Gates	Gates per IC	Required No. of ICs

- f) Find minimal expression (mixed form) for Boolean function F2 which is neither SOP nor POS expression.
- g) Fill the following table 4-9 in order to determine the gate cost for the implementation of Boolean function F2 found in part (f)

IC type	Required No. of Gates	Gates per IC	Required No. of ICs