

## Question no. 1

Consider a cache that can store 4 words,

Consider a Main Memory of 64 words

For the following addresses of RAM accesses,  
find the hits and misses using direct mapping:

10, 12, 10, 12, 63, 58, 34, 10, 34, 63, 33, 10, 63

$$\text{No. of bits of Main Memory Address} = \log_2(64) \\ = 6 \text{ bits}$$

$$\text{No. of bits of Tag} = \log_2(64/4) = 4 \text{ bits}$$

$$\text{No. of bits of Index} = 6 \text{ bits} - 4 \text{ bits} = 2 \text{ bits}$$

$$\underline{\underline{10}} \text{ (Miss)}$$
$$4 \overline{) \begin{array}{r} 2 \\ 10 \\ 8 \\ 2 \end{array}}$$

$$\text{Tag} = 10/4 = 2 = 0010$$

$$\text{Index} = 10 \% 4 = 2 = 10$$

$$\text{Address} = \begin{array}{cc} 0010 & 10 \\ \hline T & I \end{array}$$

$$\underline{\underline{12}} \text{ (Miss)}$$

$$\text{Tag} = 12/4 = 3 = 0011$$

$$\text{Index} = 0 = 00$$

$$\text{Address} = 001100$$

10 (Hit)

12 (Hit)

63 (Miss)

$$\text{Tag} = 63/4 = 15 = 1111$$

$$\text{Index} = 63 \% 4 = 3 = 11$$

Address = 111111

58 (Miss)

$$\text{Tag} = 58/4 = 14 = 1110$$

$$\text{Index} = 58 \% 4 = 2 = 10$$

Address = 111010

34 (Miss)

$$\text{Tag} = 34/4 = 8 = 1000$$

$$\text{Index} = 34 \% 4 = 2 = 10$$

Address = 100010

10 (Miss)

34 (~~Hit~~) (Miss)

63 (Hit)

33 (Miss)

$$\text{Tag} = 33/4 = 8 = 1000$$

$$\text{Index} = 33 \% 4 = 1 = 01$$

Address = 100001

10 (~~Hit~~) (Miss)

63 (Hit)

	Tag	Data	Value Bit
0 = 00	0011	12	0
1 = 01	1000	33	0
2 = 10	<del>0010</del> <del>1110</del> 1000 <del>0010</del> 1000 0010	<del>10</del> 58 34 10 34 10	0
3 = 11	1111	63	0

Question: 2

Find the hits and misses using Associative Mapping:

(LRU) is used as replacement policy

No. of Tag bits =  $\log_2(64) = 6$  bits

10 (Miss)   12 (Miss)   10 (Hit)   12 (Hit)   63 (Miss)  
 58 (Miss)   34 (Miss)   10 (Miss)   34 (Hit)   63 (Hit)  
33 (Miss)   10 (Hit)   63 (Hit)

	Tag	Data	Value Bit
00	<del>001010</del> 100010	<del>10</del> 34	0
01	<del>001100</del> 001010	<del>12</del> 10	0
10	111111	63	0
11	<del>111010</del> 100001	<del>58</del> 33	0



Question : 3

$$\text{Set bits} = 1 = \log_2(2)$$

$$\text{Tag bits} = 5$$

Find the hits and misses using 2 way set associative mapping:

(LRU) is used as replacement policy

10 (Miss)   12 (Miss)   10 (Hit)   12 (Hit)   63 (Miss)

58 (Miss)   34 (Miss)   10 (Miss)   34 (Hit)   63 (Hit)

33 (Miss)   10 (Hit)   63 (Hit)

Index bits = 2  
Tag bits = 4

Here size of cache is 4

No. of sets =  $\frac{4}{2} = 2$  set  
 $\rightarrow$  2way Associative

Here we use  $k \bmod n$   
Address  $\rightarrow$  no. of set:

	S1			S2		
	Tag	Data	Value Bit	Tag	Data	Value Bit
00	0011	12	0			
01	1000	33	0			
10	<del>0010</del> 1000	<del>10</del> 34	0	<del>1110</del> 0010	<del>58</del> 10	0
11	1111	63	0			

Set	Tag	Data	Value Bit	Tag	Data	Value Bit
0	<del>00101</del> <del>11100</del> 00101	<del>10</del> 34 10	0	<del>00110</del> 10001	<del>12</del> 34	0
1	11111	63	0	10000	33	0