Experiment 4

EE24MTECH12008
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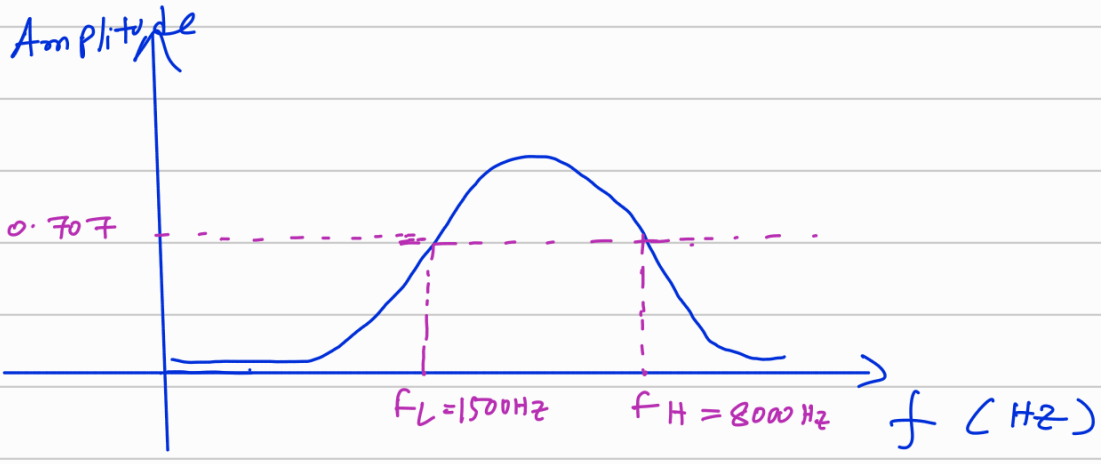
Design a band pass filter with the following specifications

Sampling frequency = 48000 Hz
f_{stop1} = 500Hz
f_{pass1} = 1500Hz
f_{pass2} = 8000 Hz
f_{stop2} = 9000 Hz

With the above specifications

→ The filter will allow frequencies between 1500 Hz and 8000 Hz

→ The filter will reject the frequencies below 500 Hz and above 9000 Hz

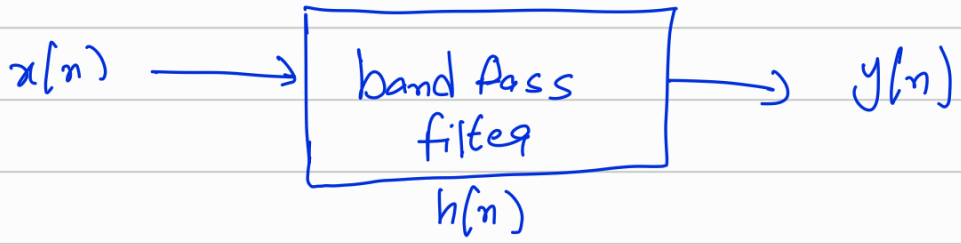


f_L = lower cutoff frequency = 1500Hz
f_H = upper Cutoff frequency = 8000 Hz

Generate the filter coefficients of the band pass filter from matlab with the above specifications

let $h(n)$ be the system response

let $x(n)$ be the input signal of length L and $h(n)$ be the system response of length M



$$y(n) = x(n) * h(n) = \sum_{k=0}^{L-1} x(k)\, h(n-k)$$

$n = 0$ to $L+M-1$

This in matlab can be implement using "conv" command which will do the convolution of two signals.

→ we apply a filter to the signal of length L and response length M. the output signal we should take from $\frac{M}{2}$ to $\frac{M}{2}+L$

i.e $y(n) = x(n) * h(n)$

$y'(n) = y\left[\frac{M}{2} : \frac{M}{2}+L\right]$

→ Inorder to have the propes output of the filter we should make sure that $\boxed{L \geq M}$

Implementing FIR filter in Verilog

In Verilog we cannot have inbuilt Conv functions for Computing the Convolution so we need to Come up with Some algoritum to design FIR filter in Verilog.

$x[n]$ → input signal of length N
$h[n]$ → filter response of length M

$y[n]$ → output of length $N+M-1$

Consider a shift register of length N
$s[n]$

initially set the shift register to 1
$s[1:N] = 1$

```
idx = 1
for n = 1 to N+M-1
    s[2:N] = s[1:N-1]
    s[1] = x[n]

    buffer(1) = s(1) * h(1)
    for i = 2 to N
        buffer[i] = buffer[i-1] + s[i] * h(i)
    end
    if idx < N
        y(n) = buffer(idx)
        idx = idx + 1
```

```
    end
    else
        y(n) = buffer[idx]
    end
end
```

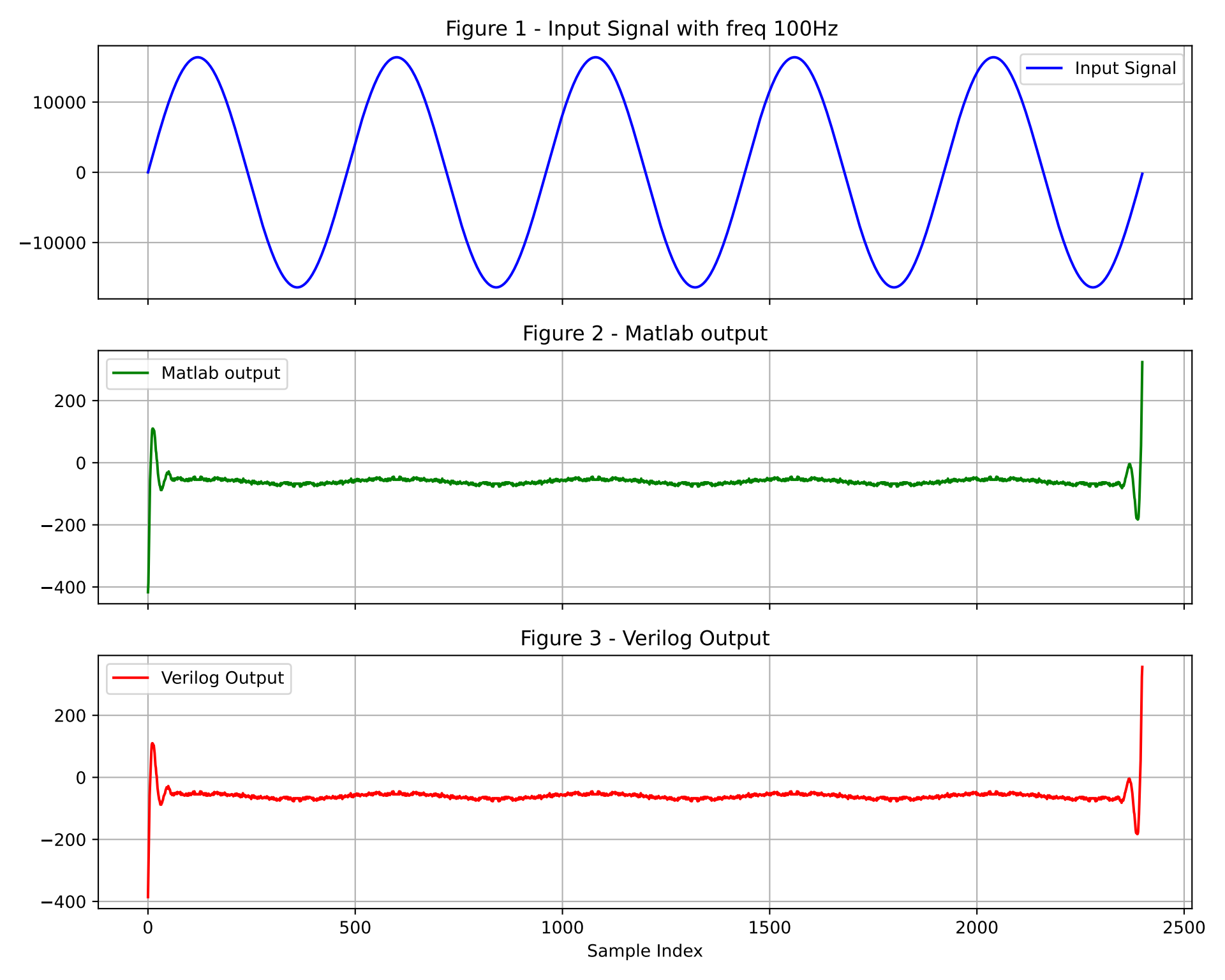


Figure 1 - Input Signal with freq 100Hz
Input Signal
10000
0
−10000
Figure 2 - Matlab output
Matlab output
200
0
−200
−400
Figure 3 - Verilog Output
Verilog Output
200
0
−200
−400
0
500
1000
1500
2000
2500
Sample Index

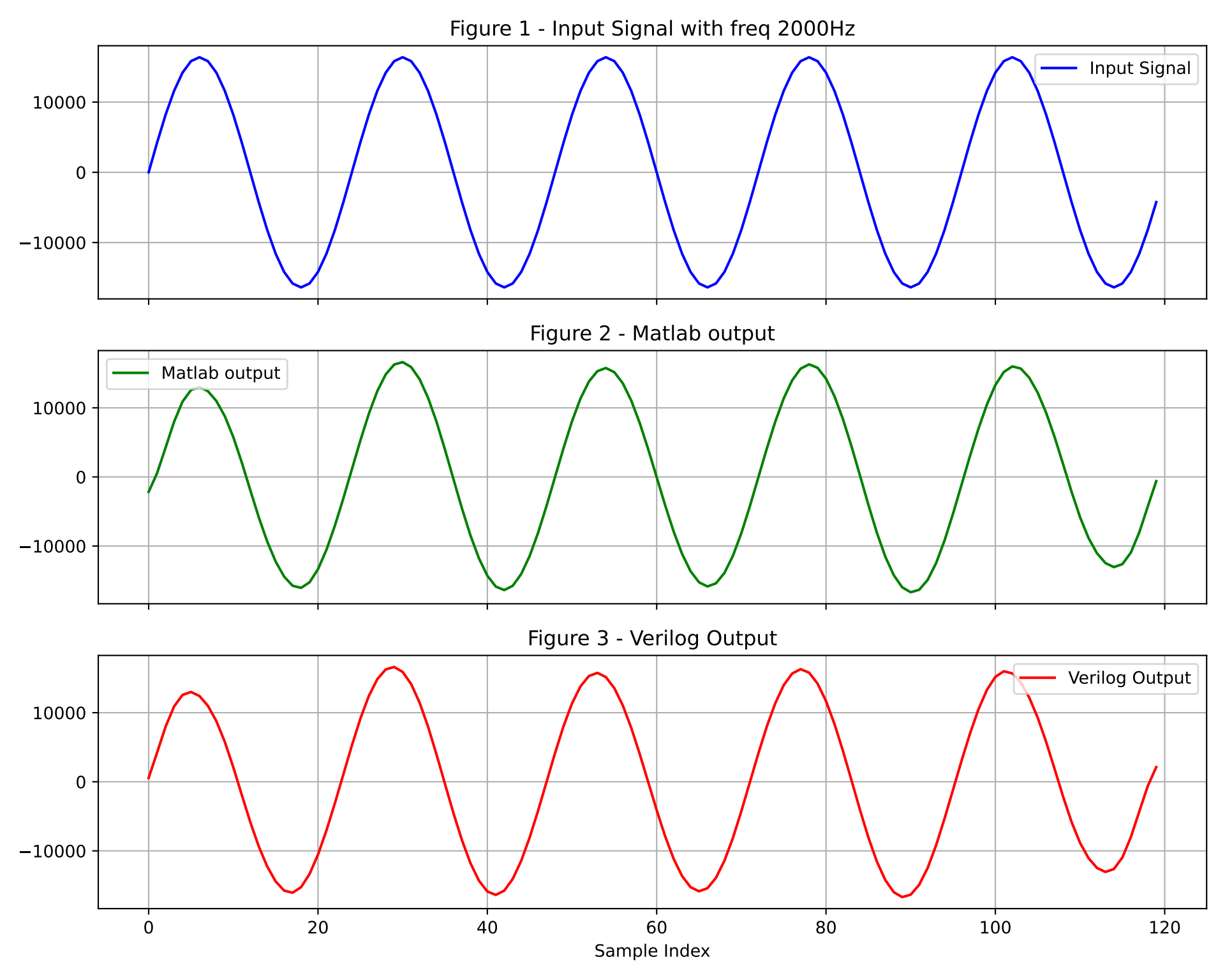


Figure 1 - Input Signal with freq 2000Hz
Input Signal
10000
0
−10000
Figure 2 - Matlab output
Matlab output
10000
0
−10000
Figure 3 - Verilog Output
Verilog Output
10000
0
−10000
0
20
40
60
80
100
120
Sample Index

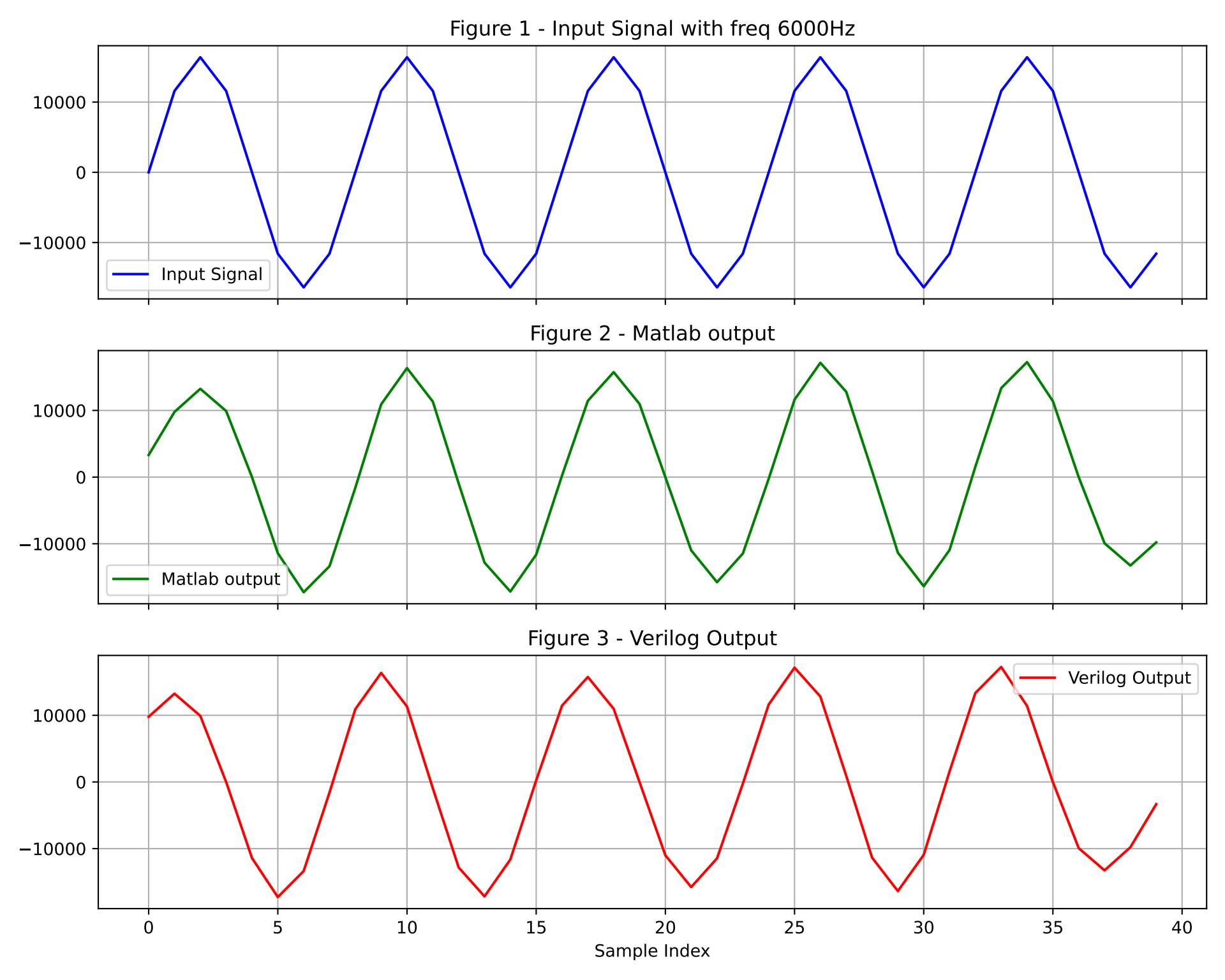


Figure 1 - Input Signal with freq 6000Hz
10000
0
−10000
Input Signal
Figure 2 - Matlab output
10000
0
−10000
Matlab output
Figure 3 - Verilog Output
10000
0
−10000
Verilog Output
0
5
10
15
20
25
30
35
40
Sample Index

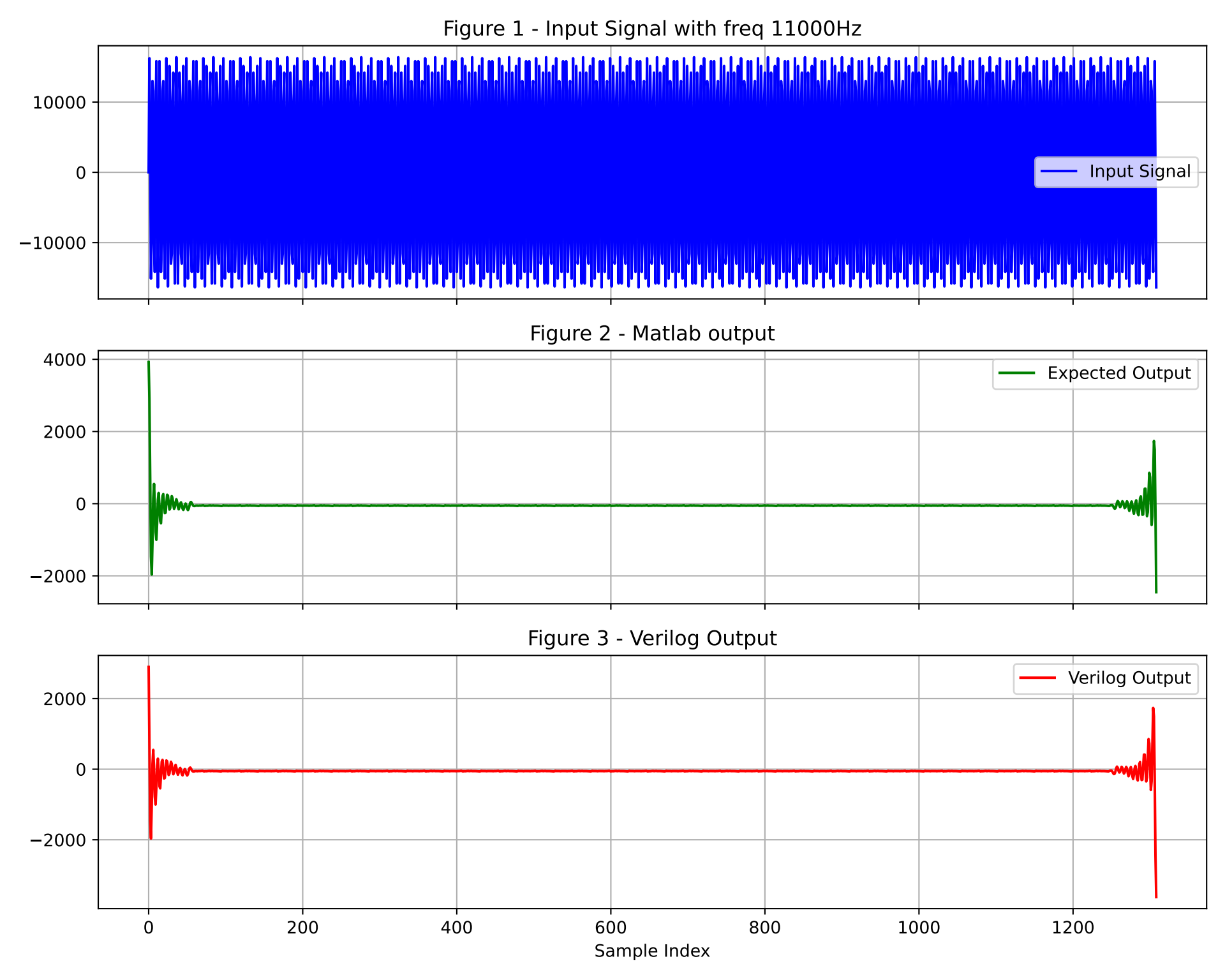


Figure 1 - Input Signal with freq 11000Hz
10000
0
−10000
Input Signal
Figure 2 - Matlab output
4000
2000
0
−2000
Expected Output
Figure 3 - Verilog Output
2000
0
−2000
Verilog Output
0
200
400
600
800
1000
1200
Sample Index