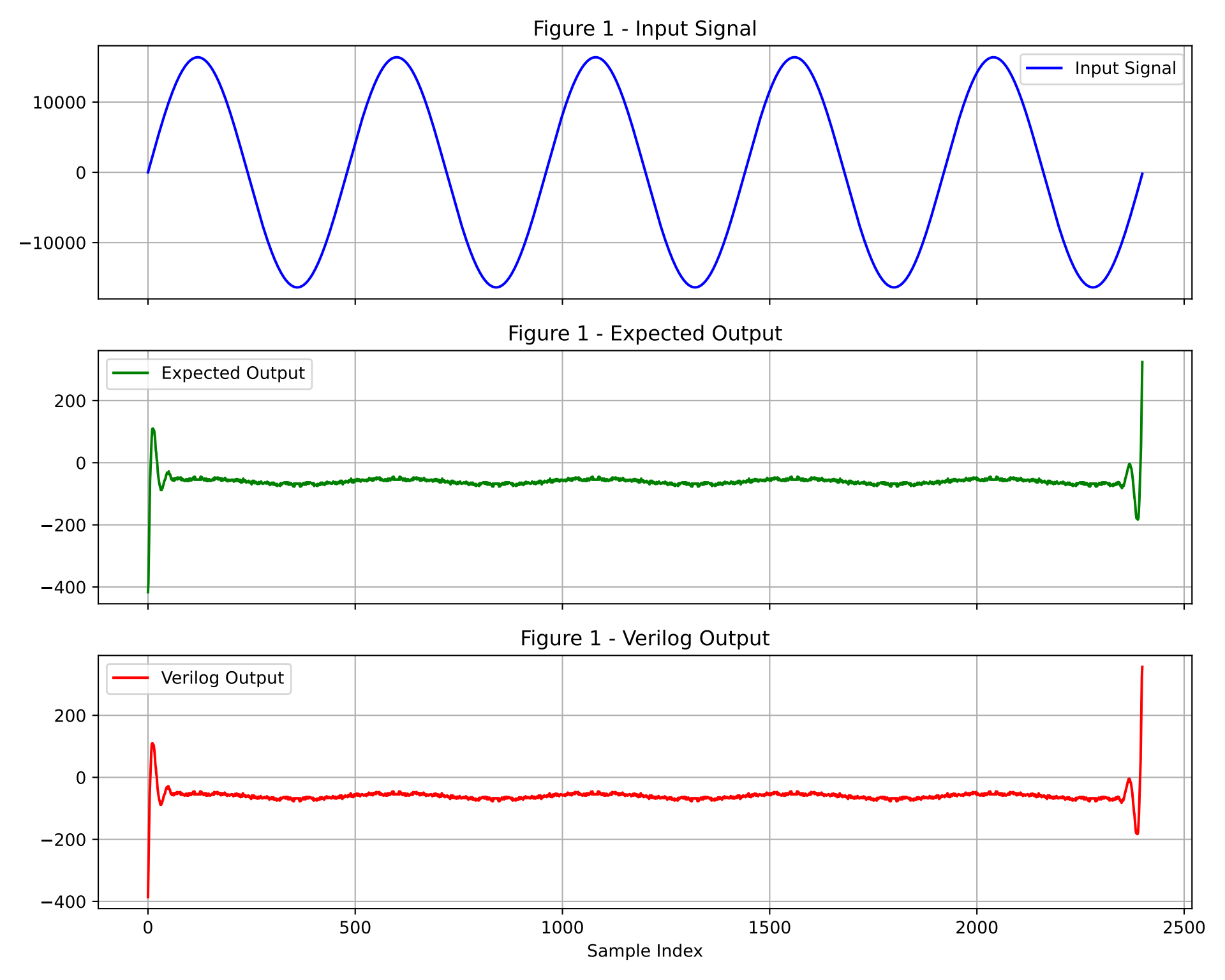
Figure 1 - Input Signal
Input Signal
10000
0
−10000
Figure 1 - Expected Output
Expected Output
200
0
−200
−400
Figure 1 - Verilog Output
Verilog Output
200
0
−200
−400
0
500
1000
1500
2000
2500
Sample Index

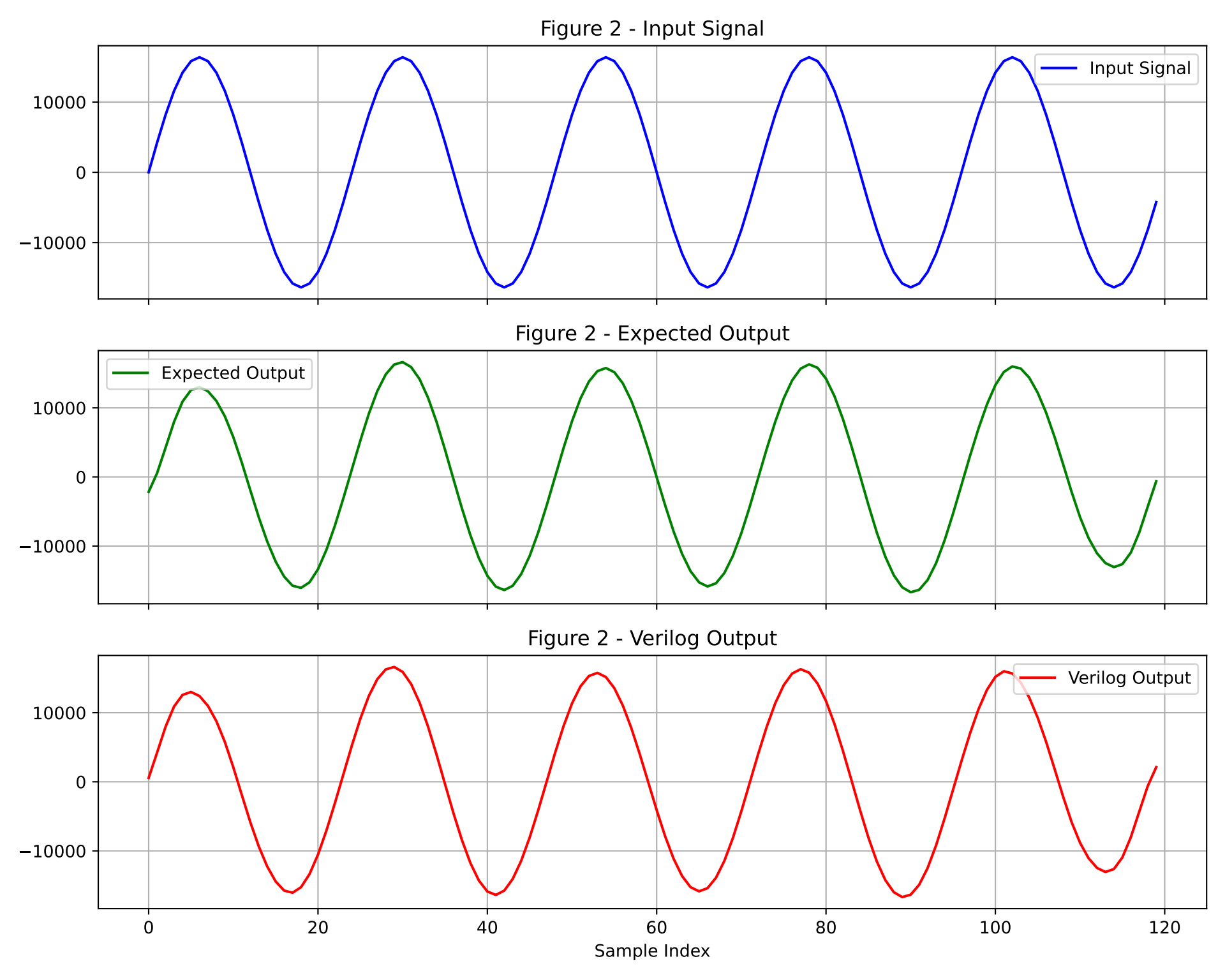
Figure 2 - Input Signal
Input Signal
10000
0
−10000
Figure 2 - Expected Output
Expected Output
10000
0
−10000
Figure 2 - Verilog Output
Verilog Output
10000
0
−10000
0
20
40
60
80
100
120
Sample Index

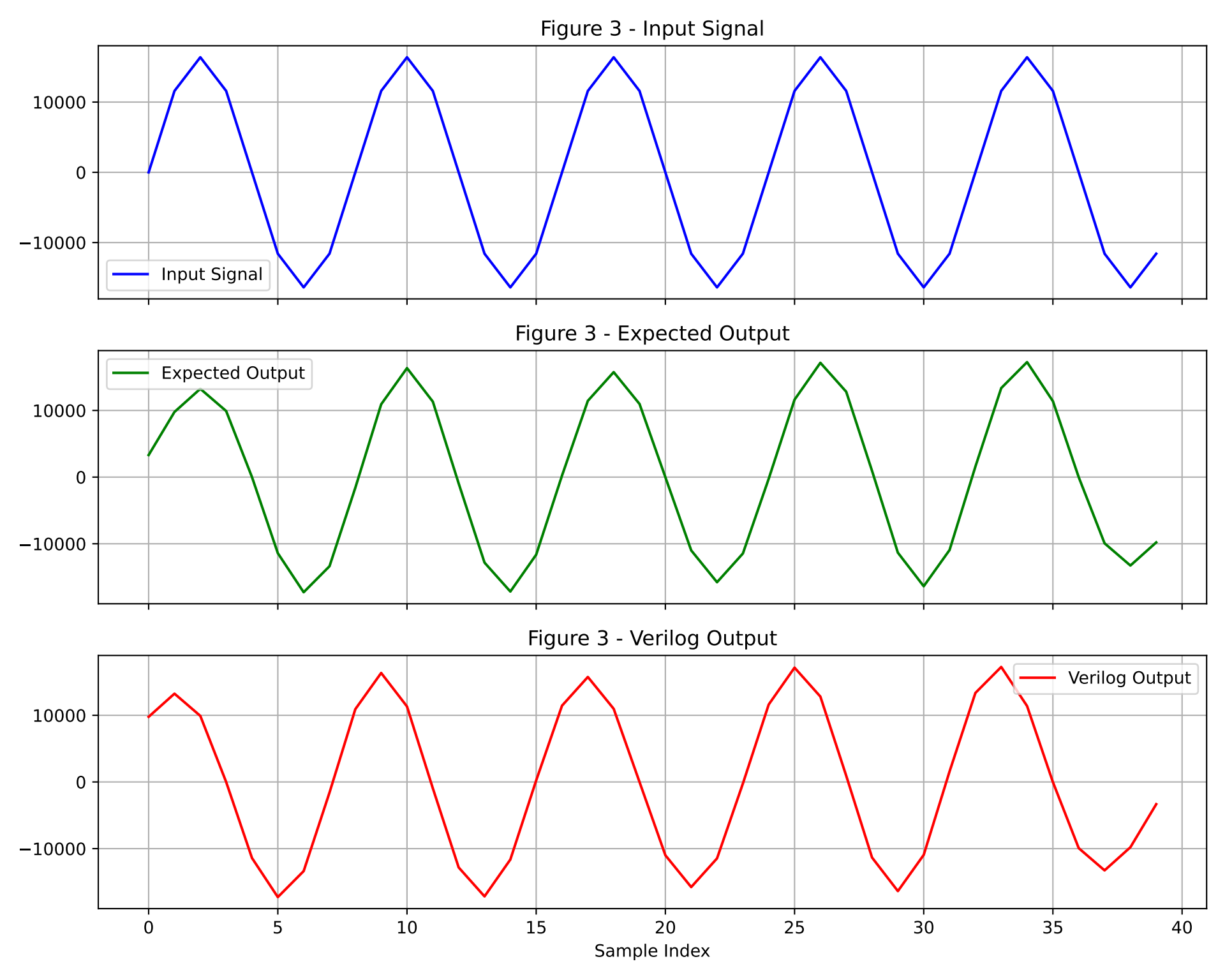
Figure 3 - Input Signal
10000
0
−10000
Input Signal
Figure 3 - Expected Output
Expected Output
Figure 3 - Verilog Output
Verilog Output
0
5
10
15
20
25
30
35
40
Sample Index

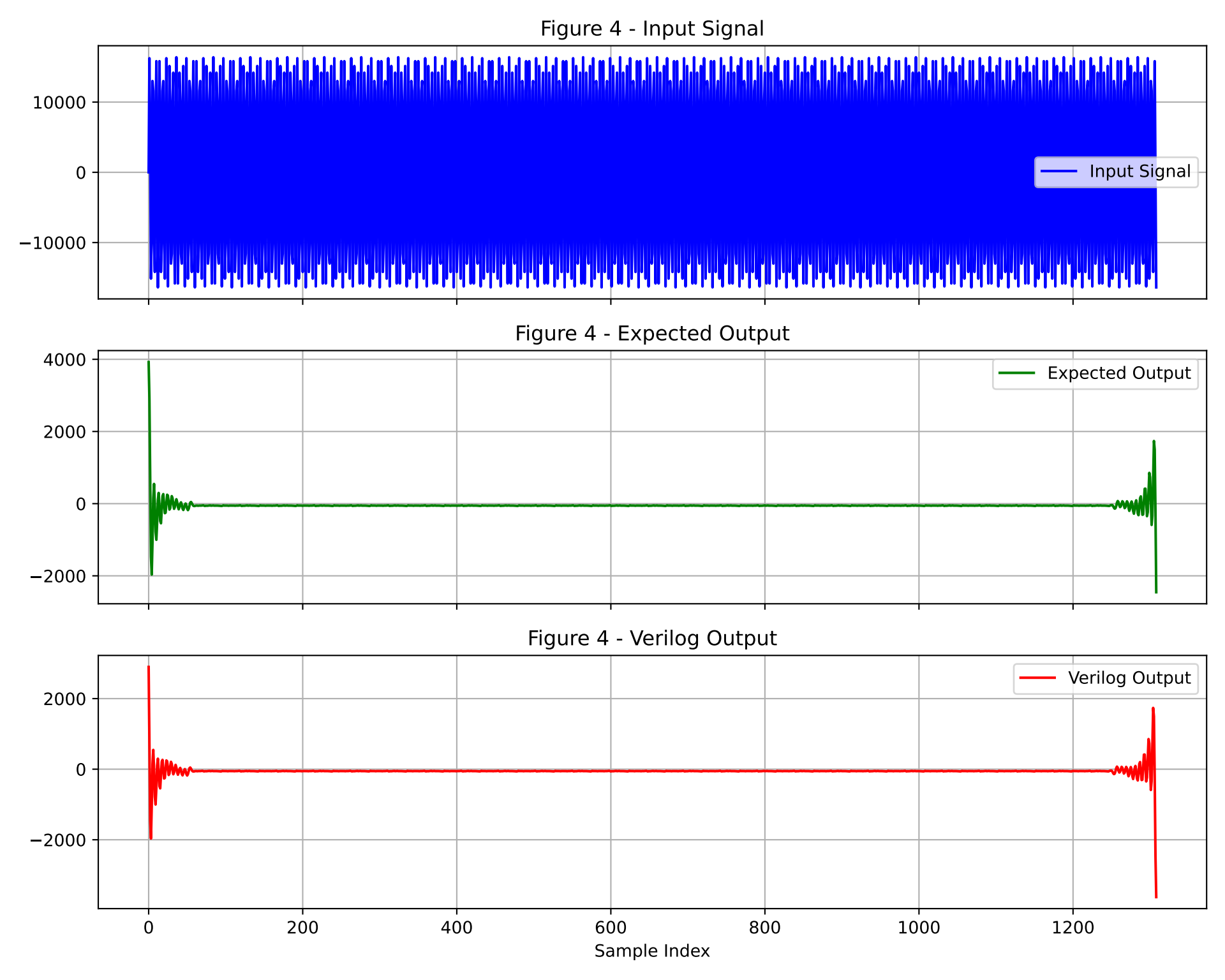
Figure 4 - Input Signal
10000
0
−10000
Input Signal
Figure 4 - Expected Output
4000
2000
0
−2000
Expected Output
Figure 4 - Verilog Output
2000
0
−2000
Verilog Output
0
200
400
600
800
1000
1200
Sample Index