

# INDIAN INSTITUTE OF TECHNOLOGY PATNA

## CS541: Foundations of Computer Systems

### Assignment 1 — Autumn 2023

Deadline: Oct. 29, 2023 — 23:59 Hrs IST

Maximum Marks: 10 marks

All questions are compulsory. Without proper derivation and explanation, marks will not be given. Make necessary assumptions (as and if) required and mention the same in the solution.

**Submission Guidelines:** Prepare a soft copy of your solution and store it in a folder. Then compress the folder as a rar/zip file (filename should be in this format: **roll-number\_assign1.rar or roll-number\_assign1.zip**). For example, if your roll number is 2303RES01, store your assignment as 2303RES01\_assign1.rar or 2303RES01\_assign1.zip. Use admission number instead of roll number if you are not provided with your roll number. Upload the same at the below link:

<https://forms.gle/mbJCC9zqNQVM4XYNA>

1. Consider a machine with clock frequency as 210Hz and the performance parameter [Considering 100 sample instructions] as per the table given below.

Instruction Category	Occurrence	Cycles per Instruction
ALU	60	5
Load & Store	19	3
Branch	14	4
Others	7	1

Now a separate program containing  $6 \times 10^6$  floating point instructions is executed on the same machine. Assume that the machine is either doing calculations in the CPU, or doing I/O operation, but it can't do both at the same time. Given that the total time taken by the program to complete I/O operations is 1 second and the CPU computation takes exact same overall time as the execution of the given sample 100 instructions, compute the performance of the machine in terms of MFLOPS. **[5 marks]**

2. Consider an instruction pipeline with 5 stages:  $S_1$  (IF),  $S_2$  (ID),  $S_3$  (OF),  $S_4$  (IE), and  $S_5$  (MO). Stages  $S_1$ ,  $S_2$ ,  $S_3$ , and  $S_5$  take 1 clock cycle each for any instruction. And stage  $S_4$  takes 1 clock cycle for ADD and SUB instructions, 2 clock cycles for MUL and BQEZ (Branch) instructions, and 3 clock cycles for DIV instruction respectively. Calculate the number of clock cycles needed to execute the following sequence of instructions, if the only branch is taken. **[5 marks]**

#### Instructions:

$I_0$ : ADD  $R_0, R_1, R_2$

$I_1$ : MUL  $R_3, R_4, R_5$

$I_2$ : DIV  $R_5, R_3, R_3$

$I_3$ : BQEZ  $R_3, I_5$

$I_4$ : MUL  $R_2, R_6, R_5$

$I_5$ : SUB  $R_5, R_6, R_5$

#### Meaning

$R_2 \leftarrow R_0 + R_1$

$R_5 \leftarrow R_3 \times R_4$

$R_3 \leftarrow R_5 / R_3$

if  $R_3 \geq 0$ , jump to  $I_5$

$R_5 \leftarrow R_2 \times R_6$

$R_5 \leftarrow R_5 + R_6$

**Note:** Draw the table as per the format given below:

.	.	.	.	.	.	.	.	.	...
.	.	.	.	.	.	.	.	.	...
.	.	.	.	.	.	.	.	.	...
$S_3$									...
$S_2$									...
$S_1$									...
	1	2	3	4	5	6	7	8	...