24th Day

Connecting DUT and TB via Interface

Interface

//input skew - tb samples the dut outputs before clock edgeby default #1, by default output skew is 0 no delay from tb output to dut input

```
interface sv_intf(input logic clk);

 logic rst;
 logic [4:0] in1, in2;
 logic [5:0] out;

 // Clocking block for testbench
 clocking tb_cb @(posedge clk);
  output rst, in1, in2;
  input out;
 endclocking

 // Clocking block for DUT (optional here, but not used in DUT)
 // We will access signals directly in DUT

 // Modport for DUT
  modport dut_mp(
   input clk, rst, in1, in2,
    output out);
```

```
 // Modport for TB using clocking block
 modport tb_mp(
  clocking tb_cb
 );

endinterface
```

DUT

```
`include "interface.sv"

module add_dut(sv_intf.dut_mp dut_intf);

 always @(posedge dut_intf.clk)
  begin
   if (dut_intf.rst)
    dut_intf.out <= 0;
   else
    dut_intf.out <= dut_intf.in1 + dut_intf.in2;
  end

endmodule
```

TB

```
module tb;

  logic clk = 0;
  always #5 clk = ~clk;

  sv_intf intf(clk);
  add_dut d1(intf);  // connects to modport dut_mp by default

  initial begin
    // Apply reset and test stimulus
    intf.tb_cb.rst <= 1;
    intf.tb_cb.in1 <= 5;
    intf.tb_cb.in2 <= 6;

    @intf.tb_cb; //for efecting inputs at posedge
    @intf.tb_cb; //for effecting out it have to come from dut

    $display("TB: when rst is applied in1=%0d, in2=%0d, out1=%0d", intf.in1, intf.in2,
intf.out);

    #10;
    intf.tb_cb.rst <= 0;

    repeat (5) begin
      @intf.tb_cb; // Synchronize to clocking block

      intf.tb_cb.in1 <= $urandom_range(0, 100);
      intf.tb_cb.in2 <= $urandom_range(0, 100);
```

```
    @intf.tb_cb;
    $display("TB: in1=%0d, in2=%0d, out1=%0d", intf.in1, intf.in2, intf.out);
  end

  $finish;

end

endmodule
```

Result

```
Compiler version U-2023.03-SP2_Full64; Runtime version U-2023.03-SP2_Full64;  Apr 11 10:20 2025
TB: when rst is applied in1=5, in2=6, out1=0
TB: in1=3, in2=1, out1=4
TB: in1=27, in2=26, out1=53
TB: in1=3, in2=30, out1=33
TB: in1=20, in2=16, out1=36
TB: in1=1, in2=14, out1=15
$finish called from file "testbench.sv", line 43.
$finish at simulation time                  115
          V C S   S i m u l a t i o n   R e p o r t
Time: 115 ns
CPU Time:      0.500 seconds;       Data structure size:   0.0Mb
```