42nd Day

Assertions

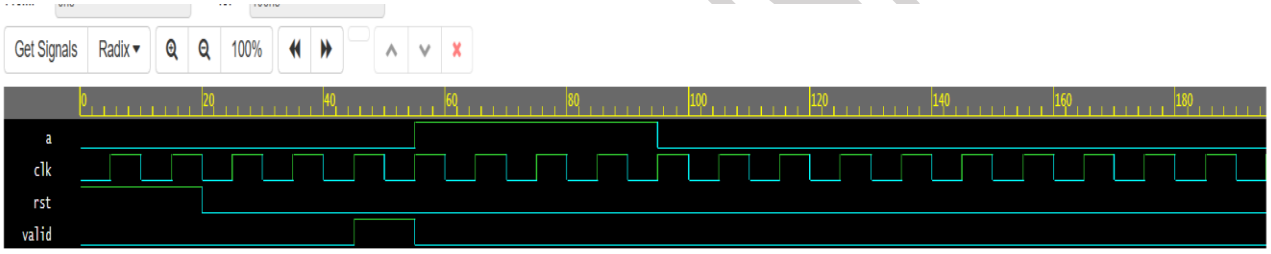
When valid high in next cycle a should be high minimum 3 clk cycles maximum 6 clock cycles

```
module tb;
  bit clk, rst, valid, a;

   always #5 clk = ~clk;

 initial begin
   rst = 1;
   valid = 0;
   a = 0;
   #20;
   rst = 0;
   #25;
   valid = 1;
   #10;
   valid = 0;
   a = 1;
   #40;
   a = 0;
 end
```

```
 initial begin
  $dumpfile("assert.vcd");
  $dumpvars(0, tb);
 end


 property p1;
  @(posedge clk)
  disable iff(rst)
  $rose(valid) |=> a[*3:6];
 endproperty


 assert property(p1)
  begin
   $display("Assertion passed at time %0t", $time);  // Success message
  end
  else
  begin
   $display("Assertion failed at time %0t", $time);  // Failure message
  end


 initial begin
  #200;
  $finish;
 end

endmodule
```

Simulation

```
Contains Synopsys proprietary information.
Compiler version U-2023.03-SP2_Full64; Runtime version U-2023.03-SP2_Full64;  May  9 10:57 2025
Assertion passed at time 85
$finish called from file "testbench.sv", line 50.
$finish at simulation time                 200
          V C S   S i m u l a t i o n   R e p o r t
Time: 200 ns
CPU Time:      0.370 seconds;       Data structure size:   0.0Mb
Fri May  9 10:57:16 2025
Finding VCD file...
```



Note: To revert to EPWave opening in a new browser window, set that option on your profile page.