17th Day

Posedge Detector

Design

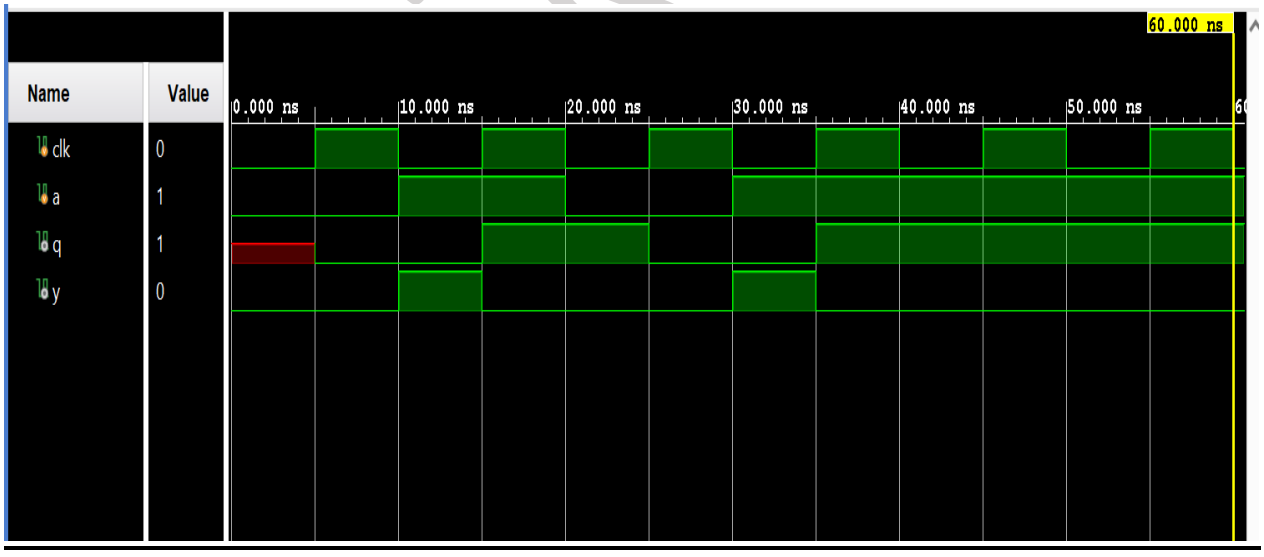
```
module posedge_detect(input clk,a,output reg q, output y);

wire y;

always @(posedge clk)
begin
q<=a;
end

assign y=a & ~q;

endmodule
```

Testbench

```
module posedge_detect_tb();

reg clk,a;
wire q;
wire y;

posedge_detect dut(clk,a,q,y);

always #5 clk=~clk;
```

```
initial
begin
clk=0;
a=0;
#10;
a=1;
#10;
a=0;
#10;
a=1;
end
endmodule
```

Simulation



Negedge Detector

Design

```
module negedge_detect(input clk,a,output reg q, output y);

wire y;

always @(posedge clk)
begin
q<=a;
end

assign y=~a & q;

endmodule
```

Testbench

```
module negedge_detect_tb();

reg clk,a;
wire q;
wire y;

negedge_detect dut(clk,a,q,y);

always #5 clk=~clk;
```

```
initial
begin
clk=0;
a=0;
#10;
a=1;
#10;
a=0;
#10;
a=1;
#10;
a=0;
#50;
$finish;
end
endmodule
```

Simulation