20th Day

Prime Detector

Design

module prime(input [3:0]a,output reg prime);

```
  always @(*)
   begin
    case(a)
     4'd2,4'd3,4'd5,4'd7,4'd11,4'd13: prime=1'b1;
     default:begin
       prime=1'b0;
      end
    endcase
   end
endmodule
```

Testbench

```
module prime_tb();
 reg [3:0]a;
 wire prime;

 prime dut(a,prime);

 initial
  begin
   repeat(20)
```

```verilog
    begin

  a=$random;

   #1;

  if(prime==1'b1)

   $display("at time=%0t, %d is prime",$time,a);


   else

   $display("at time=%0t, %d is not prime",$time, a);

   end

  end


endmodule
```

Simulation

```
at time=1,    4 is not prime
at time=2,    1 is not prime
at time=3,    9 is not prime
at time=4,    3 is prime
at time=5,   13 is prime
at time=6,   13 is prime
at time=7,    5 is prime
at time=8,    2 is prime
at time=9,    1 is not prime
at time=10,  13 is prime
at time=11,   6 is not prime
at time=12,  13 is prime
at time=13,  13 is prime
at time=14,  12 is not prime
at time=15,   9 is not prime
at time=16,   6 is not prime
at time=17,   5 is prime
at time=18,  10 is not prime
at time=19,   5 is prime
at time=20,   7 is prime

  V C S   S i m u l a t i o n   R e p o r t
Time: 20 ns
CPU Time:        0.390 seconds;        Data structure size:   0.0Mb
```