

5th Day

ALU

Design

```
module alu_4bit (  
    input [3:0] a, b,  
    input [2:0] sel,  
    output reg [3:0] result,  
    output reg carry    // Carry Output  
);  
  
always @(*) begin  
    case (sel)  
        3'b000: {carry, result} = a + b; // Addition  
        3'b001: {carry, result} = a - b; // Subtraction  
        3'b010: result = a & b; // AND  
        3'b011: result = a | b; // OR  
        3'b100: result = a ^ b; // XOR  
        3'b101: result = a && b; // logical and  
        3'b110: result = a || b; // logical or  
        default: result = 4'b0000; // Default case  
    endcase  
  
end  
  
endmodule
```

Testbench

```
module alu_tb;

    reg [3:0] a, b;

    reg [2:0] sel;

    wire [3:0] result;

    wire carry;

    alu_4bit dut ( .a(a), .b(b), .sel(sel), .result(result), .carry(carry));

    initial begin

        $monitor("A = %b, B = %b, SEL = %b -> RESULT = %b, CARRY = %b", a, b, sel, result,
        carry);

        a = 4'b1010; b = 4'b0101; sel = 3'b000; #5; // ADD
        a = 4'b1010; b = 4'b0011; sel = 3'b001; #5; // SUB
        a = 4'b1100; b = 4'b1010; sel = 3'b010; #5; // AND
        a = 4'b1100; b = 4'b1010; sel = 3'b011; #5; // OR
        a = 4'b1100; b = 4'b1010; sel = 3'b100; #5; // XOR
        a = 4'b1010; b = 4'b0000; sel = 3'b101; #5; //logical and
        a = 4'b1100; b = 4'b0000; sel = 3'b110; #5; //logical or

        $finish;

    end

endmodule
```

Simulation

```
*,
# run 1000ns
A = 1010, B = 0101, SEL = 000 -> RESULT = 1111, CARRY = 0
A = 1010, B = 0011, SEL = 001 -> RESULT = 0111, CARRY = 0
A = 1100, B = 1010, SEL = 010 -> RESULT = 1000, CARRY = 0
A = 1100, B = 1010, SEL = 011 -> RESULT = 1110, CARRY = 0
A = 1100, B = 1010, SEL = 100 -> RESULT = 0110, CARRY = 0
A = 1010, B = 0000, SEL = 101 -> RESULT = 0000, CARRY = 0
A = 1100, B = 0000, SEL = 110 -> RESULT = 0001, CARRY = 0
$finish called at time : 35 ns : File "C:/Users/manojmsd/100_days_of_RTL/100_days_of_RTL.srscs/sources_1/new/alu_4bit_tb.v" Line 41
INFO: [USF-XSim-96] XSim completed. Design snapshot 'alu_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:03 ; elapsed = 00:00:09 . Memory (MB): peak = 1410.180 ; gain = 0.160
```

Name	Value	0.000 ns	10.000 ns	20.000 ns	30.000 ns	40.000 ns	50.000 ns
> a[3:0]	1100	1010	1100	1010	1100		
> b[3:0]	1010	0101	0011	1010	0000		
> sel[2:0]	010	000	001	010	011	100	101
> result[3:0]	8	f	7	8	e	6	0
carry	0						