# 50th day

## 3bit up_counter Verification Using SV

## Design

```
module count(input clk, rst, output reg [2:0]count);


  always @(posedge clk)
    begin
    if (rst)
      count <= 0;
    else
      count<=count+1;
   end
endmodule
```

# TB_top

```
`include "interface.sv"
`include "count_test.sv"

module tb_top();

  logic clk;

  count_intf vif(clk);
  count_test test_h(vif);

  count dut(.clk(clk),.rst(vif.rst),.count(vif.count));

    initial clk = 0;

    always #5 clk = ~clk;

    initial
     begin


       #200; $finish;
      end
endmodule
```

# Interface

```
interface count_intf(input logic clk);

  logic rst;
  logic [2:0] count;

endinterface
```

# Transaction

```
class transaction;

  rand bit rst;

  bit [2:0] count;

  function void display(string name);

    $display("_______%s_________",name);

    $display("rst=%b,count=%d at time=%0t",rst,count,$time);

  endfunction

  endclass
```

# Genrator

```
`include "transaction.sv"
class count_gen;
 transaction tr;
 mailbox gen2drv;
 virtual count_intf vif;

 function new(mailbox gen2drv);
  this.gen2drv = gen2drv;
 endfunction

 task run();
  for (int i = 0; i < 15; i++) begin
   tr = new();
   if (i == 0 || i == 5)
    tr.randomize() with { rst == 1; };
   else
    tr.randomize() with { rst == 0; };

   tr.display($sformatf("GEN[%0d]", i));

   gen2drv.put(tr);
  end
 endtask

endclass
```

# Driver

```
class count_drv;
  virtual count_intf vif;
  mailbox gen2drv;
  transaction tr;

  function new(mailbox gen2drv,virtual count_intf vif);
    this.vif=vif;
    this.gen2drv=gen2drv;
  endfunction

  task run();
    forever
      begin

        gen2drv.get(tr);
        vif.rst<=tr.rst;

        @(posedge vif.clk);

        tr.display("_____driver class signals_____");

      end
  endtask
endclass
```

# Monitor

```
class count_mon;
  virtual count_intf vif;
  mailbox mon2scb;
  transaction trans;

  function new(mailbox mon2scb,virtual count_intf vif);
     this.vif = vif;
    this.mon2scb = mon2scb;
  endfunction

  task run;
    repeat(15)
      begin
        @(posedge vif.clk);
      trans = new();
      trans.rst  = vif.rst;
      trans.count=vif.count;
      mon2scb.put(trans);
      trans.display("monitor class signals");
      end
  endtask

endclass
```

# Scoreboard

```
class count_scb;
  mailbox mon2scb;
  bit [2:0] exp_count;

  function new(mailbox mon2scb);
    this.mon2scb = mon2scb;
  endfunction

  task run;
    transaction trans;
    forever
      begin
      mon2scb.get(trans);

      if (trans.rst)
         exp_count = 0;
      else
         exp_count++;

       if (exp_count != trans.count)

         $error("Mismatch  Expected  count=%0d,  Got  count=%0d",  exp_count,
trans.count);

      else
```

```
        $display("No Mismatch Expected count=%0d, Got count=%0d",exp_count,trans.count);

        end

        endtask

endclass
```

# Environment

```
`include "count_gen.sv"
`include "count_drv.sv"
`include "count_mon.sv"
`include "count_scb.sv"

class count_env;

  count_gen gen_h;
  count_drv drv_h;
  count_mon mon_h;
  count_scb scb_h;

  mailbox gen2drv;
  mailbox mon2scb;
```

```
 virtual count_intf vif;

 function new(virtual count_intf vif);

  this.vif=vif;
  gen2drv=new();
  mon2scb=new();

  gen_h=new(gen2drv);
  drv_h=new(gen2drv,vif);
  mon_h=new(mon2scb,vif);
  scb_h=new(mon2scb);
 endfunction

 task run();
  fork
    gen_h.run();
    drv_h.run();
    mon_h.run();
    scb_h.run();
  join
 endtask

endclass
```

# Test

```
`include "count_env.sv"

program count_test(count_intf vif);

  count_env env_h;

  initial
    begin
      env_h=new(vif);
      env_h.run();
    end

endprogram
```

# Simulation

```
_______GEN[0]_________
rst=1,count=0 at time=0
_______GEN[1]_________
rst=0,count=0 at time=0
_______GEN[2]_________
rst=0,count=0 at time=0
_______GEN[3]_________
rst=0,count=0 at time=0
_______GEN[4]_________
rst=0,count=0 at time=0
_______GEN[5]_________
rst=1,count=0 at time=0
_______GEN[6]_________
rst=0,count=0 at time=0
_______GEN[7]_________
rst=0,count=0 at time=0
_______GEN[8]_________
rst=0,count=0 at time=0
_______GEN[9]_________
rst=0,count=0 at time=0
_______GEN[10]_________
rst=0,count=0 at time=0
_______GEN[11]_________
rst=0,count=0 at time=0
_______GEN[12]_________
rst=0,count=0 at time=0
_______GEN[13]_________
rst=0,count=0 at time=0
_______GEN[14]_________
rst=0,count=0 at time=0
```

```
_____________driver class signals_____________
rst=1,count=0 at time=5
_____monitor class signals_____
rst=1,count=0 at time=5
No Mismatch Expected count=0, Got count=0
_____________driver class signals_____________
rst=0,count=0 at time=15
_____monitor class signals_____
rst=0,count=1 at time=15
No Mismatch Expected count=1, Got count=1
_____________driver class signals_____________
rst=0,count=0 at time=25
_____monitor class signals_____
rst=0,count=2 at time=25
No Mismatch Expected count=2, Got count=2
_____________driver class signals_____________
rst=0,count=0 at time=35
_____monitor class signals_____
rst=0,count=3 at time=35
No Mismatch Expected count=3, Got count=3
_____________driver class signals_____________
rst=0,count=0 at time=45
_____monitor class signals_____
rst=0,count=4 at time=45
No Mismatch Expected count=4, Got count=4
_____________driver class signals_____________
rst=1,count=0 at time=55
_____monitor class signals_____
rst=1,count=0 at time=55
No Mismatch Expected count=0, Got count=0
```

```
_____________driver class signals_____________
rst=0,count=0 at time=65
_____monitor class signals_____
rst=0,count=1 at time=65
No Mismatch Expected count=1, Got count=1
_____________driver class signals_____________
rst=0,count=0 at time=75
_____monitor class signals_____
rst=0,count=2 at time=75
No Mismatch Expected count=2, Got count=2
_____________driver class signals_____________
rst=0,count=0 at time=85
_____monitor class signals_____
rst=0,count=3 at time=85
No Mismatch Expected count=3, Got count=3
_____________driver class signals_____________
rst=0,count=0 at time=95
_____monitor class signals_____
rst=0,count=4 at time=95
No Mismatch Expected count=4, Got count=4
_____________driver class signals_____________
rst=0,count=0 at time=105
_____monitor class signals_____
rst=0,count=5 at time=105
No Mismatch Expected count=5, Got count=5
_____________driver class signals_____________
rst=0,count=0 at time=115
_____monitor class signals_____
rst=0,count=6 at time=115
No Mismatch Expected count=6, Got count=6
```

```
_____driver class signals_____
rst=0,count=0 at time=125
_____monitor class signals_____
rst=0,count=7 at time=125
No Mismatch Expected count=7, Got count=7
_____driver class signals_____
rst=0,count=0 at time=135
_____monitor class signals_____
rst=0,count=0 at time=135
No Mismatch Expected count=0, Got count=0
_____driver class signals_____
rst=0,count=0 at time=145
_____monitor class signals_____
rst=0,count=1 at time=145
No Mismatch Expected count=1, Got count=1
$finish called from file "testbench.sv", line 21.
$finish at simulation time                  200
          V C S   S i m u l a t i o n   R e p o r t
Time: 200 ns
CPU Time:      0.240 seconds;       Data structure size:   0.0Mb
Mon Jun 23 06:33:50 2025
Done
```