9th Day

Linear Feedback Shift Register

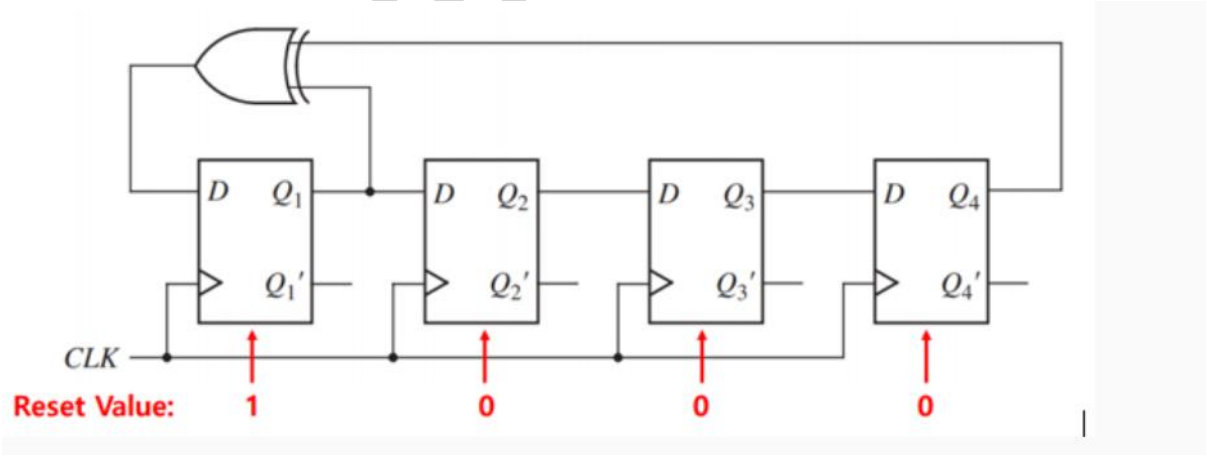
◇ Introduction

A **Linear Feedback Shift Register (LFSR)** is a sequential shift register that generates **pseudo-random binary sequences (PRBS)** using **XOR-based feedback**. LFSRs are widely used in cryptography, error detection, and random number generation due to their ability to produce long, repeating sequences with minimal hardware.

◇ LFSR Working Principle

- The LFSR consists of **D flip-flops** connected in series.
- The **feedback path** is generated using an **XOR operation** between selected bits
- On each clock cycle, the **register shifts right**, with the new input bit determined by the feedback equation.
- The initial seed (reset values) determines the sequence generated.

◇ 4-bit LFSR Design



In this implementation, the **feedback equation** is:

$D=Q1 \oplus Q4$

where **Q1 is the MSB** and **Q4 is the LSB**.

Design

```
module lfsr_4bit (input  clk,rst,output reg Q1, Q2, Q3, Q4);


// XOR feedback (D = Q3 ^ Q4)
wire D = Q1 ^ Q4;


always @(posedge clk)
  begin
   if (rst) begin
      // Reset values: Q1=1, Q2=0, Q3=0, Q4=0
      Q1 <= 1'b1;
      Q2 <= 1'b0;
      Q3 <= 1'b0;
      Q4 <= 1'b0;
   end
   else begin
      // Shift register with XOR feedback
      Q4 <= Q3;
      Q3 <= Q2;
      Q2 <= Q1;
      Q1 <= D;   // Feedback from Q1 ^ Q4
   end
 end

endmodule
```

Testbench

```
module lfsr_4bit_tb;
   reg clk, rst;
   wire Q1, Q2, Q3, Q4;

   lfsr_4bit dut (clk,rst,Q1,Q2,Q3,Q4);

   // Clock generation
   always #5 clk = ~clk; // 100MHz clock (10ns period)

   initial begin
      clk = 0;
      rst = 1;
      #20;
      rst = 0;
      #200;

      $finish;
      end

   initial
begin

      $monitor("Time = %0t | Q1 Q2 Q3 Q4 = %b%b%b%b", $time, Q1, Q2, Q3, Q4);
  end

endmodule
```

Simulation

```
# run 1000ns
Time = 0 | Q1 Q2 Q3 Q4 = xxxx
Time = 5000 | Q1 Q2 Q3 Q4 = 1000
Time = 25000 | Q1 Q2 Q3 Q4 = 1100
Time = 35000 | Q1 Q2 Q3 Q4 = 1110
Time = 45000 | Q1 Q2 Q3 Q4 = 1111
Time = 55000 | Q1 Q2 Q3 Q4 = 0111
Time = 65000 | Q1 Q2 Q3 Q4 = 1011
Time = 75000 | Q1 Q2 Q3 Q4 = 0101
Time = 85000 | Q1 Q2 Q3 Q4 = 1010
Time = 95000 | Q1 Q2 Q3 Q4 = 1101
Time = 105000 | Q1 Q2 Q3 Q4 = 0110
Time = 115000 | Q1 Q2 Q3 Q4 = 0011
Time = 125000 | Q1 Q2 Q3 Q4 = 1001
Time = 135000 | Q1 Q2 Q3 Q4 = 0100
Time = 145000 | Q1 Q2 Q3 Q4 = 0010
Time = 155000 | Q1 Q2 Q3 Q4 = 0001
Time = 165000 | Q1 Q2 Q3 Q4 = 1000
Time = 175000 | Q1 Q2 Q3 Q4 = 1100
Time = 185000 | Q1 Q2 Q3 Q4 = 1110
Time = 195000 | Q1 Q2 Q3 Q4 = 1111
Time = 205000 | Q1 Q2 Q3 Q4 = 0111
Time = 215000 | Q1 Q2 Q3 Q4 = 1011
$finish called at time : 220 ns : File "C:/Users/manojmsd/100_days_of_RTL/100_days_of_RTL.srcs/sources_1/new/lfsr_4bi
INFO: [USF-XSim-96] XSim completed. Design snapshot 'lfsr_4bit_tb_behav' loaded
```