49th day

Dff Verification Using SV

Design

```
module dff(input clk, rst, d, output reg q, output qbar);


 always @(posedge clk) begin
  if (rst)
    q <= 0;
  else
    q <= d;
 end


 assign qbar = ~q;


endmodule
```

TB_top

```
`include "interface.sv"
`include "dff_test.sv"

module tb_top();

  logic clk;

  dff_intf vif(clk);
  dff_test test_h(vif);

  dff dut(.clk(clk),.rst(vif.rst),.d(vif.d),.q(vif.q),.qbar(vif.qbar));

    initial clk = 0;

    always #5 clk = ~clk;

    initial
      begin
        $dumpfile("dff_waveform.vcd");
        $dumpvars(0, tb_top);

        #200; $finish;
      end
endmodule
```

Interface

```
interface dff_intf(input logic clk);


  logic rst;
  logic d;
  logic q;
  logic qbar;


endinterface
```

Transaction

```
class transaction;


  rand bit rst;
  rand bit d;


  bit q;
  bit qbar;


  function void display(string name);



    $display("_______%s_________",name);
```

```
    $display("rst=%b,d=%b,q=%b,qbar=%b, at time=%0t",rst,d,q,qbar,$time);

  endfunction


endclass
```

Genrator

```
`include "transaction.sv"

class dff_gen;
  transaction tr;
  mailbox gen2drv;
  virtual dff_intf vif;

  function new(mailbox gen2drv);
    this.gen2drv=gen2drv;
    this.vif=vif;
  endfunction

  task run();


    repeat(7)
      begin
```

```
        tr=new();
        tr.randomize();

        tr.display("generator class signals");
        gen2drv.put(tr);

      end

 endtask
endclass
```

Driver

```
class dff_drv;

 virtual dff_intf vif;
 mailbox gen2drv;
 transaction tr;

 function new(mailbox gen2drv,virtual dff_intf vif);
  this.vif=vif;
  this.gen2drv=gen2drv;
 endfunction

 task run();
```

```
  forever
    begin

      gen2drv.get(tr);
      vif.rst<=tr.rst;
      vif.d<=tr.d;

      @(posedge vif.clk);

      tr.display("_____driver class signals_____");

    end
  endtask
endclass
```

Monitor

```
class dff_mon;

  virtual dff_intf vif;

  mailbox mon2scb;

  transaction trans;
```

```
function new(mailbox mon2scb,virtual dff_intf vif);

  this.vif = vif;

  this.mon2scb = mon2scb;
endfunction



task run;

  repeat(7)
    begin
      @(posedge vif.clk);



    trans = new();

    trans.rst  = vif.rst;
    trans.d    = vif.d;
    trans.q    = vif.q;
    trans.qbar = vif.qbar;

    mon2scb.put(trans);

    trans.display("monitor class signals");
    end
```

```
  endtask

endclass
```

Scoreboard

```
class dff_scb;
  mailbox mon2scb;
  bit exp_q;

  function new(mailbox mon2scb);
    this.mon2scb = mon2scb;
  endfunction

  task run;
    transaction trans;
    forever
      begin
      mon2scb.get(trans);

      if (trans.rst)
         exp_q = 0;
      else
         exp_q=trans.d;

      if (exp_q != trans.q)
```

```
      $error("Mismatch Expected q=%0b, Got q=%0b", exp_q, trans.q);

    else
      $display("No Mismatch Expected q=%0b, Got q=%0b",exp_q,trans.q);

      end

      endtask

endclass
```

Environment

```
`include "dff_gen.sv"
`include "dff_drv.sv"
`include "dff_mon.sv"
`include "dff_scb.sv"

class dff_env;

  dff_gen gen_h;
  dff_drv drv_h;
  dff_mon mon_h;
  dff_scb scb_h;

  mailbox gen2drv;
```

```
 mailbox mon2scb;

 virtual dff_intf vif;

 function new(virtual dff_intf vif);

  this.vif=vif;
  gen2drv=new();
  mon2scb=new();

  gen_h=new(gen2drv);
  drv_h=new(gen2drv,vif);
  mon_h=new(mon2scb,vif);
  scb_h=new(mon2scb);
 endfunction

 task run();
  fork
    gen_h.run();
    drv_h.run();
    mon_h.run();
    scb_h.run();
  join
 endtask

endclass
```

Test

```
`include "dff_env.sv"

program dff_test(dff_intf vif);

  dff_env env_h;

  initial
    begin
      env_h=new(vif);
      env_h.run();
    end

endprogram
```

Simulation

```
_______generator class signals_________
rst=0,d=1,q=0,qbar=0, at time=0
_______generator class signals_________
rst=1,d=0,q=0,qbar=0, at time=0
_______generator class signals_________
rst=0,d=0,q=0,qbar=0, at time=0
_______generator class signals_________
rst=1,d=0,q=0,qbar=0, at time=0
_______generator class signals_________
rst=0,d=1,q=0,qbar=0, at time=0
_____________driver class signals_________________
rst=0,d=1,q=0,qbar=0, at time=5
_______monitor class signals_________
rst=0,d=1,q=1,qbar=0, at time=5
No Mismatch Expected q=1, Got q=1
_____________driver class signals_________________
rst=1,d=0,q=0,qbar=0, at time=15
_______monitor class signals_________
rst=1,d=0,q=0,qbar=1, at time=15
No Mismatch Expected q=0, Got q=0
_____________driver class signals_________________
rst=0,d=0,q=0,qbar=0, at time=25
_______monitor class signals_________
rst=0,d=0,q=0,qbar=1, at time=25
No Mismatch Expected q=0, Got q=0
_____________driver class signals_________________
rst=1,d=0,q=0,qbar=0, at time=35
_______monitor class signals_________
rst=1,d=0,q=0,qbar=1, at time=35
No Mismatch Expected q=0, Got q=0
_____________driver class signals_________________
rst=0,d=1,q=0,qbar=0, at time=45
_______monitor class signals_________
rst=0,d=1,q=1,qbar=0, at time=45
No Mismatch Expected q=1, Got q=1
$finish called from file "testbench.sv", line 21.
$finish at simulation time                  200
          V C S   S i m u l a t i o n   R e p o r t
```