18th Day

Parity gen checker

Design

```
module parity_gen_checker (
                    input  [7:0] data_in,
                    input  parity_mode,       // 0 for even parity, 1 for odd parity
                    input  enable_check,
                    output reg parity_bit,
                    output reg parity_error
);


                    // Parity Generation
                    always @(*)
                     begin
                          if (parity_mode == 1'b0)
                           begin
                                  // Even parity
                                  parity_bit = ^data_in;
                           end
                           else
                           begin
                                  // Odd parity
                                  parity_bit = ~(^data_in);
                           end
                      end
```

```
// Parity Checking
                always @(*)
                begin
                    if (enable_check)
                    begin
                        if (parity_mode == 1'b0)
                         begin
                            // Check even parity
                            parity_error = (parity_bit != ^data_in);
                        end
                      else
                       begin
                            // Check odd parity
                            parity_error = (parity_bit != ~(^data_in));
                         end
                    end
                    else
                    begin
                        parity_error = 1'b0; // No error check when disabled
                    end
                end

endmodule
```

Testbench

```
module tb_parity_gen_checker;

    reg [7:0] data_in;
    reg parity_mode;
    reg enable_check;
    wire parity_bit;
    wire parity_error;



    parity_gen_checker dut (
        .data_in(data_in),
        .parity_mode(parity_mode),
        .enable_check(enable_check),
        .parity_bit(parity_bit),
        .parity_error(parity_error)
    );

    // Task for applying stimulus
    task apply_stimulus;
        input [7:0] test_data;
        input test_parity_mode;
        input test_enable_check;
        begin
            data_in = test_data;
            parity_mode = test_parity_mode;
            enable_check = test_enable_check;
            #10; // Wait for 10 time units
        end
    endtask
```

```
    initial begin
        $display("Starting testbench...");

        // Test even parity generation and checking
        apply_stimulus(8'b10101010, 1'b0, 1'b0); // Generate even parity, no check
        #10;
        $display("Data: %b, Parity Mode: Even, Parity Bit: %b, Error: %b", data_in, parity_bit, parity_error);

        apply_stimulus(8'b10101010, 1'b0, 1'b1); // Check even parity
        #10;
        $display("Data: %b, Parity Mode: Even, Parity Bit: %b, Error: %b", data_in, parity_bit, parity_error);

        apply_stimulus(8'b10111010, 1'b0, 1'b1); // Check even parity
        #10;
        $display("Data: %b, Parity Mode: Even, Parity Bit: %b, Error: %b", data_in, parity_bit, parity_error);

        // Test odd parity generation and checking
        apply_stimulus(8'b10101010, 1'b1, 1'b0); // Generate odd parity, no check
        #10;
        $display("Data: %b, Parity Mode: Odd, Parity Bit: %b, Error: %b", data_in, parity_bit, parity_error);

        apply_stimulus(8'b10111010, 1'b1, 1'b1); // Check odd parity
        #10;
        $display("Data: %b, Parity Mode: Odd, Parity Bit: %b, Error: %b", data_in, parity_bit, parity_error);

        // Test mismatched parity error detection
        apply_stimulus(8'b11111111, 1'b0, 1'b1); // Mismatch for even parity
```

```
        #10;
        $display("Data: %b, Parity Mode: Even, Parity Bit: %b, Error: %b", data_in, parity_bit, parity_error);

        $display("Testbench complete.");
        $finish;
    end

endmodule
```

Simulation

```
Starting testbench...
Data: 10101010, Parity Mode: Even, Parity Bit: 0, Error: 0
Data: 10101010, Parity Mode: Even, Parity Bit: 0, Error: 0
Data: 10111010, Parity Mode: Even, Parity Bit: 1, Error: 0
Data: 10101010, Parity Mode: Odd, Parity Bit: 1, Error: 0
Data: 10111010, Parity Mode: Odd, Parity Bit: 0, Error: 0
Data: 11111111, Parity Mode: Even, Parity Bit: 0, Error: 0
Testbench complete.
$finish called at time : 120 ns : File "C:/Users/manojmsd/100_days_of_RTL_2/100_days
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb_parity_gen_checker_behav' lo
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
```