21st Day

SV DataTypes

```
module sv_data_types();
 reg a;
 wire b;
 logic c;
 bit d;
 int e;
 integer f;
 byte g;

 initial
  begin
   $display("a=%b, default size of reg is %0d",a,$bits(a));
   $display("b=%b, default size of wire is %0d",b,$bits(b));
   $display("c=%b, default size of logic is %0d",c,$bits(c));
   $display("d=%b, default size of bit is %0d",d,$bits(d));
   $display("e=%b, default size of int is %0d",e,$bits(e));
   $display("f=%b, default size of integer %0d",f,$bits(f));
   $display("g=%b, default size of byte is %0d",g,$bits(g));
  end

endmodule
```

SIMULATION

```
Contains Synopsys proprietary information.
Compiler version U-2023.03-SP2_Full64; Runtime version U-2023.03-SP2_Full64;  Apr  8 08:15 2025
a=x, default size of reg is 1
b=z, default size of wire is 1
c=x, default size of logic is 1
d=0, default size of bit is 1
e=00000000000000000000000000000000, default size of int is 32
f=xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, default size of integer 32
g=00000000, default size of byte is 8
          V C S   S i m u l a t i o n   R e p o r t
Time: 0 ns
```