# 6th Day

# Freq div

As we know that clk is the basic building in the sequential circuits with the help of this clk I designed frequency division which is shown below

## Why Freq Div?

**Synchronization Across Different Clock Domains:**

- Many digital systems operate at different clock speeds. Frequency division ensures that components communicate properly.
- Example: A microprocessor running at 1 GHz might need a 100 MHz bus clock.

**Reducing Power Consumption:**

- High-frequency clocks consume more power.
- Slowing down clock speed when high speed is unnecessary improves power efficiency.
- Example: Dynamic clock scaling in processors conserves battery life in mobile devices.

# Freq_division

```
module clk_division_tb();
reg clk=0;
reg clk_div=0;
reg [3:0]count=0;
parameter div=6;

always #5 clk=~clk;

always @(posedge clk)
   begin
   if(count==(div/2-1))
   begin
      clk_div <= ~clk_div;
      count<=0;
   end
   else
       count<=count+1;
   end

 initial
  begin
  #500;
  $finish;
  end
endmodule
```

## Simulation