7th Day

Universal Counter

A **universal counter** is a highly flexible digital circuit that supports multiple functionalities, including **up-counting, down-counting, and parallel loading of values**. The Verilog implementation of this universal counter is designed to provide **4-bit counting capability**, controlled via external inputs such as **reset, enable, load, and up/down mode selection**.

Design

```
module universal_counter(
   input rst, clk, en, udbar, ld,
   input [3:0] ld_val,
   output reg [3:0] cnt
);


always @(posedge clk )
  begin
      if (rst)
         cnt <= 4'b0000;  // Reset the counter to 0
      else
        begin
         if (en)
           begin
              if (ld)
                 cnt <= ld_val;  // Load input value
             else
                begin
                if(udbar)
```

```
            cnt <= cnt + 1; // Count up
          else
            cnt <= cnt - 1; // Count down
        end
      end
    end
  end
endmodule
```

Testbench

```
module univ_counter_tb( );
reg clk,rst,en,ld,udbar;
reg [3:0]ldval;
wire [3:0]cnt;

universal_counter dut(rst,clk,en,udbar,ld,ldval,cnt);

always #5 clk=~clk;

initial
begin
clk=0;
rst=1;
#10;
rst=0;
end
```

```
initial
begin
   en=1;
   ld=1;
   ldval=4'd7;
   #30;
   ld=0;
   udbar=1;
   #50;
   udbar=0;
   #50;
   ld=1;
   ldval=4'd5;
   #20;
   ld=0;
   udbar=1;
   #50;
   udbar=0;
end

initial
begin
#300;
$finish;
end
endmodule
```

Simulation