Chapter 4: The Memory System

Objectives

- Basic memory circuits
- Organization of main memory
- Cache memory concept, which shortens the effective memory access time
- Virtual memory mechanism, which increases the apparent size of the main memory
- Magnetic disks, optical disks and magnetic tapes used for secondary storage

Basic Concepts

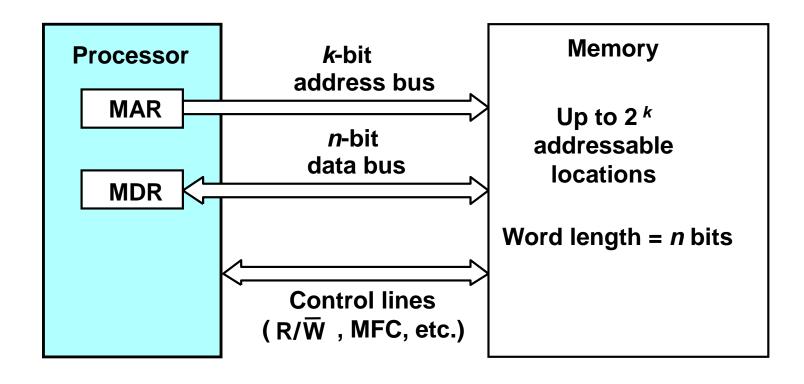


Figure 4.1. Connection of the memory to the processor.

Semiconductor RAM Memories

- Internal Organization of Memory Chips
- Static Memories
- Asynchronous DRAMs
- Synchronous DRAMs
- Structure of larger Memories
- Memory System Considerations
- Rambus Memory

Internal Organization of Memory Chips

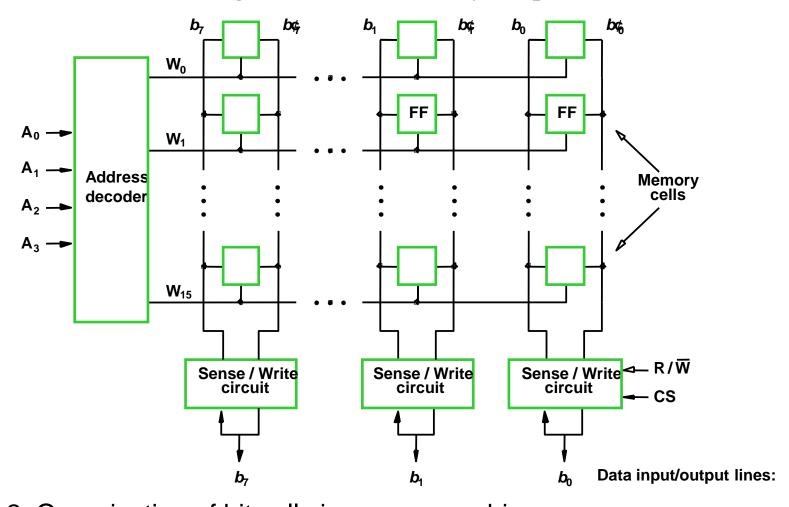


Figure 4.2. Organization of bit cells in a memory chip.

small (very) example (128 bit chip) 16 words of 8 bits each (16 x 8)

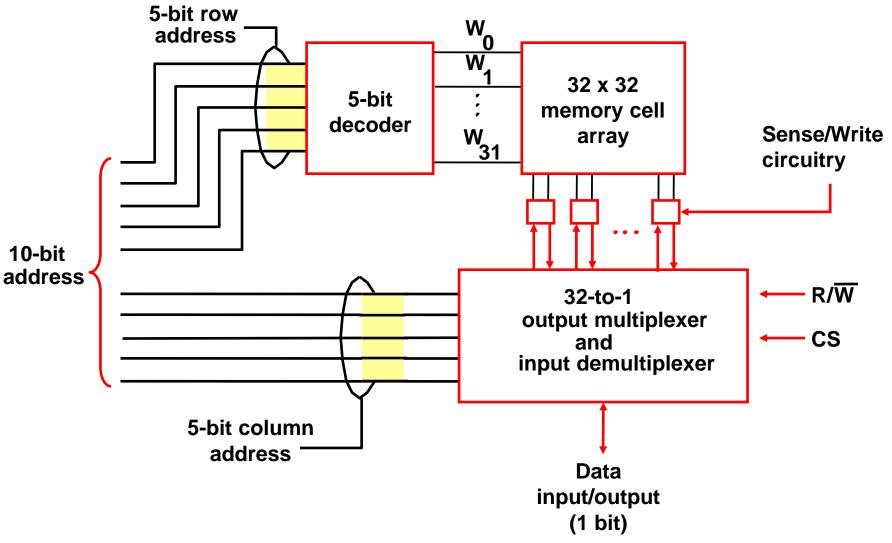


Figure 4.3. Organization of a $1K \times 1$ memory chip.

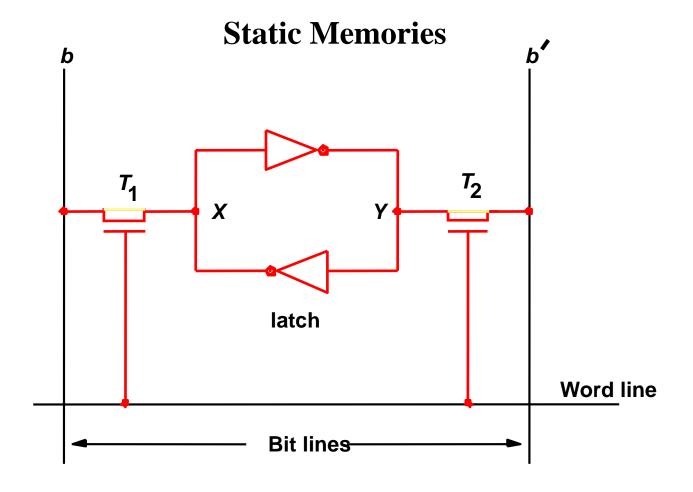


Figure 4.4. A static RAM cell. KLECET, E&C Dept. Bgm Chp4

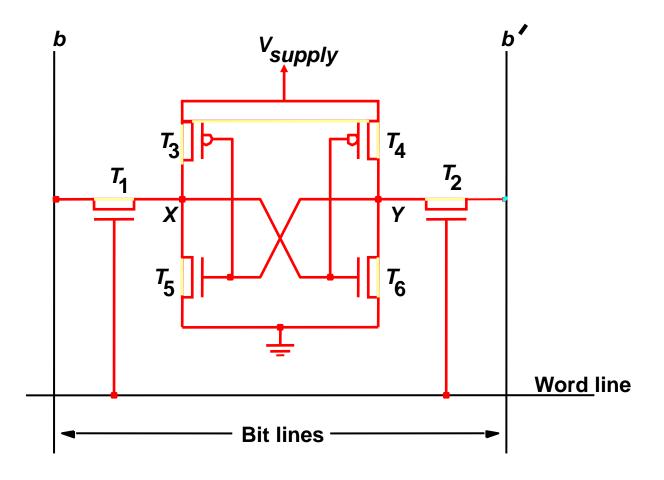


Figure 5.5. An example of a CMOS memory cell.

Asynchronous DRAMs Bit line Word line capacitor is charge on the charged to write a 1 capacitor will (voltage applied to discharge over time Word line and to the Bit line)

Figure 5.6. A single-transistor dynamic memory cell

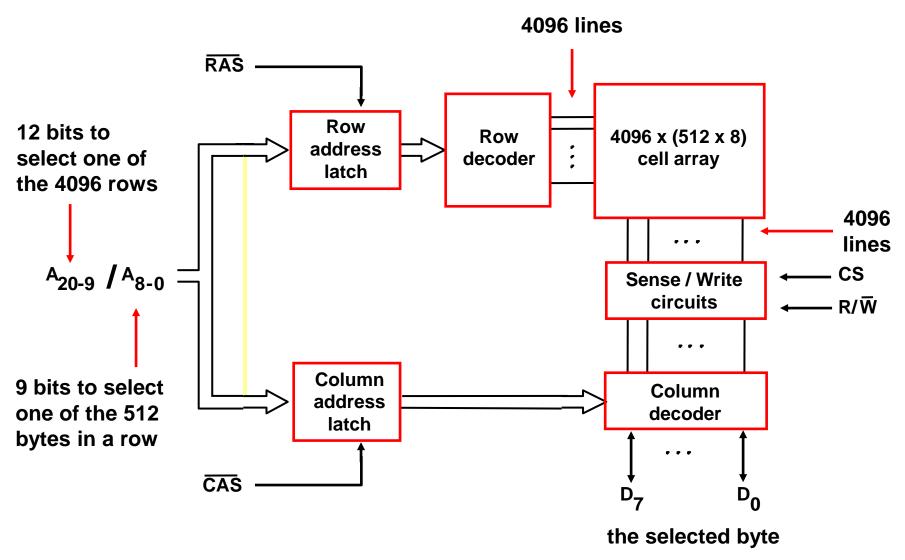
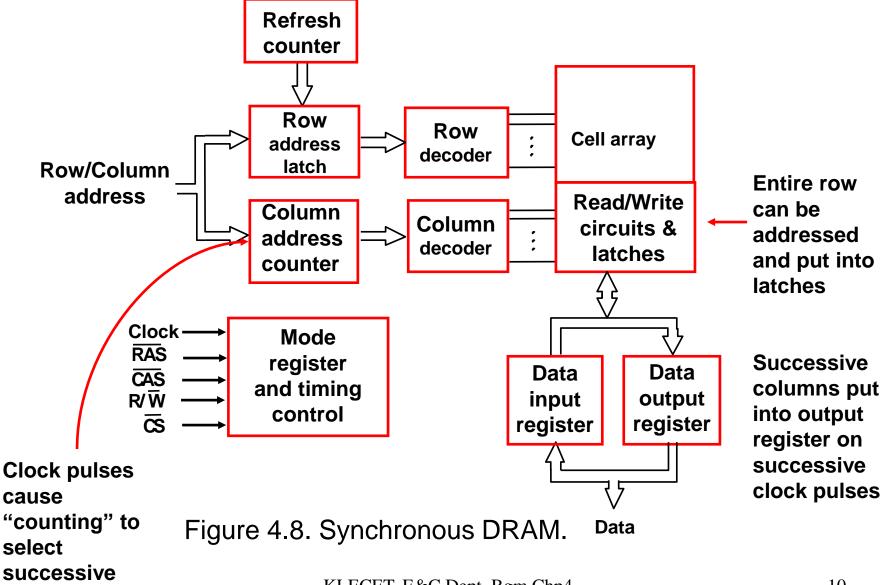


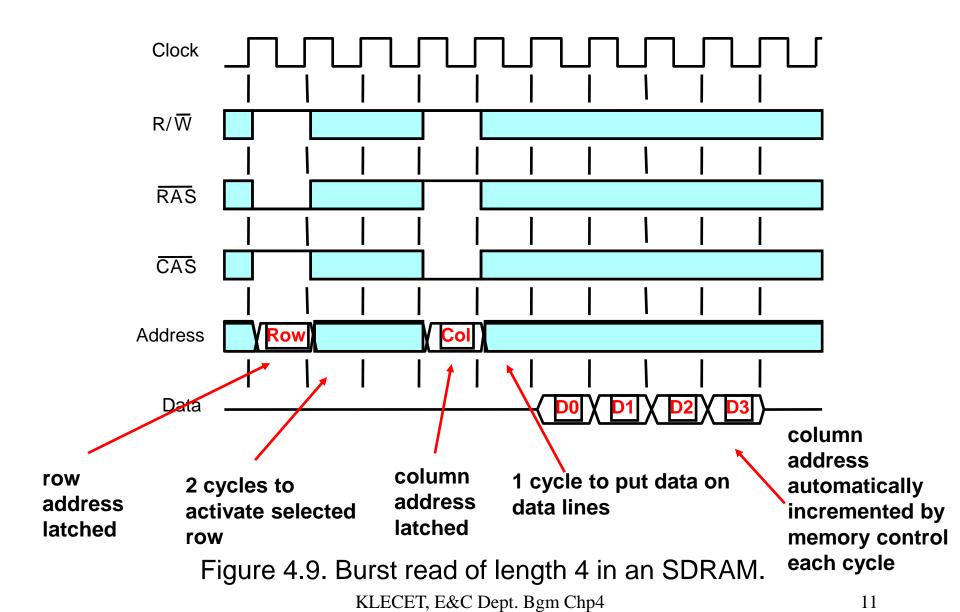
Figure 4.7. Internal organization of a 2M x 8 dynamic memory chip.

16 megabits, 2 million bytes

Synchronous DRAMs

columns





Structure of larger Memories

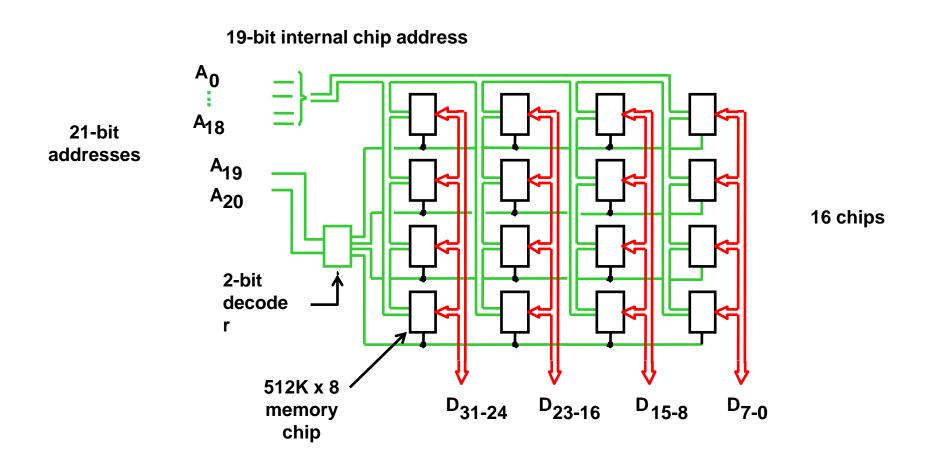


Figure 4.10. Organization of a $2M \times 32$ memory module using $512K \times 8$ static memory chips (16 chips).

Memory System Considerations

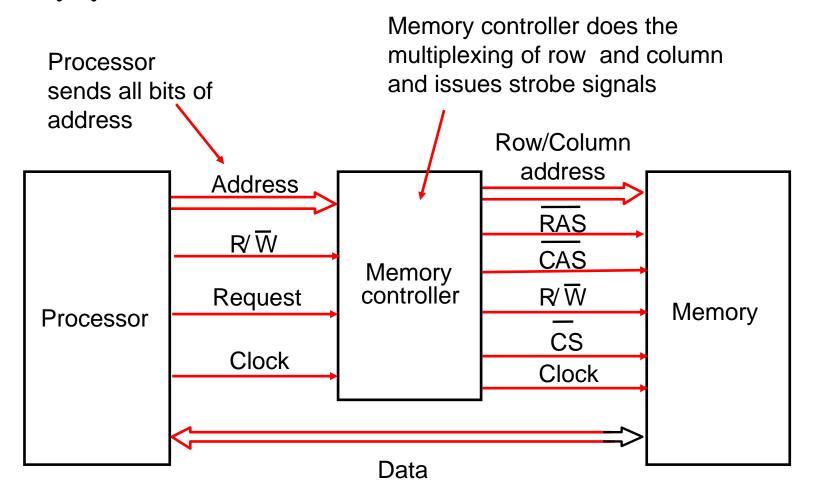


Figure 5.11. Use of a memory controller.

Read-Only Memories

- ROM
- PROM
- EPROM
- EEPROM
- Flash Memory

ROM: Read Only Memory

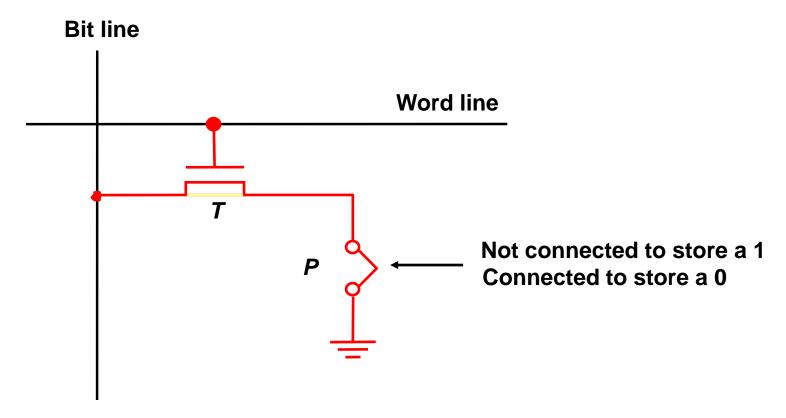


Figure 4.12. A ROM cell.

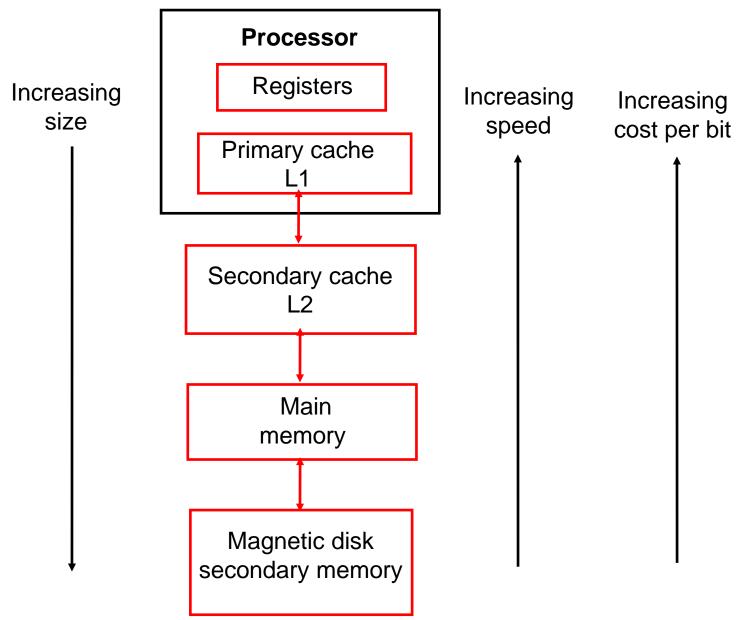
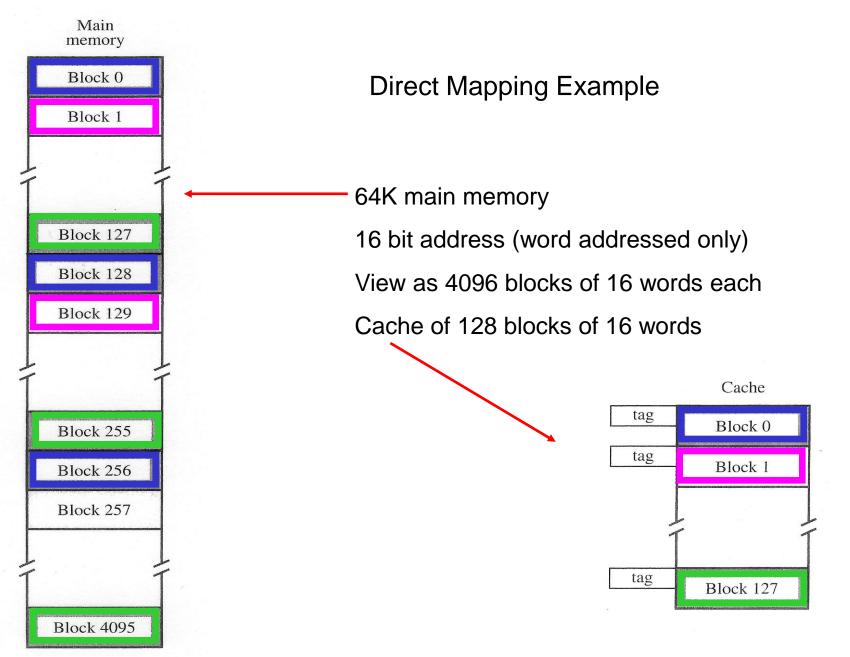


Figure 4.13. Memory hierarchy. LECET, E&C Dept. Bgm Chp4

Speed, Size and Cost

Cache Memories

- Mapping functions
- Replacement Algorithms
- Examples of Mapping



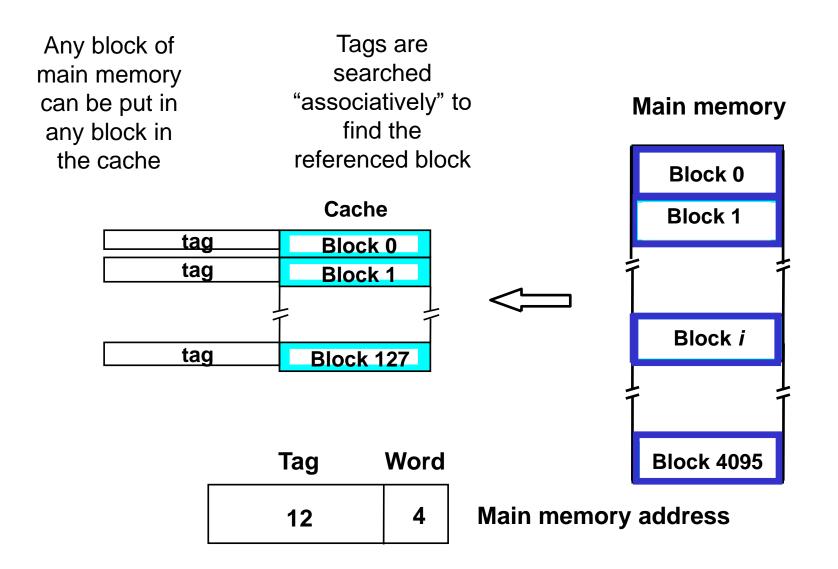
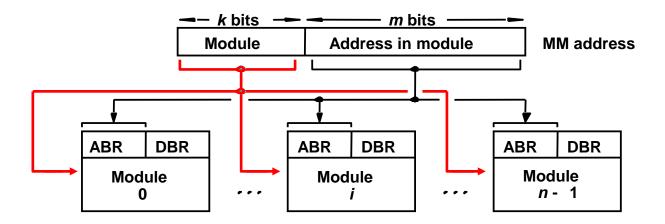


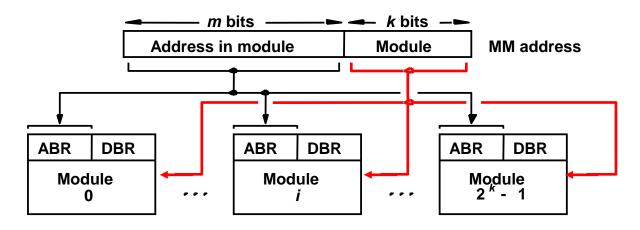
Figure 4.16. Associative-mapped cache. KLECET, E&C Dept. Bgm Chp4

Performance Consideration

- Interleaving
- Hit Rate and Miss Penalty
- Caches on the processor Chip
- Other Enhancements



(a) Consecutive words in a module



(b) Consecutive words in consecutive modules

Figure 4.25. Addressing multiple-module memory systems.

Virtual Memories

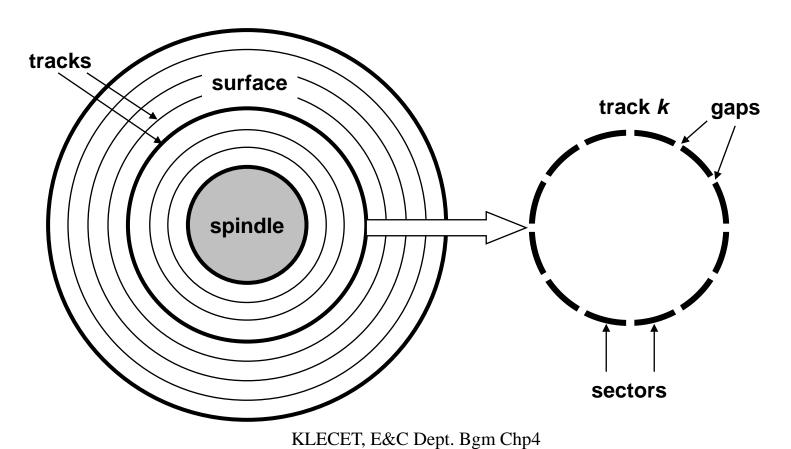
Address translation

Secondary Storage

- Magnetic Hard Disks
- Optical Disks
- Magnetic Tape systems

Disk geometry

- *Disks* consist of *platters*, each with two *surfaces*.
- Each *surface* consists of concentric rings called *tracks*.
- Each *track* consists of *sectors* separated by *gaps*.



Concluding Remarks