

## Chapter 2

# Machine Instructions and Programs

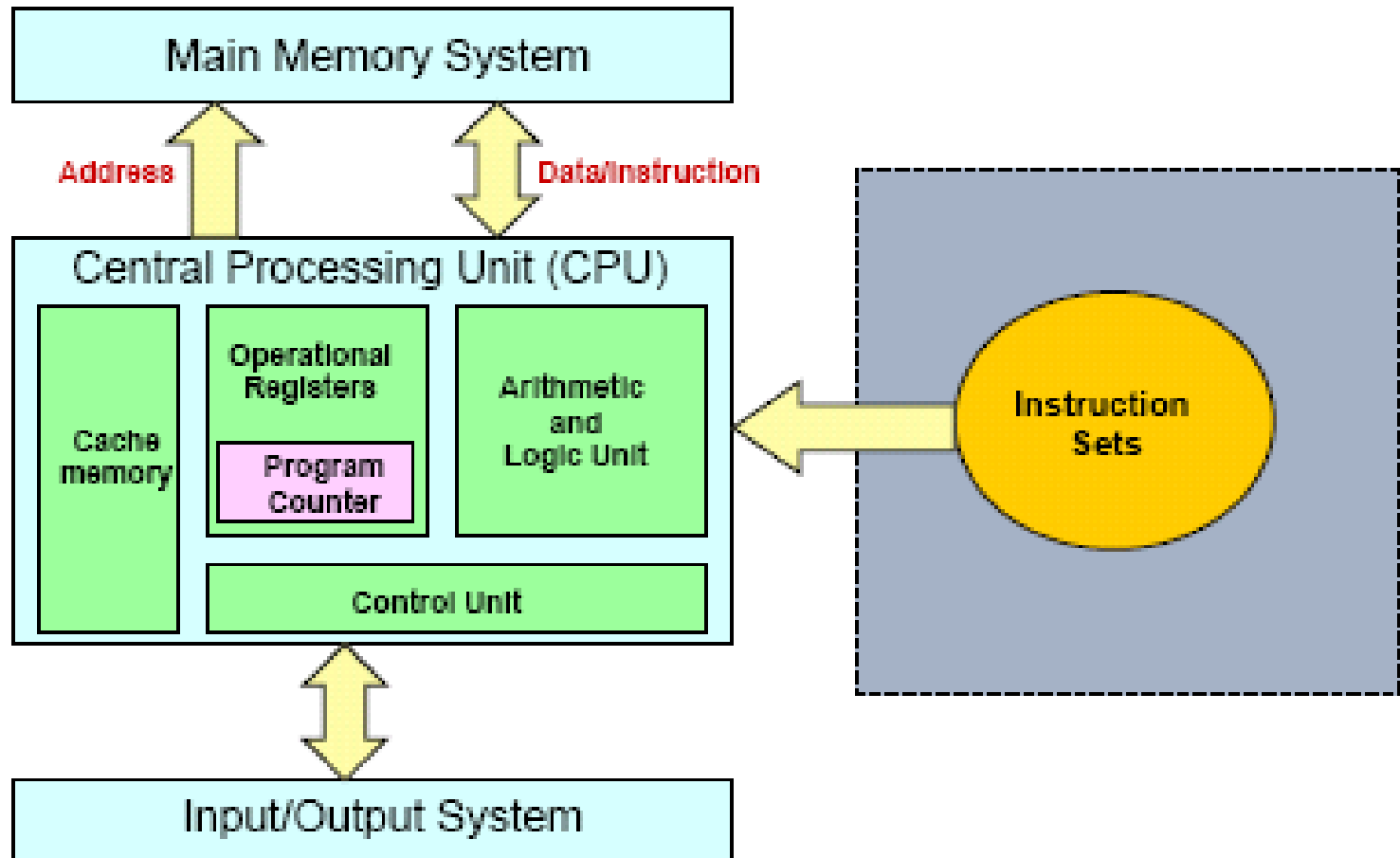
# Outline

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- Numbers, Arithmetic Operations, and Characters
- Memory Locations and Addresses
- Memory Operation
- Instructions and Instruction Sequencing
- Addressing Modes
- Assembly Language
- Basic Input/Output Operations
- Stacks and Queues
- Subroutines
- Linked List
- Encoding of Machine Instructions

# Content Coverage

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# Number Representation

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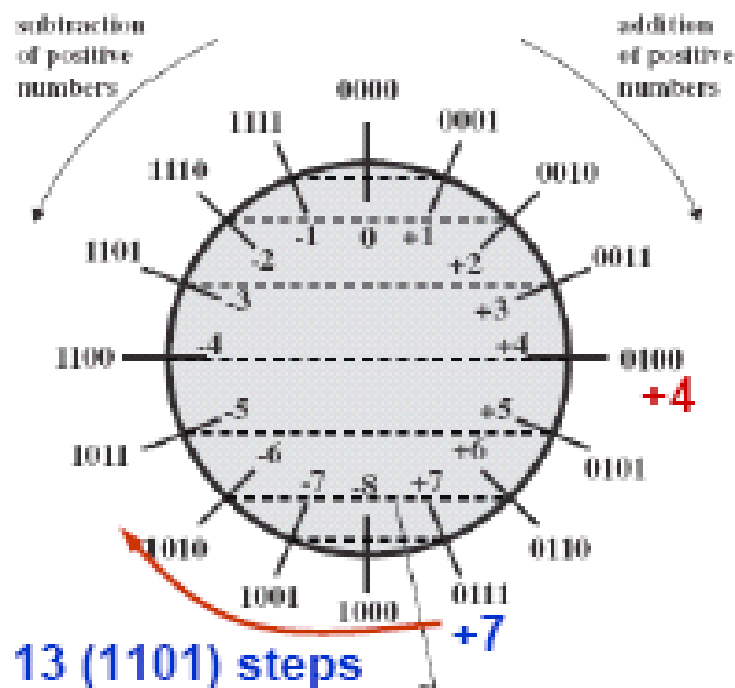
- Consider an  $n$ -bit vector  $B = b_{n-1} \dots b_1 b_0$ , where  $b_i = 0$  or  $1$  for  $0 \leq i \leq n-1$
- The vector  $B$  can represent unsigned integer values  $V$  in the range  $0$  to  $2^n - 1$ , where
  - ◆  $V(B) = b_{n-1} \times 2^{n-1} + \dots + b_1 \times 2^1 + b_0 \times 2^0$
- We need to represent positive and negative numbers for most applications
- Three systems are used for representing such numbers
  - ◆ Sign-and-magnitude
  - ◆ 1's-complement
  - ◆ 2's-complement

# Number Representation

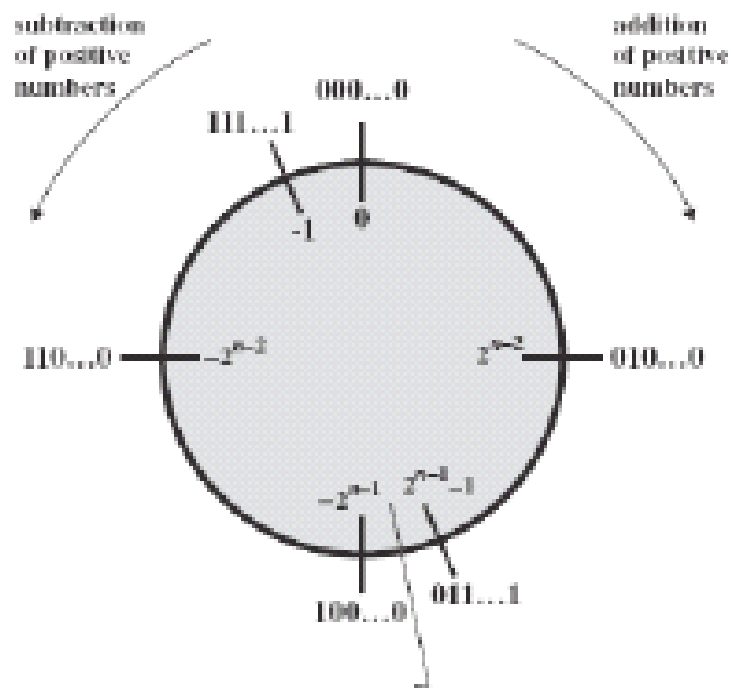
$b_3b_2b_1b_0$	sign and magnitude	1's-complement	2's-complement
0 1 1 1	+7	+7	+7
0 1 1 0	+6	+6	+6
0 1 0 1	+5	+5	+5
0 1 0 0	+4	+4	+4
0 0 1 1	+3	+3	+3
0 0 1 0	+2	+2	+2
0 0 0 1	+1	+1	+1
0 0 0 0	+0	+0	+0
1 0 0 0	-0	-7	-8
1 0 0 1	-1	-6	-7
1 0 1 0	-2	-5	-6
1 0 1 1	-3	-4	-5
1 1 0 0	-4	-3	-4
1 1 0 1	-5	-2	-3
1 1 1 0	-6	-1	-2
1 1 1 1	-7	-0	-1

# 2's-Complement System

$$+7 + (-3)$$



(a) 4-bit numbers

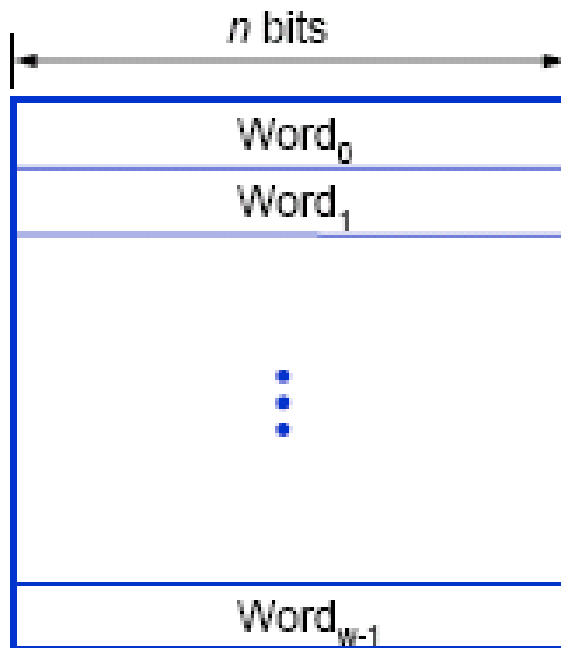


(b) n-bit numbers

# Memory Words

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Memory words



A signed integer



Four characters



ASCII  
character

# Big-Endian & Little-Endian Assignments

- Byte addresses can be assigned across words in two ways
  - ◆ Big-endian and little-endian

Word address	Byte address			
0	0	1	2	3
4	4	5	6	7
$2^k-4$	$2^k-4$	$2^k-3$	$2^k-2$	$2^k-1$

Big-endian assignment

Word address	Byte address			
0	3	2	1	0
4	7	6	5	4
$2^k-4$	$2^k-1$	$2^k-2$	$2^k-3$	$2^k-4$

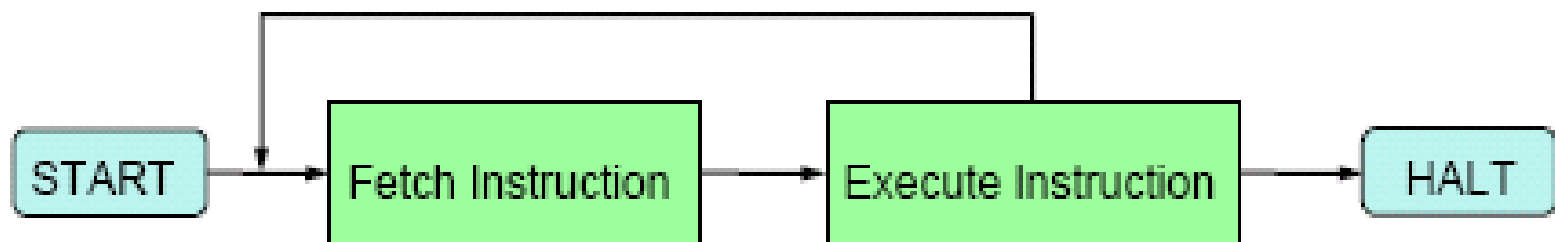
Little-endian assignment



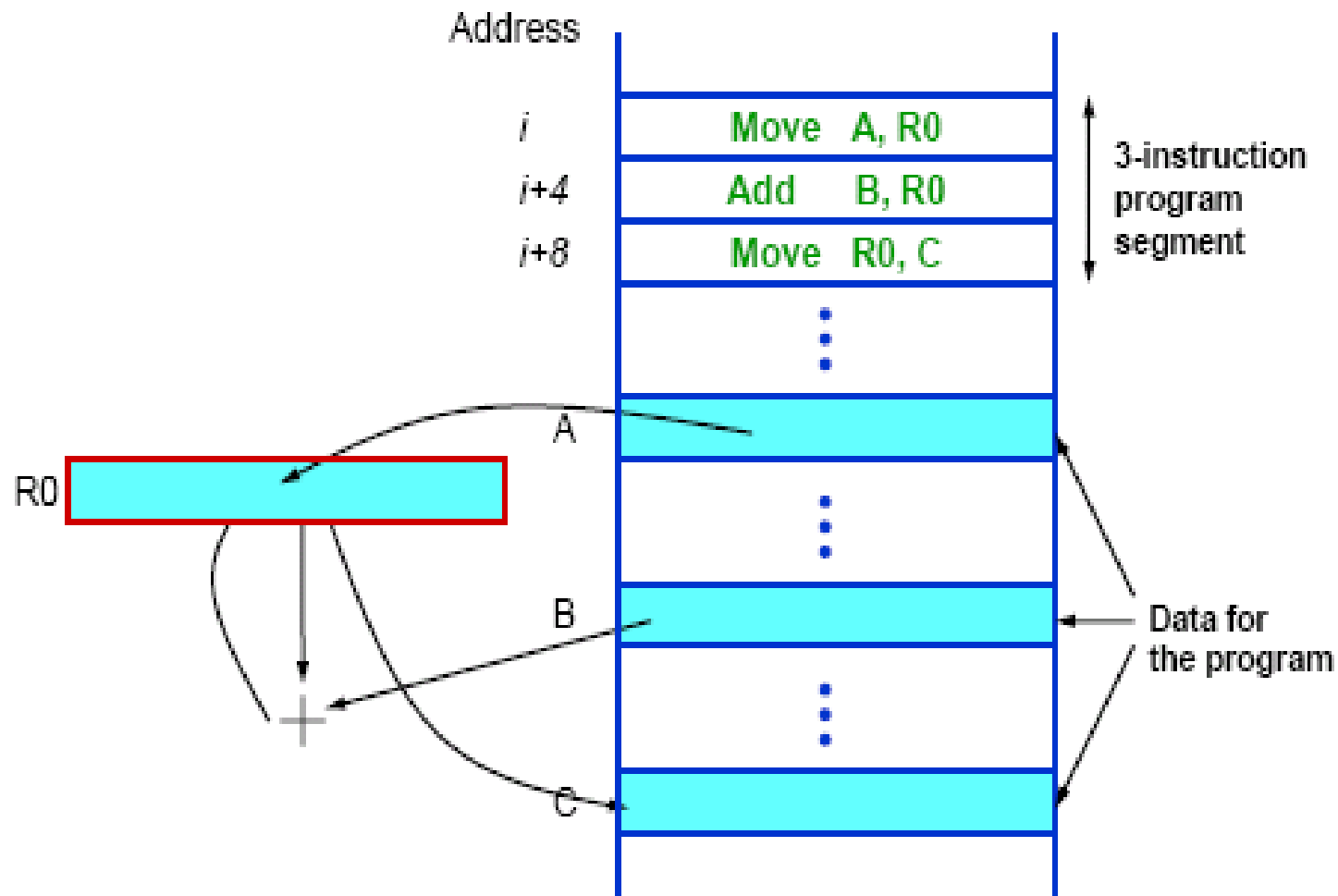
# Instruction Execution

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- How a program is executed
  - ◆ The processor contains a register called the program counter (PC), which holds the address of the instruction to be executed next. To begin executing a program, the address of its first instruction must be placed into the PC, then the processor control circuits use the information in the PC to fetch and execute instruction, one at a time, in the order of increasing address
- Basic instruction cycle



# A Program for $C \leftarrow [A] + [B]$

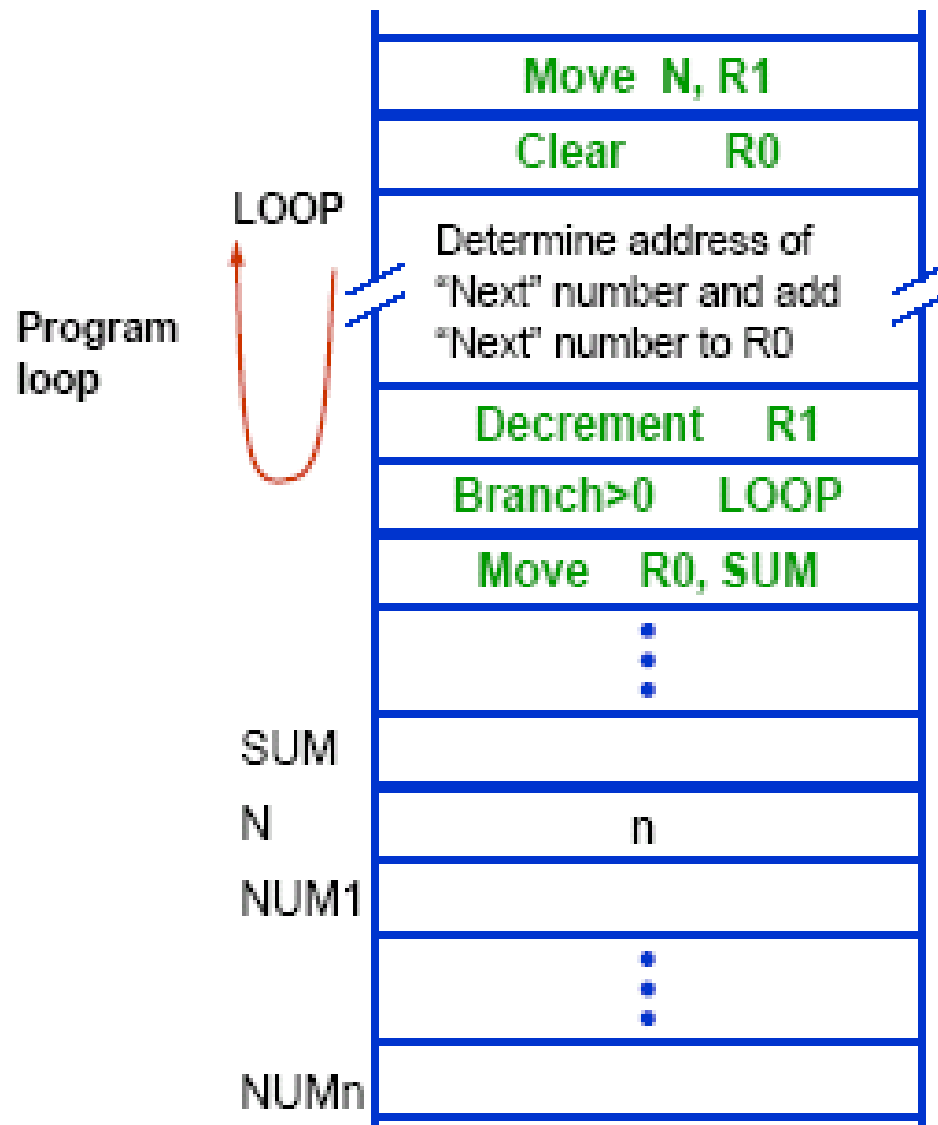


# Straight-Line Sequencing

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$i$	Move NUM1, R0
$i+4$	Add NUM2, R0
$i+8$	Add NUM3, R0
	⋮
$i+4n-4$	Add NUM $n$ , R0
$i+4n$	Move R0, SUM
	⋮
SUM	
NUM1	
NUM2	
	⋮
NUM $n$	

# Branching



# Generic Addressing Modes

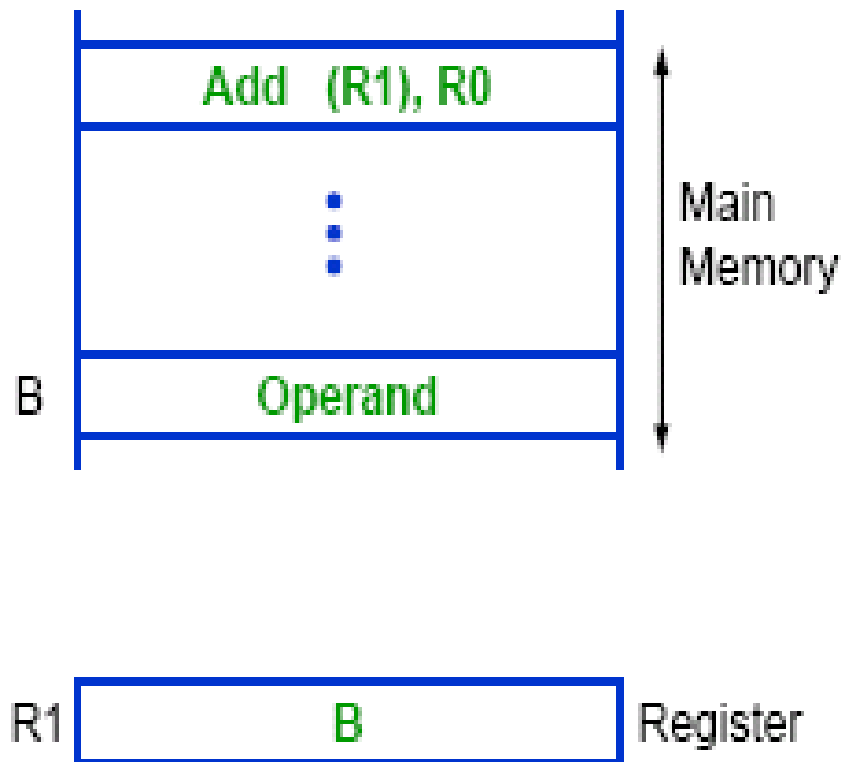
Name	Assembler syntax	Addressing function
Immediate	#Value	Operand=Value
Register	Ri	EA=Ri
Absolute (Direct)	LOC	EA=LOC
Indirect	(Ri)	EA=[Ri]
	(LOC)	EA=[LOC]
Index	X(Ri)	EA=[Ri]+X
Base with index	(Ri, Rj)	EA=[Ri]+[Rj]
Base with index and offset	X(Ri, Rj)	EA=[Ri]+[Rj]+X
Relative	X(PC)	EA=[PC]+X
Autoincrement	(Ri)+	EA=[Ri]; Increment Ri
Autodecrement	-(Ri)	Decrement Ri; EA=[Ri]

EA: effective address

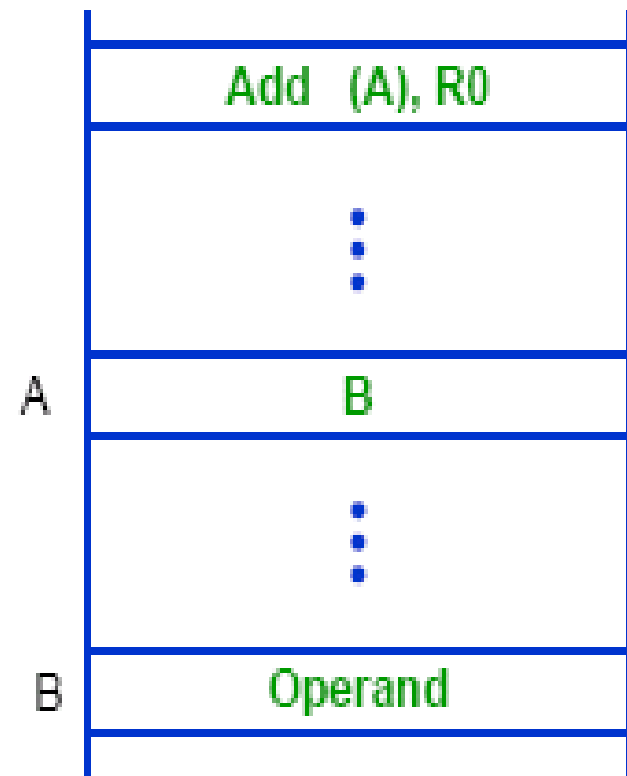
Value: a signed number

# Two Types of Indirect Addressing

Through a general-purpose register



Through a memory location



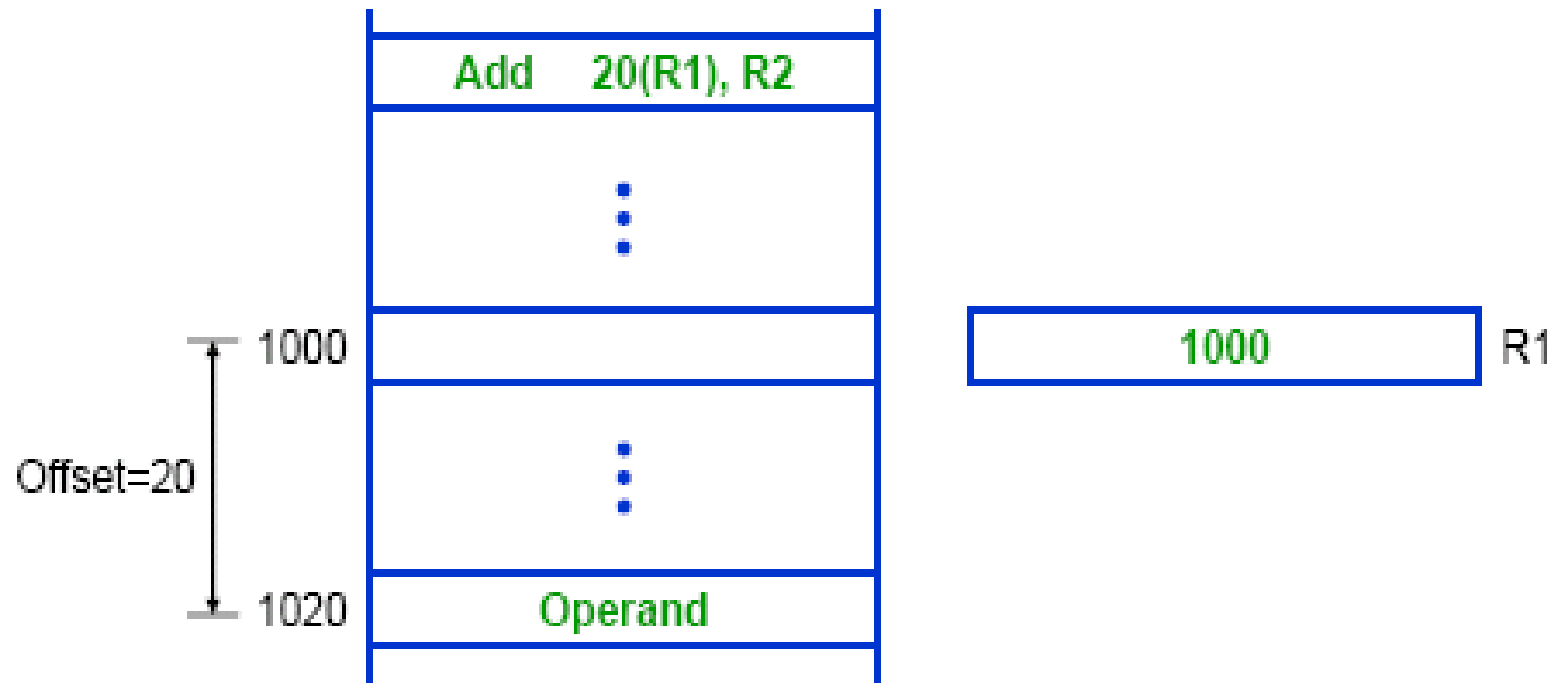
# Using Indirect Addressing in a Program

Address	Contents	
	Move N, R1	} Initialization
	Move #NUM1, R2	
	Clear R0	
→ LOOP	Add (R2), R0	
	Add #4, R2	
	Decrement R1	
	Branch>0 LOOP	
	Move R0, SUM	

# Indexed Addressing

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Offset is given as a constant

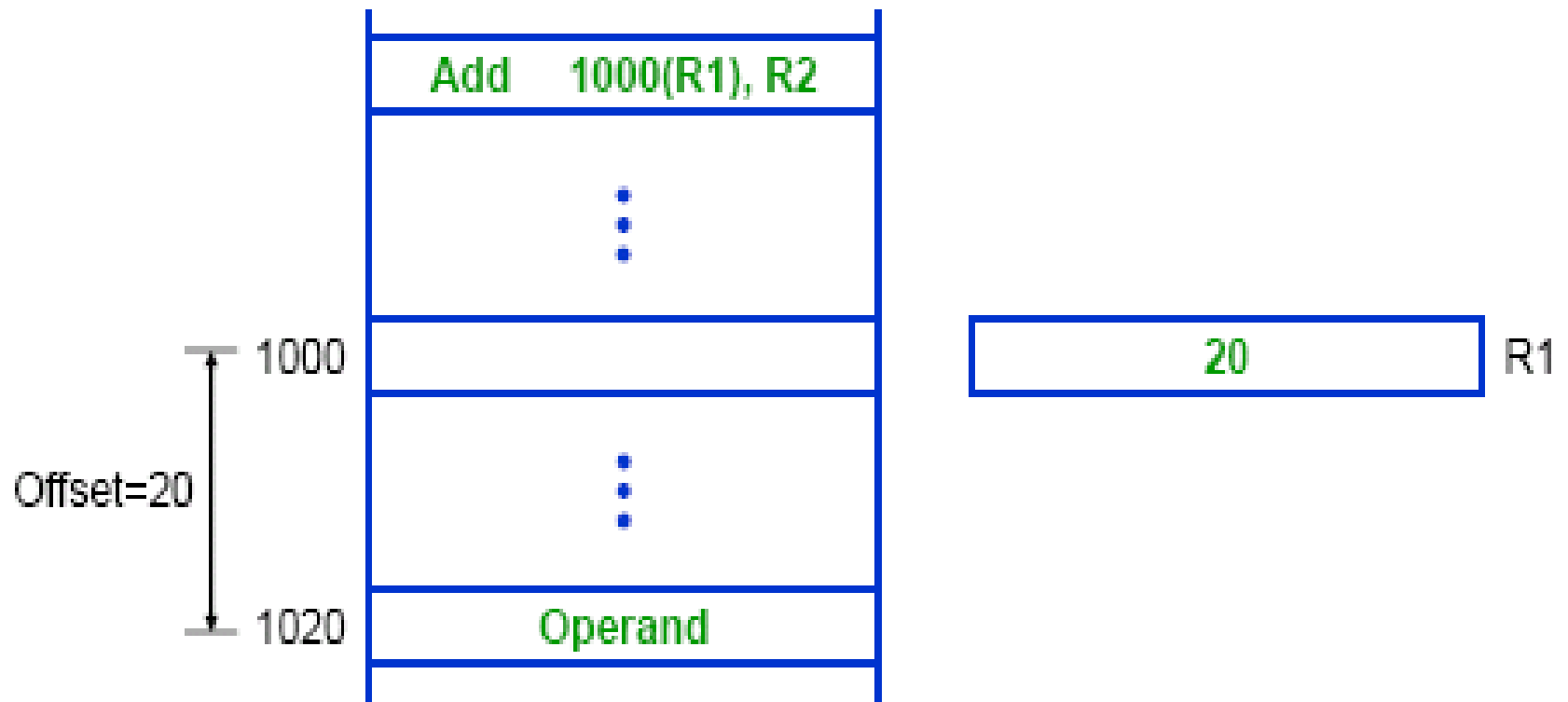




# Indexed Addressing

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Offset is in the index register



# An Example for Indexed Addressing

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N	<i>n</i>
LIST	Student ID
LIST+4	Test 1
LIST+8	Test 2
LIST+12	Test 3
LIST+16	Student ID
	Test 1
	Test 2
	Test 3
	⋮

	Move	#LIST, R0
	Clear	R1
	Clear	R2
	Clear	R3
	Move	N, R4
→ LOOP	Add	4(R0), R1
	Add	8(R0), R2
	Add	12(R0), R3
	Add	#16, R0
	Decrement	R4
→	Branch>0	LOOP
	Move	R1, SUM1
	Move	R2, SUM2
	Move	R3, SUM3

# An Example of Autoincrement Addressing

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	Move	N, R1
	Move	#NUM1, R2
	Clear	R0
→ LOOP	Add	(R2)+, R0
	Decrement	R1
	Branch>0	LOOP
	Move	R0, SUM

# Assembler

100	Move N, R1
104	Move #NUM1, R2
108	Clear R0
112	Add (R2), R0
116	Add #4, R2
120	Decrement R1
124	Branch>0 LOOP
128	Move R0, SUM
132	
	⋮
UM 200	
N 204	100
	⋮

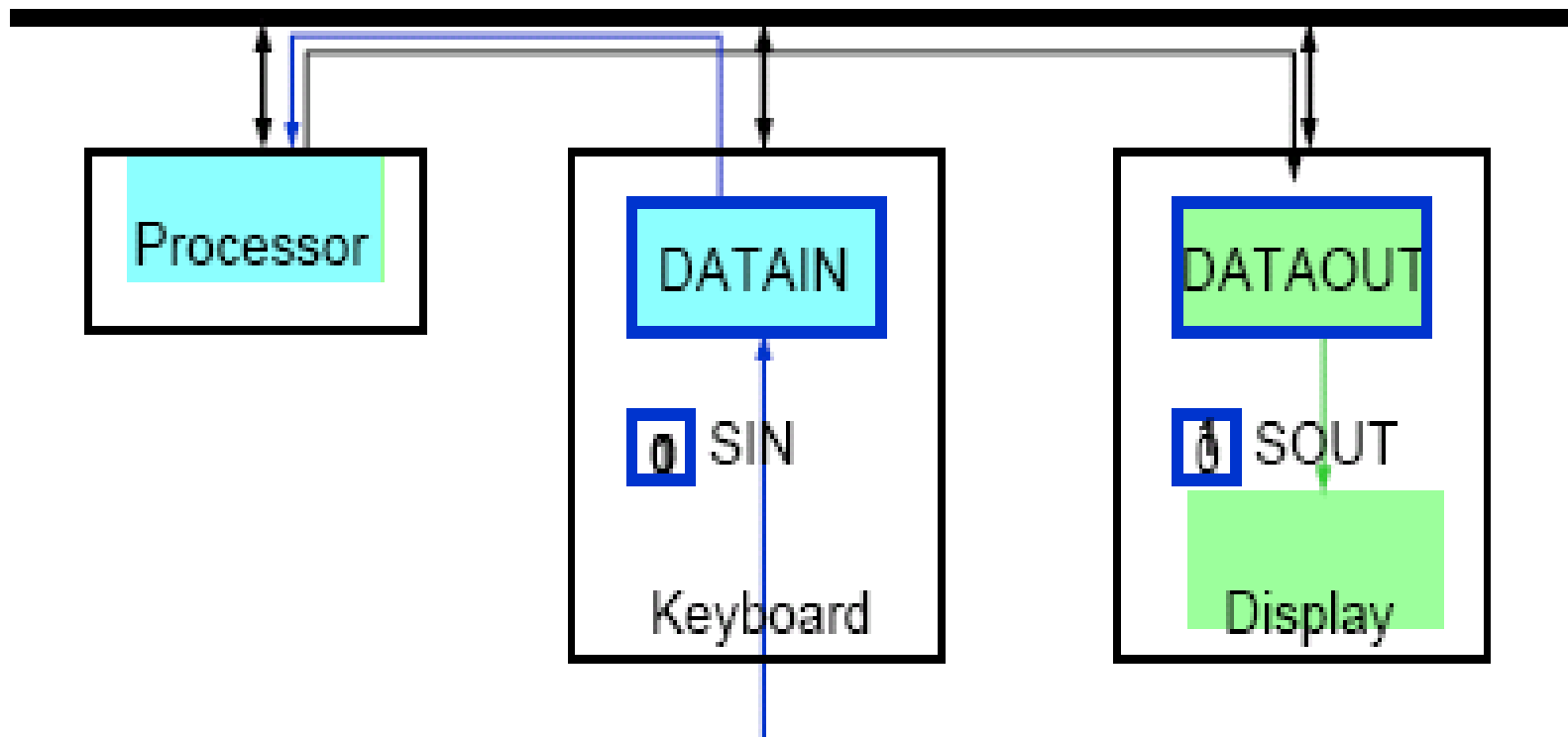
Memory arrangement

Assembler directives	SUM	EQU	200
		ORIGIN	204
	N	DATAWORD	100
	NUM1	RESERVE	400
Statements that generate machine instructions		ORIGIN	100
	START	MOVE	N, R1
		MOVE	#NUM1, R2
		CLR	R0
	LOOP	ADD	(R2), R0
		ADD	#4, R2
		DEC	R1
Assembler directives		BGTZ	LOOP
		MOVE	R0, SUM
		RETURN	
		END	START

Assembly language representation

# Basic Input/Output Operations

- Bus connection for processor, keyboard, and display



DATAIN, DATAOUT: buffer registers  
SIN, SOUT: status control flags

# Read and Write Programs

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➤ Assume that bit  $b_3$  in registers INSTATUS and OUTSTATUS corresponds to SIN and SOUT, respectively

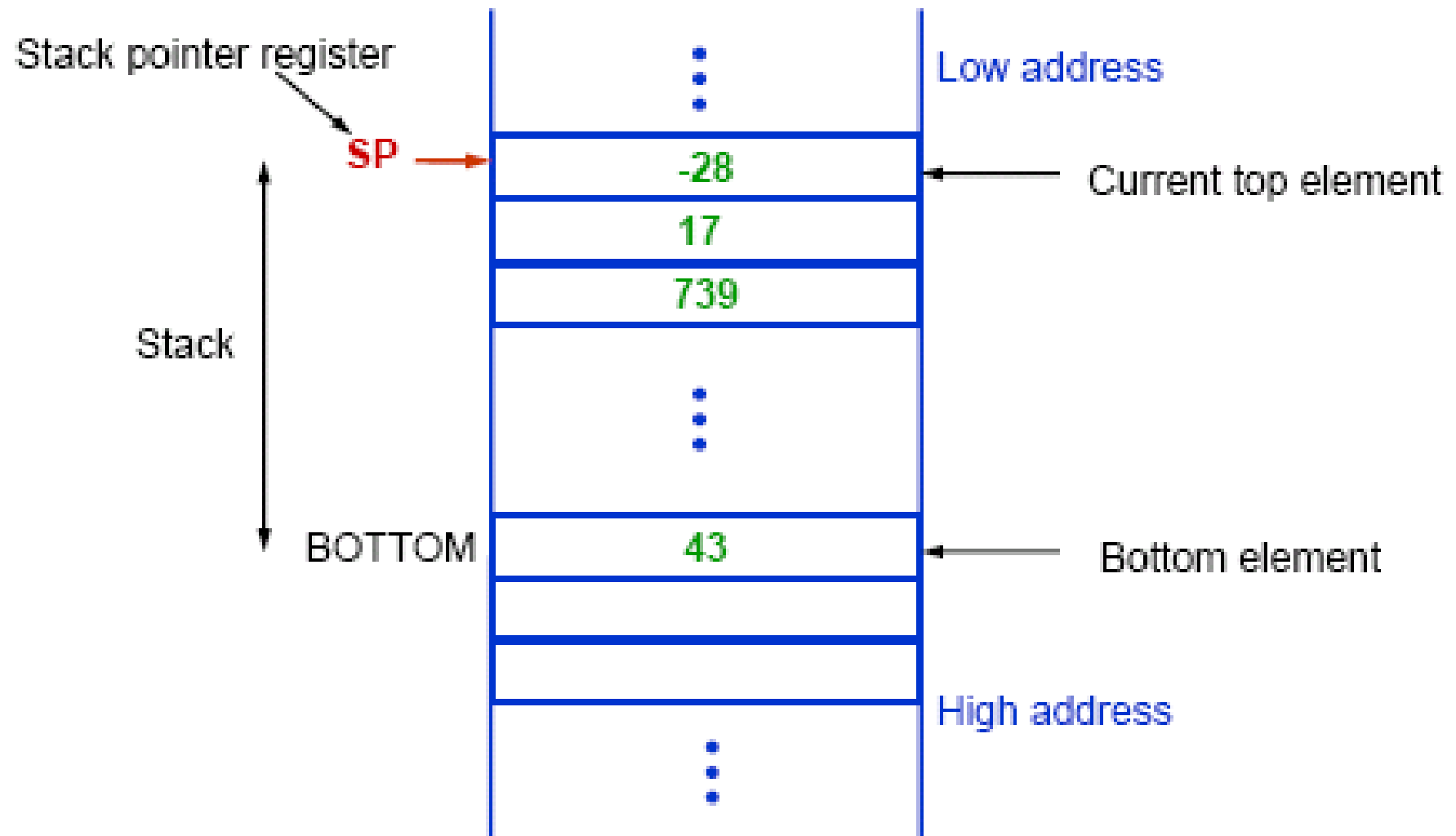
➤ Read Loop

- ◆ READWAIT    Testbit    #3, INSTATUS  
                 Branch=0   READWAIT  
                 MoveByte   DATAIN, R1

➤ Write Loop

- ◆ WRITEWAIT   Testbit    #3, OUTSTATUS  
                 Branch=0   WRITEWAIT  
                 MoveByte   R1, DATAOUT

# A Stack of Words in the Memory



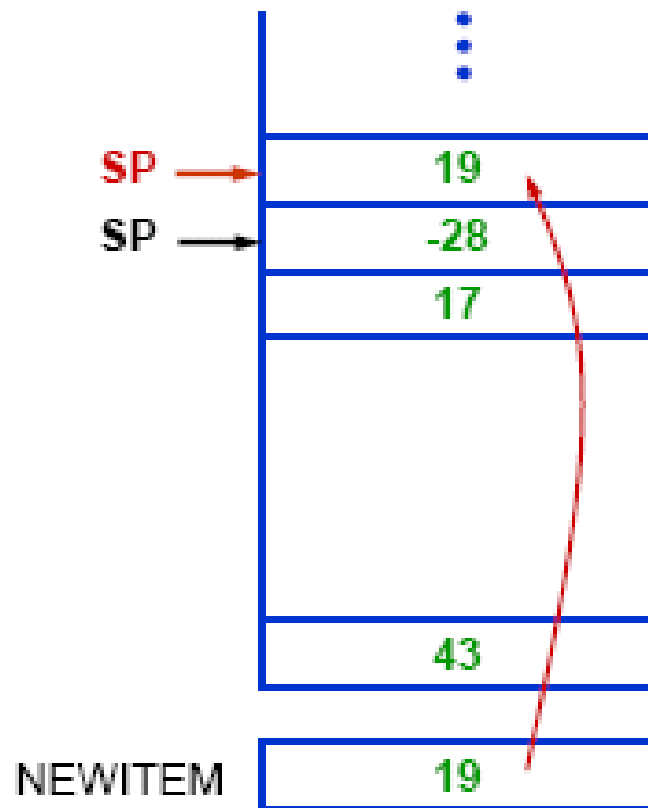
# Push and Pop Operations

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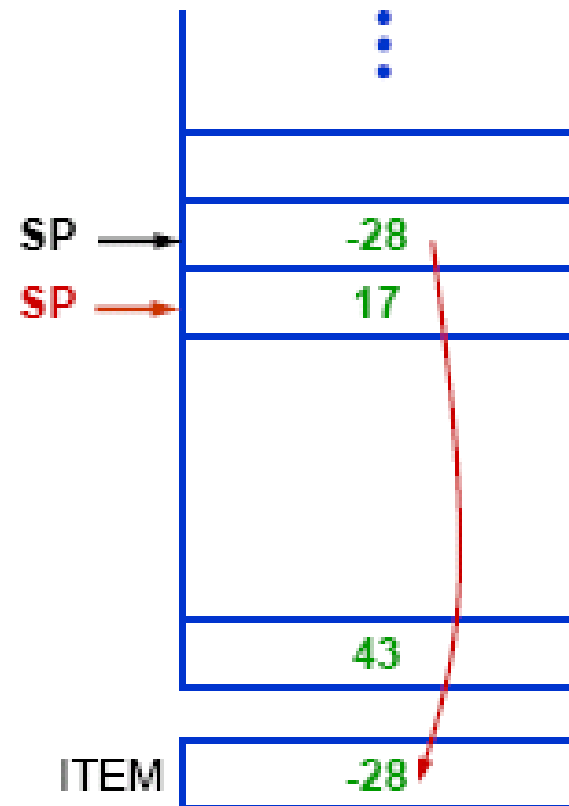
- Assume that a byte-addressable memory with 32-bit words
- The push operation can be implemented as
  - Subtract #4, SP
  - Move NEWITEM, (SP)
- The pop operation can be implemented as
  - Move (SP), ITEM
  - Add #4, SP
- If the processor has the Autoincrement and Autodecrement addressing modes, then the push operation can be implemented by the single instruction
  - Move NEWITEM, -(SP)
- And the pop operation can be implemented as
  - Move (SP)+, ITEM



# Examples



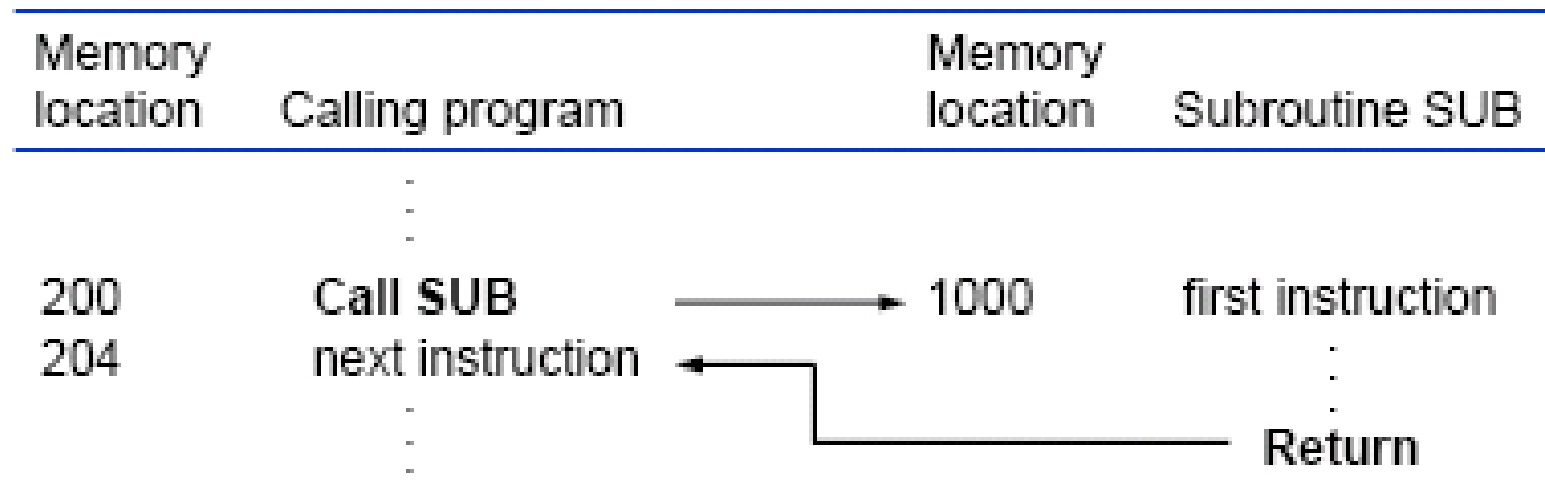
Push operation



Pop operation

# Subroutines

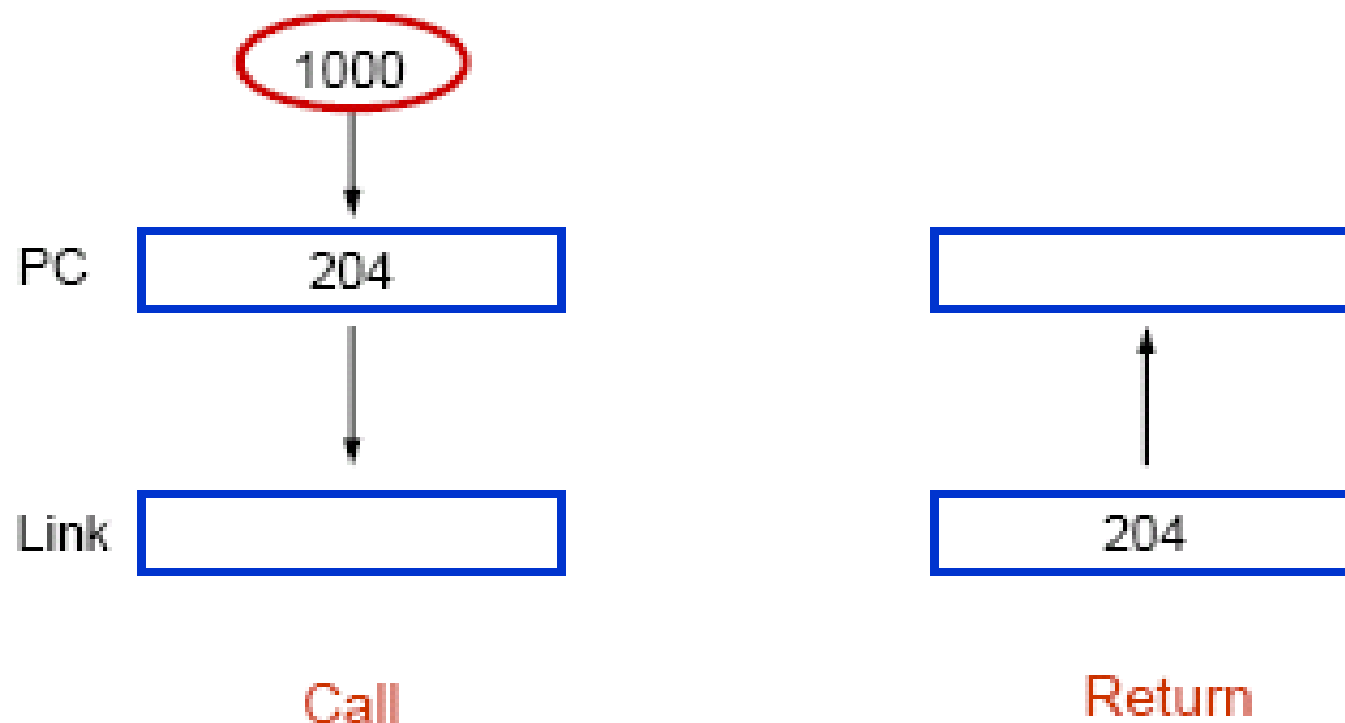
- In a given program, it is often necessary to **perform a particular subtask many times** on different data values. Such a subtask is called a *subroutine*.



- The location where the calling program resumes execution is the location pointed by the updated PC while the Call instruction is being executed. Hence the contents of the PC must be saved by the Call instruction to enable correct return to the calling program

# Subroutine Linkage

- The way in which a computer makes it possible to call and return from subroutines is referred to as its subroutine linkage method
- Subroutine linkage using a link register

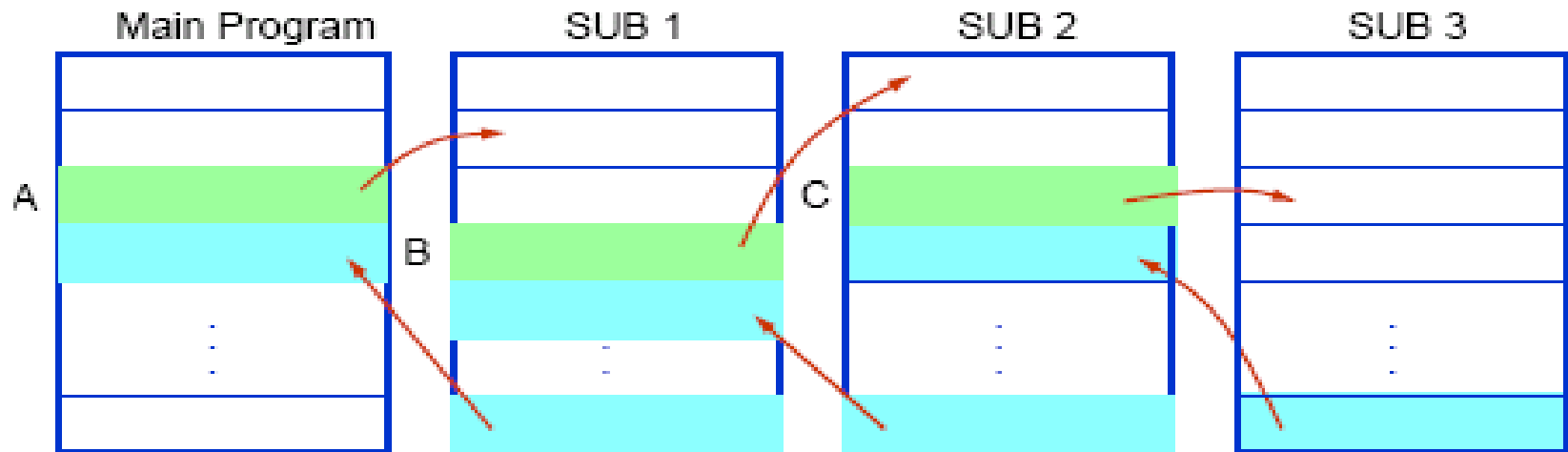


## Subroutine Nesting

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- A common programming practice, called subroutine nesting, is to have one subroutine call another
- Subroutine nesting can be carried out to any depth. Eventually, the last subroutine called completes its computations and returns to the subroutine that called it
- The return address needed for this first return is the last one generated in the nested call sequence. That is, return addresses are generated and used in a last-in-first-out order
- Many processors do this by using a stack pointer and the stack pointer points to a stack called the processor stack

# An Example of Subroutine Nesting



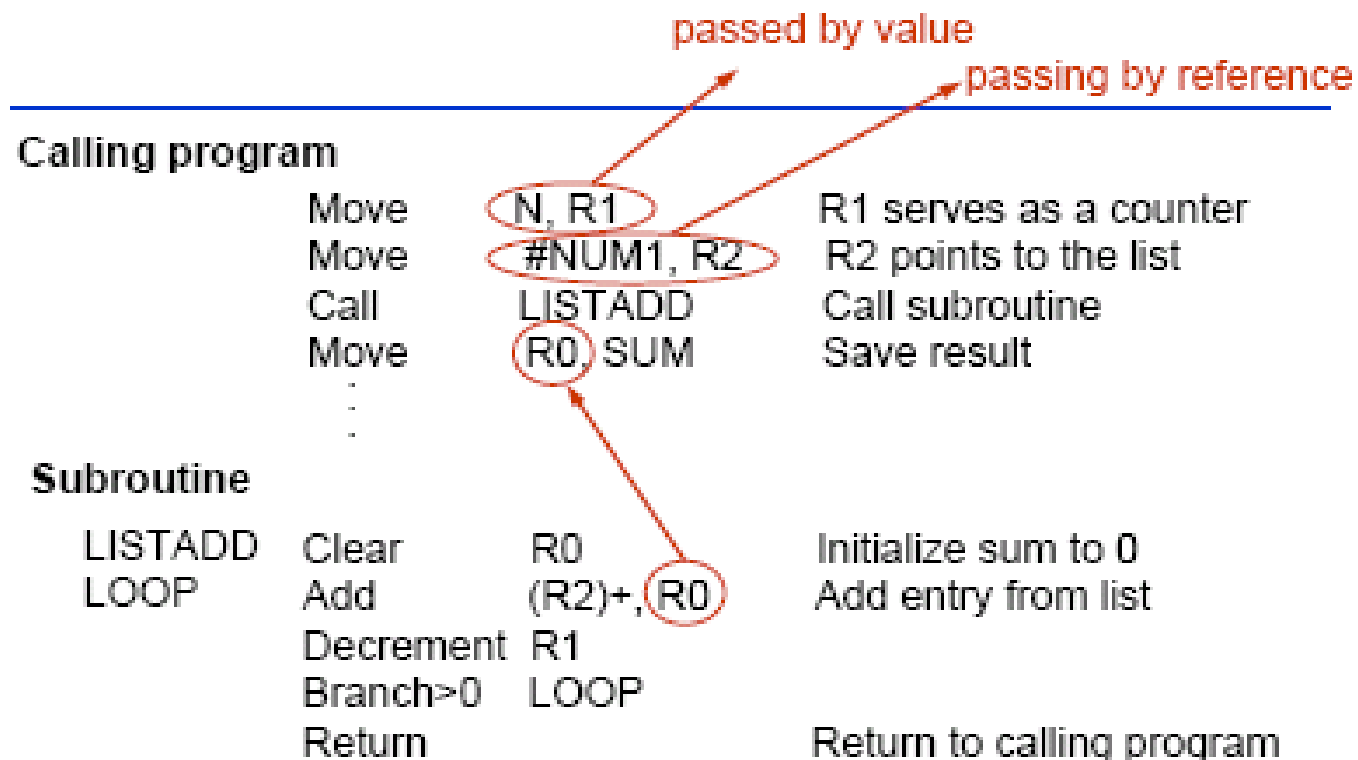
C+4
<b>B+4</b>
<b>A+4</b>

## Parameter Passing

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- When calling a subroutine, a program must provide to the subroutine the parameters, that is, the operands or their addresses, to be used in the computation. Later, the subroutine returns other parameters, in this case, the result of computation
- The exchange of information between a calling program and a subroutine is referred to as parameter passing
- Parameter passing approaches
  - ◆ The parameters may be placed in registers or in memory locations, where they can be accessed by the subroutine
  - ◆ The parameters may be placed on the processor stack used for saving the return address

# Passing Parameters with Registers



# Passing Parameters with Stack

Assume top of stack is at level 1 below.

Move	#NUM1, -(SP)	Push parameters onto stack
Move	N, -(SP)	
Call	LISTADD	Call subroutine

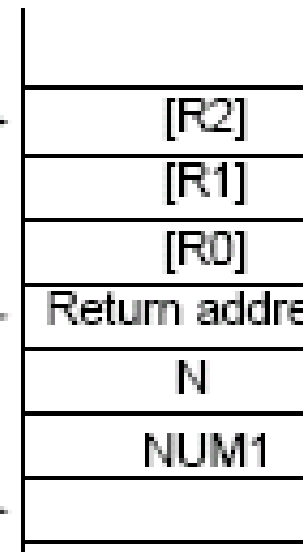
(top of stack at level 2)

Move	4(SP), SUM
Add	#8, SP

Save result

Restore top of stack  
(top of stack at level 1)

Level 3 →



LISTADD MoveMultiple R0-R2, -(SP)

Save registers  
(top of stack at level 3)

Level 2 →

Move	16(SP), R1
------	------------

Initialize counter to N.

Move	20(SP), R2
------	------------

Initialize pointer to the list

Clear	R0
-------	----

Initialize sum to 0

Level 1 →

LOOP Add (R2)+, R0

Add entry from list

Decrement	R1
-----------	----

Branch>0	LOOP
----------	------

Move	R0, 20(SP)
------	------------

Put result on the stack

MoveMultiple	(SP)+, R0-R2
--------------	--------------

Restore registers

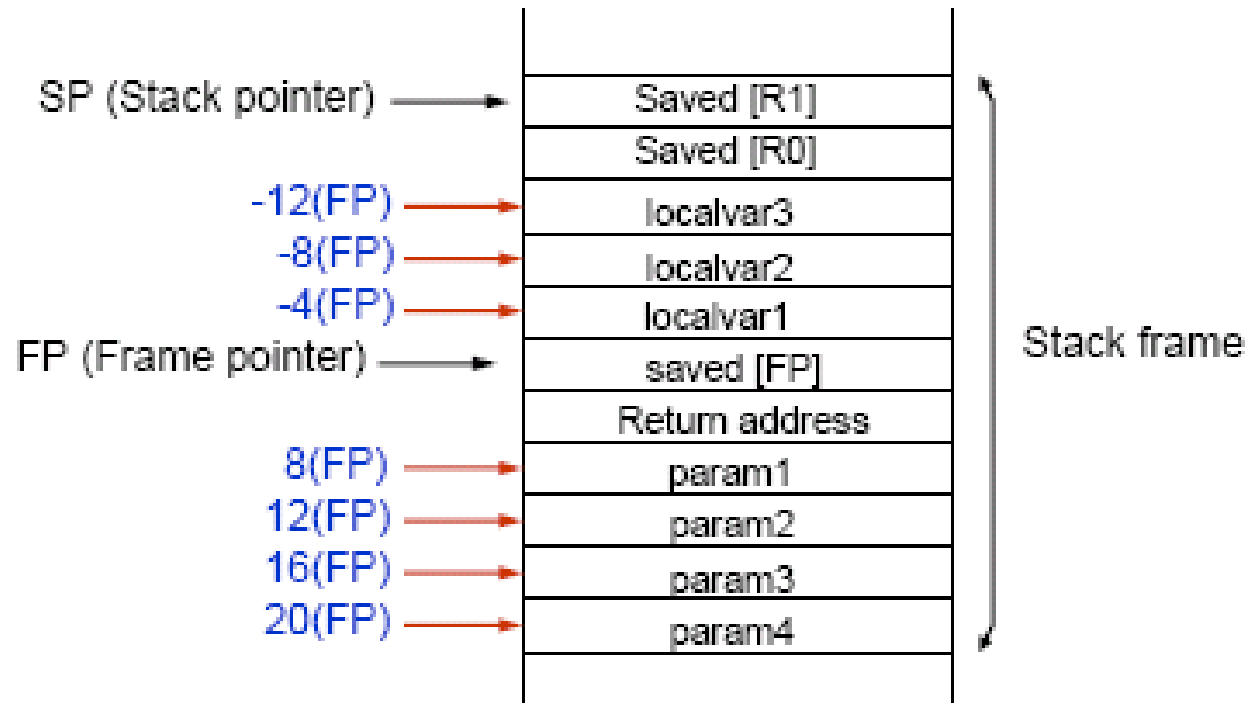
Return	
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Return to calling program



# Stack Frame

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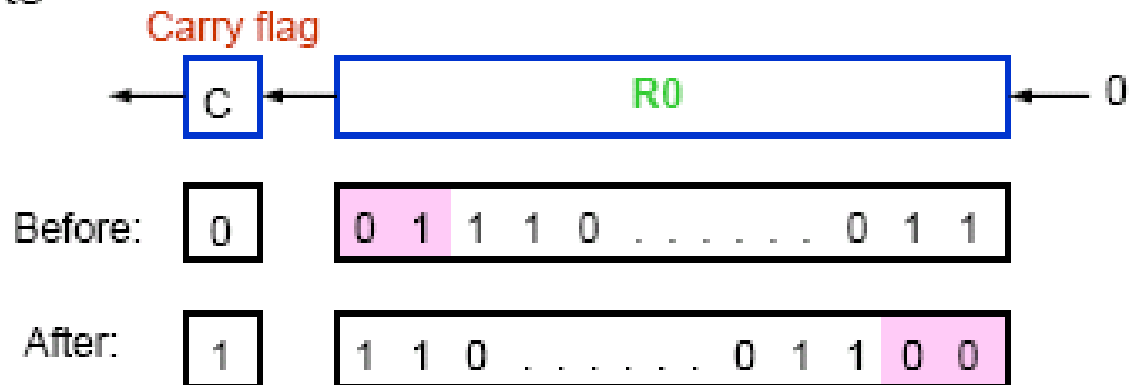


# Shift Instructions

## ➤ Logical shifts

### Logic shift left

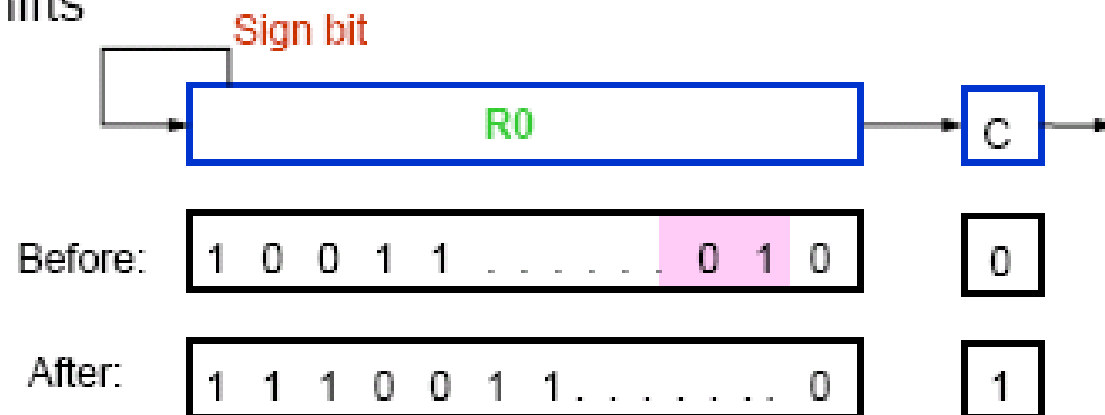
LShiftL #2, R0



## ➤ Arithmetic shifts

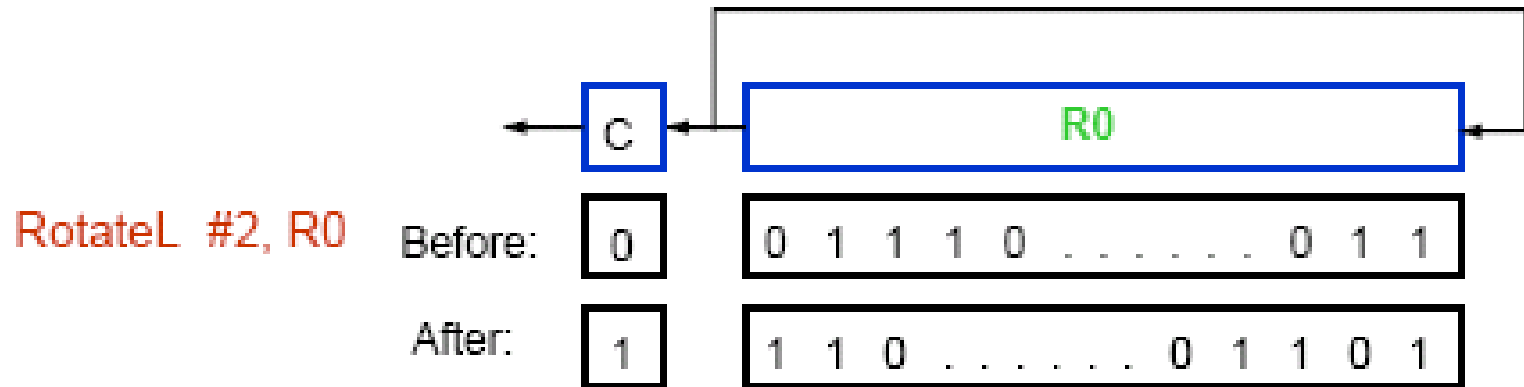
### shift right

AShiftR #2, R0

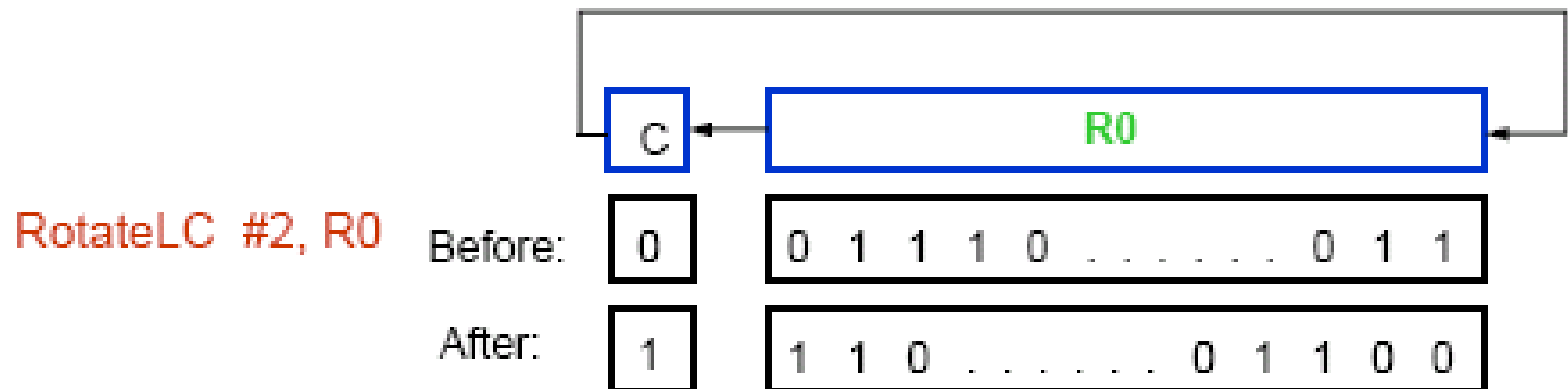


# Rotate Instructions

- Rotate left without carry



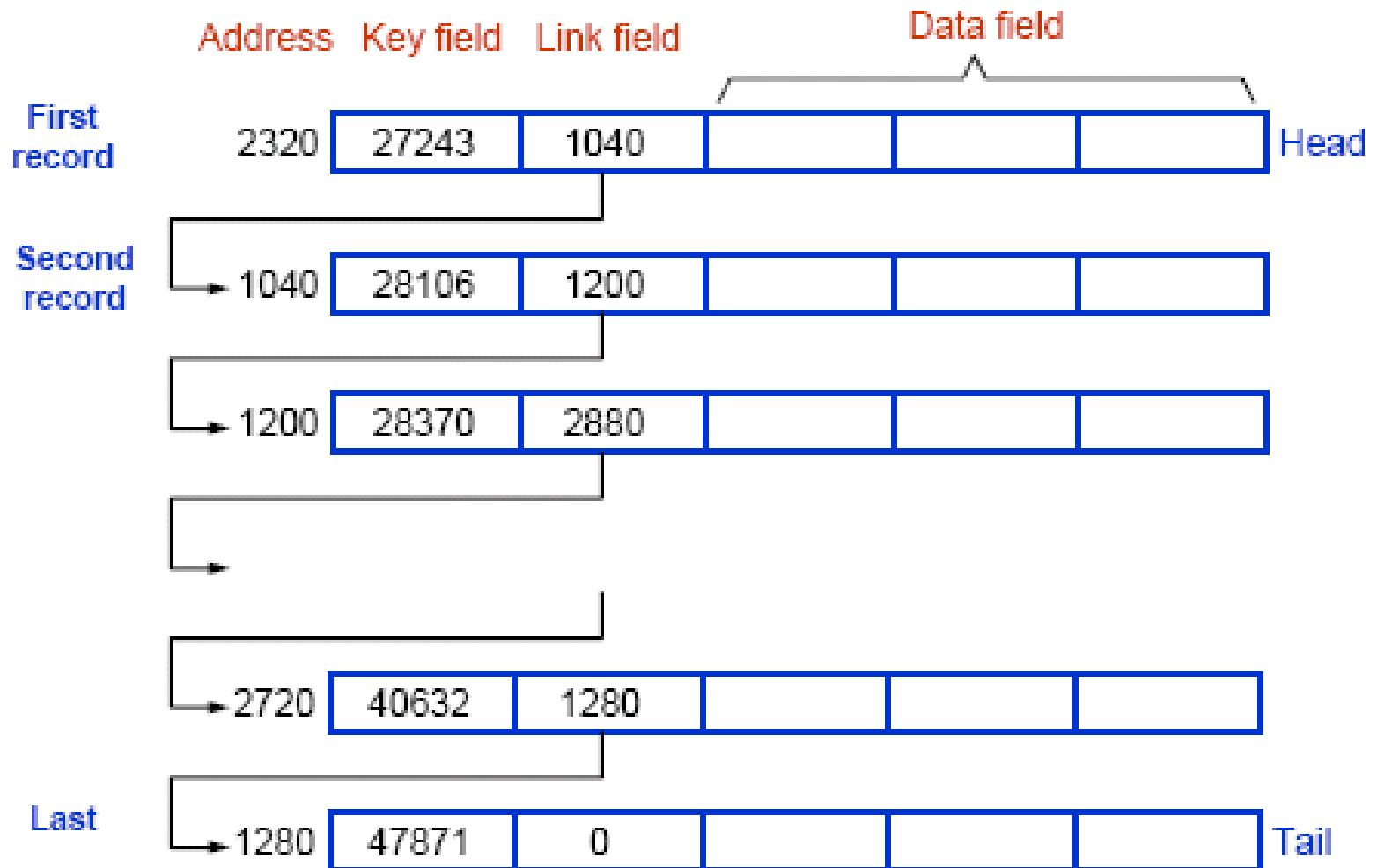
- Rotate left with carry



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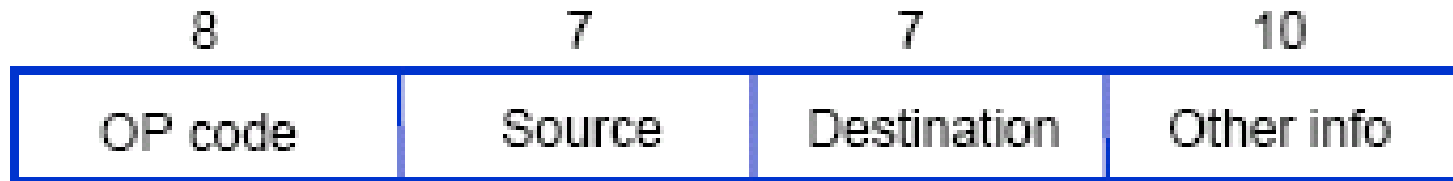


# A List of Student Test Scores

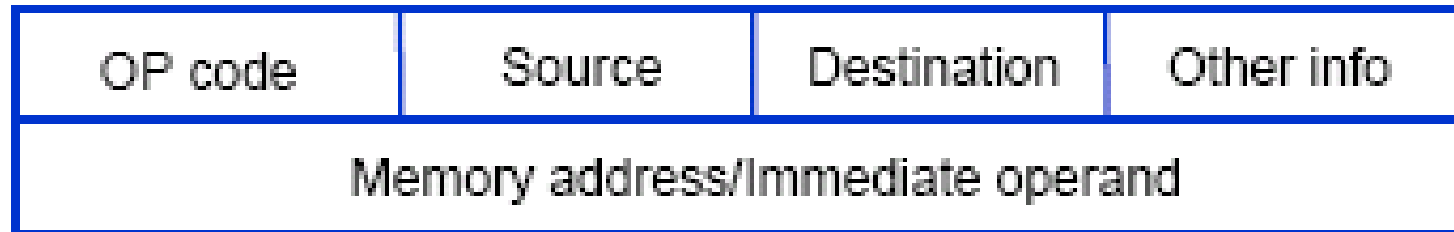


# Encoding Instructions into 32-bit Words

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One-word instruction



Two-word instruction



Three-operand instruction

# Encoding Instructions into 32-bit Words

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- But, what happens if we want to specify a memory operand using the Absolute addressing mode?
- The instruction `Move R2, LOC`
  - ◆ Require 18 bits to denote the OP code, the addressing modes, and the register
  - ◆ The leaves 14 bits to express the address that corresponds to LOC, which is clearly insufficient
- If we want to be able to give a complete 32-bit address in the instruction, an instruction must have two words
- If we want to handle this type of instructions: `Move LOC1, LOC2`
  - ◆ An instruction must have three words

# CISC & RISC

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- Using multiple words, we can implement quite complex instructions, closely resembling operations in high-level programming language
- The term *complex instruction set computer* (CISC) has been used to refer to processors that use instruction sets of this type
- The restriction that an instruction must occupy only one word has led to a style of computers that have become known as *reduced instruction set computer* (RISC)