KLE Society’s

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## ADLD-Team 2

## 4x4 Vedic Multiplier

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**PROBLEM STATEMENT**

**DESIGN OF 4X4 VEDIC MULTIPLIER IN VERILOG.**

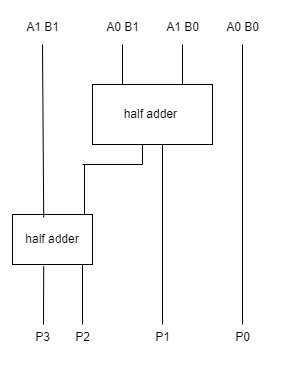
# ABSTRACT

A 4x4 Vedic Multiplier is a high-speed multiplication circuit based on the ancient Indian Vedic mathematics technique. This technique involves breaking down the multiplication process into smaller steps, making it faster and more efficient than conventional multiplication methods. The 4x4 Vedic multiplier is designed to perform multiplication operations on two 4-bit binary numbers, using only basic logic gates and a few additional components.

It is a general multiplication formula applicable to all cases of multiplication. It literally means Vertically and Crosswise. The multiplication of two operands using Vedic Multiplier is achieved by multiplication by Vertically and Crosswise and then adding all the results.

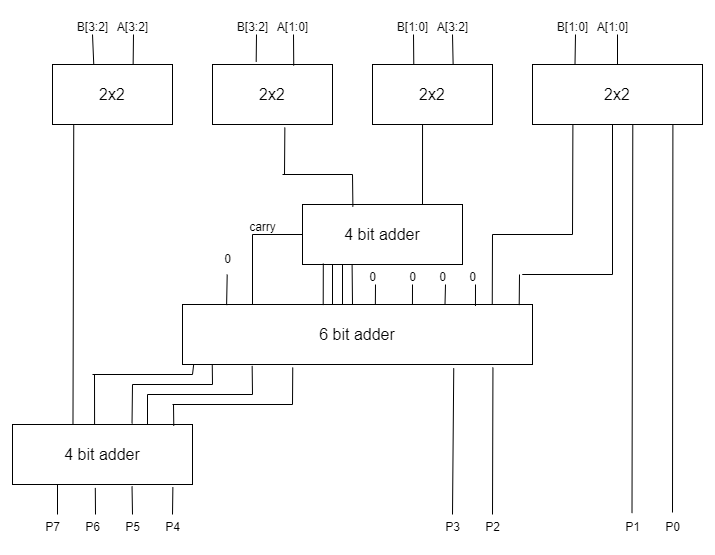
# ARCHITECTURE

2X2 VEDIC MULTIPLIER:



Above figure shows the block diagram of 2x2 Vedic Multiplier which involves AND operation and half adders.

**4X4 VEDIC MULTIPLIER**

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Overall arichetucture of 4x4 Vedic Multiplier.

**THEORY**

* The ancient vedic mathematics has a set of 16 sutras and 13 subsutras. These sutras give suitable method for arithmetic calculations. The vedic formulas requires less time than the regular formulas or method of calculations.
* Multiplier is an important block in many digital systems. We have

presented a 4-bit vedic multiplier using Urdhva Tiryagbhyam sutra of ancient vedic mathematics.

* The 4-bit vedic multiplier is implemented using 2-bit multipliers and adders.
* The 2-bit multipliers are basic blocks in the design by which the input bits are multiplied and their result are added by using the half adders.
* Firstly, the Least Significant Bits are multiplied which gives the Least Significant Bit (LSB) of the final product (vertical).
* Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier

and next higher bit of the multiplicand (crosswise).

* The sum gives second bit of the final product and the carry is

added with the partial product obtained by multiplying the

most significant bits to give the sum and carry.

* The sum is the third corresponding bit and carry becomes the fourth bit of the final product.
* In case of 4 bit multiplier we divide the no. of bits in the inputs equally in two parts.
* We analyze 4x4 bit multiplication by taking multiplicand A=A3A2A1A0 and multiplier B= B3B2B1B0.
* Following are the output line for the multiplication result,

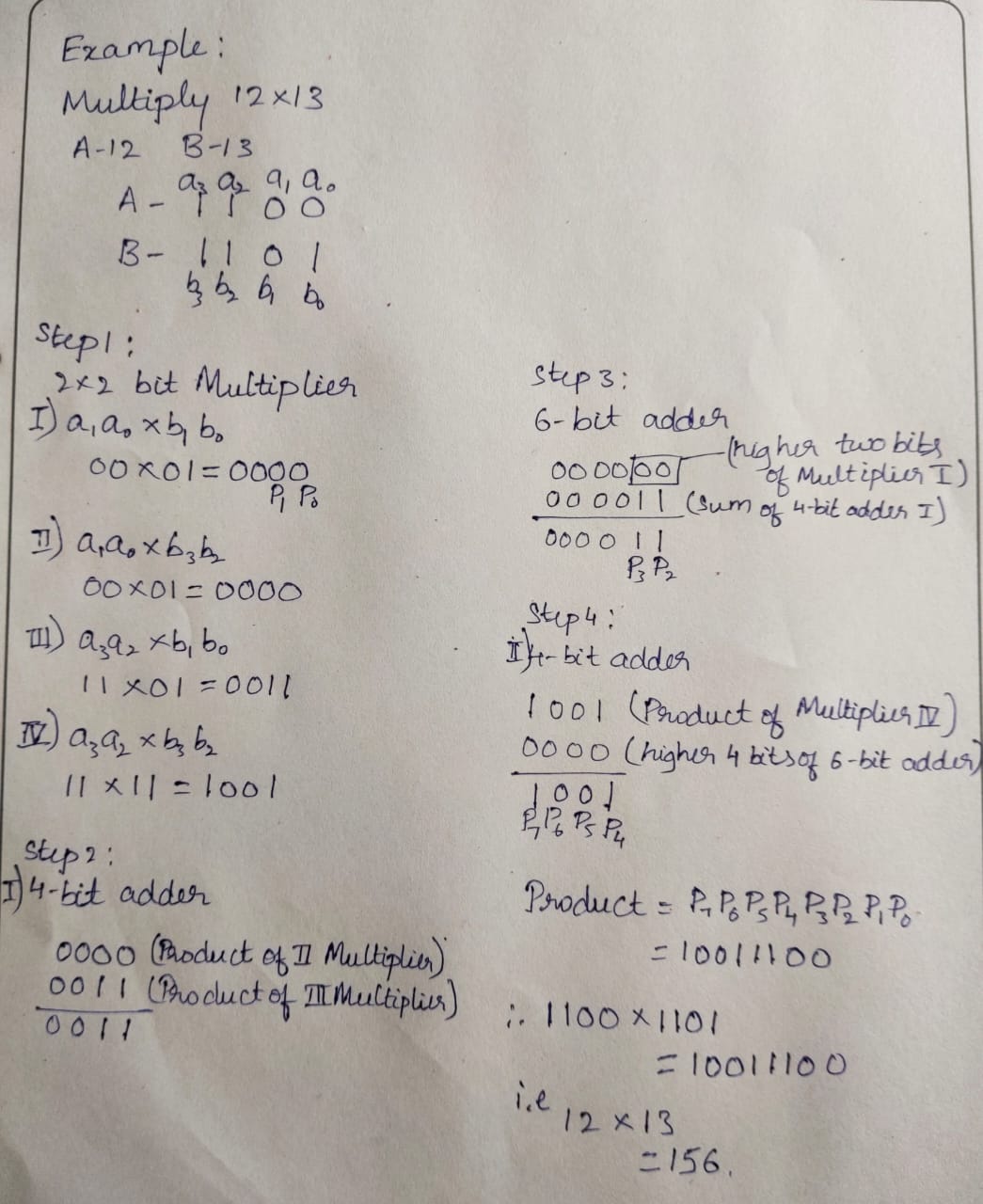
P7P6P5P4P3P2P1P0.

* The “Urdhva Tiryakbhyam” is vedic sutra which means vertical and crosswise multiplication.
* This multiplication formula is equally applicable to all

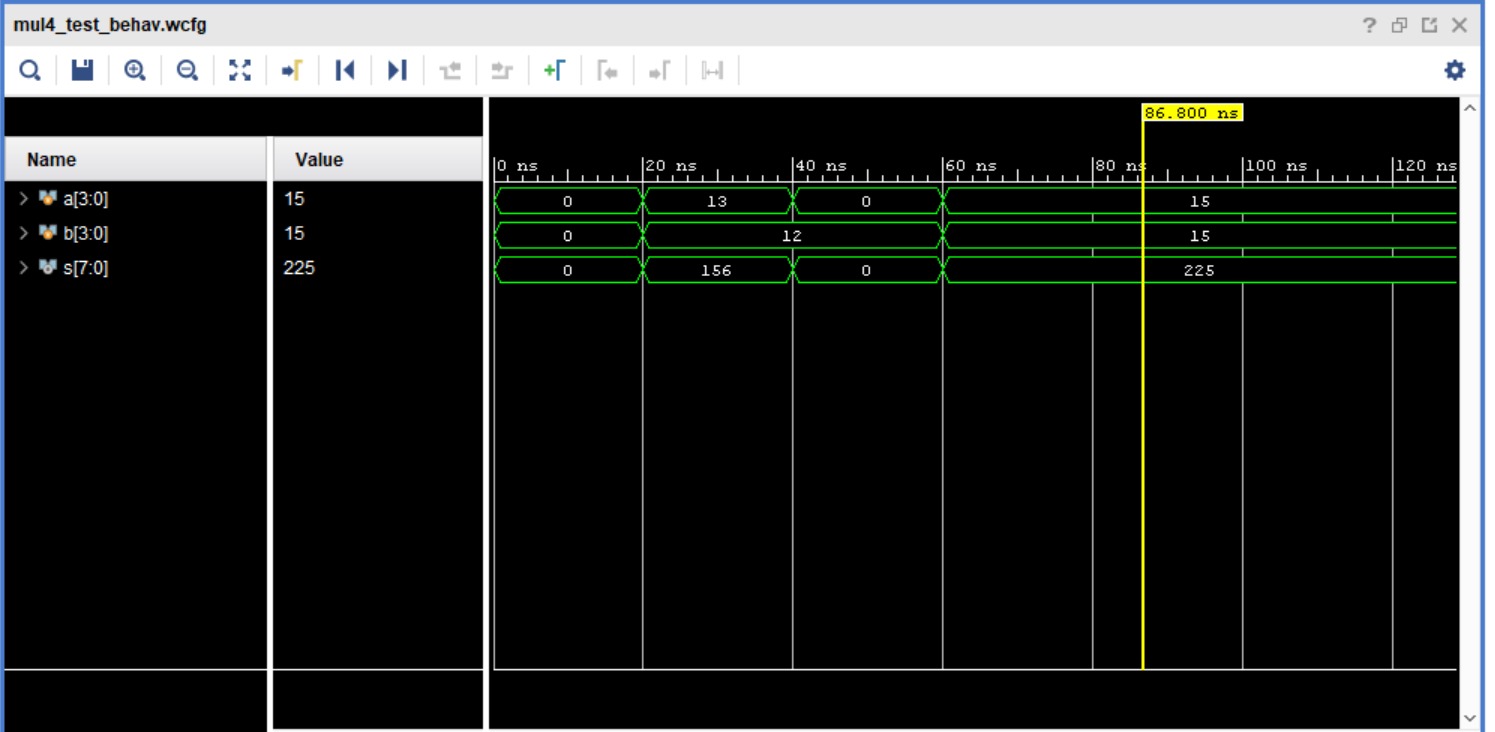
cases of algorithm for N bit numbers.

* Conventionally this sutra is used for the multiplication of two numbers in decimal number system.
* The same concept can be applicable to binary number system as we did in case of vedic mulitiper.

**EXAMPLE:**

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**RESULTS:**

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**EX: 13 X 12 = 156**

**CONCLUSION**

* In this architecture first partial products are obtained by 2x2 multipliers and then these partial products are added to obtain the result.
* In conclusion, Vedic multiplication is a fast multiplication algorithm based on ancient Indian mathematics. It involves breaking down the multiplication process into simpler steps.