



DATASHEET

SIC 4340

228-Byte ISO14443A RFID/NFC Tag IC
with built in ADC for chemical sensor interface

Rev 1.3

Features Summary

Sensor Interface Peripheral

- Resistive/Capacitive sensor interface circuit
 - Resistance-to-Voltage measurement by dumping current source
 - Effective resistance range from 1kΩ to 300kΩ
- Built-in current DAC for sensor biasing
 - 6 bits resolutions
 - 2 Ranges selectable
 - 0 – 504 μA with 8μA /Step
 - 0 – 63 μA with 1μA /Step
 - Waveform biasing selectable
 - DC biasing
 - Square wave biasing with selectable frequency 300 Hz – 50 kHz
- Built-in Oversampling ADC
 - Selectable effective resolution
 - 10 bits / 9 bits / 8 bits
 - Internal voltage reference 1.28 V
 - 3 channels input selectable.
 - Conversion rate up to
 - 48 Samplings/Sec for 10 bits effective
 - 96 Samplings/Sec for 9 bits effective
 - Single-Ended mode / Differential mode selectable.
 - Selectable post processing with average function.
 - Configurable built-in voltage buffer for high-impedance sensor.
- Adjustable timing for pre-biasing sensor before ADC conversion
 - 8 – 491,528 clock
 - 160 uS to 9.8 Sec based on 50 kHz clock

RF Interfaces & Other peripheral

- RF interface based on ISO14443A – 106 kbps
- NFC Forum tag type 2
- RF power qualifying scheme before operation
- On-chip 1.9 V regulator with output current load capacity 3.0 mA

Memory

- 236 bytes addressable EEPROM
- 192 bytes user memory EEPROM
- EEPROM organization enabling NDEF format
- EEPROM erase/write cycle up to 100,000 times
- EEPROM memory retention up to 10 years at 70°C
- EEPROM zone for initializing register
 - Automatically reload after power up

Operating Conditions

- Operating temperature from 0 to 55°C *

Package Information

- 16 Lead QFN 3x3 mm

Die Information

- Die size : 1200 um x 1200 um
- No. of Pad : 8 Pads
- Au pad size : 80 um x 80 um

Applications

- Chemical sensor NFC tag
- Tampered detection NFC tag
- Light/Humidity sensing NFC tag
- Closed Chamber Measurement

Revision History

Revision	Date	Description	Change/Update/Comment
1.0	22 Jan 2019	1 st Release	- Initial Release
1.1	19 Dec 2019	Updated Version	- Update Ordering Information
1.2	10 Jan 2020	Updated & Error Correction	- Update Ordering Information. - Update Feature summary
1.3	20 Feb 2020	Error Correction	- LDO Load Regulation

Ordering Information

Part No.	Description	Package	Marking	Product Status
P002HS4340X2QFN3-01	SIC4340, 16L QFN 3x3 mm package, Canister.	16L QFN 3x3 mm	434X YYMM	Active
P002HS4340X2DOWTB-01	SIC4340, Die on wafer with Au Bump, 12 inches wafer	Die on Wafer with Au Bump		Active
P002HS4340X2DOWTB-02	SIC4340, Die on wafer with Au Bump, 12 inches wafer with UV sheet	Die on Wafer with Au Bump and UV sheet		Active

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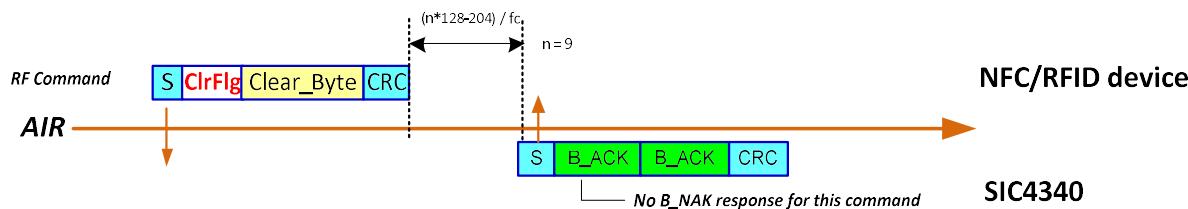


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0. Notation

0.1 Styles and Fonts for key words

This part defines styles and fonts used for the key words throughout this document. The key words are names of signal, register, pin, state of operation and command. The styles, fonts, and their indications are shown in Table 0-1.

Table 0-1: Style and Fonts key word

Symbol	Indication
<u>Signal</u>	Signal name
Register	Register name or Bit name
pin RX	Pin name
"State of Operation"	State of operation
Command	Command name for RF interface and µART interface
"Flag"	Flag name in B_ACK or B_NAK response

- To refer to a register address and a value in a register, a hexadecimal number proceeding with letter “0x” is used, for example 0x0A.
- To refer to a bit located in a register address, a symbol “.” following by a number reflecting the bit location starting from 0 to 7 is used. For example, 0x0A.0 refers to bit 0, least significant bit, in the register 0x0A.
- To refer to a set of consecutive bits located in a register address, a format “[msb:lsb]” is used after a register value. For example, a value of 0x0A.[3:0] refers to bit 3 ,2, 1, and 0 in the register 0x0A.
- To refer to a binary value in some registers, the letter “b” is placed at the end of the binary number, for example “1010b”.
- To refer to logic level, the number in single quote ‘1’ and ‘0’ are used to refer to binary logic level.

0.2 Abbreviation

Table 0-2: Abbreviation

Abbreviation	Term
ACK	Acknowledge
ADC	Analog-to-Digital converter
AFE	Analog-Front-End
B_ACK	Byte Acknowledge
B_NAK	Byte Negative Acknowledge
CRC	Cyclic redundancy check
DAC	Digital-to-Analog converter
EEPROM	Electrically Erasable Programmable Read-Only Memory
EOF	End of Frame
fc	Carrier frequency
FDT	Frame Delay time
GPIO	General Purpose Input/Output
LDO	Low-Drop-Out Regulator
NAK	Negative Acknowledge
OTP	One-time program
QFN	Quad-flat no-leads package
SOF	Start of Frame
UID	Unique Identifier

1. Functional Overview

SIC4340 is a 228-byte NFC tag IC for resistive/capacitive sensor interface which can apply for chemical sensor, light sensor etc. The SIC4340 consists of an NFC Analog-Front-End circuit supporting ISO14443A, a selectable 5-to-10 bit resolution sigma-delta ADC, an on-chip regulator, a sensor interface circuit, a temperature compensate voltage reference, a control register page and an EEPROM. The SIC4340 is designed to get sensor's voltage response at specific time after biasing. The sensor can be resistive, capacitive or combination of them.

1.1 Block diagram

Depict a conceptual block diagram of the SIC4340. The SIC4340 mainly consists of five parts as listed below.

- RF Analog Front End (RF-AFE)
- On-chip 1.9V LDO Regulator
- Digital Controller
- EEPROM & Charge Pump
- ADC, Sensor Biasing and Reference circuit

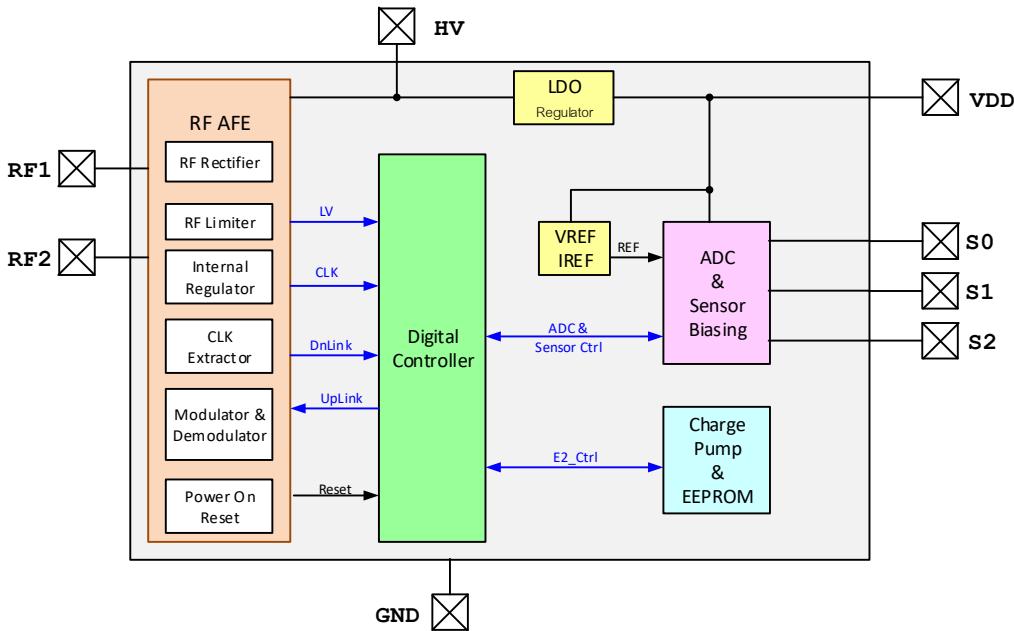


Figure 1-1: Functional block diagram

1.1.1 RF Analog-Front-End (RF-AFE)

The RF Analog-Front-End (RF-AFE), where RF1 and RF2 terminals connect to an external coil, harvests RF power to supply the internal circuit by RF rectifier. Rectifier output is directly connected to pin **HV** that can be connected with external 100-nF capacitor for more power stability. Also, the RF-AFE provides facilities for RF communication such as Modulator/Demodulator for uplink and downlink data communication, a clock extractor for the system clock and data synchronization. RF Limiter protects circuit for over voltage due to excessive power. Internal regulator generates power supply (LV) for digital controller, while Power-On-Reset detects the DC supply level that enough for operation.

1.1.2 On-chip 1.9V LDO Regulator

Provided that the input RF power is high enough, the on-chip 1.9V Low-Drop-Out (LDO) regulator provides a stable power supply voltage for internal reference, ADC, and sensor biasing circuit. A regulator output is connected to pin **VDD** that required external capacitor 100nF for more reliable ADC-result. The LDO regulator can be enabled or disabled via a control register.

1.1.3 Digital controller

The digital controller manipulates data transactions between the external interfaces (RF), internal memory (EEPROM), ADC, and sensor. Digital controller handles operations as follows.

- Decoding incoming RF downlink commands and encoding RF uplink data
- Reading and programing data from/to EEPROM.
- Controlling Sensor bias circuit.
- Handling ADC operation and processing ADC output.

Moreover, digital controller contains control registers to configure all functional parts such as LDO, ADC, Sensor, etc.

1.1.4 EEPROM and Charge Pump

EEPROM consists of EEPROM memory blocks and high-volt generator. The EEPROM memory is applied to store UID, user data, and memory lock control to serve NFC applications. The EEPROM also contains a portion of register-reloading values for predefined the control register after power-on-reset. The on-chip high-volt charge pump generates high voltage to program and erase the EEPROM.

1.1.5 ADC, Sensor interface and reference

The sensor interface circuit contains the adjustable current source and the voltage limiter. When applying current through the sensor, the voltage response reflecting the impedance changing from chemical concentration pass to the build-in ADC. The biased sensor can be resistive, capacitive or combination of them.

ADC acquires sensor's voltage response at specific time after biasing. The selectable effective output bit of conversion data can be 5, 7, 9, or 10 bits. Based on ADC structure, the conversion time is proportional to the number of bit need to obtain and the sampling frequency. The internal reference circuit generate the reference voltage defines full-scale range of ADC.

1.2 Typical operating system

The SIC4340 operates as an RFID chip with sensor interface circuit. For more power stability, two external capacitors are optionally connected to pin **HV** and **VDD**. A loop antenna is directly connected from pin **RF1** and **RF2** for NFC communication. Sensor load that can be either resistance or capacitance load is connected between pin **S2**, **S1**, **S0** and **GND** as shown in Figure 1-2.

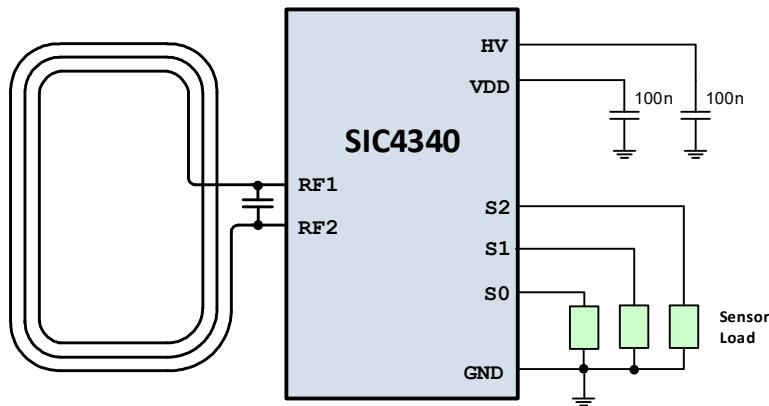


Figure 1-2: Basic SIC4340's configuration with sensor

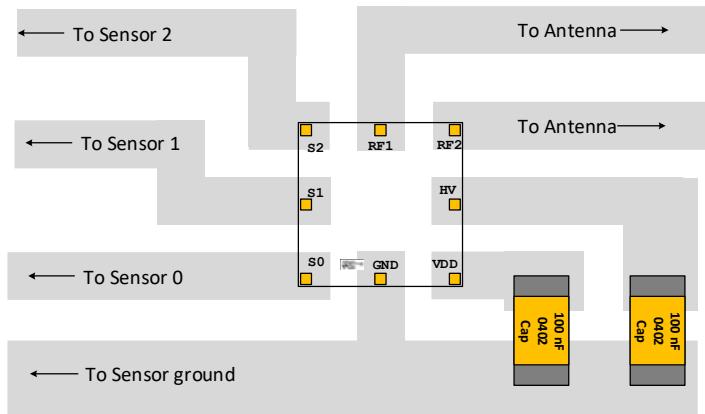


Figure 1-3: Example of Inlay with antenna and sensor interface (SIC4340 is flipped into inlay)

2.Die and Package

2.1 Die Information

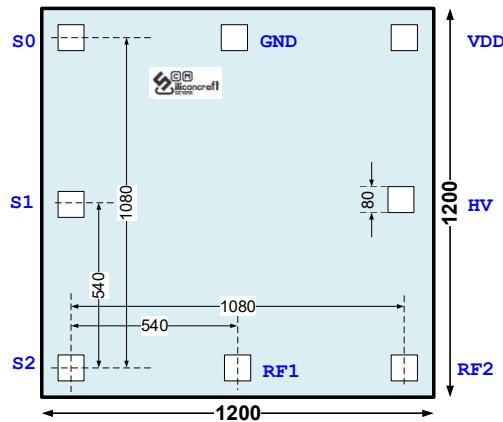


Figure 2-1: Die Information (Dimension in um)

Table 2-1: Pad description

Pad	Symbol	Type	Description
1	S0	Analog	Sensor connection pad 0
2	S1	Analog	Sensor connection pad 1
3	S2	Analog	Sensor connection pad 2
4	RF1	Power	RF-Coil connection pad 1
5	RF2	Power	RF-Coil connection pad 2
6	HV	Power	Unregulated power supply to connect with external decoupling cap
7	VDD	Power	ADC power supply to connect with external decoupling cap
8	GND	Power	Ground (Power Ground and signal ground)

2.2 Pin configuration

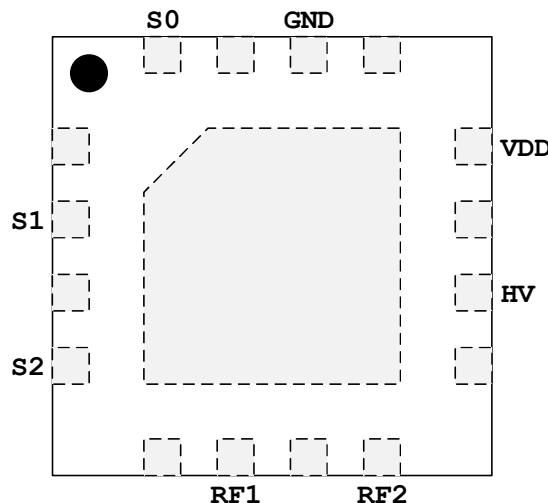


Figure 2-2: QFN 3x3 Pin arrangement (Top view)

Table 2-2: Pin description

Pin No.	Symbol	Type	Description
2	S1	Analog	Sensor connection pin 1
4	S2	Analog	Sensor connection pin 2
6	RF1	Power	RF-Coil Connection pin 1
8	RF2	Power	RF-Coil Connection pin 2
10	HV	Power	Unregulated power supply to connect with external decoupling cap
12	VDD	Power	ADC power supply to connect with external decoupling cap
14	GND	Power	Ground (power ground and signal ground)
16	S0	Analog	Sensor connection pin 0

3.Specifications

3.1 Absolute maximum rating

Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to the absolute maximum rating conditions for an extended period of time may affect the device reliability.

Only one absolute maximum rating can be applied at a time.

Table 3-1: Absolute maximum rating

Parameter	Rating
Regulated supply voltage (VDD)	-0.3 V to 2.0 V
Unregulated supply voltage (HV)	-0.3 V to 7.0 V
Input voltage (S1, T1, T2)	-0.3 V to VDD + 0.3 V
RF input current	20 mA
Operating temperature range	0 C to +55 C
Storage temperature range	-40 C to +85 C
Junction temperature	125 C
Thermal impedance (θ_{JA})(1) – QFN 3x3 – 16 pins	TBD

Note θ_{JA} is determined by 2s2p 76.2x114.3-mm PCB following JEDEC51-5, -7

3.2 Electrical characteristic

Table 3-2: Operating condition

Parameter	Description	Min	Typ	Max	Unit	Conditions
VDD	Supply voltage	1.88	1.92	1.96	V	No External Load
ESD	Electrostatic discharge tolerance	3.0			kV	HBM model

Table 3-3: RF front end characteristic

Parameter	Description	Min	Typ	Max	Unit	Conditions
f-op	RF operating frequency		13.56		MHz	
Vcoil-pp	POR threshold		6.0		Vpk-pk	
	EEPROM programming		6.0		Vpk-pk	
VRF-limit	RF Limiter Level @ 10mA input		14.0		Vpk-pk	
Vmod	Modulation Level @ 1mA input		2		Vpk-pk	
Cres	On-chip resonance capacitor	47.0	50.0	53.0	pF	
TRF_off	Minimum period for RF field-off to ensure reset	1			mS	

Table 3-4: Power consumption

Parameter	Description	Min	Typ	Max	Unit	Conditions
Idd-RF1,RF2	Power supply current into RF1, RF2		TBD		$\mu\text{A pk}$	Standalone RFID mode VDD disabled EEPROM read mode, Vrf1,2= 6 Vpk-pk
			TBD			Standalone RFID mode VDD disabled EEPROM programing mode, Vrf1,2= 6 Vpk-pk
Ivdd	No Conversion and sensor biased		30.5		μA	Power source from pin VDD ,
	ADC Conversion		437.28		μA	ISEN = 200 μA , buffer disabled
			451.88		μA	ISEN = 200 μA , buffer enabled
			166.89		μA	ISEN = 10 μA , buffer disabled
			181.49		μA	ISEN = 10 μA , buffer enabled

Table 3-5: Sensor Pin characteristic

Parameter	Description	Min	Typ	Max	Unit	Conditions
C_I/O	S1 pin capacitance		10		pF	
Vin	Analog Input Voltage Range	0		VREF	V	

Table 3-6: Operating timing

Parameter	Description	Min	Typ	Max	Unit	Conditions
Tpowerup	Startup time from power up		2	5	mS	After burst RF field until chip ready to receive command. No capacitor connected at HV

Table 3-7: EEPROM

Parameter	Description	Min	Typ	Max	Unit	Conditions
TEEprog	EEPROM programming time		3.85		mS	Programming 1 block
RFMINProg	Minimum RF voltage for programming voltage		6		Vpk-pk	
Memory Size	Total size		228		Bytes	
Twrite	Write endurance	100,000			Times	
Tmaintain	Retention	10			Years	

Table 3-8: LDO regulator

Parameter	Description	Min	Typ	Max	Unit	Conditions
VREG_IN	Regulator input voltage (HV)	2.7	3.0	7.0	V	
VDD_OUT	Regulator output voltage	1.88	1.92	1.96	V	No External Load, T = 25 C
	Regulator output voltage	1.80		2.00	V	No External Load, T = -40 C to 85 C
I_OUT	Output regulator current			3	mA	HV = 3V
$\Delta V_{outLoadReg}$	Load regulation (ΔV_{out}) : T = 25 C			10	mV	HV = 3V, Iload = 100 μ A
				20	mV	HV = 3V, Iload = 500 μ A
				40	mV	HV = 3V, Iload = 1mA
				60	mV	HV = 3V, Iload = 2mA
C_VDD	VDD decoupling capacitor	100			nF	External capacitor is optional to enhance power stability. If External capacitor is connected, capacitance should be at least C_VDD.
VDD_H	VDD level indicator (high level)	1.60	1.65	1.70	V	T = 25 C
VDD_L	VDD level indicator (low level)	1.35	1.40	1.45	V	T = 25 C

Table 3-9: Sensor Biasing Circuit (current DAC)

Parameter	Description	Min	Typ	Max	Unit	Conditions
ISEN_Resolut ion	Sensor biasing current resolution		6		bit	
ISEN_INL	Sensor biasing current - Linearity Error			0.5	LSB	T = 25 C
				1	LSB	T = 0 C to 55 C
ISEN_DNL	Sensor biasing current - Differential Linearity Error			0.5	LSB	T = 25 C
				1	LSB	T = 0 C to 55 C
ISEN_FSR	Sensor biasing current – Full scale range		63		μ A	ISEN_RNG = '0' Resolution = 1 μ A
			504		μ A	ISEN_RNG = '1' Resolution = 8 μ A
ISEN_Gn_Err	Sensor biasing current – Gain Error			+/- 0.4	%FSR	T = 25 C
				+/- 2	%FSR	T = 0 C to 55 C
ISEN_Gn_Err _Drift	Sensor biasing current – Gain Error Drift			1	% /C	
ISEN_Offset	Sensor biasing current – offset current			+/- 20	nA	
ISEN_Offset drift	Sensor biasing current – offset current drift			+ 1.8	nA / C	T = 0 to +55 C (leakage)
ISEN_PSRR	Power Supply dependent			0.5	% / V	VDD = 1.7 to 2.0 V
Vlim	Output limiting voltage	0		1.275	V	Resolution = 5mV / step
fSEN	Sensor biasing frequency	300	10k	50k	Hz	
N-warmup	Number of warmup clock	8		491528	Clock	

Table 3-10: ADC characteristics

Parameter	Description	Min	Typ	Max	Unit	Conditions
Vref	Reference voltage deviation	1.270	1.280	1.290	V	T= -40C to + 85C
ADC_Vin	Input voltage range	0		1.270	V	T = 25 C , when ADC buffer is disabled
	Voltage input buffer range	0.15		1.270	V	T = 25 C , when ADC buffer is enabled
ADC_Res	Effective Bit		5		Bit	OSR = 32
	Effective Bit		8		Bit	OSR = 128
	Effective Bit		10		Bit	OSR = 512
ADC_INL	Integral Non-linearity Error			0.5	LSB	@10 bit resolution setting VDD = 1.9V, T = 25 C
				1	LSB	@10 bit resolution setting VDD = 1.9V, T = 0 to 55C
ADC_DNL	Differential Non-linearity Error			0.5	LSB	@10 bit resolution setting VDD = 1.9V, T = 25 C
				1	LSB	@10 bit resolution setting VDD = 1.9V, T = 0 to 55C
Zeq,in	ADC equivalent input impedance		TBD		kOhm	Fadc = 10 kHz, buffer is disabled
			TBD		kOhm	Fadc = 40 kHz, buffer is disabled
		10.4			Mohm	Buffer is enabled
Offset	ADC offset			+/- 50	LSB	VDD = 1.9V
	ADC offset drift			0.25	LSB / C	Temp = 0 to 55 C
	ADC offset supply dependent			+/- 3	LSB / V	VDD = 1.7V to 2.0V
Gain_Error	ADC Gain Error			+/- 1.5	%	VDD = 1.9V, T = 25C
				+/- 2.5	%	Temp = 0 to 55 C
	ADC Gain Error drift			+/- 0.2	% /C	VDD = 1.9V
	ADC Gain Error supply dependent			+/- 0.2	% / V	VDD = 1.7V to 2.0V
Fadc	ADC operating frequency	300	10k	50k	Hz	
Tc	Conversion Time		204.8		mS	1 Sample acquisition Fadc = 10 kHz OSR = 1024 (11 bits res.) N-warmup = 8
			25.6		mS	1 Sample acquisition Fadc = 40 kHz OSR = 512 (10 bits res.) N-warmup = 8

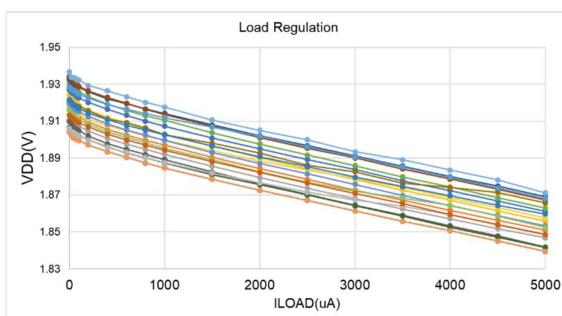


Figure 3-1: LDO characteristic - VDD vs ILOAD at T = 25 C

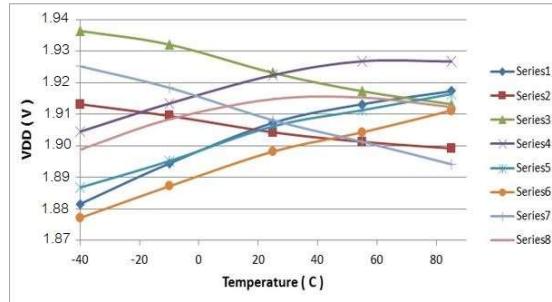


Figure 3-2: LDO characteristic - VDD vs Temperature (ILOAD = 0)

Specifications

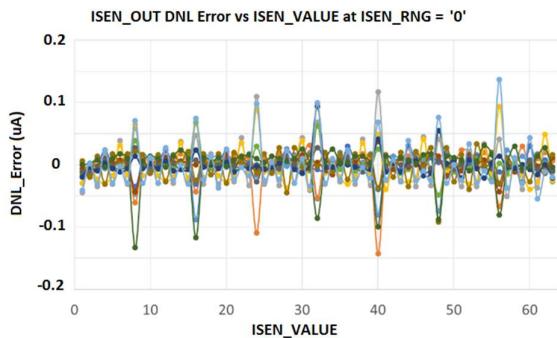
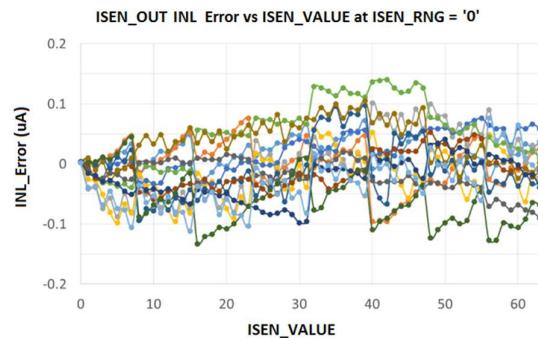
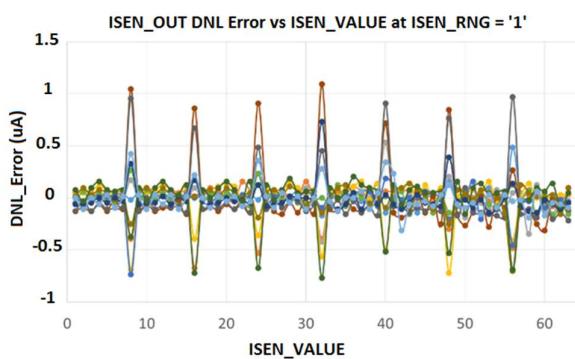
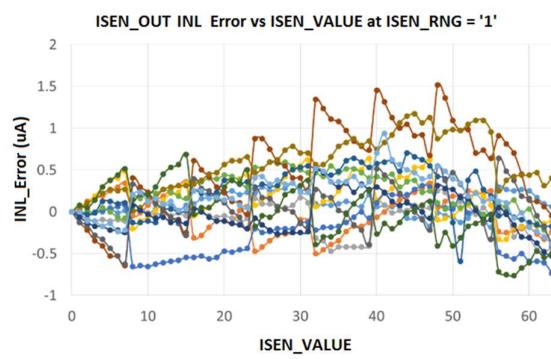
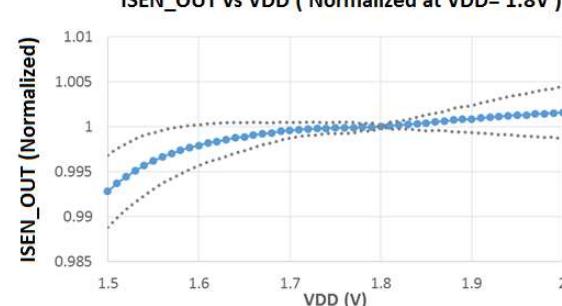
Figure 3-3: ISEN_OUT DNL Error for ISEN_RNG = '0' (1 μA / step)Figure 3-4: ISEN_OUT INL Error for ISEN_RNG = '0' (1 μA / step)Figure 3-5: ISEN_OUT DNL Error for ISEN_RNG = '1' (8 μA / step)Figure 3-6: ISEN_OUT INL Error for ISEN_RNG = '0' (8 μA / step)

Figure 3-7: ISEN_OUT vs VDD dependency

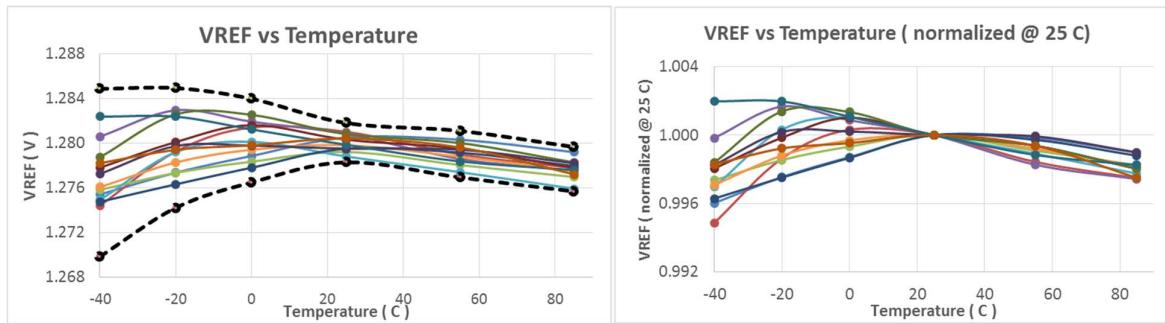


Figure 3-8: VREF vs Temperature dependency

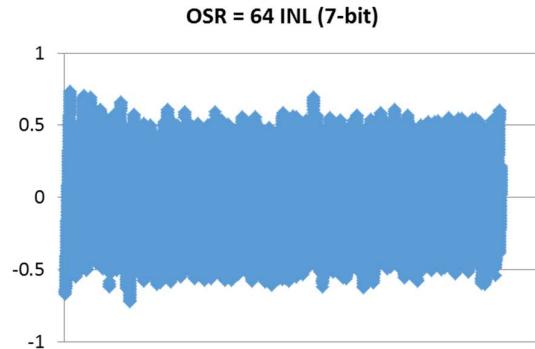
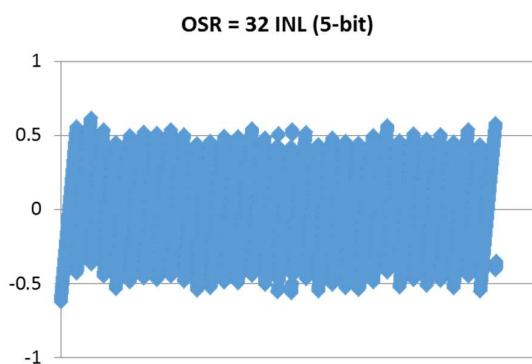


Figure 3-9: ADC INL Error for OSR = 32 and 64

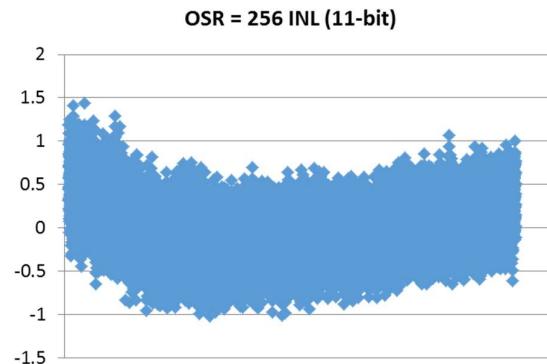
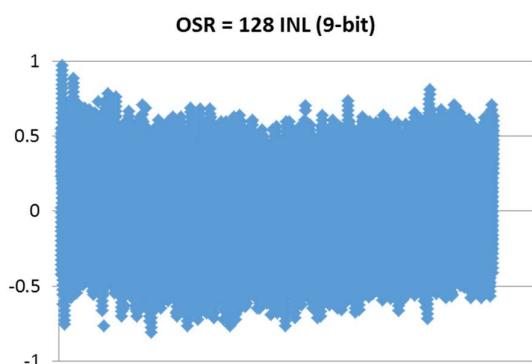


Figure 3-10: ADC INL Error for OSR = 128 and 256

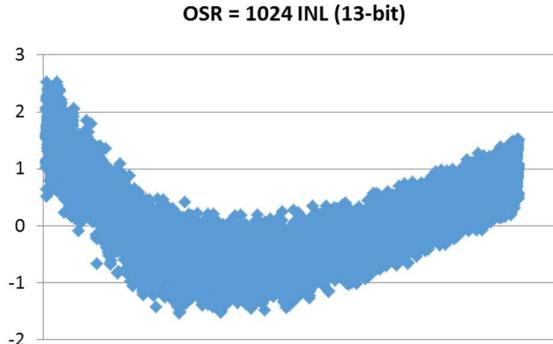
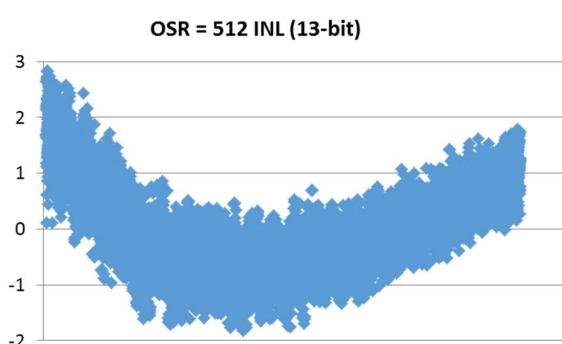


Figure 3-11: ADC INL Error for OSR = 512 and 1024

4. Communication

SIC4340 is a RF interface transponder IC which is based on ISO14443A. This section describes the RF interface behaviour.

4.1 RF interface

The RF interface of SIC4340 is based on the standard for contactless smart cards ISO 14443A-2. PCD and PICC according to ISO standard are referred respectively as NFC/RFID device and SIC4340/tag/transponder/chip throughout this document.

The SIC4340 activates itself by energizing RF field generated by its companion NFC/RF device. When the power of transponder is up and internal supply voltage is higher than the POR threshold, the chip initiates itself and be ready for an operational command and then starts transmitting in uplink as a response.

4.1.1 Downlink

In downlink, the RF device starts sending a command to the transponder by interrupting the field. The downlink communication takes place using 100% ASK modulation with the Miller coding. The transmission bit-rate is 106 kbps ($f_c/128$). Figure 4-1 depicts an example of downlink telegram.



Figure 4-1: Example of downlink telegram

4.1.1.1 Downlink bit pattern

Downlink bit pattern is based on the ISO 14443 type-A protocol as defined in Table 4-1 and Table 4-2.

Table 4-1: Sequences for the downlink bit-pattern

Sequence X	After a time of $64/f_c$ a “pause” shall occur
Sequence Y	For the full bit duration ($128/f_c$) no modulation shall occur
Sequence Z	At the beginning of the bit duration a “pause” shall occur

Table 4-2: Information to code with the downlink sequences

Logic ‘1’	Sequence X
Logic ‘0’	Sequence Y with the following two exceptions: If there are two or more contiguous ‘0’s, sequence Z shall be used from the second ‘0’ on If the first bit after a “start of frame” is ‘0’, sequence Z shall be used to represent this and any ‘0’s which follow directly thereafter
Start of communication	Sequence Z
End of communication	Logic ‘0’ followed by Sequence Y
No information	At least two Sequence Y

4.1.2 Uplink

After SIC4340 executes a command from NFC device and SIC4340 starts transmission in uplink as a response, the transponder communicates with NFC/RFID device by load modulation through inductive coupling field. The uplink bit pattern is defined based on ISO14443 type A. The uplink bit definition is described in Table 4-3 and Table 4-4. The uplink data is encoded in the Manchester format with subcarrier frequency of 847 KHz (fc/16). One-bit duration is 8 periods of the subcarrier, equivalent to bit-rate of 106 kbps (fc/128).

Figure 4-2 depicts an example of data encoding in uplink telegram.

Table 4-3: Sequence for the uplink pattern

Sequence D	The carrier shall be modulated with the subcarrier for the first half (50%) of the bit duration
Sequence E	The carrier shall be modulated with the subcarrier for the second half (50%) of the bit duration
Sequence F	The carrier is not modulated with the subcarrier for one bit duration

Table 4-4: Uplink data coding

Logical '1'	Sequence D
Logical '0'	Sequence E
Start of communication	Sequence D
End of communication	Sequence F
No information	No subcarrier

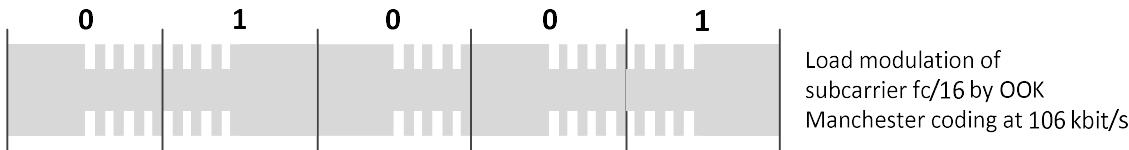


Figure 4-2: Example of uplink telegram

4.1.3 Frame pattern

The frame pattern for RF communication is based on the ISO14443 type-A protocol. There are three types of frame pattern illustrated in Figure 4-3. The frame types are as follows: short frame, standard frame and bit-oriented anti-collision frames. The purposes of each frame type are summarized in Table 4-5. This frame format is applied for both downlink and uplink. Each frame begins with a start bit and ends with an end bit. Transmission starts with the LSB of the lowest byte of transmission data. Each byte is transmitted with an odd parity. For more information, please refer to ISO14443-3.

Short frame									
	Short frame contains 7 data bits and the LSB is transmitted first.								
Standard frame									
	Standard frame contains multiple bytes, starting with the least significant byte (LSB) and ending with the most significant byte (MSB). Each byte is transmitted with odd parity.								

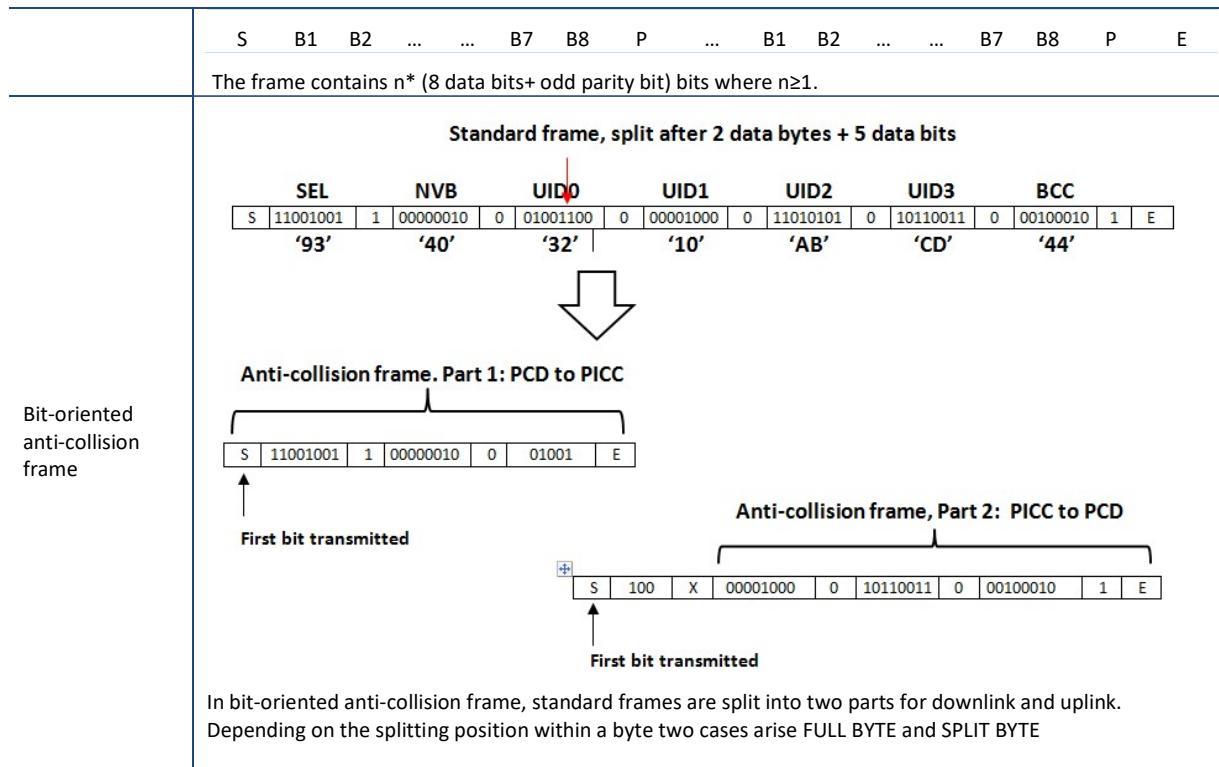


Figure 4-3: Frame format for RF communication

Table 4-5: Information to code with the uplink sequences

Frame type	Purpose	Command example
Short frame	Initiating	ISO14443A : <i>REQA, WUPA</i>
Standard frame	Transmitting regular command and data exchange between the transponder and NFC device.	ISO14443A : <i>SEL, HLTA, READE2, WRITEE2, Compatible WriteE2</i> RF-CONFIG : <i>ReadReg, WriteReg, ClearFlag, GetADC</i>
Bit-oriented anti-collision frame	Transmitting and receiving data during anti-collision loops.	ISO14443A : <i>ANTI_COLLISION</i>

4.1.4 Timing

The commands and response timing of SIC4340 are according to the standard of frame delay time of the ISO 14443A. Based on the ISO14443A, there is frame gμArd time between downlink and uplink and vice versa. Downlink frame delay time is the gμArd time between end of the last pause transmitted by the NFC/RFID device and the first modulation edge of the start bit transmitted by the transponder. Depicted in Figure 4-4, the downlink frame delay time is $(n*128+84)/fc$ or $(n*128+20)/fc$ depending on end bit value ('0' or '1' respectively). The n value must be more than 9. The transponder response starts in a defined time slot. On the other hand, uplink frame delay is the gμArd time between the last modulation transmitted by the transponder and the first pause transmitted by the NFC/RFID, which is approximately at least $1172/fc$ or $87 \mu s$. The uplink frame delay is shown in Figure 4-5.

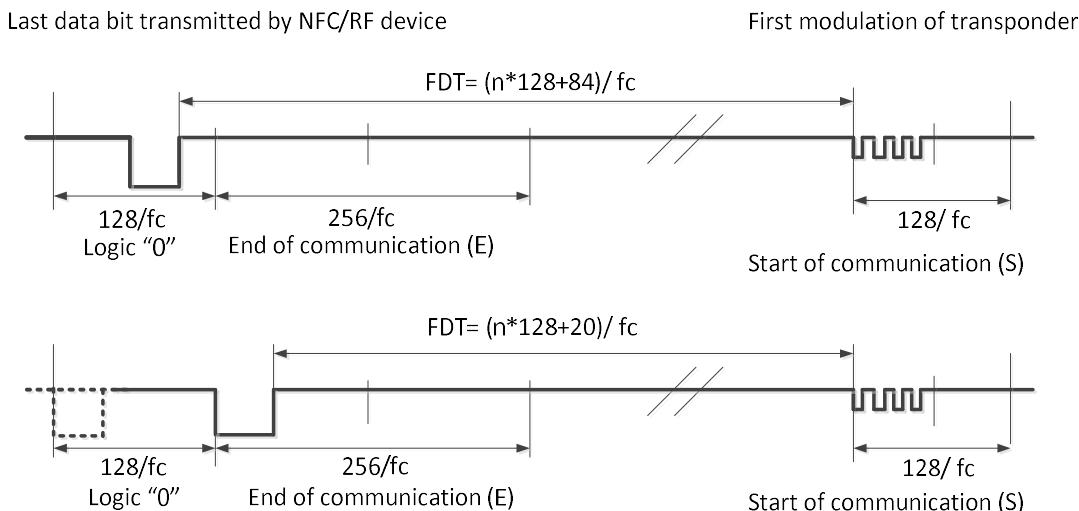


Figure 4-4: Downlink frame delay time

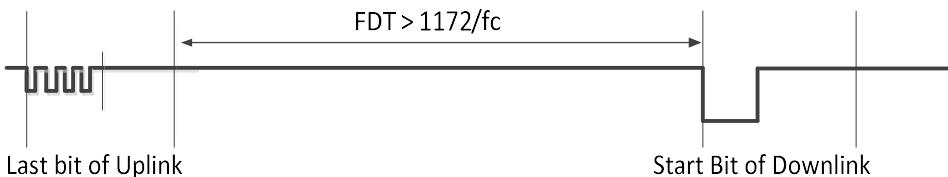


Figure 4-5: Uplink frame delay time

4.1.5 State of operation

When the SIC4340 receives an operational command from NFC/RFID device, the digital controller processes incoming commands and operates based on a current state.

Figure 4-6 depicts the transponder's state diagram.

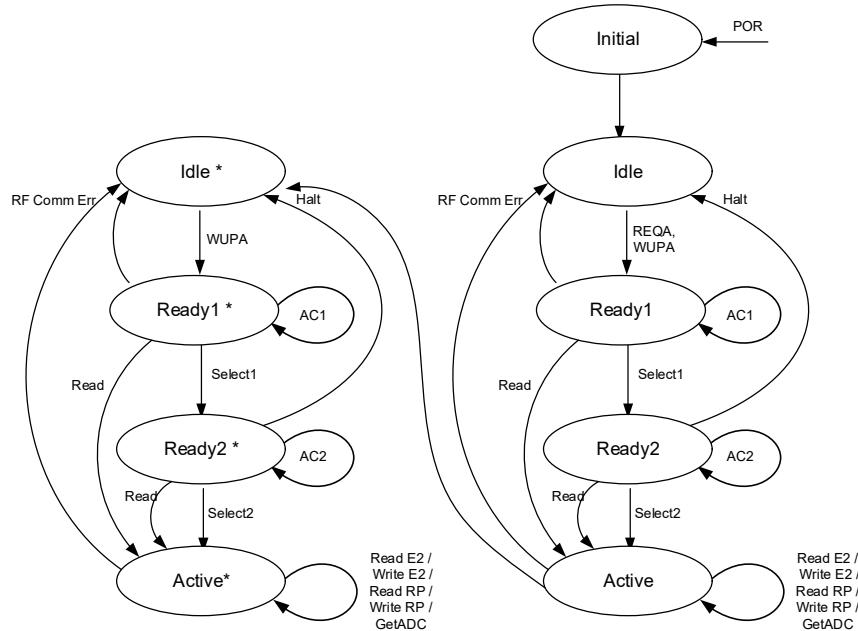


Figure 4-6: State of operation

Initial state: After POR, state of the SIC4340 enters the “*Initial*” state to initialize itself. In this state, the digital controller loads a pre-programmed reloading value from EEPROM to initialize a register configuration before entering “*Idle*”. Note that, the POR is occurred by the RF field is absent more than 100 us.

Halt & Idle state: After initialization, the SIC4340’s state go to “*Idle*” state waiting for the command **WUPA** or **REQA** to move the state to “*Ready1*”. Any other command obtained in this state is considered as an error and the state persists in the same state. Another equivalent state “*Halt*”, entering from the command **Halt**. Only the command **WUPA** can make the SIC4340 state to “*Ready1**”.

Ready1 & Ready1*: In the state “*Ready1*”, anti-collision level-1 method is applied. The digital controller expects a matched **Selection1** or **ANTI-COLLISION1**. For the **ANTI-COLLISION1**, the rest of UID is responded. For the **Select1**, when a cascaded level1 UID is matched, the digital controller responds SAK and transits to “*Ready2*”. Exceptionally **ReadE2**, any other command obtained in this state is considered as an error and the digital controller returns to “*Idle*” or “*Halt*”.

Ready2 & Ready2*: In the state “*Ready2*”, anti-collision level-2 method is applied. The digital controller decoder expects a matched **Selection2** or **ANTI-COLLISION2**. For the **ANTI-COLLISION2**, the rest of UID is responded. For the **Select2**, when a cascaded level-2 UID is matched, the digital controller responds SAK and transits to the state “*Active*”. Exceptionally **ReadE2**, any other command obtained in this state is considered as an error and digital controller returns to “*Idle*” or “*Halt*”.

Active & Active*: In the active state, the SIC4340 can perform RFID-memory access, register configuration access and Analog to Digital convertor process. The RFID-memory access commands are **ReadE2**, **WriteE2**, **Compatible WriteE2**. The register accessing commands are **ReadReg**, **WriteReg**. The Analog to Digital convertor command is **GetADC**.

The Digital state can exit “*Active*” and switches to the state “*Halt*” by the command **Halt**. If RF communication error occurs during transmission in this state, the digital controller returns to “*Idle*” or “*Halt*”. In case of RF-access memory command error or framing error, transponder replies a 4-bit NAK. In case of bad power conditions, transponder replies an 8-bit B_NAK and remains in “*Active*” state.

5. EEPROM Organization

The SIC4340 contains a 236-byte non-volatile EEPROM memory, conforming to the NFC Tag Type 2 arrangement as shown in Figure 5-1. The memory is incorporated with 59 pages of 4 bytes each. First section contained 64 bytes is for NFC static memory area and the rest areas are NFC dynamic memory areas. For control bits, **UID**, **Static Lock Byte**, **OTP** are stored in the NFC static memory area while **Calibration Data**, **Dynamic Lock Byte (Lock Byte2 – Lock Byte4)** and **Register Reload Value** (RL REG 4 – RL REG 27) are stored in the NFC dynamic memory area. Usable user memory for application is 192 bytes (Page 4 to Page 51).

Page (Dec)	Page (Hex)	Byte 0	Byte 1	Byte 2	Byte 3	Memory Type	Description	Note
0	00	UID0	UID1	UID2	BCC0	R/O	UID / Lock	64-byte NFC Static Memory
1	01	UID3	UID4	UID5	UID6	R/O		
2	02	BCC1	Internal	Lock Byte0	Lock Byte1	R/O, R/W		
3	03	OTP	OTP	OTP	OTP	R/W (OTP)		
4	04					R/W	52-byte User Data	172-byte NFC Dynamic Memory
...	...					R/W		
15	0F					R/W		
16	10					R/W		
...	...					R/W	96-byte User Data	172-byte NFC Dynamic Memory
39	27					R/W		
40	28	Cal Data	Cal Data	Cal Data	Cal Data	R/W		
...	...	Cal Data	Cal Data	Cal Data	Cal Data	R/W		
51	33	Cal Data	Cal Data	Cal Data	Cal Data	R/W	48-byte Test & Calibration Data	172-byte NFC Dynamic Memory
52	34	Lock Byte2	Lock Byte3	Lock Byte4	RFU	R/W		
53	35	RL REG 4	RL REG 5	RL REG 6	RL REG 7	R/W		
54	36	RL REG 8	RL REG 9	RL REG 10	RL REG 11	R/W		
55	37	RL REG 12	RL REG 13	RL REG 14	RL REG 15	R/W	24-byte Reload Register	172-byte NFC Dynamic Memory
56	38	RL REG 16	RL REG 17	RL REG 18	RL REG 19	R/W		
57	39	RL REG 20	RL REG 21	RL REG 22	RL REG 23	R/W		
58	3A	RL REG 24	RL REG 25	RL REG 26	RL REG 27	R/W		

Figure 5-1: SIC4340 EEPROM memory map

5.1 UID

UID is a factory pre-programmed, write-protected identification number that is composed of a 7-byte serial number along with its two check bytes. **UID** is stored in byte 0 of page 0 to byte 0 of page 3 of the EEPROM as depicted in. When the SIC4340 receives the **ANTI-COLLISION** command, it responds the NFC/RFID reader device with the rest **UID**. **BCC** is kept in the EEPROM during manufacturing to ensure that uplinked **UID** is stored in EEPROM correctly. Note that **UID0** is set to 0x39.

5.2 Static lock byte

Byte 2 and 3 of page 2 (0x02) of EEPROM memory contain static lock bytes named **Lock Byte0** and **Lock Byte1**. Each bit, also known as lock bit, controls programmability for its addressed page or corresponding group of lock bits itself. When a certain lock bit in **Lock Byte0** or **Lock Byte1** is set to '1', the addressed page cannot be changed. Reminded, tBits of these lock bytes are one-time program (OTP). Therefore, once it is programmed to '1', such a bit is unable to clear back to '0'.

Three LSB bits of **Lock Byte0** function as lock of lock-bits of static user memory. When an individual bit in these three LSB bits is set, the corresponding page lock bit values cannot be altered everlastingly and the addressed pages remain locked or unlocked state based on the last individual lock bit value. Note that new lock bit value is effective after (re)entering the "*Idle*" or "*Halt*" state.

Byte in Page 2 (Page 0x02)		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 2	Lock Byte 0	Lock Page 7	Lock Page 6	Lock Page 5	Lock Page 4	Lock Page OTP	Lock of Lock Bit 15-10	Lock of Lock Bit 9-4	Lock of OTP Lock Bit
Byte 3	Lock Byte 1	Lock Page 15	Lock Page 14	Lock Page 13	Lock Page 12	Lock Page 11	Lock Page 10	Lock Page 9	Lock Page 8

Figure 5-2:Lock configuration in static memory

5.3 OTP

Page 3 of EEPROM memory is the OTP page with four OTP bytes. All bits of these OTP bytes are set to '0' from manufacturing and can be programmed to '1' bit-wise by the **WriteE2** or **Compatible WriteE2** commands. Once any OTP bit is programmed to '1', it cannot be back to '0' by any write command. Example of OTP programing behaviour is shown in Figure 5-3.

Absolute byte Address	Byte 12	Byte 13	Byte 14	Byte 15
Byte in Page 3 (Page 0x03)	Byte 0	Byte 1	Byte 2	Byte3
Default value	0000 0000	0000 0000	0000 0000	0000 0000
Program with	1111 1111	0000 1100	0000 0101	0000 0000
Result in page 3	1111 1111	0000 1100	0000 0101	0000 0000
Program with	0000 0000	1111 1100	0000 0000	0000 0111
Result in page 3	1111 1111	1111 1100	0000 0101	0000 0111

Figure 5-3: OTP behavior in Page 3

5.4 User memory

Page 4 to page 51 of the EEPROM is the user memory. Initially, all blocks of user memory are programmed to '0' during manufacturing. They can be written by **WriteE2** or **Compatible WriteE2** commands and read by **ReadE2** command. Address of EEPROM is designed to support NFC data in the TLV format such as Lock Control, Memory control or NDEF message. NFC data such URL can be stored in the memory. Figure 5-4 shows an example of URL written in the user memory under the TLV format. For more information, please refer to the "NFC Forum Tag Type2 specification" standard.

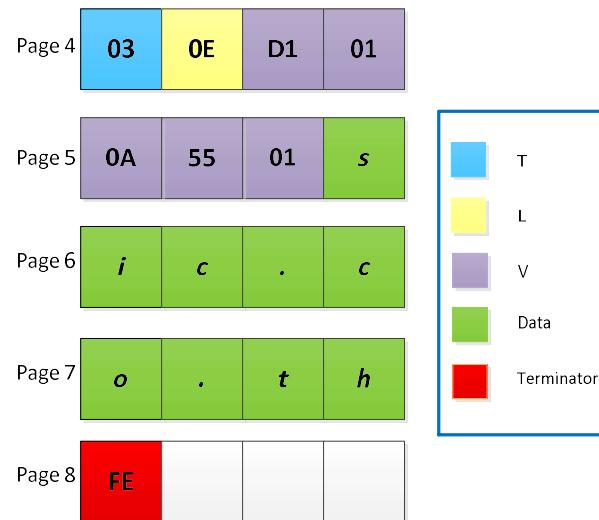


Figure 5-4: URL written in the user memory under the TLV format

5.5 Test and Calibration Data

Page 40 to 51 of EEPROM contains test and calibration data as shown in Figure 5-5. Page 40 to 45 records TESTER Parameter such as voltage, current that are tested via pin T1 and T2. Page 46 stores ADC parameter, **ADC_GAIN_ERROR** and **ADC_OFFSET_ERROR**, which use for calculating the exact value. Page 47 records **TESTER version** and **TABLE version** applied for production tracking. Page 48 and 49 also contain ADC buffer parameter that applied for ADC calculation output when ADC buffer is enabling. The calculation method will be described in 10.1.

Page (Dec)	Page (Hex)	Byte 0	Byte 1	Byte 2	Byte 3
40	0x28			TESTER PARAM 0	
41	0x29			TESTER PARAM 1	
42	0x2A			TESTER PARAM 2	
43	0x2B			TESTER PARAM 3	
44	0x2C			TESTER PARAM 4	
45	0x2D			TESTER PARAM 5	
46	0x2E		ADC_GAIN_ERROR		ADC_OFFSET_ERROR
47	0x2F			TESTER Version	TABLE Version
48	0x30		ADC_RESULT_BUFF_020		ADC_RESULT_BUFF_080
49	0x31		ADC_RESULT_BUFF_120		RFU
50	0x32			RFU	
51	0x33			RFU	

Figure 5-5: Test and calibration memory when TABLE version = 0x03

5.6 Dynamic lock byte

Page 52 of the EEPROM contains **Dynamic lock** bytes. Function of each bit of **Dynamic lock** bytes is to set an associated read/write memory area to be read-only. Lock configuration of dynamic memory is shown in Figure 5-6.

Byte in Page 52 (Page 0x34)		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0	Lock Byte 2	Lock Page 36-39	Lock Page 32-35	Lock Page 28-31	Lock of Lock Byte2 Bit 5-7	Lock Page 24-27	Lock Page 20-23	Lock Page 16-19	Lock of Lock Byte2 Bit 1-3
Byte 1	Lock Byte 3	RFU (OTP)	RFU (OTP)	RFU (OTP)	RFU (OTP)	Lock Page 48-51	Lock Page 44-47	Lock Page 40-43	Lock of Lock Byte3 Bit 1-3
Byte 2	Lock Byte 4	RFU (OTP)	RFU (OTP)	RFU (OTP)	RFU (OTP)	Lock Page 57-58	Lock Page 55-56	Lock Page 53-54	Lock of Lock Byte4 Bit 1-3
Byte 3	Lock Byte 5	RFU (OTP)	RFU (OTP)	RFU (OTP)	RFU (OTP)	RFU (OTP)	RFU (OTP)	RFU (OTP)	RFU (OTP)

Figure 5-6: Lock configuration of dynamic memory

5.7 Register Reload value

Page 53 to 58 of EEPROM contain reloading values for the register page. Reloading process to the register page performs during the “**Initial**” state. 24-byte data in EEPROM starting from Byte0 of Page53 to Byte3 of Page58 are transferred to Address 4 to Address 27 of the register page.

6. Register

6.1 Register overview

The SIC4340 consists of two types of 32-byte addressable register pages namely Read only and Read/Write. The register pages initialize automatically from EEPROM after POR. Behaviours of register pages are described in the following Table 6-1. The overview of the register map is shown in Table 6-2. The register names are listed in the far-right column.

Table 6-1: Type of register

Type	Description
Read only	The read only register is used to display the status of the internal state machine. Writing these registers will not affect their values.
Read/ Write	The read-write register is used to configure and control behaviors of the NFC/RFID reader device IC. These registers can be written and read by the external controller.

Table 6-2: SIC4340 register map

Addr	Type	Bit								Register Name
		7	6	5	4	3	2	1	0	
0x00	Status							VDD_RDY_H	VDD_RDY_L	VDD status
0x01	Status									ADC Result
0x02	Status									ADC Result
0x03	Status									ADC Result
0x04	Config									ADC Divider
0x05	Config									ADC Prescaler
0x06	Config									ADC Samp Delay
0x07	Config									ADC Nwait
0x08	Config									ADC Bit Config
0x09	Config									ADC Mode Config
0x0A	Config									ADC BUF Config
0x0B	Config									ADC CH Config
0x0C	Config									ISEN Config
0x0D	Config									ISEN Value
0x0E	Config									VLM Value
0x0F	N/A									
0x10	N/A									
0x11	N/A									
0x12	N/A									
0x13	Config									VDD_EN
0x14	Config									
0x15	N/A									
0x16	N/A									
0x17	N/A									
0x18	Config							ISEN_EN	VLM_DAC_EN	ADC_ANA_EN
0x19	N/A									
0x1A	Config				GAP_CMPEN_E_N					GAP_CMPEN
0x1B	N/A									

6.2 Register detail

6.2.1 Register 0x00 : VDD Status

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	-	-	VDD_RDY_H	VDD_RDY_L
Parameter	Type	Function and Description					
VDD_RDY_H	R/O - Status	'1' indicates that VDD level is more than VDD_H voltage level '0' indicates that VDD level is less than VDD_H voltage level					
VDD_RDY_L	R/O - Status	'1' indicates that VDD level is more than VDD_L voltage level '0' indicates that VDD level is less than VDD_L voltage level					

Note that VDD_H and VDD_L voltage level is defined in 3.2 Electrical characteristic.

These registers are real time power status. Once VDD is low, they raise the error flag high and be responded with B_NAK format until the flag is cleared by command **Clear_Flag**. When **VDD_RDY_H** is '1', ADC and sensor interface are correctly operated. If **VDD_RDY_H** is '0' and **VDD_RDY_L** is '1', ADC and sensor can still operate but accuracy of ADC is decreased. In this situation, the maximum effective bit result is 5 bits. While **VDD_RDY_L** is '0', ADC and sensor interface cannot be executed.

6.2.2 Register 0x01, 0x02 and 0x03 : ADC Results

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_Result [23:16]							
ADC_Result [15:8]							
ADC_Result [7:0]							
Parameter	Type	Function and Description					
ADC_Result	R/O - Status	The results from Analog to Digital conversion					

The MSB of ADC conversion results is located at the MSB of ADC_Result register page, which is ADC_Result[23], and followed by the other respectively to the right side as the example below.

ADC_Result[23:0] (Hex)	Register 0x01 (Hex)	Register 0x02 (Hex)	Register 0x03 (Hex)
45 9A F2	45	97	F2
06 7B 80	06	7B	80

Note that , **ADC_Result[23:8]** is only returned to **GetADC** command response.

6.2.3 Register 0x04 : ADC_Divider (D)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_Divider [7:0]							
Parameter	Type	Function and Description					
ADC_Divider	R/W - Config	ADC_Divider , defined as D, is a divisor of clock sensor frequency with factor of (128 + D). The ADC_Divider D is used together with ADC_Prescaler P .					

6.2.4 Register 0x05 : ADC_Prescaler (P)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_Prescaler [2:0]							
Parameter	Type	Function and Description					
ADC_Prescaler	R/W - Config	ADC_Prescaler , defined as P, is an exponent of the divisor of clock sensor frequency with factor of 2^P . The ADC_Prescaler P is used together with ADC_Divider D .					

SIC4340 can generate sensor bias frequency varying from 300Hz to 50kHz which controlled by 2 parameters as shown in below equation:

$$fsensor = fc / [2^P * (D + 128)]$$

The operating frequency fc is typically 13.56MHz extracting from NFC carrier. The divided frequency ***fsensor*** also defines ADC sampling rate.

6.2.5 Register 0x06 : ADC_Sampling_Delay

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_Samp_Delay_Time [7:0]							
Parameter	Type	Description					
ADC_TS_Delay	R/W - Config	Define the ADC sampling delay time from rising edge of sensor biasing clock. The sampling time is $Samp_Delay = (ADC_Ts_Delay[7:0]) \times 2^P / fc$					

6.2.6 Register 0x07 : ADC_Nwait

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0				
Nwait_Multiplier [3:0]				Nwait_Prescaler [3:0]							
Parameter	Type	Description									
Nwait_Multiplier	R/W - Config	Nwait_Multiplier, defined as M, and Nwait_Prescaler, defined as N, define the number of warm up clock to pre-bias sensor prior to actual ADC sampling and conversion									
Nwait_Prescaler	R/W - Config	$\#Warm_Clock = 8 + (M * 2^N)$									

6.2.7 Register 0x08 : ADC_Bit_Config

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0			
-	ADC_AVG [2:0]			ADC_Signed	ADC_NBit [2:0]					
Parameter	Type	Description								
ADC_AVG	R/W - Config	Defines the number of average for one conversion $\#average = 2^{ADC_AVG}$								
ADC_Signed	R/W - Config	Defines the display ADC_Result register style								
		0 Unsigned bit result								
ADC_NBit	R/W - Config	Define the number of ADC effective output bits by changing the oversampling ratio (OSR) as shown in Table								

ADC_NBit [2:0]	Over Sampling Ratio $OSR = 2^{(5+ADC_Nbit)}$	Designed #Effective Output Bit
000	32	5
001	64	7
010	128	8
011	256	9
100	512	10
101	1024	10
110	2048	10
111	4096	10

6.2.8 Register 0x09 : ADC_Mode_Config

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
		ADC_Auto_Conv_Period [2:0]		-	ADC_Resp	ADC_Conv_Mode[1:0]			
Parameter		Type	Description						
ADC_Auto_Conv_Period		R/W - Config	Define the period for ADC Conversion in auto conversion mode (ADC_Conv_Mode = "11b") "000" : 50 ms "001" : 100 ms "010" : 200 ms "011" : 500 ms "100" : 1 sec "101" : 2 sec "110" : 5 sec "111" : 10 sec						
ADC_Auto_Resp		R/W - Config	Define timing response of GetADC command in auto conversion mode (ADC_Cov_Mode = "11b") '0' : When receive GetADC command, SIC4340 will immediately response. '1' : When receive GetADC command, SIC4340 will hold its response until ADC automatically start the next conversion.						
ADC_Conv_Mode		R/W - Config	Define mode operation of ADC conversion "0X" : Single Conversion Mode. : ADC starts conversion only when receive GetADC command, "10" : Continuous Mode. : ADC continuously converts, and result is updated every OSR period in the ADC_Result register "11" : Auto Conversion Mode. : ADC automatically starts conversion following period defined by ADC_Auto_Conv_Period .						

The timing detail also describes in Section 7.4.2.

6.2.9 Register 0x0A : ADC_BUF_Config

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
				ADC_BUF_EN			ADC_LPF [1:0]
Parameter		Type	Description				
ADC_BUF_EN		R/W - Config	'0' : ADC input buffer is disable '1' : ADC input buffer is enable – suitable for high output impedance input source (> 50kΩ)				
ADC_LPF [1:0]		R/W - Config	Configure low pass corner frequency of the anti-aliasing filter corner for ADC input "00" : no anti-aliasing filter "01" : 1250 kHz "10" : 623 kHz "11" : 325 kHz				

6.2.10 Register 0x0B : ADC_CH_Config

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0				
			ADC_SING_MODE	ADC_CHN [1:0]		ADC_CHP [1:0]					
Parameter	Type	Description									
ADC_SING_MODE	R/W - Config	Define the ADC input topology '0' : differential input : the ADC converts different voltage between ADC positive input VINP and ADC negative input VINN to output data. '1' : single ended input : the ADC convert voltage from ADC positive input VINP only while ADC negative Input VINN is internally connected to ground									
ADC_CHN [1:0]	R/W - Config	Define the ADC negative input channel "00" : S0 "01" : S1 "10" : S2 "11" : Not Connected									
ADC_CHP [1:0]	R/W - Config	Define the ADC positive input channel "00" : S0 "01" : S1 "10" : S2 "11" : Not Connected									

6.2.11 Register 0x0C : ISEN_Config

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		ISEN_CH [1:0]			ISEN_DC	ISEN_VLM_EN	ISEN_RNG
Parameter	Type	Description					
ISEN_CH[1:0]	R/W - Config	Define the output channel of current bias to sensor "00" : S0 "01" : S1 "10" : S2 "11" : Not Connected					
ISEN_DC	R/W - Config	Define the waveform of current bias to sensor '0' : pulse current with 50% duty cycle '1' : constant – DC current					
ISEN_VLM_EN	R/W - Config	'0' : Disable the output voltage limiter '1' : Enable the output voltage limiter					
ISEN_RNG	R/W - Config	Define the step size of current driver '0' : 1 µA / Step '1' : 8 µA / Step					

For correctly operation, ISEN_CH[1:0] value must be same with ADC_CH[1:0] value.

6.2.12 Register 0x0D : ISEN_Value

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0				
		ISEN_VALUE[5:0]									
Parameter	Type	Description									
ISEN_VALUE[5:0]	R/W - Config	Define the sensor driven current amplitude. The output current is described as follows $IOUT = ISEN_VALUE[5:0] * ISEN_Step$ ISEN_Step is depended on setting of ISEN_RNG bit.									

6.2.13 Register 0x0E : VLM_Value

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VLM_VALUE[7:0]							
Parameter	Type	Description					
VLM_VALUE[7:0]	R/W - Config	Define the limiter voltage for preventing sensor burning or overvoltage The voltage can be calculated from $V_{limit} = VLM_VALUE[7:0] \times 5mV$					

6.2.14 Register 0x13 : VDD_Config

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VDD_EN							
Parameter	Type	Description					
VDD_EN	R/W - Config	Enable LDO output at VDD pin					

Note that VDD_EN is disable, ADC and Sensor interface cannot operate.

6.2.15 Register 0x18 : Sensor Config

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ISEN_EN VLM_DAC_EN ADC_EN							
Parameter	Type	Description					
ISEN_EN	R/W - Config	Set to '1' to enable sensor current driver circuit					
VLM_DAC_EN	R/W - Config	Set to '1' to enable internal DAC module that defines output limiter voltage level					
ADC_EN	R/W - Config	Set to '1' to enable ADC module					

SIC4340 automatically sets ISEN_EN, VLM_EN, and ADC_EN to '1' when **GetADC** command is executed. User is not need to set to '1' before conversion. And these bits are also automatically cleared after conversion finish.

6.2.16 Register 0x1A : GAP_CMPEN_Config

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0			
-	-	-	GAP_CMPEN_EN	-	GAP_WID_CMPEN [2:0]					
Parameter	Type	Description								
GAP_CMPEN_EN	R/W Config	Set to '1' for enabling timing compensation module to adjust ADC conversion period to match desired period In auto conversion mode (ADC_Conv_mode = '11') , downlink gaps make the received clock absent. The clock counting system on chip stops and time value does not match to real time going on. Then, , the sampling period can be error due to missing clock.								
GAP_WID_CMPEN	R/W Config	Define the fine tuning parameter for compensation time (T_CMP) for each downlink gap in the multiple of clock period $T_{CMP} = (32 + CMPEN_VALUE) / fc$ where fc is carrier frequency 13.56 MHz "000" : CMPEN_VALUE = 0 (T_CMP = 2.360 us) "001" : CMPEN_VALUE = 4 (T_CMP = 2.655 us) "010" : CMPEN_VALUE = 8 (T_CMP = 2.950 us) "011" : CMPEN_VALUE = 12 (T_CMP = 3.245 us) "100" : CMPEN_VALUE = -4 (T_CMP = 1.180 us) "101" : CMPEN_VALUE = -8 (T_CMP = 1.475 us) "110" : CMPEN_VALUE = -12 (T_CMP = 1.770 us) "111" : CMPEN_VALUE = -16 (T_CMP = 2.065 us)								

Note that , the timing detail is described in session 7.4.2.3.

7. Architecture and Peripheral Interface

As shown in Figure 7-1, the SIC4340 contains the configurable peripheral from register : RF AFE, LDO, Sensor biasing circuit and ADC. This section describes the relation between function of each sub block and related registers.

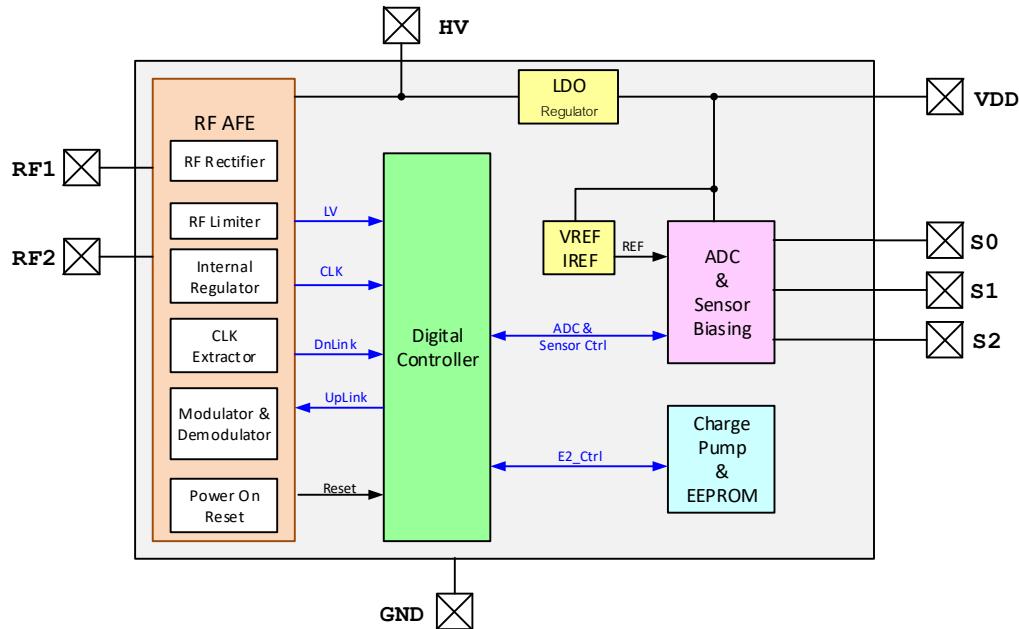


Figure 7-1: Configurable peripheral components

7.1 RF Analog-Front-End

As depicted in Figure 7-2, the RF Analog Front End (RF –AFE) harvest power to supply all internal operation circuit. To prevent device damage from too high RF power input, the RF limiter is equipped between RF1 and RF2 terminals the maximum voltage appears at the coil will be limited to 7V. The RF bridged rectifies AC coupling signal at coil into DC supply. The rectified power supply at node HV is fed to the LDO for power supply source to the ADC and the sensor biasing circuit. Moreover, this node also link to HV pad that can be connected to external capacitor (e.g. 100 nF) for more power stability.

The LV internal regulator creates low voltage supply from HV and this voltage **LV** supply power to digital controller and other RF-AFE circuits. The power-on-reset (POR) circuit detects the LV voltage level. When the **LV** voltage is high enough, **POR** signal trig the digital controller for starting operation.

For RF communication following ISO14443A standard, RF command is sent by on-off keying modulation. RF demodulator monitors the gaps that appear at the coil and sent **GAP** detection signal to digital controller to operate following the command. After the command execution finish, the **MOD** signal is sent back to RF Modulator to modulate RF field at coil by changing network impedance. The clock extractor block generates clock signal from RF and created system clock for all digital control circuits.

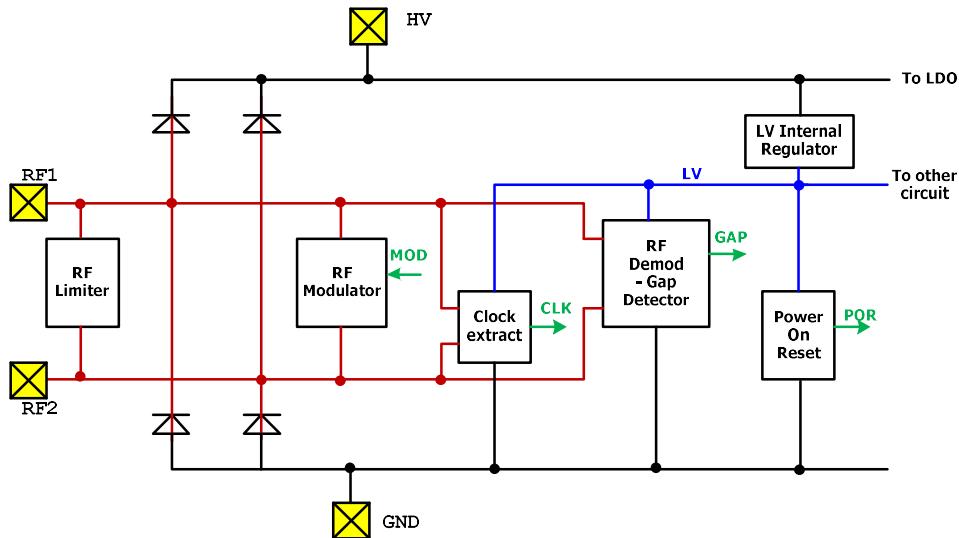


Figure 7-2: Simplified block diagram of RF-AFE

7.2 Low-Drop-Out (LDO) regulator

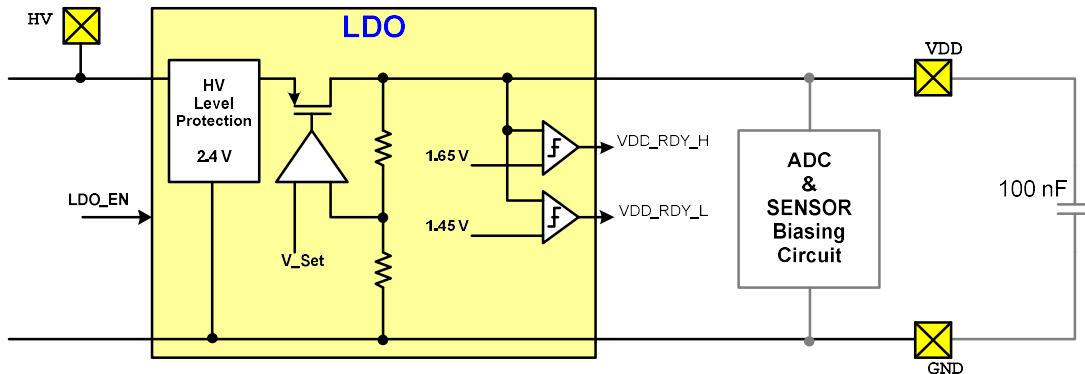


Figure 7-3: Simplified block diagram of RF-AFE

The Low-Drop-Out (LDO) regulator provided a 1.9 V supply to the analog-to-digital converter (ADC), the sensor biasing circuit and the reference circuit. External capacitor 100 nF can be connected to pin **VDD** and pin **GND** for LDO stability especially high current consumption sensor load. The VDD level of the LDO is factory trimmed within $\pm 3\%$ accuracy.

Simplified circuit diagram of the LDO is depicted in Figure 7-3. The LDO can operate when the register **VDD_EN** (0x13.0) is set to '1'. The LDO is designed to protect system power failure resulting from any power supply overloading or fault and ensure communications between the SIC4340 and NFC/RFID reading devices(e.g. pin **VDD** is mistakenly shorted to ground). In such overloading situation, If sensor load requires current from the LDO more than the harvesting capability from the RF coil, the HV voltage will decrease and HV level protection circuit is activated to decreases supplying output current. Then, voltage output at pin **VDD** drops.

The LDO supply output level at **VDD** is continuously monitored by two voltage comparators, indicating by signal **VDD_RDY_H** and **any power supply overloading**. The VDD Status indicator reports in register VDD Status (0x01.[1:0]). If the VDD voltage is in well condition, each register VDD Status (0x01.[1:0]) shows '1'. When the VDD output is lower than the setting voltage, VDD status indicator reported in register 0x01.[1:0] shows '0' and the warning flag ("VDD_DROP_H" and "VDD_DROP_L") are asserted in B_NAK response. To clear the flag ("VDD_DROP_H" and "VDD_DROP_L"), the NFC/RFID reader shall issue the command **Clear_Flag**. However, after the command **Clear_Flag** is sent, these flag can still persist as long as VDD level is still below the threshold voltage. The threshold level for **VDD_RDY_H** and **VDD_RDY_L** are about 1.65V and 1.45V respectively.

To guarantee the sensor and ADC operation, users should carefully ensure the maximum amount of load which should be less than the sourcing capability. When the **VDD_DROP_H** flag is set (to "1'b"), the sensor and ADC can start conversion and still operate until the process is finished. The **VDD_DROP_H** is a warning flag indicating the VDD is at marginal minimum level for sensor interface circuit and ADC operation. If **VDD_DROP_L** flag is set (to "1'b"), the sensor and ADC is immediately stop operation. To restart the operation, user must ensure incoming power level at RF coil, executes **ClearFlag** command and re-execute ADC conversion.

Table 7-1: Registers associated with the LDO

Register	Address	Function	Type	Factory preset value
VDD_EN	0x13.0	Enables LDO to generate supply voltage at VDD	Read/Write	'1'
VDD_RDY_H	0x01.0	Indicator shows voltage on pin VDD is higher than a defined level, approx. 1.65 V.	Read only	'1'
VDD_RDY_L	0x01.1	Indicator shows voltage on pin VDD is higher than a defined level, approx. 1.45 V.	Read only	'1'

Table 7-2: Pins related to LDO

Pin Name	Pad #	Function
HV	6	Unregulated power supply pin - For large load supplying, 0.1μF decoupling capacitor is required at this pin.
VDD	7	VDD supply pin - Output power port for LDO - Power supply for ADC and Sensor biasing circuit - At least 0.1μF decoupling capacitor is required at this pin.

7.3 Sensor Biasing Circuit

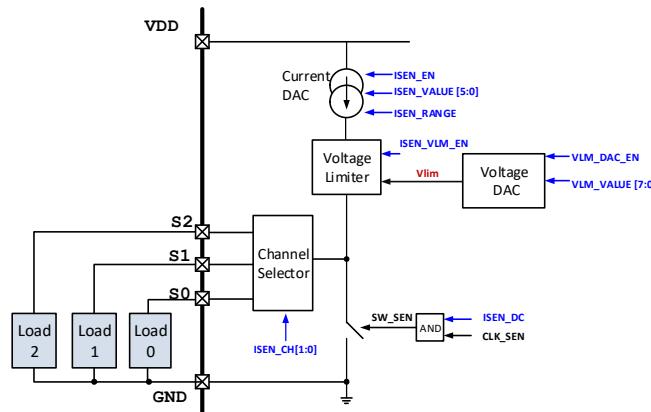


Figure 7-4: Sensor biasing circuit

Figure 7-4 shows the sensor biasing circuit structure. Current DAC, with resolution of 6 bits controlled by **ISEN_VALUE [5:0]** register, generates the current output to external sensor load. The amount of current can be set into two ranges namely 0μA-to-64μA and 0μA-to-504μA depending on register **ISEN_RANGE** setting. The channel selector controlled by register **ISEN_CH[1:0]** multiplexes the current fed to external load just only one pin at a time.

Table 7-3 shows current resolution, maximum and minimum of biasing current in each range.

Table 7-3: Sensor biasing output current

ISEN_RANGE	Amount of current	Current resolution	Max Current	Min Current	Accuracy
1	ISEN_VALUE [5:0] x 8μA	16 μA	504 μA	0 μA	+/- 8 μA
0	ISEN_VALUE [5:0] x 1μA	1 μA	63 μA	0 μA	+/- 0.5 μA

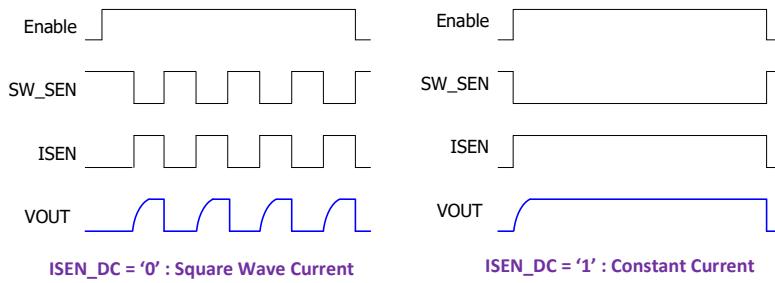


Figure 7-5: Waveform example when configure ISEN_DC = '0' & '1' (external load is resistor parallel with capacitor)

Figure 7-5 shows the sensor biasing current waveform that can be selectable by register **ISEN_DC** (0x0C.2). When **ISEN_DC** = '1', constant biasing current is fed to external sensor. On the other hands, if **ISEN_DC** = '0', biasing current will be a 50% duty cycle square waveform controlled by internal switch. The waveform frequency is equal to ADC sampling frequency which controlled by **ADC_Divider[7:0]** (D) and **ADC_Prescale[2:0]** (P) in register page. The detail of frequency is described in ADC session. The purpose of biasing the sensor square wave is required in some type of sensor.

Voltage limiter can be optionally enabled by register **ISEN_VLM_EN** (0x0C.1) to protect over voltage on the sensor. The protection voltage, **Vlim**, is generated from 8 bits voltage DAC which enabled by **VLM_DAC_EN** (0x18.1). **Vlim**, ranging from 0V to 1.275V with resolution of 5mV, is set by register **VLM_VALUE[7:0]** (0x0E.[7:0]). The limiter allows the voltage swing between 0 to **Vlim** level. When the voltage reaches near the setting **Vlim** level, the voltage limiter characteristic reduces the current fed to external sensor. However, because of finite sharp limiting characteristic, the actual effective swing value range versus setting value **Vlim** is not the same. The reliable voltage which current is not limited is from 0V to (**Vlim**-0.1V). If the limiter is not select to use (**ISEN_VLM_EN** ='0'), voltage crossing the sensor under can be as high as VDD. The example waveform is shown in Figure 7-6.

Sensor biasing circuit is activated when ADC operates or setting **ISEN_EN** bit in register page.

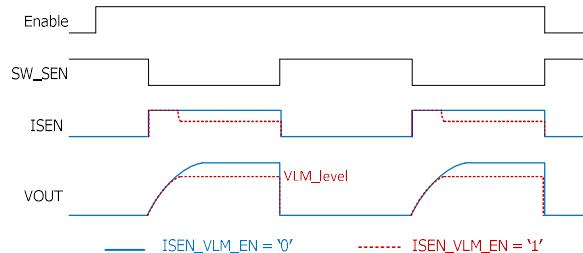


Figure 7-6: Conceptual waveform when ISEN_VLM_EN = '1' & '0' (external load is resistor parallel with capacitor)

Table 7-4: Sensor limiting voltage

Amount of voltage	Resolution	Min Vlim	Max Vlim
VLM_VALUE[7:0] x 5mV	5 mV	0	1.275 V

Table 7-5: Registers associated with the sensor biasing circuit

Register	Address	Function	Type	Factory preset value
ISEN_VALUE	0x0D.[5:0]	Defines output sourcing current value	Read/Write	"1100_1000"
ISEN_RANGE	0x0C.0	Defines output sourcing current range	Read/Write	"1"
ISEN_VLM_EN	0x0C.1	Enables output voltage limiter	Read/Write	"1"
ISEN_DC	0x0C.2	Defines sourcing current output waveforms	Read/Write	"0"
VLM_VALUE	0x0E.[7:0]	Defines output limiting voltage	Read/Write	"0000_0000"
ISEN_CH	0x0C.[5:4]	Defines ISEN output channel. "00" : S0 "10" : S2 "01" : S1 "11" : Not Connected	Read/Write	"11"
ISEN_EN	0x18.2	Enables current source circuit	Read/Write	"0"
VLM_DAC_EN	0x18.1	Enables internal DAC to create limiting voltage	Read/Write	"0"

Note that **ISEN_EN** and **VLM_DAC_EN** are automatically set when **GetADC** command is executed.

7.4 Analog-to-Digital Converter

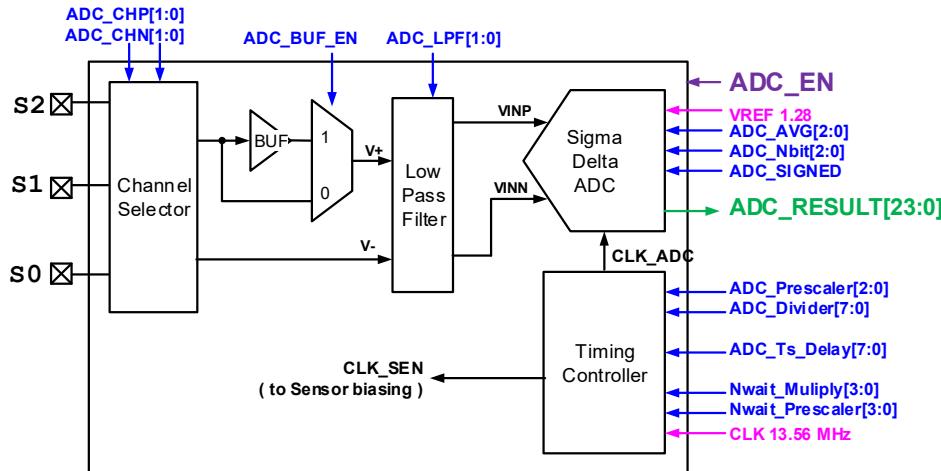


Figure 7-7: ADC Block Diagram

Figure 7-7 shows the ADC internal block diagram that comprised of Input channel selector, Voltage Buffer, Low Pass filter, Timing Controller, and Sigma-Delta ADC. The input channel selector, controlled by **ADC_CHP[1:0]** and **ADC_CHN[1:0]**, selects the positive input voltage and negative input voltage to ADC respectively. The built-in voltage buffer, controlled by **ADC_BUF_EN** bit, can be enabled to auxiliary repeat the input signal from pin in case of high-impedance source. However, the support voltage range is from 0.15 to 1.3V. In case of using sensor biasing (ISEN), the buffer should be used when sensor biasing current is less than 100 μ A.

To correct measurement error due to buffer offset, data in EEPROM page 48 and 49 storing buffer offset value measured during manufacturing can be received to calibrate measurement result. The calculation method will be described in the table below.

The Low Pass Filter (LPF), which corner frequency is configured by **ADC_LPF**, filters high frequency signal and noise before feeding signal to Sigma-Delta ADC. Table 7-6 shows the corner frequency following **ADC_LPF** configuration.

Table 7-6: ADC_LPF configuration

ADC_LPF	Corner Frequency
“00”	Disable LPF
“01”	1260 kHz
“10”	623 kHz
“11”	325 kHz

Sigma Delta ADC converts analog input voltage into digital output with selectable topology, differential or single-ended, controlled by **ADC_SING_MODE**. In differential mode, the equivalent input is different voltage between VINP and VNN node (VINP – VNN). In the singled ended mode, VNN is automatically connected to ground, so the voltage input is voltage at VINP node. For SIC4340, it support only single-ended mode, setting to differential mode causes incorrect ADC operation.

The voltage input range should be between 0 V to internal VREF 1.28V. The 24-bits **ADC_RESULT** is displayed in register page after conversion finishes. However, the output valid bit, resolution, is controlled by register **ADC_Nbit**. The detail of ADC conversion will be described in Table 7-7.

Table 7-7: Registers associated ADC signal path

Register	Address	Function	Type	Factory preset value
ADC_SING_Mode	0x0B.4	Define the ADC input topology ‘0’ : Differential Mode ‘1’ : Single Ended Mode (VNN is internally connected to GND)	Read/Write	“1”
ADC_CHP	0x0B.[1:0]	Define the ADC positive input channel “00” : S0 “10” : S2 “01” : S1 “11” : Not Connected	Read/Write	“11”

ADC_CHN	0x0B.[3:2]	Define the ADC negative input channel “00” : S0 “10” : S2 “01” : S1 “11” : Not Connected	Read/Write	“11”
ADC_LPF	0x0A.[1:0]	Define the ADC low pass corner frequency	Read/Write	“01”
ADC_BUF_EN	0x0A.4	Enable internal voltage buffer	Read/Write	“0”

Note that for typical operation, ADC_CH value should be same with ISEN_CH.

Timing controller creates 2 signals, **CLK SEN** and **CLK ADC** that have the same frequency, to operate sensor biasing circuit and Sigma-delta ADC respectively. This controller also controls sampling frequency, sampling point and number of warm up clock which are defined from register page. The detail of sampling scheme will be described in 7.4.1.

7.4.1 ADC Sampling scheme

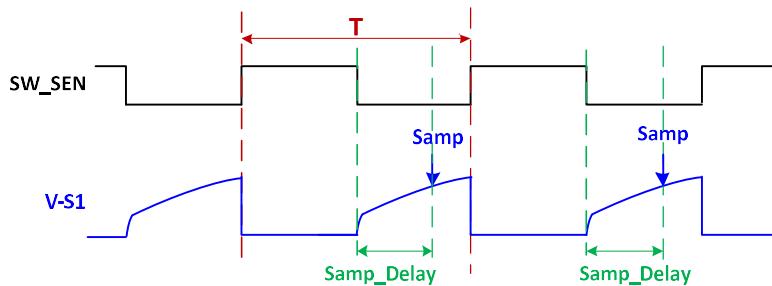


Figure 7-8: ADC Sampling Timing – Frequency and Sampling point

Figure 7-8 shows the conceptual of ADC sampling scheme. The ADC sampling frequency, equal to sensor bias frequency, can be set by two parameters : **ADC_Divider(D)** and **ADC_Prescaler(P)**, in register page. Equation below shows bias frequency formula :

$$f_{sen} = f_{adc} = 1/T = fc / [2^P \times (D+128)]$$

SIC4340 can produce biasing frequency from 300 Hz to 50 kHz. The carrier frequency (fc) is typically 13.56 MHz extracting from NFC carrier, the P values is defined following Table 7-8.

Table 7-8: frequency Prescaler

ADC Prescale[2:0]	Prescaler value (P)
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Table 7-9: Frequency setting value example

ADC Prescale[2:0]	Prescaler value (P)	ADC Prescale[2:0]	Prescaler value (P)
0	143	50.04 kHz	Maximum frequency
0	211	40 kHz	
2	211	10 kHz	Default Frequency
7	255	276.6 Hz	Minimum frequency

Because response waveform varies depend on sensor characteristic and models, if sensors model is a combination of resistance and capacitance, the sampling time will be effect to sampling voltage as shown in Table 7-8. Register **ADC_Ts_Delay[7:0]** controls delay time from rising edge of current sourcing to sampling point. The amount of delay is in multiple of prescaler clocks defined by **ADC_prescaler(P)** as shown in below equation :

$$\text{Samp_Delay} = ((\text{ADC_Ts_Delay}[7:0]) \times 2^P) / f_C$$

ADC_TS_Delay[7:0] allows flexibility in selecting the most sensitive or most suitable point for various type of sensor and the sampling period can be varied from 1% up to 49% duty cycle of sampling period.

Some sensor may require warm-up sampling prior to real sampling. SIC4340 provides pre-sampling biasing clock before real sampling for each conversion as shown in Figure 7-9. The number of warm up clock can be set by **Nwait_Multiplier[3:0] (M)** and **Nwait_Prescaler[3:0] (N)** as a following equation.

$$\#WarmUp = 8 + (M \times 2^N)$$

The period of warm-up clock is as same as period of sensor biasing frequency. The examples of number of warm-up clock is shown in Table 7-10.

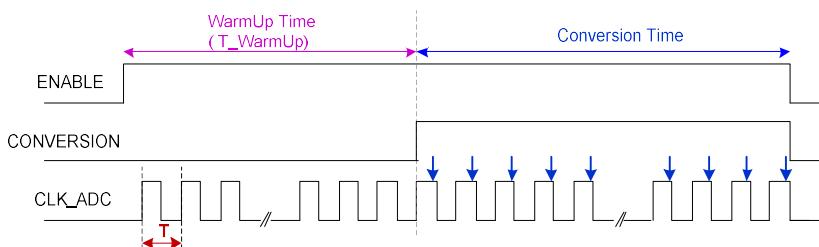


Figure 7-9: Warm Up Time timing

Table 7-10: The example of number of warm-up clock vs **Nwait_Multiplier[3:0]** and **Nwait_Prescaler[3:0]**

Nwait_Multiplier [3:0] (M)	Nwait_Prescaler [3:0] (N)	Number of Warm Up Clock
0000	0000	$8 + (0)$
0001	0001	$8 + (1 \times 2^1)$
0100	0010	$8 + (4 \times 2^2)$
0111	0110	$8 + (7 \times 2^6)$
1011	1001	$8 + (11 \times 2^9)$
1111	1111	$8 + (15 \times 2^{15})$

Table 7-11: Registers associated with ADC Sampling Scheme

Register	Address	Function	Type	Factory preset value
ADC_Divider	0x04.[7:0]	Defines ADC sampling frequency	Read/Write	"1101_0011"
ADC_Prescaler	0x05.[2:0]	Defines ADC sampling frequency	Read/Write	"010"
ADC_Ts_Delay	0x06.[7:0]	Defines ADC sampling times	Read/Write	"0101_1000"
NWait_Multiply	0x07.[7:4]	Defines number of warm up clocks	Read/Write	"1000"
NWait_Prescaler	0x07.[3:0]	Defines number of warm up clocks	Read/Write	"0000"

7.4.1 ADC Resolution and display

The register **ADC_NBit** defines oversampling ratio (OSR) that is the number of down-sampling clock of the circuit to yield the target number resolution of ADC bit. The more resolution is set, the longer conversion time is required. The typical **OSR** value and the effective output bit resolution is shown in Table 7-12.

Table 7-12: ADC_NBit[2:0] and resolution

ADC_NBit[2:0]	OSR	Resolution – effective bits (Differential mode)	Resolution – effective bits (Single ended mode)
000	32	6	5
001	64	8	7
010	128	9	8
011	256	10	9
100	512	10	9
101	1024	11	10
110	2048	11	10
111	4096	11	10

Due to internal ADC's architecture is designed in fully differential style, the ADC's input voltage range, VINP – VINN, can span from -VREF to +VREF. Setting to single ended mode , **ADC_SING_MODE** = '1' , cause the input voltage span from 0 to +VREF which half of fully differential as shown in Figure 7-10. Furthermore, it also reduces dynamic range by half or equivalent to 1 bit.

When set **ADC_Signed** to '1', the **ADC_RESULT** is displayed in the two's complement signed integer format which is suitable for further calculation. Normally, for single ended operation, the MSB of **ADC_RESULT** is always '0' because it can span from 0 to +VREF only. Table 7-13 and Table 7-14 show the possible **ADC_RESULT** output value related to **ADC_Signed** and effective output bit.

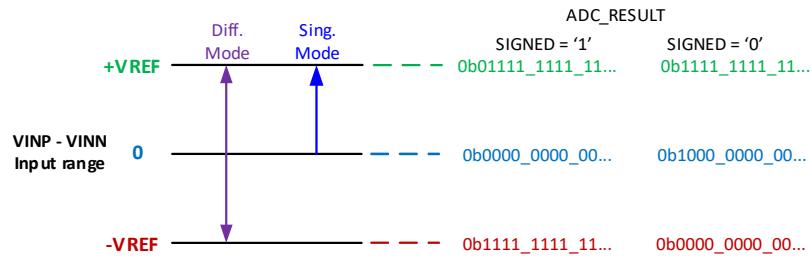


Figure 7-10: ADC input range and output display

Table 7-13: Minimum, and maximum value when ADC_Signed = '0'

Effective Output Bit	ADC_Signed = '0'						Single ended resolution	
	Min			Max				
	Min (Bin)	Min (Dec)	VOUT	Max (Bin)	Max (Dec)	VOUT		
6	000000	0	-VREF	111111	63	+VREF	5	
8	00000000	0	-VREF	11111111	255	+VREF	7	
10	00000000_00	0	-VREF	11111111_11	1023	+VREF	9	
11	00000000_000	0	-VREF	11111111_111	2048	+VREF	10	

Table 7-14: Minimum, and maximum value when ADC_Signed = '1'

Effective Output Bit	ADC_Signed = '1'						Single ended resolution	
	Min			Max				
	Min (Bin)	Min (Dec)	VOUT	Max (Bin)	Max (Dec)	VOUT		
6	111111	-32	-VREF	011111	31	+VREF	5	

8	11111111	-128	-VREF	01111111	127	+VREF	7
10	11111111_11	-512	-VREF	01111111_11	511	+VREF	9
11	11111111_111	-1024	-VREF	01111111_111	1023	+VREF	10

SIC4340 provides 24-bits register, located on register page address 0x01 to 0x03, to display results from ADC conversion. The results are displayed in MSB-to-LSB format from left to right.

The MSB of conversion results is arranged to the MSB of **ADC_RESULT [23:0]** for all output setting bit following by some fraction on the right hand side. Table 7-15 displays the example of readout value for each output bit in single ended mode.

Table 7-15: ADCOUT[23:0] display format and valid result

Valid Output Bit	ADCOUT[23:0]		Effective Result		Full Scale (Sing Mode)
	Bin	Hex	Bin	Dec	
6	01001100_10110100_11001101	4C B4 CD	010011	19	32
8	01001100_10110100_11001101	4C B4 CD	01001100	76	128
10	01001100_10110100_11001101	4C B4 CD	01001100_10	306	512
11	01001100_10110100_11001101	4C B4 CD	01001100_101	713	1024

The ADC also has averaging function. By setting register **ADC_AVG[2:0]**, the number of sample to be averaged is based on setting value as defined in Table 7-16.

The averaging function is performed within the ADC command. So, total conversion time can be calculated by equation as follows.

$$T_{conv} = \{ (N_AVG + 1) \times OSR \} + \#WarmUp / f_{adc}$$

Table 7-16: The number of averaged sample

ADC_AVG [2:0]	# Average Sample (N_AVG)
000b	1
001b	2
010b	4
011b	8
100b	16
101b	32
110b	64
111b	128

Table 7-17: Example for conversion time with various configuration

f _{adc}	#WarmUp	OSR	N_AVG	Conversion Time
10.0 kHz	8	1024	1	205.6 ms
10.0 kHz	8	1024	2	308.0 ms
10.0 kHz	8	1024	4	512.8 ms
40.0 kHz	8	1024	4	128.2 ms
40.0 kHz	8	512	4	64.1 ms
40.0 kHz	200	512	4	69.0 ms

Table 7-18: Registers associated with ADC Resolution, Result, Conversion time

Register	Address	Function	Type	Factory preset value
ADC_RESULT	0x01 – 0x03	ADC Conversion result	Read Only	0x00_00_00
ADC_NBit	0x08.[2:0]	Defines effective output bits	Read / Write	"101"
ADC_SIGNED	0x08.[3]	Defines output display format	Read / Write	"1"

ADC_AVG	0x08.[7:5]	Defines average times for conversion	Read / Write	"000"
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7.4.2 ADC Conversion Mode

There are three types of operation mode: (1) *Single Mode*; (2) *Continuous Mode*; (3) *Auto Conversion Mode*, to support different kinds of application. These modes are selectable from register **ADC_Conv_Mode[1:0]**.

7.4.2.1 Single Mode

This mode is for one time conversion. After receive command **GetADC** from NFC device, SIC4340 enables the sensor biasing circuit. After delay for settling circuit following T_{WarmUp} , SIC4340 starts conversion. When ADC conversion finish, **ADC_RESULT<23:0>** is kept in the register page and only 16-bits MSB **ADC_RESULT** response to NFC device. The timing is also shown in Figure 7-11.

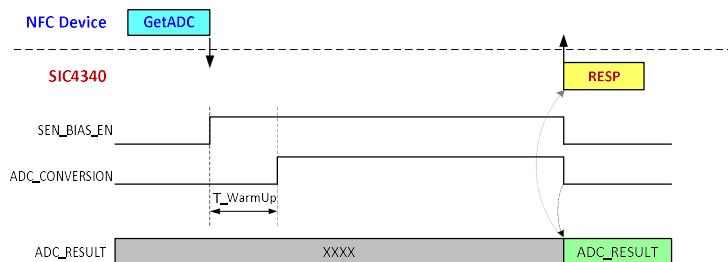


Figure 7-11: Timing for command **GetADC** operating in single mode

7.4.2.2 Continuous Mode

This mode is activated after changing **ADC_CONV_MODE<1:0>** to "10"b by either writing register or reloading from EEPROM. In this mode, after each conversion round finishes, SIC4340 automatically re-starts conversion immediately and **ADC_RESULT<23:0>** is updated. Issuing command **GetADC** receives response packet containing ADC conversion result in which the value is from the register **ADC_RESULT<23:0>** at that time. The timing for this mode is also shown in Figure 7-12. To stop this mode, change register **ADC_CONV_MODE<1:0>** to other mode.

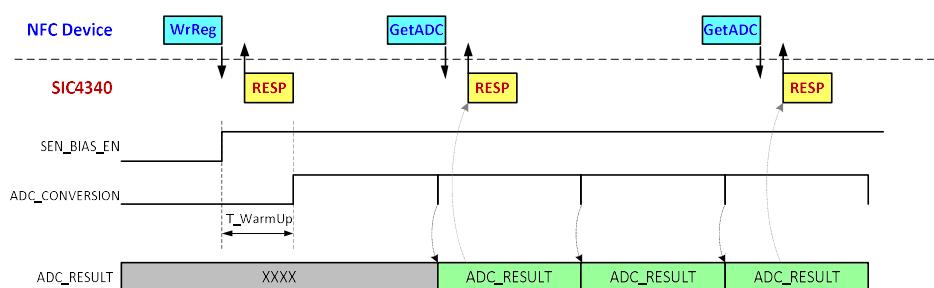


Figure 7-12: Timing for command **GetADC** operation with continuous mode

7.4.2.3 Auto Conversion Mode

In this mode, a dedicate timer involves in controlling sampling period of the ADC for each conversion round. SIC4340 also restarts conversion after finished each round similar to continuous mode. The difference is SIC4340 does not restart conversion immediately after previous conversion finishes, the ADC control circuit waits for system tick from the time before start of conversion. The period is defined from register **ADC_Auto_Conv_Period <2:0>**. The period for each conversion (**T_Auto_Period**) is shown in Table 7-19. This function is to ease real-time control in software or firmware in exercise sensor periodically.

Table 7-19: T_Auto_Period value

ADC_Auto_Conv_Period <2:0>	T_Auto_Period
000	50 ms
001	100 ms
010	200 ms
011	500 ms
100	1 s
101	2 s
110	5 s
111	10 s

The internal timer use carrier frequency as a clock source for counting. However, ISO14443A downlink pattern creates a missing clock due to gap in 100% ASK modulation. This causes counting time error from real time. Timing compensation scheme controlling by register **GAP_CMPEN_Config (0x1A)** enables period adjustment to match real time.

Figure 7-13 shows the concept timing diagram for gap compensation adjustment. When the gap occur at the antenna, clock signal that extracted from RF signal will be disappeared and internal timer counter stop. These creates a little bit error for **T_Auto_Period** value. So, the compensation scheme is introduced for reduce the error occurred from RF gap.

The gap period time is normally depended on reader and antenna characteristic. However, from ISO14443A standard, the nominal value of gap period is about 32.fc or 3.260 us.

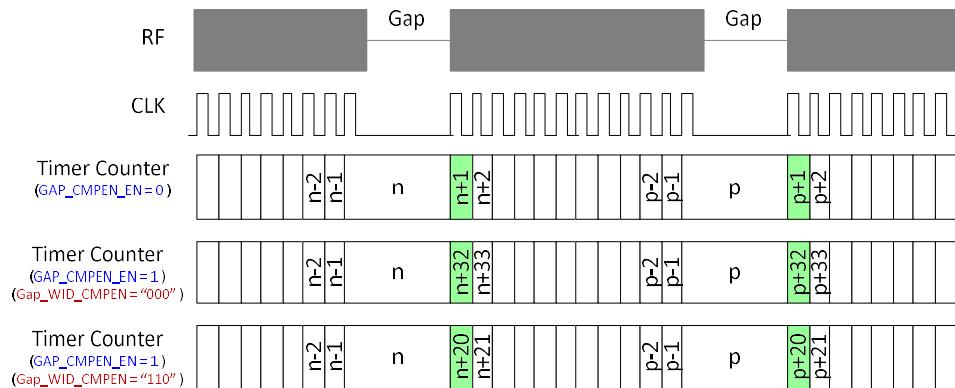
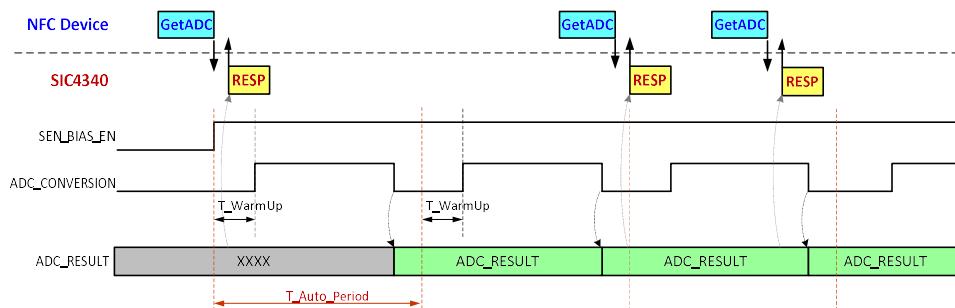
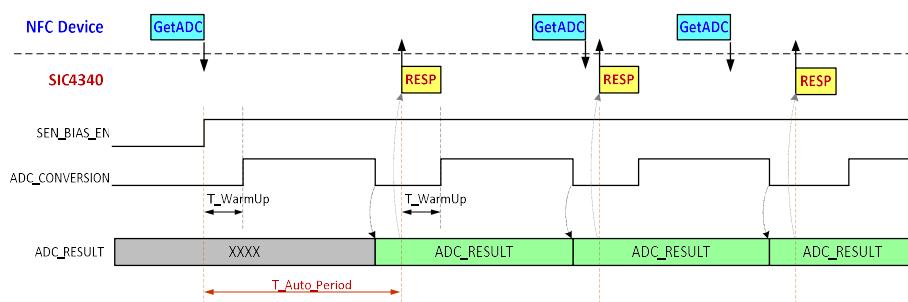


Figure 7-13: Gap Width Compensation scheme

The timing response in this mode can be controlled by bit **ADC_Auto_Resp** in register page (??). Clearing this bit to '0', SIC4340 immediately response ADC_RESULT kept in register page at that time. On the other side, setting to '1', SIC4340 returns response containing recent ADC conversion at the end of period. In this uplink duration, ADC does not operate. Then, in this scheme where uplink and ADC conversion is interleave, ADC conversion is not disturbed from power fluctuation due to uplink process. The basic timing for this mode is shown in Figure 7-14 and Figure 7-15.

Figure 7-14: Timing for command **GetADC** operating in Auto Conversion mode and **ADC_Auto_Resp= '0'**Figure 7-15: Timing for command **GetADC** operating in Auto Conversion mode and **ADC_Auto_Resp= '1'**

Note that, for both Continuous mode and Auto Conversion Mode, the command **GetADC** is just for getting results only, it does not affect or relate to ADC conversion process. These two modes can be stopped out by changing mode to *Single Mode*.

8. Commands

The SIC4340 supports two sets of operational commands which are basic RFID commands based on ISO14443A-3 standard and Register-accessing command.

8.1 Basic RFID commands

The basic RFID commands make the SIC4340 communicate with NFC/RFID reader devices in both downlink and uplink. This group of commands' format is based on the PICC states of the ISO 14443-3 standard. The Basic RFID commands are utilized in identifying UID and accessing EEPROM memory as a normal RFID.

8.1.1 REQA

REQA command changes the SIC4340 being in the "*Idle*" state into the "*Ready1*" state and make the transponder participate in further anti-collision and selection procedures. In response of **REQA**, the transponder sends 2 bytes **ATQA** back to the NFC/RFID reader device. Although the formula for response time ($(n*128-204) / fc$) looks different from that stated in the ISO 14443 standard, it is as same as that of the ISO 14443 standard because it count from end of downlink frame.

Table 8-1: **REQA** command format

CMD	REQA	
Format	0x26 (7 bits)	
Response	Successful operation	ATQA (2 bytes)
	Error	No response
Operation	Change state from the " <i>Idle</i> " state into the " <i>Ready1</i> " state.	

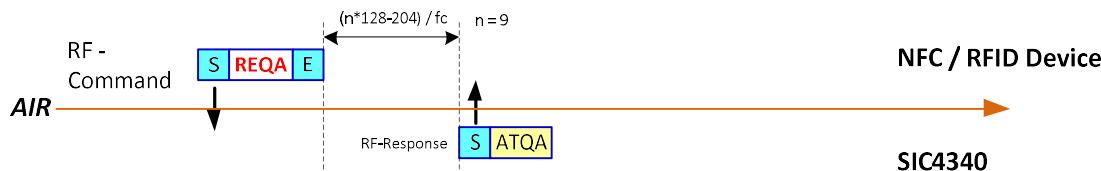


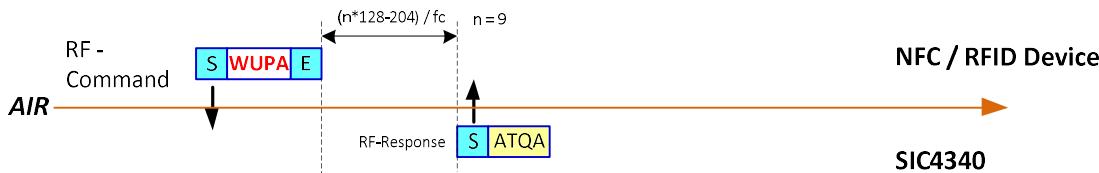
Figure 8-1: **REQA** command frame with a response

8.1.2 WUPA

The purpose of **WUPA** command is as same as **REQA**. The only difference is **WUPA** can be used in both "*Idle*" and "*Halt*" state.

Table 8-2: **WUPA** command format

CMD	WUPA	
Format	0x52 (7 bits)	
Response	Successful operation	ATQA (2 bytes)
	Error	No response
Operation	Change state from the " <i>Idle</i> " or " <i>Halt</i> " state into the " <i>Ready1</i> " state.	

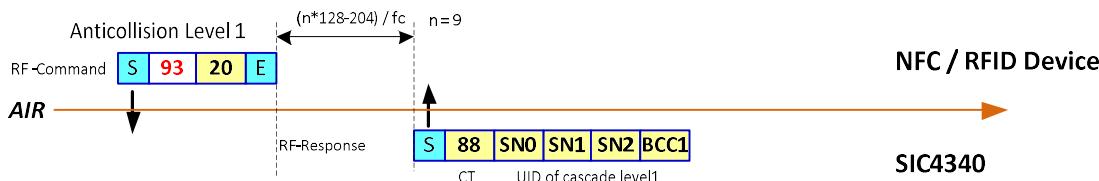
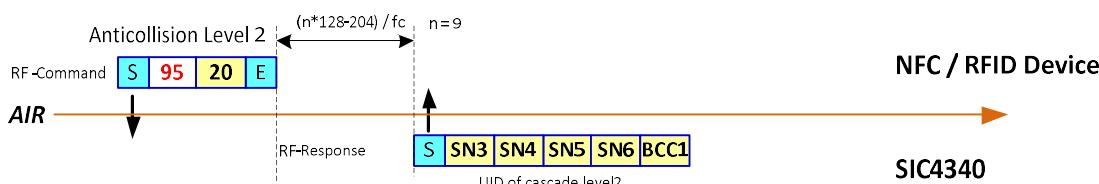
Figure 8-2: **WUPA** command frame with a response

8.1.3 ANTI-COLLISION

The **ANTI-COLLISION** command is used in the anti-collision procedure with bit oriented anti-collision frames. The purpose of **ANTI-COLLISION** command is to identify the target transponder and retrieve UID. The **ANTI-COLLISION** command can be used in both cascade level 1, which states are “Ready1”, “Ready1*” and cascade level 2 which states are “Ready2” and “Ready2*” state. The **ANTI-COLLISION** consists of SEL code representing current cascaded level, number of valid bit (NVB) and data. In the cascade level 1, the SEL code is 0x93 while the SEL code is 0x95 for the cascaded level 2. Transaction of **ANTI-COLLISION** command and its response in both cascade level 1 and cascade level 2 are depicted in Figure 8-3 and Figure 8-4. For the cascade level 1, the SIC4340 response CT (cascade tag) code and first 3-byte of UID. The CT code is 0x88.

Table 8-3: **ANTI-COLLISION** command format

CMD	ANTI-COLLISION	
Format	SEL + NVB + Data Cascade level1 : 0x93 + NVB + Data Cascade level2 : 0x95 + NVB + Data	
Response	Successful Operation	UID
	Error	No response
Operation	Response remaining part of UID and it BCC	

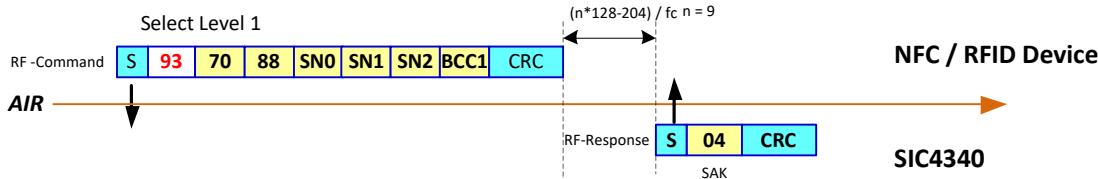
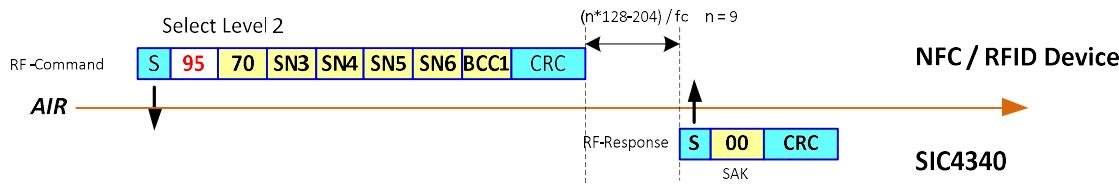
Figure 8-3: **ANTI-COLLISION** in the cascade level 1 with a responseFigure 8-4: **ANTI-COLLISION** in the cascade level 2 with a response

8.1.4 SELECT

The **SELECT** command format is based on the same structure as the **ANTI-COLLISION** command with 2-byte CRC appended at the end. The SIC4340 responds to NFC/RFID reader device with a **SAK** (select acknowledgement) code of 0x04 in “**Ready1**”, “**Ready1****” state, indicating UID is not complete and **SAK** code of 0x00 in “**Ready2**”, “**Ready2****”, indicating UID is complete and state transits to “**Active**” state or “**Active****”. Figure 8-5 and Figure 8-6 show the **SELECT** command for the cascade level1 and cascade level2, respectively.

Table 8-4: **SELECT** command format

CMD	SELECT
Format	SEL + NVB + Data Cascade level1 : 0x93 + 0x70 + UID (4 bytes) + BCC + CRC Cascade level2 : 0x95 + 0x70 + UID (4 bytes) + BCC + CRC
Response	Successful operation SAK + CRC SAK = 0x04 for cascade level 1 SAK = 0x00 for cascade level 2
	Error No response
Operation	Change state from “ Ready1 ” or “ Ready1** ” to “ Ready2 ” or “ Ready2** ” , or change state from “ Ready2 ” or “ Ready2** ” to “ Active ” or “ Active** ”. Respond SAK (select acknowledgement).

Figure 8-5: **SELECT** level1 command frame with a responseFigure 8-6: **SELECT** level2 command frame with a response

8.1.5 HLTA

The purpose of **HLTA** command is to move transponder that is already processed into a waiting state. The SIC4340 receiving **HLTA** in “**Active**” or “**Active****” state changes its state to “**Halt**”. By using this command, the NFC/RFID reader device can identify the transponders, which are already read and those have not yet been read. The SIC4340 that receives **HLTA** in “**Ready1**” and “**Ready2**” transits to “**Idle**”. Receiving **HLTA** in other state changes the state to the “**Halt**” state. There is no response sent back to NFC/RFID reader device for this command. Note that any change of lock bit in EEPROM is reloaded when state jumps back to “**Idle**” or “**Halt**” and lock bit effects after that.

Table 8-5: **HLTA** command format

CMD	HLTA
Format	0x50 + 0x00 + CRC
Response	None
Operation	Change state from “ Active ” or “ Active** ” to “ Halt ” state Reload lock bit in EEPROM to make it effect take place

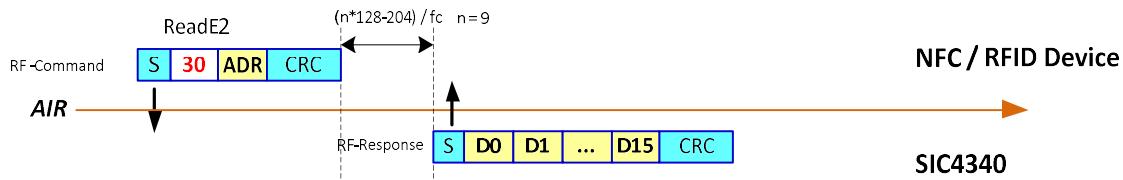
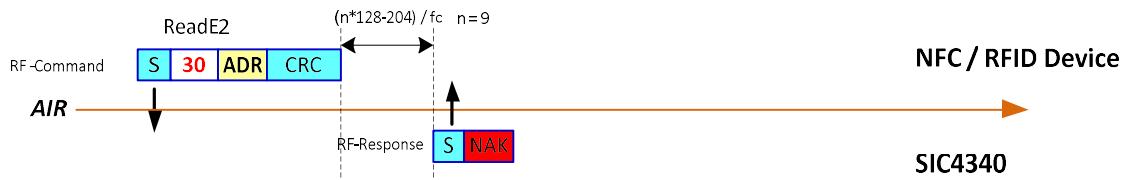
Figure 8-7: **HALT** command frame

8.1.6 ReadE2

The purpose of **ReadE2** command is to read the EEPROM content. The **ReadE2** command contains a page address with a valid CRC. If the transponder gets a valid address in command, it responds the NFC/RFID reader device by sending 16 bytes (4 pages) starting from the addressed page and if the address is not valid it sends a 4-bit NAK.

Table 8-6: **ReadE2** command format

CMD	ReadE2
Format	0x30 + Block + CRC (2 bytes)
Response	Successful operation
	Error
Operation	Read data from EEPROM at a specific address

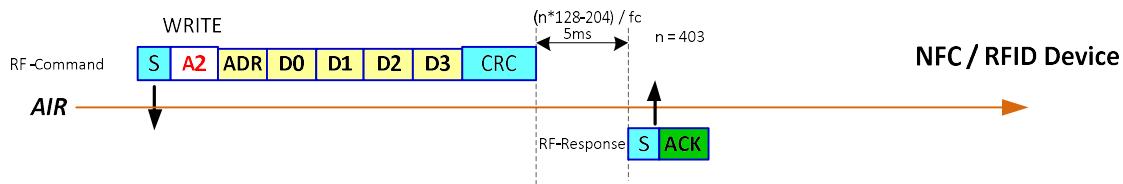
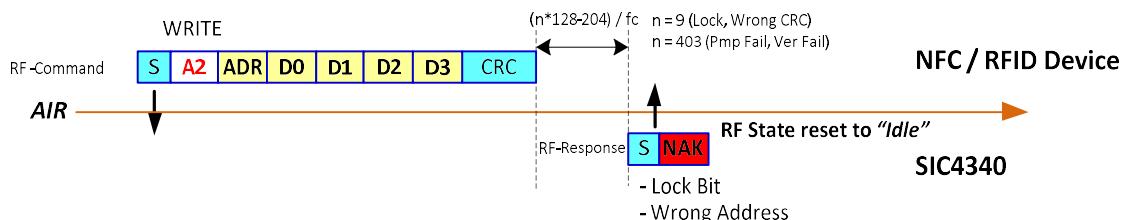
Figure 8-8: **ReadE2** command frame with responseFigure 8-9: **ReadE2** command frame with a negative acknowledgement in response

8.1.7 WriteE2

The purpose of **WriteE2** command is to write the EEPROM, program lock bits, set bits in the OTP byte and preset an initial register value. The SIC4340 is receiving the **WriteE2** command with a valid address in the “**Active**” or “**Active***” state programs received 4-bytes data to the addressed page and sends an ACK to the NFC/RFID reader device. If the address is not valid or the addressed page is already locked, the SIC4340 responds with a NAK.

Table 8-7: **WriteE2** command format

CMD	WriteE2
Format	0xA2 + ADR + D0 + D1 + D2 + D3 + CRC (2 bytes)
Response	Successful operation
	ACK (4 bits)
Operation	Check permission at target address and write data to EEPROM

Figure 8-10: **WriteE2** command frame with an **ACK** response indicating successful operationFigure 8-11: **WriteE2** command frame with a **NAK** response indicating unsuccessful operation

8.1.8 Compatible WriteE2

The purpose of **Compatible WriteE2** command is to make programming process backward compatible with the MIFARE classic system. The command contains a page address with a CRC. If the SIC4340 gets a valid address, it responds the NFC/RFID reader device with an **ACK**, else a **NAK**. The NFC/RFID reader device again sends 16-byte data but only the first 4 bytes are written into the memory. It is recommended to set the remaining bytes to '0'. Process of executing the **Compatible WriteE2** command is depicted in the Figure 8-12 and Figure 8-13.

Table 8-8: **Compatible WriteE2** command format

CMD	Compatible Write E2
Format1	0xA0 + ADR + CRC (2 bytes)
Response1	Successful operation ACK (4 bits)
	Error NAK (4 bits)
Format2	Block Data (16 bytes) + CRC (2 bytes)
Response2	Successful operation ACK (4 bits)
	Error NAK (4 bits)
Operation	Check permission at target address and write data to EEPROM (only first 4 bytes are written)

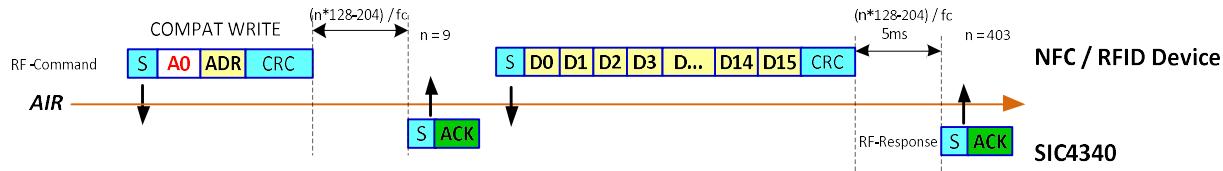
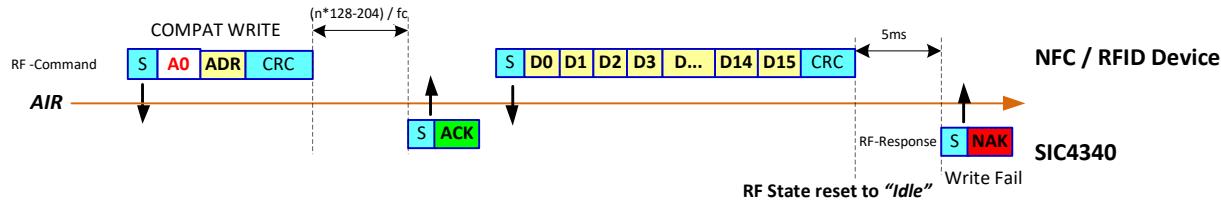
Figure 8-12: Two-step operation of **Compatible Write E2** with an **ACK** response

Figure 8-13: One-step operation of **Compatible Write E2** with a NAK responseFigure 8-14: Two-step operation of **Compatible Write E2** with a NAK response

8.2 RF-Reg & RF-ADC commands

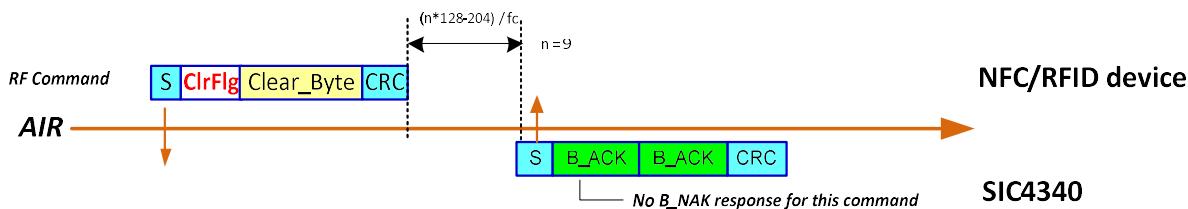
8.2.1 Clear_Flag

NFC/RF devices send the **Clear_Flag** command to clear the error flags presenting in the last **B_NAK** to make the communication process going on. The error flags are **VDD_DROP_H** and **VDD_DROP_L**. The command contains "Clear_Byt", which can be set to clear each error flag individually. The detail of "Clear_Byt" is shown in Table 8-9.

If there is no protocol error such as CRC error, RF error or framing error, the response from this command is always **B_ACK**. Although response is **B_ACK**, it does not ensure that the associated flag in "Clear_Byt" is cleared. NFC/RF device needs to read the register 0x00 to check the current status of the flags again or check **B_ACK** or **B_NAK** in the next response frame. It is possible that the failed situation is still present. For example, input power is still weak. Then, **VDD_DROP_H** is still flagged, although the command **Clear_Flag** is sent.

Table 8-9: **Clear_Flag** command format

CMD	Clear_Flag
Format	0xB4 + Clear_Byt + CRC
Response	Successful operation
	B_ACK + B_ACK + CRC
	-
Clear_Byt	Clear_Byt.bit0 : Clear "VDD_DROP_L" flag Clear_Byt.bit1 : Clear "VDD_DROP_H" flag Clear_Byt.bit2-6 : RFU <i>Example : Clear_Byt = 0x03 : VDD_DROP_H and VDD_DROP_L</i>

Figure 8-15: **Clear_Flag** command frame

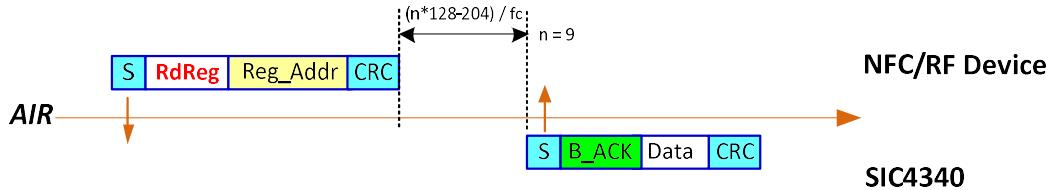
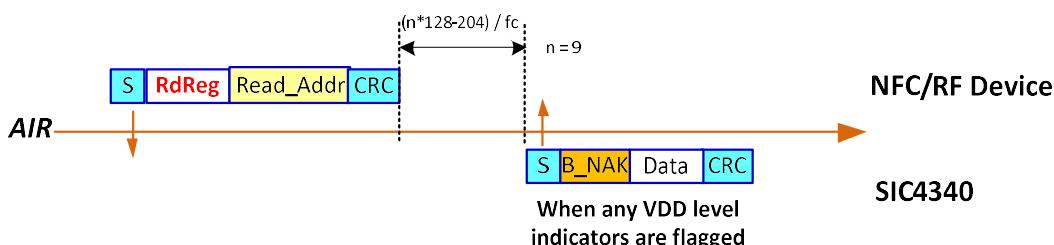
8.2.2 ReadReg

The purpose of **ReadReg** command is to read register value. The response frame consists of **B_ACK** or **B_NAK** with the current accessed register value. If the reading address is out of range, data in response package is 0x00. If the last clearing is not complete or power is insufficient until the indicator flags again, the response contains with a **B_NAK**.

Table 8-10: **ReadReg** command format

CMD	ReadReg
Format	0xB5 + Reg_Addr + CRC
Response	Successful operation : B_ACK + Data + CRC Operation error : B_NAK + Data + CRC

		when any VDD Level indicators are flagged
	CRC error,RF error,Framing error	NAK (4 bits)
Operation	Read Data from register. If the address is out of range, response frame consists of B_ACK with data 0x00	

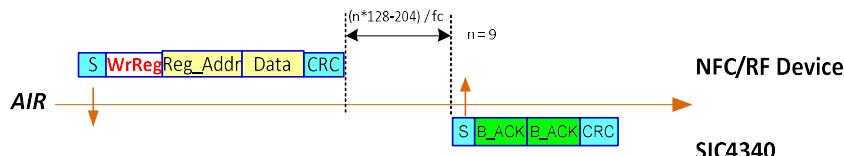
Figure 8-16: **ReadReg** command frame with a positive acknowledge responseFigure 8-17: **ReadReg** command frame with a negative acknowledge response

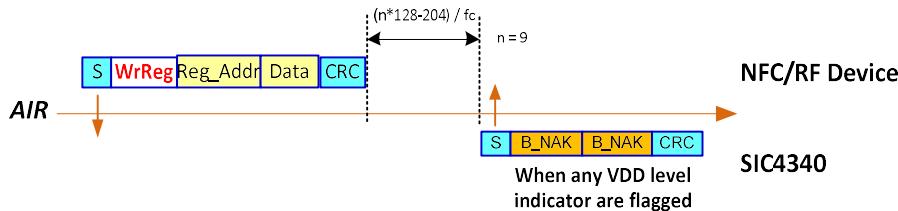
8.2.3 WriteReg

The purpose of **WriteReg** command is to write a register value. The response frame can be B_ACK or B_NAK depending the input power level. If the address is out of range or address is read-only, response frame is still B_ACK. If the last clearing is not complete or power is insufficient until the indicator flags again, the response contains with a B_NAK.

Table 8-11: **WriteReg** command format

CMD	WriteReg
Format	0xB6 + Reg_Addr + Data + CRC
Response	Successful operation
	B_ACK + B_ACK + CRC
	B_NAK + B_NAK + CRC when any VDD level indicators are flagged
CRC error, RF error, Framing error	NAK (4 bits)
Operation	Write data to register. If the address is out of range or address is read-only, response frame is still B_ACK.

Figure 8-18: **WriteReg** command frame with a positive acknowledge response

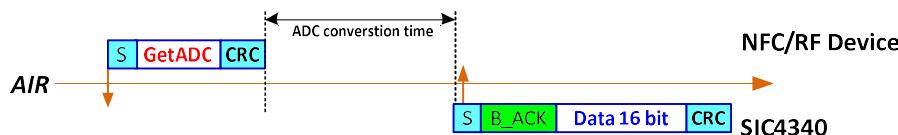
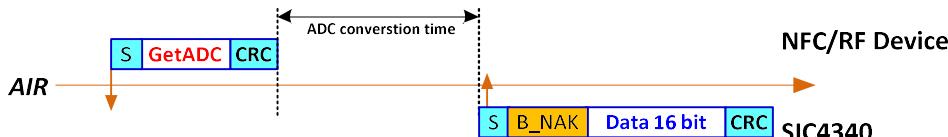
Figure 8-19: **WriteReg** command frame with a negative acknowledge response

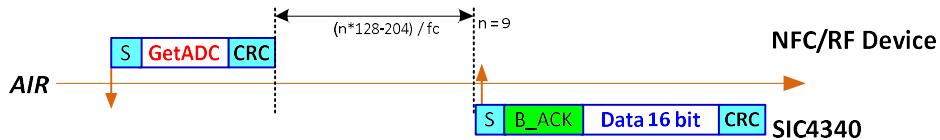
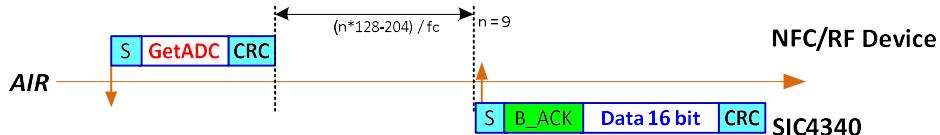
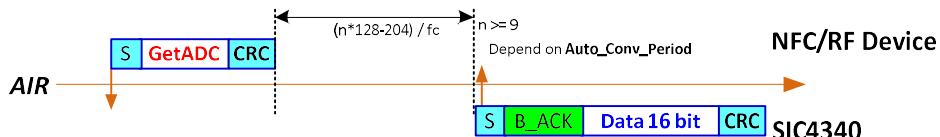
8.2.4 GetADC

The purpose of **GetADC** command is to acquire ADC_RESULT. The response frame can be **B_ACK** or **B_NAK** with the 16-bits MSB results, **ADC_RESULT<23:8>**. If the last clearing flag is not complete or power supply at **VDD** is still too low until the indicator flags again, the response contains with a **B_NAK**. The **B_NAK** indicates that **ADC_RESULT** may not be reliable due to insufficient power supply level. The response time is depended on **ADC_CONV_MODE** and **ADC_Auto_Resp** as defined in 7.4.2.

Table 8-12: **GetADC** command format

CMD	WriteReg
Format	0xB8 + 0x00 + CRC
Response	Successful operation
	B_ACK + ADC_RESULT<23:8> + CRC
	B_NAK + ADC_RESULT<23:8> + CRC when any VDD level indicators are flagged
	NAK (4 bits)
Operation	Depend on ADC_CONV_MODE<1:0> : "0X" – Single Mode <ul style="list-style-type: none"> • Turn on sensor driver and start conversion. • Wait until conversion complete and response ADC_RESULT
	"10" – Cont Mode <ul style="list-style-type: none"> • Response current ADC_RESULT in Register Page
	"11" – Auto Mode with ADC_Auto_Resp = '0' <ul style="list-style-type: none"> • Response current ADC_RESULT in Register Page
	"11" – Auto Mode with ADC_Auto_Resp = '1' <ul style="list-style-type: none"> • Wait until timer trigs and response ADC_RESULT

Figure 8-20: **GetADC** command frame with a positive acknowledge response when **ADC_Conv_Mode = "00"** (Single Mode)Figure 8-21: **GetADC** command frame with a negative acknowledge response when **ADC_Conv_Mode = "00"** (Single Mode)

Figure 8-22: **GetADC** command frame with a positive acknowledge response when **ADC_Conv_Mode** = "10" (Cont. Mode)Figure 8-23: **GetADC** command frame with a positive acknowledge response when **ADC_Conv_Mode** = "11" (Auto. Mode) and **ADC_Auto_Resp** = '0'Figure 8-24: **GetADC** command frame with a positive acknowledge response when **ADC_Conv_Mode** = "11" (Auto. Mode) and **ADC_Auto_Resp** = '1'

8.3 Response Acknowledge

SIC4340 uses two kinds of acknowledgement to respond to NFC/RFID devices. The first type of acknowledgement is a 4-bit type compliant to the NFC Tag Type 2 standard and the second type of acknowledgement is an 8-bit type used in the RF-Reg and RF-ADC communication and the register page access. If the SIC4340 answers with a 4-bit NAK, the RF state goes back to "*Idle*" or "*Halt*". If the response is an 8-bit NAK, the RF state still remains in "*Active*". The 8-bit acknowledgement contains status flags, resulting from event capturing **VDD** voltage related level. The detail of 4-bit and 8-bit flag responses are summarized in Table 8-13 and Table 8-14 respectively.

Table 8-13: 4-bits ACK/NAK

Response Flag	Code	Description
ACK	1010b	Positive acknowledge indicate operation is successful.
NAK	0000b	Negative acknowledge indicate accessing address is out of range or accessed block is locked.
	0001b	Negative acknowledge indicate parity or CRC is error, or data in write command is less than 4 bytes.

Table 8-14: 8-bits ACK/NAK

Response Flag	Code	Description		
B_ACK	0x1A	Positive acknowledge indicate operation is successful.		
B_NAK	0xYY	Bit	Error flag	Command can cause error
		Bit 0	VDD_DROP_L	RdReg, WrReg, GetADC
		Bit 1	VDD_DROP_H	RdReg, WrReg, GetADC
		Bit 2 to 6	Always set to logic '0'	

		Bit 7	Always set to logic '1'
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Table 8-15 shows meaning of error flag in B_NAK and its trigger event. When any flags are set, command **Clear_Flag** can reset these bits to '0'. Note that each error can separately be flagged depending on a situation. The purpose of the flags is to record events related to power to show the reliability of the ADC Conversion.

Table 8-15: Meaning of error flag in B_NAK

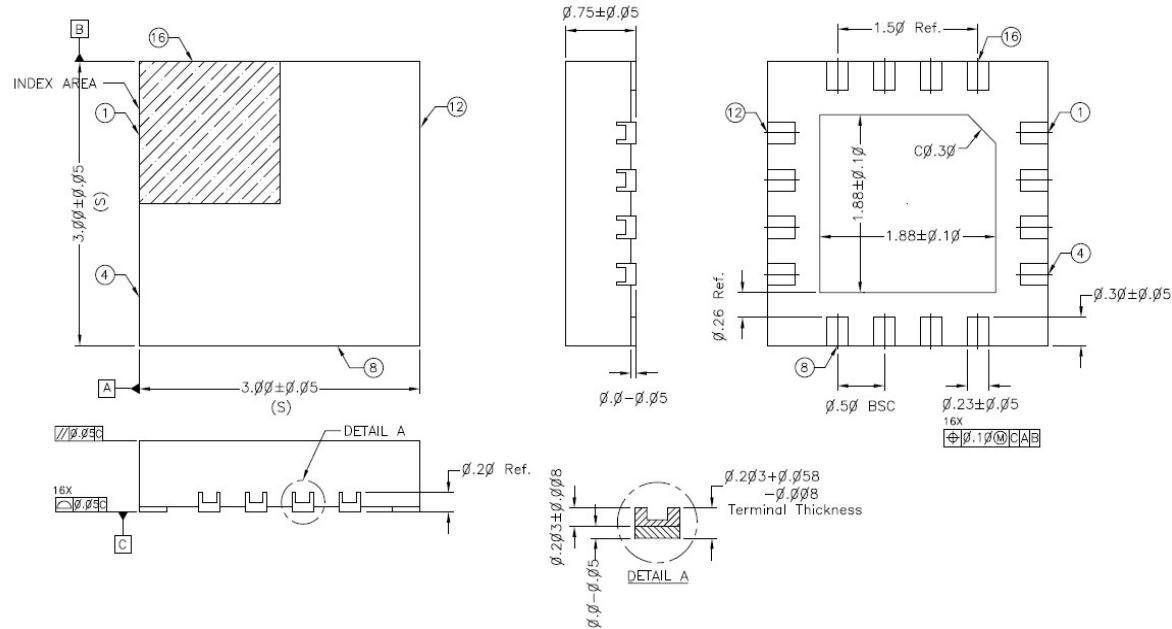
Error flag	Type	Description	Trigger Event
VDD_DROP_L	Flag	Voltage on VDD drop lower than VDD_L level	VDD_RDY_L status becomes '0'
VDD_DROP_H	Flag	Voltage on VDD drop lower than VDD_H level	VDD_RDY_H status becomes '0'

To ensure the ADC operation, SIC4340 monitors the VDD voltage level and displays through two status bits in the register page as shown in the left column of Table 8-16. If any status bits go to failed state, the inverted value of such failed status is stored in the **B_NAK** flag as shown in the right column of Table 8-16.

Table 8-16: VDD level Status and VDD level Flag

Status	Error Flag in "BNAK"
VDD_RDY_L (Reg : 0x00.0)	" VDD_DROP_L " (BNAK : Bit 0)
VDD_RDY_H (Reg : 0x00.1)	" VDD_DROP_H " (BNAK : Bit 1)

9. Packaging and Dimension



NOTE : CONTROL DIMENSION IN MM.

Figure 9-1: QFN3x3-16 pin package dimension

10. Appendix

10.1 ADC Calculation Method

To acquire conversion voltage from **GetADC** command, the calibration data stored in the EEPROM must be applied for calculation the correct output. The calculation procedure is separated into 2 method depended on **ADC_BUF_EN** configuration in register page.

10.1.1 Calculation when **ADC_BUF_EN = '0'**

In case of **ADC_BUF_EN = '0'**, after receiving **ADC_RESULT** from SIC4340, the application program or software must do a procedure following Figure 10-1. The calibration data stored in EEPROM page 0x2E must be applied for calculation as the example shown in Table 10-1 and Table 10-2.

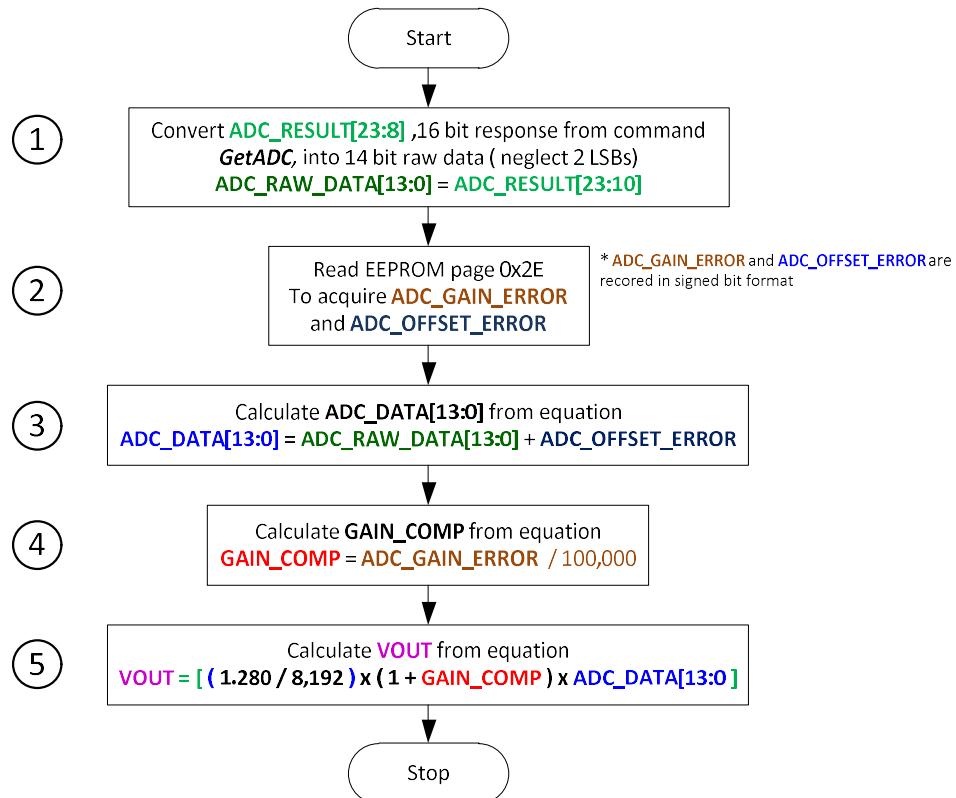


Figure 10-1: Operation flow for calculating output voltage (VOUT) from GetADC command when **ADC_BUF_EN = '0'**

Table 10-1: ADC output calculation example-1 when ADC_BUF_EN = '0'

Step	Parameter	Method	Value	Unit
0	ADC_RESULT[23:8]	Response from GetADC command	68 A1	Hex
1	ADC_RAW_DATA[13:0]	ADC_RAW_DATA[13:0] = ADC_RESULT[23:10]	1A 28	Hex
2	ADC_OFFSET_ERROR	Read from EEPROM page 0x2E byte 2 & 3	00 24	Hex
	ADC_GAIN_ERROR	Read from EEPROM page 0x2E byte 0 & 1	FE 80	Hex
3	ADC_DATA[13:0]	ADC_RAW_DATA[13:0] + ADC_OFFSET_ERROR (signed bit)	1A 4C	Hex
4	GAIN_COMP	ADC_GAIN_ERROR / 100,000 (signed bit)	-0.00384	Gain
5	VOUT	VOUT = [(1.280 / 8,192) x (1 + GAIN_COMP) x ADC_DATA[13:0]]	1.0478	Volt

Table 10-2: ADC output calculation example-2 when ADC_BUF_EN = '0'

Step	Parameter	Method	Value	Unit
0	ADC_RESULT[23:8]	Response from GetADC command	68 A1	Hex
1	ADC_RAW_DATA[13:0]	ADC_RAW_DATA[13:0] = ADC_RESULT[23:10]	1A 28	Hex
2	ADC_OFFSET_ERROR	Read from EEPROM page 0x2E byte 2 & 3	FA 00	Hex
	ADC_GAIN_ERROR	Read from EEPROM page 0x2E byte 0 & 1	01 00	Hex
3	ADC_DATA[13:0]	ADC_RAW_DATA[13:0] + ADC_OFFSET_ERROR (signed bit)	19 C8	Hex
4	GAIN_COMP	ADC_GAIN_ERROR / 100,000 (signed bit)	0.00256	Gain
5	VOUT	VOUT = [(1.280 / 8,192) x (1 + GAIN_COMP) x ADC_DATA[13:0]]	1.0339	Volt

10.1.2 Calculation when ADC_BUF_EN = '1'

In case of ADC_BUF_EN ='1', application program or software must do a procedure Figure 10-3 which is approached by linear interpolation concept as shown Figure 10-2. The calibration data stored in EEPROM page 0x30 and 0x31 must be applied for calculation as the example in Table 10-3 and Table 10-4.

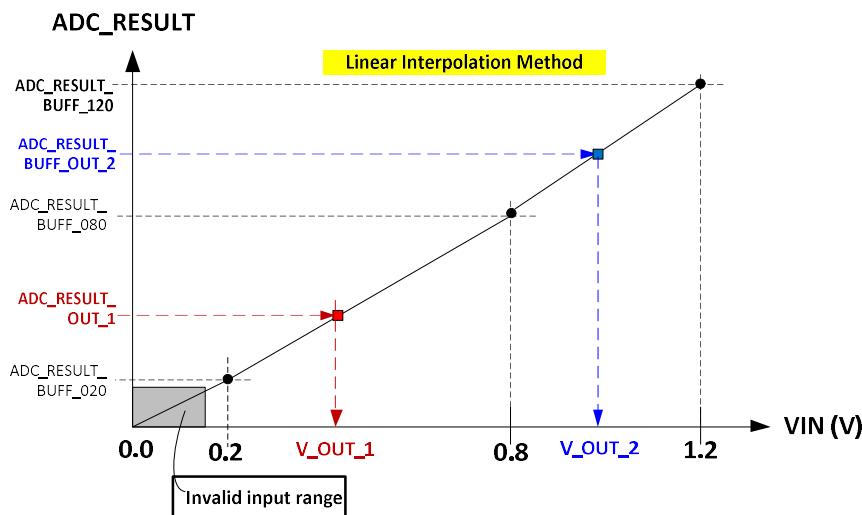


Figure 10-2: Linear interpolation scheme

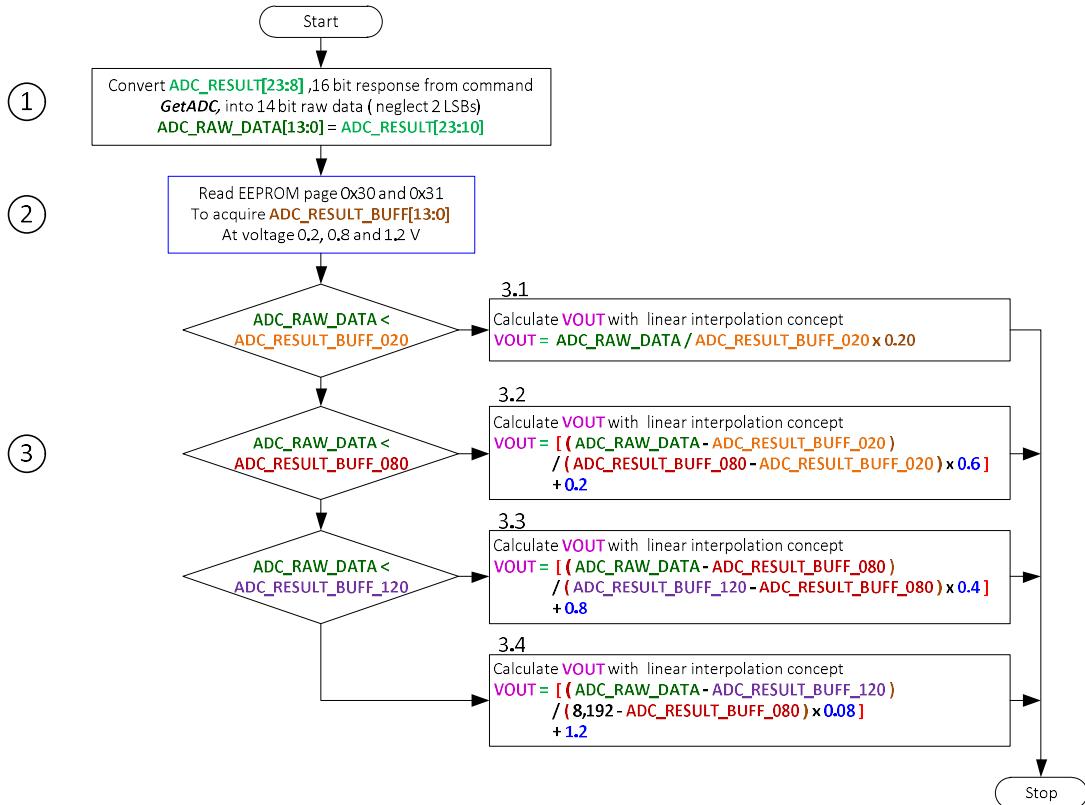


Figure 10-3: Operation flow for calculating output voltage (VOUT) from GetADC command when ADC_BUF_EN = '1'

Table 10-3: ADC output calculation example-3 when ADC_BUF_EN = '1'

Step	Parameter	Method	Value	Unit
0	ADC_RESULT[23:8]	Response from GetADC command	58 05	Hex
1	ADC_RAW_DATA[13:0]	ADC_RAW_DATA[13:0] = ADC_RESULT[23:10]	16 01	Hex
2	ADC_RESULT_BUFF_020	Read from EEPROM page 0x30 byte 0 & 1	04 F6	Hex
	ADC_RESULT_BUFF_080	Read from EEPROM page 0x30 byte 2 & 3	14 04	Hex
	ADC_RESULT_BUFF_120	Read from EEPROM page 0x31 byte 0 & 1	1E 24	Hex
3	VOUT	$\begin{aligned} \text{VOUT} = [(\text{ADC_RAW_DATA} - \text{ADC_RESULT_BUFF_080}) \\ / (\text{ADC_RESULT_BUFF_120} - \text{ADC_RESULT_BUFF_080}) \times \\ 0.4] \\ + 0.8 \\ (\text{Condition 3.3}) \end{aligned}$	0.8785	Volt

Table 10-4: ADC output calculation example-4 when ADC_BUF_EN = '1'

Step	Parameter	Method	Value	Unit
0	ADC_RESULT[23:8]	Response from GetADC command	1F CA	Hex
1	ADC_RAW_DATA[13:0]	ADC_RAW_DATA[13:0] = ADC_RESULT[23:10]	07 F2	Hex
2	ADC_RESULT_BUFF_020	Read from EEPROM page 0x30 byte 0 & 1	04 F6	Hex
	ADC_RESULT_BUFF_080	Read from EEPROM page 0x30 byte 2 & 3	14 04	Hex
	ADC_RESULT_BUFF_120	Read from EEPROM page 0x31 byte 0 & 1	1E 24	Hex
3	VOUT	$\begin{aligned} \text{VOUT} = [(\text{ADC_RAW_DATA} - \text{ADC_RESULT_BUFF_020}) \\ / (\text{ADC_RESULT_BUFF_080} - \text{ADC_RESULT_BUFF_020}) \times \\ 0.6] \\ + 0.2 \end{aligned}$	0.3189	Volt

		(Condition 3.2)		
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