Vikas M

Design and Verification Engineer
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Career Objective

Highly motivated to excel in the VLSI domain, I am seeking an entry-level position as a Design and Verification Engineer. Eager to apply my theoretical knowledge and practical skills, I aim to contribute to organizational success that will provide me boundless growth, opportunities in VLSI

Professional Training **[28/6/2023-17/2/2024]**

Advanced VLSI Design and verification course
Maven silicon VLSI Design and Training Center, Bengaluru.

Education

- **Sir M Visvesvaraya Institute of Technology Bengaluru** **[2020-2023]**
  BE in Electronics and communication Engineering, cgpa - 8

- **SJM Polytechnic, Chitradurga** **[2017-2020]**
  Diploma in Electronics and communication, Percentage - 72%

- **Prathana High School** **[2016-2017]**
  SSLC percentage - 68%

Projects

1.Router 1x3 -RTL design and verification

Description: Router is a networking device which routes the incoming packet from a source network to one of the destination networks among the three, based on the address available in the packet.

Languages: Verilog HDL, System Verilog and UVM
Tools: Module sim**,** Questa Sim, VC Spyglass.

2.AHB to APB Bridge IP core – verification

Description: The AHB to APB bridge is an AHB slave which works as an interface between the high speed AHB and the low Performance APB buses.

Languages: System Verilog and UVM
Tools: Questa Sim and VCS.

3.Medicine delivery Robot

Description: In this project we done a proto type of medical dispatching robot it will deliver medicine to the patient time to time.

Language: Embedded C.
Tools: Arduino IDE.

VLSI Domin Skills

- **HDL**: Verilog
- **HVL**: System Verilog
- **EDA Tool**: Mentor Graphics-Questasim Xilinx-ISE
- **Verification Methodology**: Constraint Random Coverage Driven Verification.
- **TB Methodology**: UVM
- **Protocols**: AHB, APB
- **Domain**: ASIC/FPGA Front-End Design and Verification
- **Operating System**: Linux, Windows
- **Core Skills**: RTL Coding using synthesizable constructs of Verilog, Code Coverage, Functional coverage, synthesis, static timing analysis.
- **Programming Languages:** Good knowledge of OOPs concept, Class, Inheritance, Polymorphism, C Programing, MATLAB. Digital Electronics, Verilog, System Verilog, UVM.

Design Skills

- **Digital Electronics**: Combinational Sequential circuits, FSM, Memories, CMOS implementation, Stick diagram.
- **Verilog Programming**: Data types, Operators, Processes, BA NBA, Delays in Verilog, begin - end fork join blocks, looping branching construct, System tasks Functions, compiler directives, FSM coding, Synthesis issues, Races in simulation, pipelining RTL TB Coding.
- **Advance Verilog**: Generate block, Continuous Procedural Assignments, Self-checking testbench, Automatic Tasks, Named Events and Stratified Event Queue.
- **Code Coverage**: Statement and branch coverage, Condition Expression Coverage, Toggle FSM Coverage. Advanced Verilog Code Coverage.

Verification skills

- **Memories:** Dynamic array, Queue, Associative array, Task Function- Pass by reference
- **Interface**: Modport and Clocking block.
- **Basic and Advanced Object- Oriented Programming**: Handle assignments, copying the object contents, Inheritance, Polymorphism, static properties and methods, virtual classes and parameterized classes.
- **Constraint Randomization**: Constraint overriding, distribution and conditional constraints, soft, static and inline constraints. Thread Synchronization Techniques: events, semaphores and Mailbox-built in-methods.
- **Functional Coverage**: Cover groups, bins and cross coverage.
- **System Verilog Assertions:** Types of assertions, assertion blocks, sequences with edge definitions and logical relationship. sequences with different timing relationships. Clock definitions, implication and repetition operators, different sequences compositions, inline and binding assertions, advanced SVA features and assertion coverage.
- **Universal Verification Methodology**: UVM Objects components UVM Factory Overriding methods stimulus Modelling UVM phases UVM Configuration TLM UVM sequence, virtual sequence sequence.

Tools

- Mentor Graphics- Model-sim
- Design Compiler
- Questa-sim
- Synopsis VCS
- Xilinx-ISE, Vivado
- VC SpyGlass

Strengths

Time Management, Self-Motivation, Hardworking, adaptability.

Declaration

I here to declare above information is correct to the best of my knowledge and belief.

Date:

Place: Bengaluru

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