

Total No. of Questions : 6
P88

SEAT No. : _____

[Total No. of Pages : 2]

OCT. -16/B/E/Insem. - 144

B.E. (E & TC)

ELECTRONIC PRODUCT DESIGN

(2012 Pattern) (Semester - I) (Elective - II) (404185B)

Time : 1 Hour

[Max. Marks : 30]

Instructions to the candidates:

- 1) Attempt Q. No.1 or Q. No.2, Q. No.3 or Q. No.4, Q. No.5 or Q. No.6.
- 2) Figures to the right indicates full marks.
- 3) Neat diagrams must be drawn wherever necessary.
- 4) Assume suitable additional data if necessary.
- 5) Use of nonprogrammable calculator is permitted.

Q1) a) What are the aspects in design for manufacturing? [4]

b) Write short notes on any two: [6]

i) Cognitive ergonomics.

ii) Man machine interface.

iii) Types of grounding.

OR

Q2) a) What are five elements in designing of a product? [5]

b) What is importance of packaging? Explain related factors. [5]

Q3) a) How the test plan is formalized? [4]

b) Explain: [6]

i) Functional model verses architectural model.

ii) Specifications verses requirements.

OR

P.T.O.

- Q4)** a) Explain the importance of test cases and test procedure. [4]
b) Write in brief on any two: [6]
- Functional Design.
 - Egoless design.
 - Prototyping.

- Q5)** a) What are good programming practices? [4]
b) Explain the concept of Black, white and grey box tests. [6]

OR

- Q6)** a) What is software testing and debugging? [4]
b) Explain waterfall model of software development. [6]

Total No. of Questions : 6]

P85

SEAT No.:

[Total No. of Pages : 2]

OCT. -16/B.E./Insem. - 140

B.E. (E & Te)

EMBEDDED SYSTEMS & RTOS

(2012 Pattern) (Semester - I) (Elective - I)

Time : 1 Hour]

/Max. Marks : 30

Instructions to the candidates:

- 1) Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.
- 4) Assume suitable data if necessary.

Q1) a) Explain the following design metric power size. [5]

b) Explain the characteristics of Embedded system. [5]

OR

Q2) a) Explain waterfall model with a neat diagram. [5]

b) Explain the various stages involved in design process. [5]

Q3) a) Explain the concept of Foreground / Back ground systems. [5]

b) Define task. Draw and explain task state diagram. [5]

OR

Q4) a) Explain Round Robin scheduling algorithm. [5]

b) What is priority inversion? How does it help to improve the performance [5]
of Embedded system.

P.T.O.

Q3) a) Explain Queue
b) Explain Competition
c) Explain

Q5) a) Explain the features of Mucos II RTOS. [5]

b) Explain any two task related functions. [5]

OR

Q6) a) Explain the following functions related to mailbox [5]

i) OSM box Create ()

ii) OSM box Pend ()

b) What is intertask communication? Explain the following functions [5]

i) OS sem Post ()

ii) OS sem Accept ()

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Total No. of Questions :6]

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SEAT No. : _____

[Total No. of Pages :2

OCT. -16/BE/Insem. - 140

B.E. (E & Te)

**EMBEDDED SYSTEMS & RTOS
(2012 Pattern) (Semester - I) (Elective - I)**

Time : 1 Hour]

[Max. Marks :30

Instructions to the candidates:

- 1) Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q6.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.
- 4) Assume suitable data if necessary.

Q1) a) Explain the following design metric power size. [5]

b) Explain the characteristics of Embedded system. [5]

OR

Q2) a) Explain waterfall model with a neat diagram. [5]

b) Explain the various stages involved in design process. [5]

Q3) a) Explain the concept of Foreground / Back ground systems. [5]

b) Define task. Draw and explain task state diagram. [5]

OR

Q4) a) Explain Round Robin scheduling algorithm. [5]

b) What is priority inversion? How does it help to improve the performance of Embedded system. [5]

P.T.O.

Q3) a) Compa
b) C
c) Exp

Q5) a) Explain the features of Mucos II RTOS. [5]

b) Explain any two task related functions. [5]

OR

Q6) a) Explain the following functions related to mailbox [5]

i) OSM box Create ()

ii) OSM box Pend ()

b) What is intertask communication? Explain the following functions [5]

i) OS sem Post ()

ii) OS sem Accept ()

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Aug 15

Total No. of Questions : 6]

P4875

SEAT No. :

[Total No. of Pages : 2

B.E./Insem. - 38

B.E. (E & T/C)

**VLSI DESIGN & TECHNOLOGY
(2012 Pattern) (Semester - I)**

Time : 1 Hour]

[Max. Marks : 30

Instructions to the candidates:

- 1) Answer Q1 or Q2, Q3 or Q4, Q5 or Q6.
- 2) Figures to the right side indicate full marks.

Q1) a) Explain different architectural modeling types in VHDL. Give brief example of each. [5]

b) Write VHDL code for 4 : 1 MUX & write test bench for it. [5]

OR

Q2) a) Draw FSM diagram & write VHDL code for 100 Moore sequence detector. [5]

b) What is need of function? Explain function call & function body in brief. [5]

Q3) a) Explore the architecture of FPGA in detail. [5]

b) Compare CPLD w.r.t FPGA. [5]

OR

Q4) a) How does logic get implemented in CPLD & FPGA? What is conceptual difference? [5]

b) Explore Place & Rout (PAR) as well as timing verification w.r.t. CPLD/ FPGA. [5]

P.T.O.

Q5) a) List & explain signal integrity issues. [5]

b) What is need of power optimization? Explain any one method. [5]

OR

Q6) a) What is clock jitter? How to eliminate? [5]

b) Explore interconnect routing techniques. [5]

Total No. of Questions : 6]

P81

SEAT No. :

[Total No. of Pages : 1]

OCT.-16/BE/Insem. - 136

B.E. (E & TC)

**VLSI DESIGN & TECHNOLOGY
(2012 Course)**

Time : 1 Hour

/Max. Marks : 30

Instructions to the candidates:

- 1) Solve Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6.
- 2) Figures to the right side indicate full marks.

Q1) a) What is meant by synthesizable & non-synthesizable statement? Give two examples of each. [5]

b) Write VHDL code for half adder by structural & behavioural modeling. [5]

OR

Q2) a) List & explain different delays involved in chip design. [5]

b) Explain data objects with suitable examples. [5]

Q3) a) Compare PROM, PLA, PAL & CPLD. [5]

b) Explore CPLD/FPGA oriented design flow. [5]

OR

Q4) a) Draw CPLD architecture in detail. Explain in brief. [5]

b) Give typical features & specifications of FPGA. [5]

Q5) a) What is clock skew? What are techniques to minimize? [5]

b) Why should supply & ground bounce be taken care? How are these minimized? [5]

OR

Q6) a) Explore different wire parasitics. [5]

b) With the help of suitable diagram, explain I/O architecture in brief. [5]



Total No. of Questions : 6]
P4947

SEAT No. :

[Total No. of Pages : 2

BE/In Sem. - 42
B.E. (E & TC)
EMBEDDED SYSTEMS & RTOS
(2012 Course) (Semester -I) (Elective - I)

Time : 1 Hour]

/Max. Marks : 30

Instructions to the candidates:

- 1) Answer Q1 or Q2, Q3 or Q4, Q5 or Q6.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.
- 4) Assume suitable data, if necessary.

- Q1) a)** Explain the following design metric. Time to market, Unit cost. [5]
b) Explain Embedded processor technology. [5]

OR

- Q2) a)** Explain V-shape model. [5]
b) Explain the following design metric NRE cost, size. [5]

- Q3) a)** Explain the following. [5]
i) Non Preemptive kernel
ii) Preemptive kernel
b) Explain Mutual Exclusion. [5]

OR

- Q4) a)** What is Deadlock? When it occurs? [5]
b) What is multitasking? Explain the advantages of multitasking. [5]

PTO.

Total No. of Questions : 6]
P4947

SEAT No. :

[Total No. of Pages : 2

BE/In Sem. - 42

B.E. (E & TC)

EMBEDDED SYSTEMS & RTOS
(2012 Course) (Semester -I) (Elective - I)

Time : 1 Hour]

Instructions to the candidates:

/Max. Marks : 30

- 1) Answer Q1 or Q2, Q3 or Q4, Q5 or Q6.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.
- 4) Assume suitable data, if necessary.

- Q1)** a) Explain the following design metric. Time to market, Unit cost. [5]
b) Explain Embedded processor technology. [5]

OR

- Q2)** a) Explain V-shape model. [5]
b) Explain the following design metric NRE cost, size. [5]

- Q3)** a) Explain the following. [5]
i) Non Preemptive kernel
ii) Preemptive kernel
b) Explain Mutual Exclusion. [5]

OR

- Q4)** a) What is Deadlock? When it occurs? [5]
b) What is multitasking? Explain the advantages of multitasking. [5]

PTO.

- (Q3) a) Co
b) Exp
c) Ci*
- Q5)** a) Explain any two task related functions. [5]
b) Explain the following time related functions. [5]
i) OSTime Dly ()
ii) OSTime Dly HMSM ()
- OR
- Q6)** a) What is semaphore? How does it help in resource sharing in RTOS kernel. [5]
b) Explain the following functions related to message Q. [5]
i) OSQ Create ()
ii) OSQ Pend ()



Total No. of Questions : 6]

P81

SEAT No. :

[Total No. of Pages : 1]

OCT.-16/BE/Insem.-136

B.E. (E & TC)

VLSI DESIGN & TECHNOLOGY

(2012 Course)

Time : 1 Hour

[Max. Marks : 30]

Instructions to the candidates:

- 1) Solve Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6.
- 2) Figures to the right side indicate full marks.

- Q1)** a) What is meant by synthesizable & non-synthesizable statement? Give two examples of each. [5]
b) Write VHDL code for half adder by structural & behavioural modeling. [5]

OR

- Q2)** a) List & explain different delays involved in chip design. [5]
b) Explain data objects with suitable examples. [5]

- Q3)** a) Compare PROM, PLA, PAL & CPLD. [5]
b) Explore CPLD/FPGA oriented design flow. [5]

OR

- Q4)** a) Draw CPLD architecture in detail. Explain in brief. [5]
b) Give typical features & specifications of FPGA. [5]

- Q5)** a) What is clock skew? What are techniques to minimize? [5]
b) Why should supply & ground bounce be taken care? How are these minimized? [5]

OR

- Q6)** a) Explore different wire parasitics. [5]
b) With the help of suitable diagram, explain I/O architecture in brief. [5]

Total No. of Questions :8
P1863

SEAT No. :
[Total No. of Pages :2

[4859]-1044

B.E. (E & TC)

b-ELECTRONIC PRODUCT DESIGN
(2012 Pattern) (Elective - II) (End - Sem) (Semester - I) (404185)

Time :2½ Hours]

/Max. Marks :70

Instructions to the candidates:

- 1) Attempt Q. No. 1 or Q. No. 2, Q.No. 3 or Q.No. 4, Q.No. 5 or Q.No. 6, Q.No. 7 or Q.No. 8.
- 2) Figures to the right side indicate full marks.
- 3) Neat diagrams must be drawn wherever necessary.
- 4) Assume suitable additional data if necessary.
- 5) Use of nonprogrammable calculator is permitted.

- Q1)** a) Explain successful design elements in Electronic Product design. [7]
b) How to formulate specifications? Explain difference between specifications and requirements with suitable example. [6]
c) State different software models. Explain waterfall model of software development with suitable diagram. [7]

OR

- Q2)** a) Explain the concept of design for manufacturing in electronic product Design. [7]
b) Draw a flow chart of formulation of test plan and explain. Explain how test plan is formulated. [6]
c) What is real time software? Explain its significance in product design with example. [7]

- Q3)** a) Explain configurations of routing topologies in PCB layout Designing. [7]
b) Explain importance of grounding methodologies. compare those Technologies. [7]
c) Write short notes on:
i) Image planes.
ii) Functional partitioning. [4]

OR

- Q4)** a) Write short notes on: [10]
i) Bypassing and decoupling capacitors.
ii) Impedance matching.
- b) Explain design techniques for ESD protection. [4]
- c) What are the design techniques used to prevent crosstalk. [4]
- Q5)** a) Write short notes on (any two): [8]
i) Active components
ii) Passive components
iii) Electromechanical Components
- b) What are the steps of debugging? [8]

OR

- Q6)** a) Compare different types ADCs with respect to parameters: Resolution, conversion time, power dissipation, errors. [8]
- b) Explain validation and verification in manufacturing of electronic product with suitable flow chart. [8]
- Q7)** a) What are the methods of documentation? [8]
- b) Explain the need of documentation? [8]

OR

- Q8)** a) What is bill of material? Explain with example. [8]
- b) Explain visual techniques of documentation. [8]

EEE

Q4) a) Write short notes on: [10]

- i) Bypassing and decoupling capacitors.
- ii) Impedance matching.

b) Explain design techniques for ESD protection. [4]

c) What are the design techniques used to prevent crosstalk. [4]

Q5) a) Write short notes on (any two): [8]

- i) Active components
- ii) Passive components
- iii) Electromechanical Components

b) What are the steps of debugging? [8]

OR

Q6) a) Compare different types ADCs with respect to parameters: Resolution, conversion time, power dissipation, errors. [8]

b) Explain validation and verification in manufacturing of electronic product with suitable flow chart. [8]

Q7) a) What are the methods of documentation? [8]

b) Explain the need of documentation? [8]

OR

Q8) a) What is bill of material? Explain with example. [8]

b) Explain visual techniques of documentation. [8]

EEE

Nov 15

Total No. of Questions : 8]

SEAT No. :

P3654

[Total No. of Pages : 2

[4859]-1037

B.E. (E & TC)

**COMPUTER NETWORKS
(2012 Pattern) (Semester - I)**

Time : 2½ Hours]

/Max. Marks : 70

Instructions to the candidates:

- 1) Answer Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right side indicate full marks.
- 4) Assume suitable data if necessary.

- Q1)** a) Draw OSI reference model and explain functions of data link layer and presentation layer. [7]
b) A channel has data rate of 4kbps and propagation delay of 20ms. Calculate the frame size if the channel efficiency is 50%. [7]
c) What is backbone network? What are its types? Explain with necessary diagrams. [6]

OR

- Q2)** a) Draw TCP/IP protocol suite. List with example addresses present at every layer. [7]
b) Explain flow control in datalink layer. [7]
c) Explain Basic service set and Extended service set in WLAN. [6]

- Q3)** a) Compare IPv4 and IPv6. [6]
b) List the various protocols giving their significance at network layer. [6]
c) Explain the various classes of IP addressing with their respective ranges. Also list the range of private IP addresses and the standard mask for first three classes of IP addresses. [6]

OR

P.T.O.

- Q4)** a) Draw and explain IPv4 frame format. [6]
b) Write short note on DHCP. [6]
c) Give the classification of commonly used Unicast Routing protocols and explain Distance Vector Routing protocol with an appropriate example. [6]

- Q5)** a) Draw the TCP frame format. Explain the use of flags. [6]
b) Explain the reliability, delay, jitter and bandwidth requirements for the internet applications E-mail and video conferencing. [6]
c) Explain in brief port numbers and socket address. [4]

OR

- Q6)** a) Explain 3 way/step handshaking for connection establishment and 4 step connection termination. [6]
b) Explain the features of Stream Control Transmission Protocol (SCTP). [6]
c) Draw and explain UDP frame format. [4]

- Q7)** a) What are the main responsibilities of Application Layer? Explain in brief. [6]
b) Explain DNS in Internet. [6]
c) Explain the RSA algorithm. Also explain its limitations. [4]

OR

- Q8)** a) Compare symmetric and asymmetric cipher. [6]
b) Write short note on electronic mail system. [6]
c) Explain the Substitution cipher with its advantages and disadvantages. [4]



Total No. of Questions : 10]

P2019SEAT No. :

[Total No. of Pages : 2]

[5059] - 622

B.E. (E & T/C)
COMPUTER NETWORKS
(2012 Pattern) (Semester - I)

Time : $2\frac{1}{2}$ Hours]

/Max. Marks : 70

Instructions to the candidates:

- 1) Answer Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8, Q9 or Q10.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Use of calculator is allowed.
- 4) Assume suitable data, if necessary.
- 5) Figures to the right indicate full marks.

- Q1)** a) Classify different transmission media. Give advantages and disadvantages of fiber cable? [6]
 b) Explain communication in Datagram Network? [4]

OR

- Q2)** a) State and explain stop and wait ARQ protocol? [6]
 b) Write a short note on Gigabit Ethernet? [4]

- Q3)** a) Explain and correlate any four connecting devices with OSI reference model? [4]
 b) Explain flow control in data link layer? [6]

OR

- Q4)** a) Compare Bluetooth with Zigbee? [4]
 b) What characteristics can be used to group stations in VLAN? [6]

- Q5)** a) Explain IPv6 protocol? [5]
 b) Explain unicast and multicast routing? Give one application of multicasting. [6]
 c) Explain remote and mobile host communication in mobile IP? [6]

OR

P.T.O.

- Q6)** a) What is ICMPv4? Explain general format of ICMPv4 messages? [5]
b) Explain different performance parameters of Network layer? [6]
c) Explain different network layer services? [6]

- Q7)** a) Explain various transport layer protocols? [7]
b) List the services provided to upper layers by transport layer. Explain any one in detail. [6]
c) Explain what is socket? [4]

OR

- Q8)** a) Explain port numbers and socket addresses? [7]
b) Explain the features of SCTP? [4]
c) Explain connection establishment and connection termination with respect to the transport layer? [6]

- Q9)** a) Compare symmetric key cryptography with asymmetric key cryptography. Explain RSA algorithm. [8]
b) Write a short note on:
i) WWW
ii) HTTP

OR

- Q10)** a) Explain FTP and TELNET in detail with respect to Server and Client communication? [8]
b) How does electronic mail system work? What is the role of SMTP and POP-3 server in E-mail system? [8]

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May 17

Total No. of Questions : 10]

P3044

SEAT NO. :

[Total No. of Pages : 2

[5154]-612

B.E.(E & TC)

COMPUTER NETWORKS

(2012 Course) (Semester - I) (End Sem.) (404182)

Time : 2½ Hours]

/Max. Marks : 70

Instructions to the candidates:

- 1) Answer the questions-Q(1) or Q(2), Q(3) or Q(4), Q(5) or Q(6), Q(7) or Q(8), Q(9) or Q(10).
- 2) Figures to the right side indicate full marks.
- 3) Neat diagrams must be drawn wherever necessary.
- 4) Use of Electronic calculator is allowed.
- 5) Assume Suitable data, if necessary.

- Q1)** a) Draw & explain Star topology with advantages & disadvantages. [4]
b) Explain function of physical layer with OSI diagram. [6]

OR

- Q2)** a) Explain coaxial cable with characteristics, application, advantages & disadvantages. [6]
b) Explain with suitable example different address used in TCP/IP suit? [4]

- Q3)** a) Explain stop & wait ARQ? [5]
b) Draw & explain transition state diagram used in PPP protocol. [5]

OR

- Q4)** a) Prove that throughput of slotted ALOHA is around 37%. [4]
b) Explain different transmission medium defined for IEEE 802.3? [6]

- Q5)** a) Explain classful Addressing? [6]
b) Explain encapsulation of ARP packet? [4]
c) Explain Bootstrap Protocol? [7]

OR

PTO.

- Q6)** a) Draw and explain function of each field of DHCP message format? [9]
b) Explain design goal often used in Routing algorithm? [8]

- Q7)** a) Draw & explain state diagram for simple connection management scheme at Transport Layer. [7]
b) Explain four ways of releasing using three way handshake in TCP protocol? [10]

OR

- Q8)** a) Explain different services provided by transport layer? [6]
b) Explain real time transport protocol? [5]
c) Which are parameters for the service primitives and library procedures? [6]

- Q9)** a) List basic security requirement for high security in line encryptor. [6]
b) Write a short note on World Wide Web? [5]
c) Write components of DNA? [5]

OR

- Q10)** a) State & explain Post office Protocol? [6]
b) State advantages & disadvantages of HTML? [5]
c) State & explain Security attacks? [5]

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Total No. of Questions : 8]

SEAT No. :

P3603

[Total No. of Pages : 2

[4959] - 1081
BE (E & TC)
VLSI Design & Technology (End - Sem)
(2012 Pattern)

Time : 2½ Hours

[Max. Marks : 70]

Instructions to the candidates:-

- 1) Neat diagrams must be drawn wherever necessary.
- 2) Use of electronic pocket calculator is allowed.
- 3) Assume suitable data, if necessary.
- 4) Answer any one questions out of Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.

- Q1)** a) What is meant by concurrent & sequential statements in VHDL? Explore in detail with two examples of each. [7]
b) With the help of suitable schematics, compare PROM, PLA & PAL architectures. What is need of CPLD? [7]
c) What is clock skew? Explain the solutions to it. [6]

OR

- Q2)** a) Write VHDL code for Mod - N counter. Write suitable test bench for it. [7]
b) Explain PLD targeted design flow in detail. [7]
c) What is supply & ground bounce? What are remedies to it? [6]

- Q3)** a) Draw ac equivalent ckt of MOSFET & explain various capacitances involved. [9]
b) What is technology scaling? What are types? Explain each in detail. [9]

OR

- Q4)** a) With the help of mathematical analysis & suitable schematic, explain DC transfer characteristics of CMOS Inverter. [9]
b) What are merits of transmission gate? Design 4 : 1 mux using transmission gates. [9]

- (Q5) a) Draw the ckt diagram for push pull CMOS inverter as an amplifier & explain. Give the expressions for output voltage range, output resistance & bandwidth. [8]*
- b) With the help of suitable schematic, explain cascode amplifier. What are its merits? Give the expressions for voltage gain and output resistance. [8]*
- OR
- (Q6) a) Explain current mirror in detail. Why is it needed? [8]*
- b) Explain current sink & current source in detail. Give expressions for output voltage range & output resistance. [8]*
- (Q7) a) What are the types of fault? Explain each in brief. [8]*
- b) What is need of BIST? Explain typical BIST in detail. [8]*
- OR
- (Q8) a) With the help of block diagram, explain TAP controller in detail. [8]*
- b) Explain boundary scan technique. [8]*



Nov 15

Total No. of Questions : 8]

P3653

SEAT No. :

[Total No. of Pages : 2

[4859]-1036

B.E. (E & T/C)

VLSI DESIGN & TECHNOLOGY

(2012 Pattern) (Semester - I)

Time : 2½ Hours]

/Max. Marks : 70

Instructions to the candidates:

- 1) Answer any one question out of Q.No. 1 or 2, Q.No. 3 or 4, Q.No. 5 or 6, Q.No. 7 or 8.
- 2) Neat diagrams should be drawn wherever necessary.
- 3) Use of electronic pocket calculator is allowed.
- 4) Assume suitable data, if necessary.

- Q1)** a) Write VHDL code for 8 bit serial in serial out shift register by structural & behavioural modeling methods. [7]
b) What is need of FPGA? List typical specifications of FPGA. [7]
c) Explain I/O architecture in detail. [6]
- OR
- Q2)** a) What are flip flop timings? What is meta-stability? What are solutions? [7]
b) Explore the architecture of CPLD in detail. [7]
c) What are different wire parasitics? How do they play important role in routing? [6]
- Q3)** a) Derive the expressions for power dissipations in CMOS. What are the techniques to minimize the dissipations? [9]
b) Design CMOS logic for $Y = AB + CDEFG + H$. Compute area on chip. [9]
- OR
- Q4)** a) What is power delay product? Derive the expression for it. What is its significance? [9]
b) Explain linear delay model in detail. [9]

P.T.O.

- Q5)** a) Compare push-pull, current source & active load inverters with respect to voltage gain, voltage range, output resistance & bandwidth in detail. [8]
b) Draw the schematic of CMOS differential amplifier and give the expressions for voltage gain, output resistance, CMRR & ICMR. [8]

OR

- Q6)** a) Draw common drain amplifier. Compare with common source & common gate amplifiers with respect to gain, output resistance & bandwidth. [8]
b) Draw & explain CMOS operational amplifier. Give the expressions for voltage gain & output resistance. [8]

- Q7)** a) What is need of DFT? Explain with suitable example. [8]
b) Explain fault models in detail. [8]

OR

- Q8)** a) With the interface ports involved, explain JTAG in detail. [8]
b) What is partial & full scan path? [8]



Total No. of Questions : 08]

SEAT No. :

P2018

[Total No. of Pages : 2

[5059] - 621

B.E. (E & TC)

VLSI DESIGN & TECHNOLOGY
(2012 Pattern) (Semester - I)

Time : $2\frac{1}{2}$ Hours]

[Max. Marks : 70]

Instructions to the candidates:

- 1) Answer Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8.
- 2) Neat diagrams should be drawn wherever necessary.
- 3) Use of electronic pocket calculator is allowed.
- 4) Assume suitable data, if necessary.

Q1) a) State the difference between [6]

- i) Signal and variable
- ii) Functions and procedures

[8]

b) Draw and explain the following for FPGA

- i) Logic cell
- ii) CLB
- iii) Programmable switch matrix
- iv) I/O block

c) What is the need of clock distribution? Explain techniques of clock [6]
distribution.

OR

Q2) a) Write VHDL code and test bench for D FLIP FLOP using function for [8]
clock event.

b) Explain with diagram SRAM and anti-fuse programming techniques [6]
used in FPGA?

c) What is floor planning? Explain in detail. [6]

Q3) a) Draw and explain CMOS transfer characteristics in detail showing all regions in the characteristics. [8]

b) Design CMOS logic for $Y = \overline{AB+CD+E}$. Calculate W/L ratio for N_{MOS} and P_{MOS} area needed on chip. [10]

OR

Q4) a) Explain transmission gate. States its advantages. Implement a circuit of 2:1 multiplexer using transmission gate. Comment on the number of transistor required using transmission gates and conventional method. [10]

b) Explain the following. [8]

- Velocity saturation
- Body effect
- Hot electron effect
- Channel length modulation

Q5) a) Explain common source amplifier with the help of circuit diagram. Draw AC equivalent circuit and expression for voltage gain, output resistance. [8]

b) Explain device parasitic and their limitation on the performance of CMOS circuits. [8]

OR

Q6) a) Draw and explain difference amplifier using MOS transistors. [8]

b) Draw and explain current sink and source circuits. [8]

Q7) a) Explain the need of design for testability. Explain scan path testing. [8]

b) Explain stuck-at-0 and stuck-at-1 faults with example. [8]

OR

Q8) Write short note on.

- TAP controller with state diagram. [16]
- Built In Self Test (BIST)



MAY 17

Total No. of Questions : 8]

SEAT No : _____

[Total No. of Pages : 2]

P 3043

[5154]-611

B.E.(Electronics & Telecommunication)
VLSI DESIGN & TECHNOLOGY
(2012 Pattern) (End Semester) (404181)

[Max. Marks : 70]

Time : 2½ Hours

Instructions to the candidates:

- 1) Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Assume suitable data, if necessary.

Q1) a) Explain the following: [10]

- | | |
|---------------|---------------|
| i) Constants | ii) Variables |
| iii) Signals | iv) Functions |
| v) Procedures | |

b) Write VHDL code for half adder by structural and behavioral modelling technique. [10]

OR

Q2) a) Describe the PLD design flow. [10]

b) Write the VHDL programming for D flip-flop and its test bench. [10]

Q3) a) Derive the static and dynamic power dissipations in CMOS. [7]

b) Explain the following terms. [4]

- | | |
|-----------------|----------------|
| i) Clock jitter | ii) Clock skew |
|-----------------|----------------|

c) Draw and explain CMOS transfer characteristics. [7]

OR

Q4) a) Define Scaling and explain any one type of scaling. [6]

b) Explain the following: [4]

- | | |
|------------------------------|-----------------|
| i) Channel Length Modulation | ii) Body effect |
|------------------------------|-----------------|

c) Explain the working of a transmission gate and Implement a circuit of 2:1 multiplexer using transmission gate. [8]

P.T.O.

- Q5) a) Draw and explain active load inverter in detail. [8]*
- b) Explain current sink and current source and their characterization with their areas of improvement. [8]*

OR

- Q6) a) Draw and explain CMOS operational amplifier with voltage gain and output resistance. [8]*
- b) Draw the schematic of CMOS differential amplifier and give the expressions for output resistance, CMRR & ICMR. [8]*

- Q7) a) Explain the fault models with examples. [8]*
- b) Explain the need of DFT with suitable example. [8]*

OR

- Q8) a) Draw the TAP controller state diagram and explain. [10]*
- b) Explain the following terms: [6]*
- i) Partial scan
 - ii) Full scan
 - iii) JTAG
- + + +

Total No. of Questions : 8)

SEAT No. :

P2024

[Total No. of Pages : 3]

[5059] - 629

**B.E. (Electronics and Telecommunication Engineering)
(Elective - II(B))**

**ELECTRONIC PRODUCT DESIGN
(2012 Pattern)**

Time : 2.30 Hours/

/Max. Marks : 70

Instructions to the candidates:

- 1) Answer Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.
- 4) Use of logarithmic tables, slide rule, Mollier charts, electronic pocket calculator and steam tables is allowed.
- 5) Assume suitable data, if necessary.

- Q1)** a) Explain different types of Energy coupling mechanisms in brief. [8]
 b) Explain how mapping of functions to hardware is done in architectural design. [6]
 b) List and explain different commonly identifiable limitations of software. [6]

OR

- Q2)** a) Explain filtering actions by frequency selective filters, common mode filters and amplitude selective filters. [7]
 b) Explain the concept of coupling and cohesion with respect to partitioning of a system. [6]
 c) Discuss about the development plan of risk abatement in software development. [7]

- Q3)** a) Explain with neat diagrams, the different considerations for effective image planes. [8]
 b) Explain the need of functional partitioning on PCB. Also explain how it is effectively done? [8]

P.T.O

OR

Q4) Define/Explain the following terms associated with PCB design.

[16]

- a) Containment
- b) Electromagnetic interference (EMI)
- c) Electromagnetic compatibility (EMC)
- d) Immunity
- e) Susceptibility
- f) Suppression
- g) Electrostatic discharge (ESD)
- h) Transmission modes of RF energy

Q5) a) With the help of suitable examples explain how the equipment are important for effective troubleshooting and debugging. [8]

b) Discuss tips for troubleshooting of analog circuits and digital circuits. Also discuss the check list for powering circuits during troubleshooting and debugging. [8]

OR

Q6) a) With respect to debugging process, explain the different ways of characterization of component or problem. [8]

b) Explain how simulation, prototyping and parametric testing support the engineering development, system integration and training. [8]

Q7) a) List types of documents, their specific subtypes. Also explain their specific use and format. [12]

b) Discuss about records, accountability and liability with respect to documentation. [6]

b) Write short notes on following documents.

i) Cognitive

ii) Man machine interface

iii) Types of grounding

OR

Q8) a) Explain role of audience in documentation. [8]

b) Write short notes on following documents.

i) Engineering notebook. [5]

ii) Drawing and schematic. [5]



Q3) a) How
b) Explain:
c) Function
d) Specification

May 17

Total No. of Questions : 8]

SEAT No. : _____

P3050

[Total No. of Pages : 2]

[5154]-619

B.E. (Electronics & Telecommunication)

ELECTRONIC PRODUCT DESIGN

(2012 Pattern) (End Sem) (Elective - II) (Semester - I)

Time : 2½ Hours]

[Max. Marks : 70]

Instructions to the candidates:

- 1) Attempt Q.No.1 or Q.No.2, Q.No.3 or Q.No.4, Q.No.5 or Q.No.6, Q.No.7 or Q.No.8.
- 2) Figures to the right indicates full marks.
- 3) Neat diagrams must be drawn wherever necessary.
- 4) Assume suitable additional data if necessary.
- 5) Use of non programmable calculator is permitted.

- Q1)** a) Explain man machine dialogue. [8]
b) What are the issues while formulating a test plan? [8]
c) What are the metrics in software designing? [4]

OR

- Q2)** a) What is shielding? Explain with neat diagrams. [8]
b) What are the performance and efficiency measures in hardware testing? [6]
c) Explain different software models with advantages and disadvantages. [6]

- Q3)** a) What is bypassing and decoupling issue in PCB? Explain with suitable example. [6]
b) What are the grounding methodologies? Explain with suitable sketches. [6]
c) Write in brief about routing topologies. [6]

OR

- Q4)** a) What is functional partitioning? Explain critical frequency concept. [8]
b) What are the techniques used in ESD protection. [6]
c) Calculate the characteristic impedance for a stripline geometry when the thickness of PCB laminates is 1.6mm and its relative permittivity is 3.2. The width of embedded track is 1mm and its thickness is 35 microns. [4]

P.T.O.

- Q5)** a) What is role of A to D converter in product design? Explain the parameters while designing A to D converter. [6]
b) What is integration, verification and validation in electronic product designing? [6]
c) What is an operational amplifier explain with typical application. [4]

OR

- Q6)** a) What is testing and debugging? Explain the steps in debugging. [8]
b) What are electromechanical components? Explain any two electromechanical components. [8]

- Q7)** a) Define documentation and explain different types of documentation. [6]
b) What is accountability and liability? [6]
c) Write in brief on presentation and preservation of documents. [4]

OR

- Q8)** a) What is the importance of bill of material? Explain bill of material with suitable example. [8]
b) Explain the layout of documentation. [8]

[4959] - 1085
B.E. (E&TC) (Semester - I)
Embedded Systems & Rtos
(2012 Course) (Elective - I)

[Max. Marks : 70]

Time : 3 Hours]

Instructions to the candidates:-

- 1) Neat diagrams must be drawn wherever necessary.
- 2) Figures to the right indicate full marks.
- 3) Assume suitable data, if necessary.

Q1) a) Explain the following design metrics :

- i) Power
- ii) Size

b) With the help of block diagram, explain the architecture of embedded system.

[4]

OR

Q2) a) Explain the spiral model.

[6]

b) Explain the Foreground | Back ground systems with reference to RTOS [4]

Q3) a) Explain any two scheduling algorithms.

[6]

b) Explain the context switching.

[4]

OR

Q4) a) Write a program in embedded C to implement mail box.

[7]

b) Explain any two task related functions.

[3]

Q5) a) Explain the embedded Linux development environment with a block diagram.

[8]

b) Explain the memory storage considerations for embedded Linux system. [8]

OR

- Q6)* a) Explain the steps to execute any C program on embedded system development board. (ARM 9). [8]
[8]
- b) Explain the Binary utilities.

- Q7)* a) Explain various file systems used in Embedded Linux. [8]
[8]
- b) Explain the device driver concept used in embedded Linux.

OR

- Q8)* a) What is universal boot loader? Explain. [8]
[8]
- b) What are boot loader challenges?

- Q9)* a) Explain the embedded software development tools. [8]
[8]
- b) Explain mobile phone with suitable block diagram and state its software requirements. [10]

OR

- Q10)* a) Explain the issues in hardware - software design. [8]
[8]
- b) Explain the different lab tools required for embedded system design. [10]



P3238

[4859] - 1040

B.E. (ESTC)

EMBEDDED SYSTEM & RTOS
(2012 Pattern) (Elective - I)

[Max. Marks : 70]

Time : 3 Hours]

Instructions to the candidates :

- 1) Neat diagrams must be drawn wherever necessary.
- 2) Figures to the right indicate full marks.
- 3) Assume suitable data, if necessary.

Q1) a) Explain the characteristics of embedded system. [5]

b) Explain the waterfall model.

OR

Q2) a) Write a program in embedded C to implement scheduler. [7]

b) Explain the different states of task. [3]

Q3) a) Explain the classification of embedded system. [3]

b) Write a program in embedded C to implement semaphore. [7]

OR

Q4) a) Write a program in embedded C to implement mailbox. [7]

b) Compare MUCOS RTOS with LINUX RTOS. [3]

Q5) a) Explain the importance of embedded Linux in the development of embedded system. [8]

b) Explain the memory storage considerations for embedded Linux system. [8]

OR

P.T.O.

Q6) a) Explain the cross development environment used for embedded Linux. [8]

b) Explain in detail the steps to execute any C program on embedded system development board (ARM 9) [8]

Q7) a) Explain the Linux kernel configuration steps. [8]
b) Explain module utilities used in embedded linux. [8]

OR

Q8) a) Explain the steps to configure U-Boot. [8]

b) Explain the following file system in linux. [8]

iii) ext4

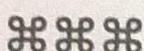
Q9) a) Explain the embedded software development tools. [8]

b) Explain Automatic chocolate vending machine with suitable block diagram and state its hardware requirements. [10]

OR

Q10) a) Explain the porting issues of operating system (os) in an embedded platform. [8]

b) Explain the lab tools required for embedded system design. [19]



Total No. of Questions : 10]

SEAT No. : _____

P2022

[Total No. of Pages : 2

[5059] - 625

B.E. (E&TC)

EMBEDDED SYSTEM AND RTOS

(2012 Pattern) (Semester - II)

Time : 2½ Hours]

[Max. Marks : 70

Instructions to the candidates:

- 1) Answer any one Question out of Q. No. 1 or 2, Q. No. 3 or 4, Q. No. 5 or 6, Q. No. 7 or 8, Q. No. 9 or 10.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right side indicate full marks.
- 4) Use of logarithmic tables, slide molles charts, electronic pocket calculator and steam tables is allowed.
- 5) Assume suitable data, if necessary.

- Q1)* a) Design the medium scale embedded system. [6]
b) With example explain how design metrics are depend on each other [4]

OR

- Q2)* a) Compare foreground/Background system with RTOS. [5]
b) What is difference between Spiral and V model? [5]

- Q3)* a) What is the need of semaphore? How do you create counting semaphore? [4]
b) Write algorithm/ program for reading ADC data using Q services of RTOS. [6]

OR

- Q4)* a) Why mutual exclusion is necessary while using shared resources ? [4]
b) Write algorithm / program to use semaphore for shared resources. [6]

P.T.O

- Q5)** a) Compare Bootloader and BIOS. [6]
b) What are storage consideration in case of embedded linux? [5]
c) What are the features of embedded linux? [5]

OR

- Q6)** a) Explain cross development tools for Embedded linux target. [4]
b) What does the root file system contain? [2]
c) Compare NOR and NAND flash memories for embedded linux [4]
environment.
d) What are processor and memory requirement of embedded linux. [6]

- Q7)** a) Explain Linux kernel configuration steps. [6]
b) Explain different file system used in linux. [5]
c) Explain features of Universal bootloaders. [5]

OR

- Q8)** a) Draw and explain linux kernel architecture. [5]
b) What are the bootloader challenges. [5]
c) What is device driver ? What is use of device driver in embedded linux
system? Explain different types of device driver used in embedded
system. [6]

- Q9)** a) Explain software and hardware codesign in embedded system. [4]
b) Compare simple IDE with sophisticated IDE. [4]
c) Explain mobile phone as embedded system with software and hardware
requirements. [10]

OR

- Q10)a)** Explain software development tools for embedded system. [8]
b) What are hardware and software requirement of Automatic chocolate
vending machine ?
c) What are the features of IDE? [6]
[4]



May 17

Total No. of Questions : 10]

SEAT No. _____
(Total No. of Pages : 2)

P3047

[5154]-615

B.E. (Electronics & Telecommunication)
EMBEDDED SYSTEM & RTOS
(2012 Course) (Semester - I) (Elective - I)

(Max. Marks : 70)

Time : 2½ Hours]

Instructions to the candidates:

- 1) Answer Q.No.1 or Q.No.2, Q.No.3 or Q.No.4, Q.No.5 or Q.No.6, Q.No.7 or Q.No.8, Q.No.9 or Q.No.10.
- 2) Figures to the right indicate full marks.
- 3) Neat diagram must be drawn wherever necessary.
- 4) Use of non programmable electronics pocket calculator is allowed.
- 5) Assume suitable data, if necessary.

- Q1)** a) Explain features of embedded system and classify them with example [5]
b) Explain various processor technologies in design of embedded processors. [5]

OR

- Q2)** a) Explain difference between V model and Water fall model of software design. [5]
b) Explain design metrics with respect to camera as embedded system. [5]

- Q3)** a) Explain kernel architecture & configuration for RTOS. [5]
b) Explain the importance of clock tick in function RTOS. Explain the time management functions in μ C/OS-II. [5]

OR

- Q4)** a) What do you mean by task communication & explain various IPC techniques. [5]
b) Explain OSMailboxCreate() and OSMailboxPost() function. [5]

P.T.O.

- Q5)* a) Compare BIOS with boot loader in embedded system. [8]
b) Explain tracing & profiling tools. [8]

OR

- Q6)* a) List and explain various file systems used in Embedded Linux. [8]
b) What is binary utilities? Discuss miscellaneous binary utilities. [8]

- Q7)* a) Define software testing. Explain various level of testing. [8]
b) Explain concept of loadable device driver for Linux kernel. [8]

OR

- Q8)* a) Draw and explain Linux kernel architecture. [8]
b) Discuss different Linux file systems. [8]

- Q9)* a) Explain the use of ICE for testing embedded system with diagram. [9]
b) Explain mobile phone with its hardware & software requirements. [9]

OR

- Q10)a)* Explain embedded system hardware & software requirements in automatic chocolate vending machine. [9]
b) Explain GNU debugger. What is hardware assisted debugging? [9]

Q3) a) How
b) Explain
c) Function
d) Specification

MDVIS

Total No. of Questions : 8]

SEAT No. :
[Total No. of Pages : 2]

P1863

[4859]-1044

B.E. (E & TC)

b-ELECTRONIC PRODUCT DESIGN

(2012 Pattern) (Elective - II) (End - Sem) (Semester - I) (404185)

/Max. Marks : 70

Time : 2½ Hours

Instructions to the candidates:

- 1) Attempt Q. No. 1 or Q. No. 2, Q.No. 3 or Q.No. 4, Q.No. 5 or Q.No. 6, Q.No. 7 or Q.No. 8.
- 2) Figures to the right side indicate full marks.
- 3) Neat diagrams must be drawn wherever necessary.
- 4) Assume suitable additional data if necessary.
- 5) Use of nonprogrammable calculator is permitted.

- Q1)** a) Explain successful design elements in Electronic Product design. [7]
b) How to formulate specifications? Explain difference between specifications and requirements with suitable example. [6]
c) State different software models. Explain waterfall model of software development with suitable diagram. [7]

OR

- Q2)** a) Explain the concept of design for manufacturing in electronic product Design. [7]
b) Draw a flow chart of formulation of test plan and explain. Explain how test plan is formulated. [6]
c) What is real time software? Explain its significance in product design with example. [7]

- Q3)** a) Explain configurations of routing topologies in PCB layout Designing. [7]
b) Explain importance of grounding methodologies. compare those Technologies. [7]
c) Write short notes on:
i) Image planes.
ii) Functional partitioning. [4]

OR

P.T.O.

- (Q4)* a) Write short notes on: [16]
i) Bypassing and decoupling capacitors.
ii) Impedance matching.
b) Explain design techniques for ESD protection. [4]
c) What are the design techniques used to prevent crosstalk. [4]
- (Q5)* a) Write short notes on (any two): [8]
i) Active components
ii) Passive components
iii) Electromechanical Components
b) What are the steps of debugging? [8]

OR

- (Q6)* a) Compare different types ADCs with respect to parameters: Resolution, conversion time, power dissipation, errors. [8]
b) Explain validation and verification in manufacturing of electronic product with suitable flow chart. [8]
- (Q7)* a) What are the methods of documentation? [8]
b) Explain the need of documentation? [8]

OR

- (Q8)* a) What is bill of material? Explain with example. [8]
b) Explain visual techniques of documentation. [8]

EEE

- Q1) a) i) Man-Machine dialogue
 ii) Types of design
 iii) Minimizing cost
 b) What are five elements of successful design?
 c) What is importance of product specification?
 d) How the test plan is formalized?
 e) Explain:
 i) Functional model versus architectural model
 ii) Specifications versus requirements
 OR

Aug 15

Total No. of Questions : 6]

P4994

SEAT No. :
 [Total No. of Pages : 2]

BE/In Sem.-46

B.E.(E&TC)

EL-II:ELECTRONIC PRODUCT DESIGN

(2012 Course) (Semester - I)(Elective-II) (404185B)

/Max. Marks : 30

Time : 1 Hour

Instructions to the candidates:

- 1) Answer Q1 or Q2,Q3 or Q4,Q5 or Q6.
- 2) Figures to the right indicates full marks.
- 3) Neat diagrams must be drawn wherever necessary.
- 4) Assume suitable additional data if necessary.
- 5) Use of nonprogrammable calculator is permitted.

- Q1)** a) Explain five elements of successful design. [6]
 b) Explain the concept of man-machine dialogue. [4]

OR

- Q2)** Write notes on any two of the following. [10]

- a) Ergonomics
- b) Temperature, Vibration and shock tests.
- c) Grounding

- Q3)** a) What is shielding? Explain it with neat diagrams. [6]
 b) What are the major differences between system requirements and design system specifications. [4]

OR

- Q4)** a) What are the purpose and goals of an architectural design? [6]
 b) What are major constraints which are considered in formulating the system architecture. [4]

- Q5)** a) What is black box test? Grey box test and white box test? [6]

P.T.O.

[4]

b) Explain egoless design.

OR

Q6) a) Explain waterfall model of software development.
b) What are the good programming practices?

[6]

[4]



- Q1) a) What is V-shape model?
 b) What is unit cost?
 c) How the test plan is developed?
 d) Explain the deadlock?

2015 E&TC.

Aug 15

Total No. of Questions : 6]

P4947

SEAT No. : [Total No. of Pages : 2]

BE/In Sem. - 42

B.E. (E & TC)

EMBEDDED SYSTEMS & RTOS
(2012 Course) (Semester -I) (Elective - I)

Time : 1 Hour]

[Max. Marks : 30]

Instructions to the candidates:

- 1) Answer Q1 or Q2, Q3 or Q4, Q5 or Q6.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.
- 4) Assume suitable data, if necessary.

Q1) a) Explain the following design metric. Time to market, Unit cost. [5]

b) Explain Embedded processor technology. [5]

OR

Q2) a) Explain V-shape model. [5]

b) Explain the following design metric NRE cost, size. [5]

Q3) a) Explain the following. [5]

i) Non Preemptive kernel

ii) Preemptive kernel

b) Explain Mutual Exclusion. [5]

OR

Q4) a) What is Deadlock? When it occurs? [5]

b) What is multitasking? Explain the advantages of multitasking. [5]

PTO.

[5]

Q5) a) Explain any two task related functions.

[5]

b) Explain the following time related functions.

i) OSTime Dly()

ii) OSTime Dly HMSM()

OR

Q6) a) What is semaphore? How does it help in resource sharing in RTOS kernel.

[5]

b) Explain the following functions related to message Q.

[5]

i) OSQ Create()

ii) OSQ Pend()



Total No. of Questions : 6]

P82

SEAT No. :

[Total No. of Pages : 2

OCT.-16/BE/Insem. - 137
B.E. (E & TC)
COMPUTER NETWORKS
(2012 Course) (Semester - I) (404182)

Time : 1 Hour

[Max. Marks : 30

Instructions to the candidates:

- 1) Solve Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6.
- 2) Figures to the right indicate full marks.
- 3) Neat diagrams must be drawn wherever necessary.

Q1) a) Draw OSI-Reference model. Explain function of Data Link Layer. [5]

b) Draw and explain mesh topology with advantages and disadvantages. [5]

OR

Q2) a) Draw TCP/IP protocol suit. Explain different address. [6]

b) Explain circuit switching. [4]

Q3) a) A slotted ALOHA network transmits 250 bit frame using shared channel of 200 kbps bandwidth. Find the throughput if the system (all stations together) produces 1000 frames per second. [5]

b) Explain GO-BACK-N protocol in data link layer. [5]

OR

Q4) a) Explain different frame formats used in HDLC. [6]

b) Explain CSMA/CD protocol. Explain why it is not suitable for wireless communication. [4]

P.T.O.

- Q5) a) Define and explain basic service set and extended service set. [6]*
- b) Explain DCF MAC sublayer. [4]*
- OR*
- Q6) a) Draw Bluetooth layer and explain. [6]*
- b) Explain switch and routers. [4]*

.....

Total No. of Questions : 6]

P4893

SEAT No. : _____

[Total No. of Pages : 1

Q3) a) b) c) d) e) f)

B.E./Insem. - 39

B.E. (E&TC)

**COMPUTER NETWORKS
(2012 Pattern) (Semester - I)**

Time : 1 Hour

[Max. Marks : 30

Instructions to the candidates:-

- 1) Answer Q 1 or Q 2, Q 3 or Q 4, Q 5 or Q 6.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right side indicate full marks.
- 4) Assume suitable data if necessary.

- Q1)** a) Draw the TCP/IP model. List and Explain functions of transport layer. [6]
b) Draw and Explain mesh topology with advantages and disadvantages. [4]

OR

- Q2)** a) Explain unguided media in brief. [6]
b) Compare circuit switching with packet switching. [4]

- Q3)** a) Explain character stuffing framing method. [6]
b) Explain CSMA/CD protocol. [4]

OR

- Q4)** a) Explain HDLC frame format. [6]
b) Explain sliding window protocol with the selective repeat. [4]

- Q5)** a) Explain architecture of 802.11 standard. [6]
b) List the connecting devices with layers of OSI model and explain any one. [4]

OR

- Q6)** a) Explain Bluetooth frame format. [6]
b) Explain in brief Zigbee protocol with its applications. [4]



- Q2) a) What is
 b) What is
 c) How the test plan
 d) Explain:
 e) Functional model vs
 f) Specifications versus requirements
 OR
- Q3) a) Explain:
 b) Explain:
 c) Explain:
 d) Explain:
 e) Explain:
 f) Explain:
 OR

Total No. of Questions : 6]

P81

SEAT No. :

[Total No. of Pages : 1

OCT. -16/BE/Insem. - 136

B.E. (E & TC)

VLSI DESIGN & TECHNOLOGY

(2012 Course)

Time : 1 Hour]

/Max. Marks : 30

Instructions to the candidates:

- 1) Solve Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6.
- 2) Figures to the right side indicate full marks.

Q1) a) What is meant by synthesizable & non-synthesizable statement? Give two examples of each. [5]

b) Write VHDL code for half adder by structural & behavioural modeling. [5]

OR

Q2) a) List & explain different delays involved in chip design. [5]

b) Explain data objects with suitable examples. [5]

Q3) a) Compare PROM, PLA, PAL & CPLD. [5]

b) Explore CPLD/FPGA oriented design flow. [5]

OR

Q4) a) Draw CPLD architecture in detail. Explain in brief. [5]

b) Give typical features & specifications of FPGA. [5]

Q5) a) What is clock skew? What are techniques to minimize? [5]

b) Why should supply & ground bounce be taken care? How are these minimized? [5]

OR

Q6) a) Explore different wire parasitics. [5]

b) With the help of suitable diagram, explain I/O architecture in brief. [5]



- Q2) a) What
b) How the test plan is formalized?
Q3) a) Explain:
b) Functional model verses architectural model.
c) Specifications verses requirements.

Total No. of Questions : 6]

SEAT No. : _____

[Total No. of Pages : 2

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OCT. -16/BE/Insem. - 144

B.E. (E & TC)

ELECTRONIC PRODUCT DESIGN

(2012 Pattern) (Semester - I) (Elective - II) (404185B)

[Max. Marks : 30]

Time : 1 Hour

Instructions to the candidates:

- 1) Attempt Q. No.1 or Q. No.2, Q. No.3 or Q. No.4, Q. No.5 or Q. No.6.
- 2) Figures to the right indicates full marks.
- 3) Neat diagrams must be drawn wherever necessary.
- 4) Assume suitable additional data if necessary.
- 5) Use of nonprogrammable calculator is permitted.

Q1) a) What are the aspects in design for manufacturing? [4]

b) Write short notes on any two: [6]

- i) Cognitive ergonomics.
- ii) Man machine interface.
- iii) Types of grounding.

OR

Q2) a) What are five elements in designing of a product? [5]

b) What is importance of packaging? Explain related factors. [5]

Q3) a) How the test plan is formalized? [4]

b) Explain: [6]

- i) Functional model verses architectural model.
- ii) Specifications verses requirements.

OR

P.T.O.

- Q4)** a) Explain the importance of test cases and test procedure.
b) Write in brief on any two:
i) Functional Design.
ii) Egoless design.
iii) Prototyping.

- Q5)** a) What are good programming practices?
b) Explain the concept of Black, white and grey box tests.

OR

- Q6)** a) What is software testing and debugging?
b) Explain waterfall model of software development.