

Lab Assignment 5

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1. SAR ADC

1.1. Overview

A Successive Approximation Register, unlike the Flash ADC, convert analog signals to digital form by approximating the input signal step by step essentially using binary search.

1.2. Basic Principle of Operation

The SAR ADC operates by iteratively approximating the input voltage. The key components include:

- **Sample-and-Hold Circuit:** Samples the input signal, so that the comparator has a steady value to compare against. (So that the binary search converges)
- **Comparator:** Compares the input signal to the output the ADC, routed through a DAC to check whether the input is higher or lower.
- **Digital-to-Analog Converter (DAC):** Converts the approximated digits back to an analog value for comparison with the input signal.
- **SAR Logic:** A binary search algorithm to successively approximate the input signal.

1.3. 5-Bit SAR ADC

A 5-bit SAR ADC will require 5 comparison steps to approximate the input signal. For an input range of $0 - V_{max}$, the ADC will divide the input range into 32 levels, corresponding to a resolution of 5 bits. Each bit is determined one-by-one, starting from the MSB till the LSB.

2. Designing the SAR ADC

2.1. SAR Logic

To design the SAR ADC, we start from the SAR logic. The logic is the same as binary search. We start at the middle value (Which, in 5 bits is 10000). Then, every iteration, we need to shift the comparator bit into the bits of interest. Let the bits be $A_4A_3A_2A_1A_0$, and the comparator bit be C

1. In the first iteration, $A_4A_3 \rightarrow C\bar{A}_3$
2. In the second iteration, $A_3A_2 \rightarrow C\bar{A}_2$
3. In the third iteration, $A_2A_1 \rightarrow C\bar{A}_1$
4. In the fourth iteration, $A_2A_1 \rightarrow C\bar{A}_0$
5. In the Last iteration, $A_1 \rightarrow C$

One way to do this would be to draw up the K-Maps of the variables, But it all simplifies to the following setup. A counter, checking the iteration, and a register that holds the current state.

The circuit diagram is shown here.

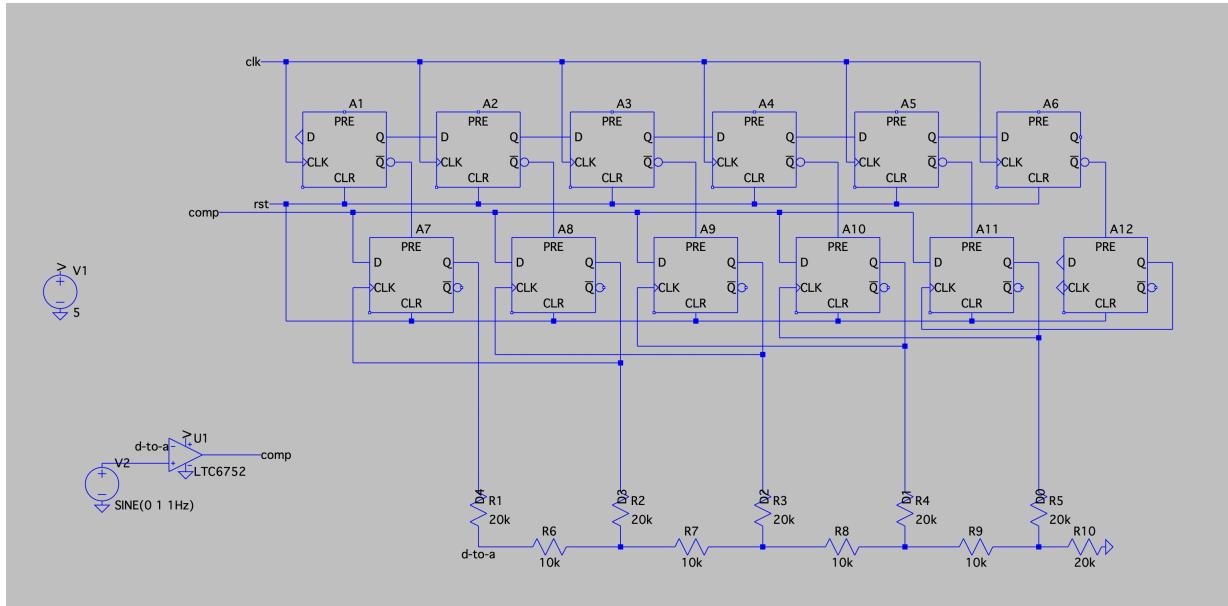


Figure 1. Schematic of SAR ADC

2.2. DAC

The Digital-to-Analog Converter (DAC) is responsible for converting the current digital output of the SAR logic into an analog voltage. This analog voltage is then compared to the input voltage by the comparator. We built a simple R-2R model.

2.3. Comparator

The comparator compares the analog input voltage to the analog voltage generated by the DAC. The comparator's output (the comparator bit, C) indicates whether the DAC output is higher or lower than the input voltage. This comparator bit is used by the SAR logic to determine the next bit.

2.4. Sample and Hold Circuit

The S/H circuit samples the analog input voltage and holds it steady during the successive approximation process. This is necessary because the input voltage may change while the ADC is performing the conversion. The S/H circuit "freezes" the input voltage, allowing the comparator to make an accurate comparison against the DAC output at each step. The S/H circuit consists of a transistor and a capacitor. When the switch is closed, the capacitor samples the input voltage. When the switch is opened, the capacitor holds the sampled voltage.

This is the intended operation of the circuit

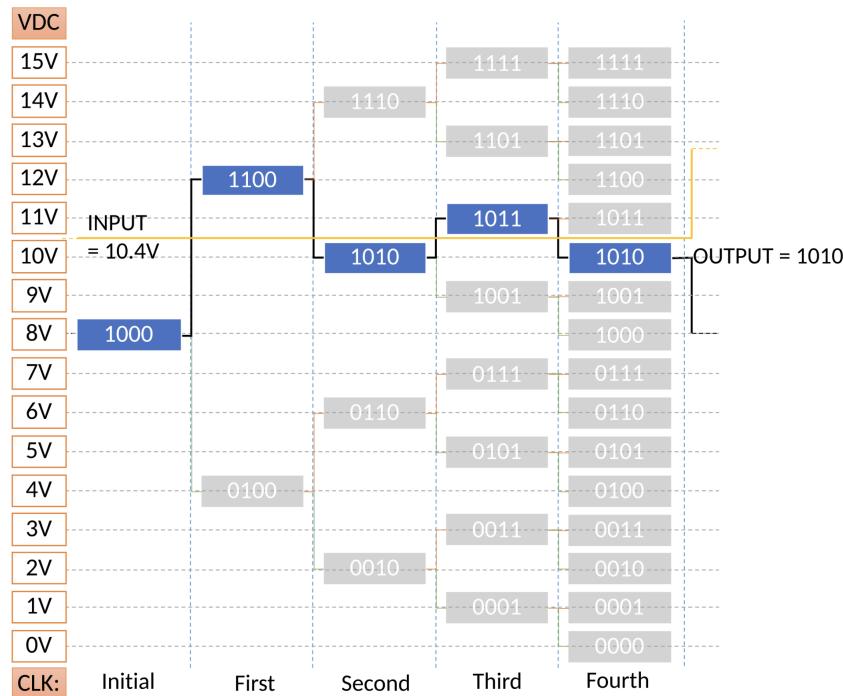


Figure 2. Schematic of SAR ADC

3. The output

At Clock frequency 20Hz, and reset frequency 4Hz, we get these results. (Because the reset happens almost instantaneously, the voltage level is not held for long enough).

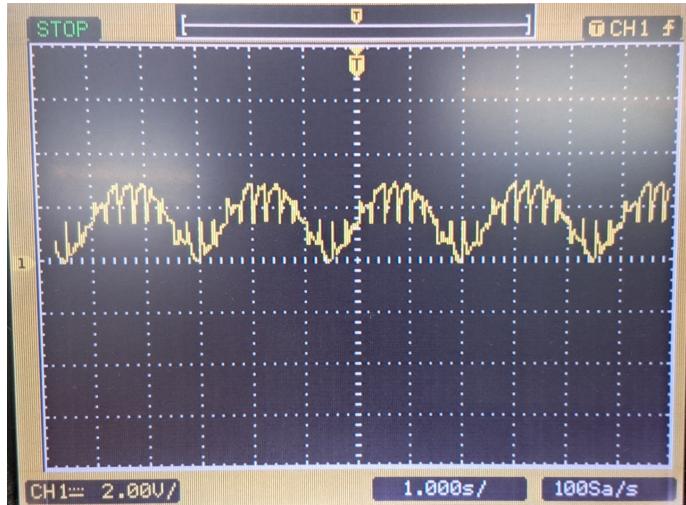


Figure 3. Output of the ADC, for a triangle wave of 400mHz

We tested at the Base clock of arduino, and got these results

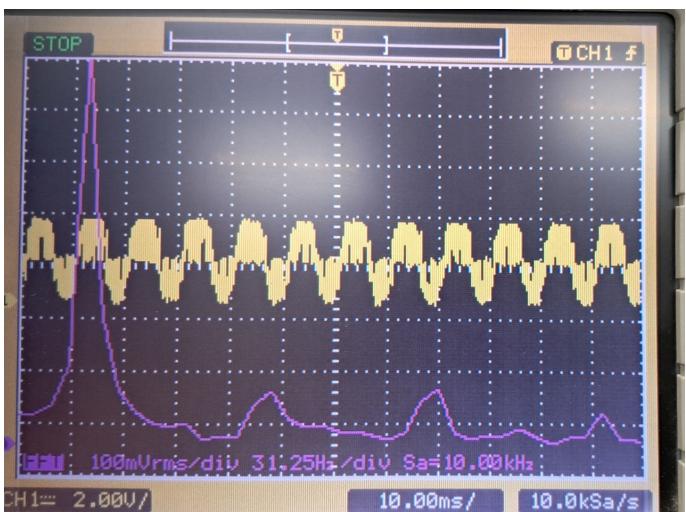


Figure 6. Output of the ADC, for a sine wave of 50Hz

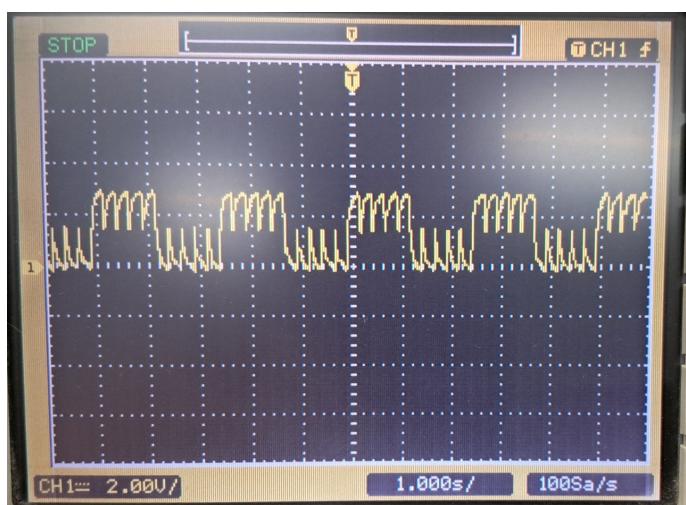


Figure 4. Output of the ADC, for a square wave of 400mHz

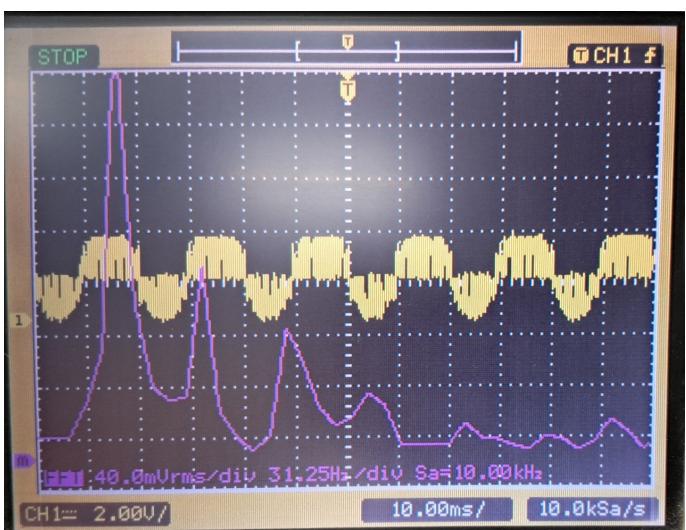


Figure 7. Output of the ADC, for a sine wave of 500Hz

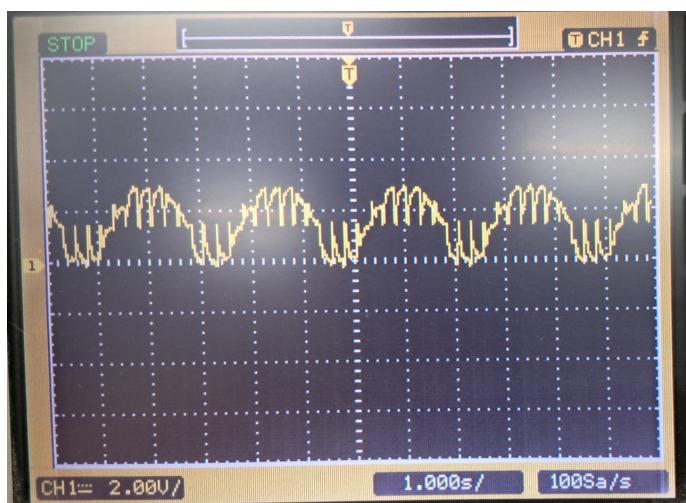


Figure 5. Output of the ADC, for a sine wave of 400mHz

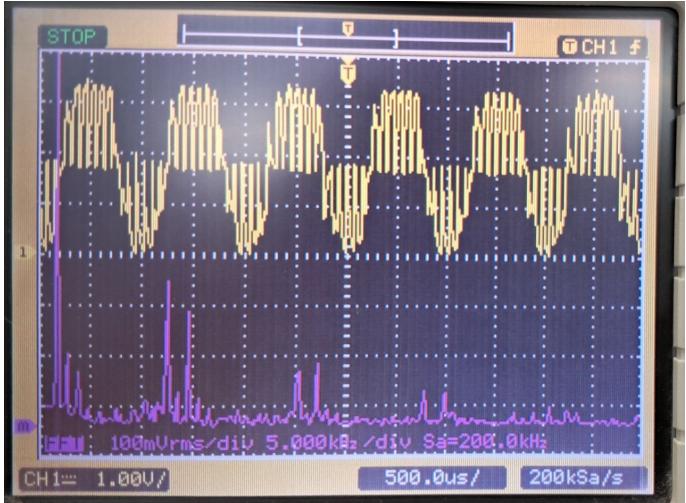


Figure 8. Output of the ADC, for a sine wave of 1kHz

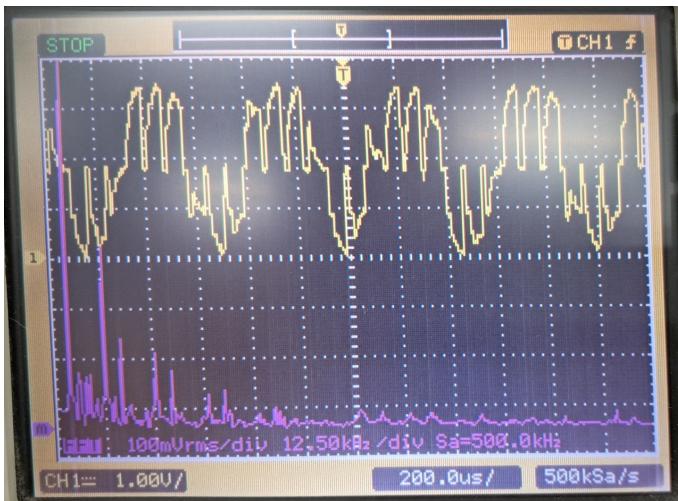


Figure 9. Output of the ADC, for a sine wave of 2kHz

4. Analysis

Other than the fundamental frequency, there are peaks in the sine signal in Figure 8, that correspond to the 1st, 2nd and 3rd overtones.

There are also peaks adjacent to these, which arise due to aliasing. (Higher harmonics are undersampled) The various noise ratios, and thresholds can be calculated from this data.

These peaks are less distinguished and more of a continuous range of frequencies is found, for the sine signal in Figure 7 Nevertheless, the fundamental frequency is dominant, with the first, second and third overtones non-negligibly low. The cleanest spectrum is found for the sine signal of 50Hz, in Figure 6, with only the fundamental frequency showing up.

The spectrum of sine signal of 2000Hz, shown in Figure 9, has many harmonics, which would indicate insufficient sampling.

5. Challenges and Sources of Error

The circuit had to be rebuilt multiple times due to failing components from the lab. Along with this, the Comparator circuit had to be built and tested more than 7 times due to bad ICs.

6. Conclusion

A working 5- bit SAR ADC was built successfully.