# SVCE INNOVATES 2025 STUDENTS’ RESEARCH DAY

Registration form

**Title of the Innovative idea/Project: Integrating Processing-in-Memory with ARM Architecture for Next-Gen Computing**

**Details of the team**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Team Member** | **Name** | **Branch & Year** | **Mail Id** | **Mobile number** |
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**Broad areas under which this research work can be categorized: 1. Embedded Systems**

**2. VLSI**

**3. Machine Learning**

# SVCE INNOVATES 2025

**Title of the innovative idea/project: Integrating Processing-in-Memory with ARM Architecture for Next-Gen Computing**

**Team ID(to be assigned by department coordinator) :**



**ABSTRACT**

Many modern real-time applications involve the computation of data-intensive tasks, especially in Artificial Intelligence (AI) and Machine Learning (ML) models that train on vast datasets to produce meaningful predictions or results. These large-scale operations, which require continuous data storage and processing, reduce CPU efficiency and overwhelm the memory controller.

For example, building a Convolutional Neural Network (CNN) model requires performing matrix multiplications, additions, and shifts on large datasets fetched from memory. During a single execution layer, data must be transferred from memory to the CPU via the memory channel. The CPU issues a request to the memory controller, which then sends commands across the memory channel to the memory module containing the data. The memory module reads and returns the data through the memory channel, and the data moves through the cache hierarchy before being stored in the CPU cache. The CPU can only operate on the data once it is loaded from the cache into a CPU register. After processing, the computed data must be transferred back to memory.

This continuous data movement between memory and the processing unit creates a significant data movement bottleneck, making execution inefficient and slow. To mitigate this issue, Processing-in-Memory (PIM) technology can be utilized. PIM integrates a processing unit, known as the PIM layer, into the processor's memory, allowing data to be processed directly within the memory module instead of being transferred to the CPU's ALU. This reduces unnecessary data movement and power consumption, and thus improves latency and computational efficiency.

This research study aims to integrate PIM technology into an ARM-based processor and evaluate its performance by training a CNN model while measuring efficiency improvements.