Design Analysis of XOR (4T) based Low Voltage CMOS Full Adder Circuit

Subodh Wairya, Garima Singh,Vishant, R. K.Nagaria, S. Tiwari

Abstract--**This paper presents a comparative study of high-speed, low-power and low voltage full adder circuits. Our approach is based on XOR-XNOR (4T) design full adder circuits combined in a single unit. This technique helps in reducing the power consumption and the propagation delay while maintaining low complexity of logic design. Simulation results illustrate the superiority of the designed adder circuits against the conventional CMOS, TG and Hybrid adder circuits in terms of power, delay and power delay product (PDP) at low voltage. Noise analysis shows designed full adder circuit's work at high frequency and high temperature satisfactorily. Simulation results reveal that the designed circuits exhibit lower PDP, more power efficiency and faster when compared to the available full adder circuits at low voltage. The design is implemented on UMC 0.18µm process models in *Cadence Virtuoso Schematic Composer* at 1.8 V single ended supply voltage and simulations are carried out on *Spectre S*.**

Index Terms—**XOR circuit, VLSI, Full Adder, Transmission gate, Hybrid Adder.**

I. Introduction

Low-power design of VLSI circuits has been identified & has resulted in explosive growth of integration of sophisticated multimedia-based applications into wireless & mobile electronics gadgetry in the recent years. Increasing demand for mobile electronic devices such as cellular phones, PDA's and laptops requires the use of power efficient VLSI circuits. The adders are important component in applications such as digital signal processing (DSP) architectures and microprocessors. Adder is the core element of complex arithmetic circuits like addition, multiplication, division, exponentiation, etc. The XOR-XNOR circuits are basic building blocks in various circuits especially-Arithmetic circuits (adder & multipliers), Compressors, Comparators, Parity Checkers, Code Converters, Error-detecting or Error-correcting codes, and Phase Detector.

There are standard implementations with various logic styles that have been used in the past to design full-adder cells [1-4] and the same are used for comparison in this paper. Although, they all have similar function, the way of producing the intermediate nodes and the transistor count is varied. Different logic styles tend to favour one performance aspect at the expense of the others. The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit.

Authors are with the Department of Electronics & Communication Engineering, Motilal Nehru National Institute of Technology (MNNIT), Allahabad-211004, India: (e-mail: swairya@gmail.com, rkn@mnnit.ac.in, stiwari@mnnit.ac.in).

In nano-scaling, power consumption depends upon the application, the kind of circuit implemented, and the design techniques used. Different performance aspects become important, disallowing the formulation of universal rules for optimal logic styles. The circuit propagation *delay* is determined by number of inversion levels, the number of transistors in series, transistor sizes (i.e. channel widths) and intra-cell wiring capacitances. Some of them use one logic style for the whole full adder while the others use more than one logic style for their implementation. The performance parameters of all adders may be reduced without significantly increasing the power consumption and transistor sizes can be achieve minimum power delay (PDP) by optimizing the transistor sizes of full adder circuit. All adders were designed with minimum default transistor sizes initially and then simulated. The aim of this study is to reduce the operating voltage V_{DD} (0.8V), however our new adder cell is useful in building up large circuits such as multipliers despite increase in transistor count.

To summarize, some of the performance criteria are considered in the design and evaluation of adder cells and some are utilized for the ease of design, robustness, silicon area, delay, and power consumption. The paper is organized section wise. Section II describes the review of full adder circuit topologies and illustrates the concept of XOR-XNOR (4T) based Hybrid full adder. Section III highlights some 1-bit adder cell modules which are based on XOR-XNOR (4T) gates. In Section IV implementations of XOR(4T) function based full adder are discussed. In Section V the reported and newly design full adder design topologies are simulated and the simulation results and compared. Finally section VI puts forth the conclusion to the research.

II. Review of Full Adder Topologies

In recent years, several variants of different logic styles have been proposed to implement 1-bit adder cells [5-20]. There are two types of full adders in case of logic structure. One is static style and the other is dynamic style. Static full adders are generally more reliable, simpler and consume less power than the dynamic ones. Their papers have investigated different low voltage approaches with full swing realizing of static adders using CMOS technology.

Static CMOS logic styles have been used to implement the low-power 1-bit adder cells. In general, they can be broadly divided into two major categories: the Complementary

978-1-4577-2168-7/11/$26.00 ©2011 IEEE

CMOS and the Pass-Transistor logic circuits. The complementary CMOS (C-CMOS) full adder is based on the regular CMOS structure with P type Metal Oxide Semiconductor (pMOS) pull-up and N type Metal Oxide Semiconductor (nMOS) pull-down transistors [3-5]. The series transistors in the output stage form a weak driver. Therefore, additional buffers at the last stage are required to provide the necessary driving power to the cascaded cells. The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing, which provides reliable operation at low voltage and arbitrary transistor sizes. Moreover, the layout of complementary CMOS circuit is straightforward and area-efficient due to the complementary transistor pairs and smaller number of interconnecting wires.

Another adder is the Complementary Pass Transistor Logic (CPL) with swing restoration, which uses 32 transistors [6-8]. CPL adder produces many intermediate nodes and their complement to make the outputs. The most important feature of CPL is the small stack height and the internal node low swing, which contribute to the lowering of power consumption. The CPL suffers from static power consumption due to the low swing at the gates of the output inverters. Double Pass-Transistor logic (DPL) and Swing restored pass- transistor logic (SRPL) are related to CPL. SRPL style is derived from the CPL. Here, the output inverters are cross-coupled to a latch structure which performs swing restoration and output buffering at the same time. SRPL gates are highly sensitive to transistor sizing and show acceptable performance only in very special circuit arrangements. (e.g., no gates in series, small output loads). It has poor output driving capability, slow switching and large short-circuit currents. To lower the power consumption of CPL circuits, LCPL and SRPL circuit styles are used. Double pass-transistor logic (DPL) uses complementary transistors to maintain full swing operation and reduce the dc power consumption. This eliminates the need for restoration circuitry. One disadvantage of DPL is the large area used due to the presence of pMOS transistors.

Some designs of full adder circuits based on transmission-gates are shown in Figure 1. Transmission gate logic circuit is a special kind of pass-transistor logic circuit [4],[16]. The main disadvantage of transmission gate logic is that it requires double the number of transistors than pass-transistor logic or more to implement the same circuit. TG gate full adder cell has 20 transistors.

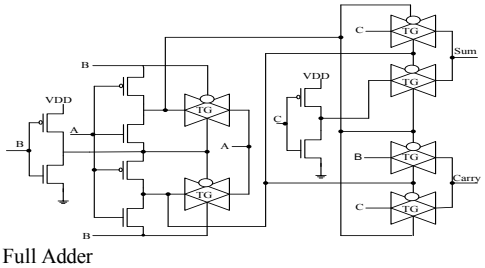


Fig. 1 TG Full Adder

There are various issues related to the full adder like power consumption, performance, area, noise immunity and regularity and good driving ability. All the full adder circuits can be divided into two groups on the basis of output. The first group of full adders has a full swing output. C-CMOS, CPL, TG, TGA, Hybrid, 14Tand16T belong to the first group [5-11]. The second group comprises full adders (10T, 9T & 8T) without full swing outputs [12-20]. This full adder usually have lower number of transistors & subsequently less power consuming and occupies lesser area. The second group of non full swing full adders is useful in building up larger circuits as multiple bit input adder and multipliers. One such application is the Manchester Carry- Look Ahead chain.

III. LOGIC DESIGN MODULES OF XOR-XNOR (4T) BASED HYBRID FULL ADDER

More than one logic style is used for implementation of the hybrid adders. The hybrid adder cells may be classified in various categories depending upon their structure and logical expression of the Sum and Carry outputs signals.

A. Reported Logic Design Approaches of XOR-XNOR (4T) Based Full Adder Module with Full Swing output Logic

Most adder topologies are based on two XOR circuits: one to generate H (XOR) with $\overline{H}$ (XNOR), and the other to generate the Sum output function as shown in Figure 2 & 3. The Carry signal is obtained by using one MUX (multiplexer).

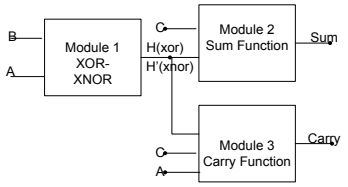
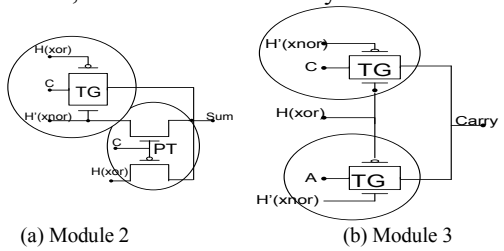


Fig. 2 Basic Design Modules approach for Full Adder circuit

$$\text{Sum} = A \oplus B \oplus C \text{ and Carry} = AB + C(A \oplus B)$$

$$H = A \oplus B, \text{ Sum} = H \oplus C \text{ and Carry} = A \cdot \overline{H} + C \cdot H$$



(a) Module 2 (b) Module 3

Fig.3 Basic logic approach for Full Adder with Full Swing output

A new set of low power 4 transistor XOR and XNOR circuits called powerless P-XOR and Groundless G-XNOR respectively are proposed in [15-17]. The P-XOR and G-XNOR consumes less power than other design because it has no power supply or ground connection. The performance of the complex logic circuits is affected by the individual performance of the XOR-XNOR circuits that are included in them.

B. !4 T and 16T Full Adder with Full Swing output Logic

A high performance full adder cell circuit 14T & 16T has been designed using low power 4T XOR-XNOR design and transmission gates as shown in Figure 4. 14T transistors utilizes the low power XOR/XNOR circuit and a pass transistor network to produce a non full swing sum signal and uses four transistors to generate a full swing carry signal, which do not provide enough driving power [13]. Due to using pass transistor networks, the output signals of 14T do not provide good driving power.

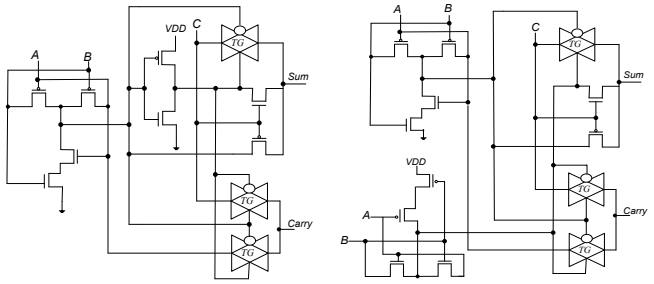


Fig. 4 (a) 14T Full Adder (b) 16T Full Adder

A 16T adder is derived from the 14 transistors circuit [9], which has 16 transistors, generates full swing XOR and XNOR signals by utilizing a pass transistor based DCVS circuit. As mentioned in [11], this leads to higher speed and better performance in comparison with the circuit proposed in [12]. Then it utilized this circuit together with a pass-transistor network to generate a non full swing sum signal and with a transmission gate network to generate a full swing carry signal. Similar to the 14 transistors circuit it has a threshold voltage loss problem in internal nodes but the loss is not propagated to the output nodes. Despite the threshold voltage loss in internal nodes, this circuit maintains a full output voltage swing. The power consumption of this adder is better than the conventional CMOS design and other high gate count adders.

C. 10T Full Adder

The designs of the 10T adder cell are based on an optimized design for the XOR function and pass transistor logic to implement the addition logic function. Two XOR operations are required to calculate the Sum function. Each XOR operation requires 4T transistors. 2X1 MUX is used for Carry function implemented using two transistors. In ref. [15] different components have been combined to make 41 new 10T transistor full adders. Some 10T full adders can be designed by interchanging the inputs of the module having lowest propagation delay amongst all the 10T full adder circuits.

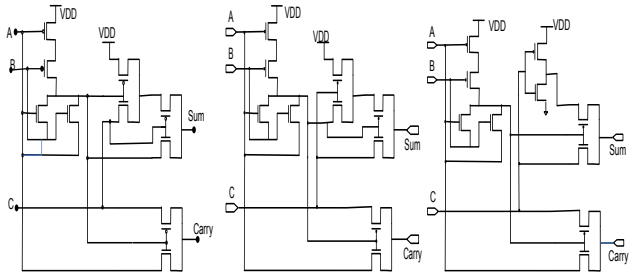


Fig.5 (a) 9A Full Adder (b) 9B Full Adder (c) 13A Full Adder

The 9A full adder is shown in Figure 5(a), implements 4-transistor XOR-XNOR circuit, 4-transistor groundless XNOR circuit and 2X1 multiplexer. The 9B full adder has shown in Figure 5(b), implements using 4-transistor XOR-XNOR circuit, 4-transistor groundless XNOR circuit and 2X1 multiplexer. Full adder 9B can be designed from full adder 9A by interchanging the inputs of 4-transistor groundless XNOR. A transistor –level implementation for 10 transistor full adder 13A is shown in Figure 5(c). 10 transistors full adders 13A and 9B have better critical delay than the 10 transistors SERF full adder in all loading condition. The XNOR node before the inverter and the outputs of the cell have voltage drop. Threshold voltage (Vth) loss in circuit nodes leads to serious problems especially at low supply voltages, such as very little noise margin, high leakage power, and serious problems in cascading.

D.SERF Full Adder

The Static Energy Recovery Full adder (SERF) is a 10 transistor (10T) adder shown in Figure 6 [14]. The circuit is claimed to be extremely low power consuming because it does not contain direct path to the ground and the charge stored at the load capacitance is reapplied to the control gates (energy recovery). The elimination of the path to the ground reduces the total power consumption by reducing the short circuit power consumption. This circuit is one of the best full adders in terms of power consumption. There are some problems in this circuit. First Sum is generated from two cascaded XNOR gates which leads a long delay. Second, it cannot work correctly with a low voltage.

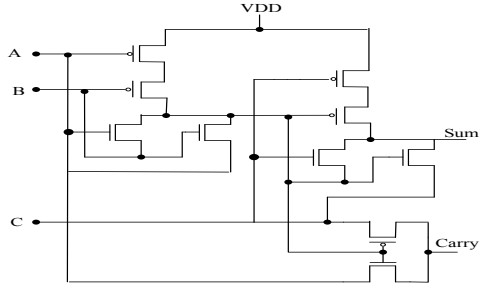


Fig. 6 SERF Full Adder

The combination of low power and low transistor count makes the SERF adder cell a feasible option for low power design. But the disadvantage with this design is relatively slower than peer designs and it cannot be cascaded at low V_{DD} operation due to multiple- threshold loss problem.

E. CLRCL Full Adder

The double threshold loss problem encountered by the 10T full adders (SERF) is alleviated by a full adder circuit featuring complementary and level restoring carry logic (CLRCL) as shown in Figure 7. The goal is to reduce the circuit complexity and to achieve faster cascaded operation.

The strategy is to avoid multiple threshold voltage losses in carry chain by proper level restoring.

Liu, Hwang, Sheu and Ho, however, could minimize the threshold loss problem in a 10T full adder reported in [17] as a Complementary and Level Restoring Carry Logic (CLRCL) full adder. In the CLRCL adder, 2X1 MUX and CMOS inverters are used to realize the Sum and Carry functions using the following Boolean equations:

$$Sum = A \oplus B)\overline{Carry} + \overline{A \oplus B})B$$

$$Carry = A \oplus B)B + \overline{A \oplus B})A$$

The inverters have been used to combine the output threshold voltage loss and also as a buffer along the Carry function chain to speed up the Carry propagation. DC and transient analysis illustrated that the CLRCL full adder encounters only one threshold voltage loss problem and requires the minimum V_{DD}.

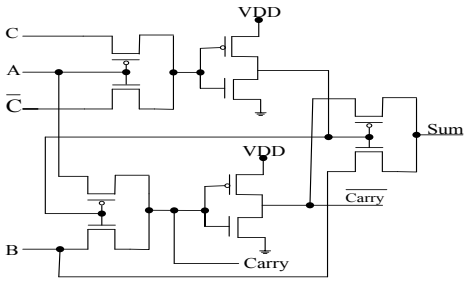


Fig. 7 CLRCL Full Adder

In addition, the performance edge of the CLRCL circuit in both speed and power consumption becomes even more significant as the word length of the adder increases. The limitation of CLRCL full adder design is a skew between inputs to the various sub-sections in CLRCL full adder.

F. XOR-XNOR (4T) based Full Adder

Another reported full adder cell is based on low power XOR-XNOR (4T) [20] pass transistor logic design and transmission gates as shown in Figure 8 [21]. This hybrid circuit is a designed combination of TG with PT logic style that shows high-speed and energy efficiency. The reported circuit has the least number of transistors and no complementary input signals are required.

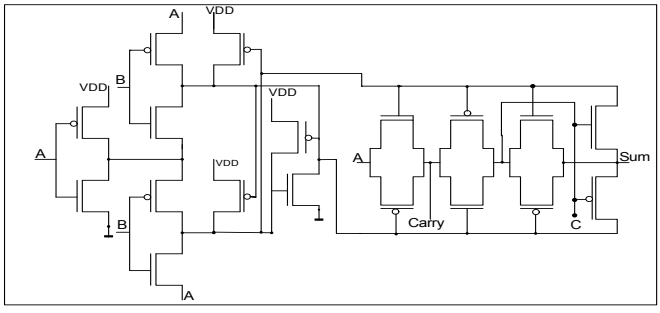


Fig. 8 XOR-XNOR (4T) based 16T (4T) Full Adder

IV. PROPOSED DESIGN FULL ADDER BASED ON XOR (4T)

The designed structure of a XOR based full adder consists of one exclusive OR/NOR function (XOR /XNOR), two transmission gates in the middle, and one XOR gate on the right. The complementary outputs of the XOR/XNOR gate are used to control the transmission gate which together realizes a multiplexer circuit producing the Carry output function.

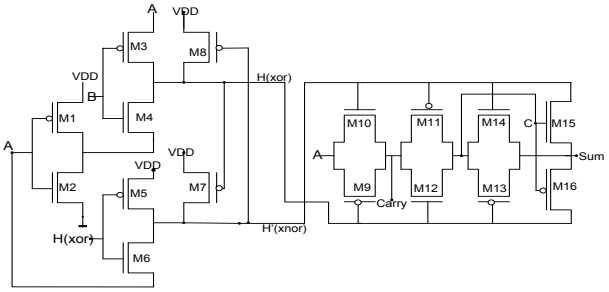


Fig. 9 Schematic for Designed Full Adder

Proposed design full adder circuit is a combination of two logic styles that offers high-speed and low-power consumption at low voltage (0.8V) as shown in Figure 9. Intermediate XOR and XNOR function output is generated using 4T-transistor and CMOS inverter respectively. Two cross-coupled pMOS transistors arrangement that eliminates the non-swing operation at low voltage (less than 1V), are connected between XOR and XNOR function outputs. The complementary outputs of the XOR & XNOR logic gate are used to control the transmission gate which together realizes a Sum output function with pass transistors. Aspect ratio of the inverter circuit must be high for better driving capabilities. Lowering the supply voltage appears to be a well known means of reducing power consumption. However, lowering the supply voltage also increases the circuit delay and degrades the drivability of cells designed with certain logic design styles. By selecting proper (W/L) ratio we can optimize the circuit's performance parameters without decreasing the power supply. The voltage degradation due to threshold drop can be minimized by increasing the W/L ratio of transistor M4. An equation [19] relating threshold voltage of a MOS transistor to the channel length and width is given as:

$$V_T = V_{T0} + \gamma\left(\sqrt{V_{SB} + \phi_0} - \sqrt{\phi_0}\right) - \alpha_l \frac{t_{ox}}{L}(V_{SB} + \phi_0) - \alpha_v \frac{t_{ox}}{L}(V_{DS}) + \alpha_W \frac{t_{ox}}{L}(V_{SB} + \phi_0)$$

where,

V_{T0} is the zero bias threshold voltage,

γ is bulk threshold coefficient,

φ_0 is $2\varphi_F$, where φ_F is the Fermi potential,

t_{OX} is the thickness of the oxide layer,

α_l, α_v and α_w are the process dependent parameters.

The above equation shows that by increasing the channel width (W) it is possible to decrease the threshold voltage (V_{th}) & subsequently minimizes the voltage degradation due to threshold voltage by increasing the width of M4 transistor keeping the length constant.

V. SIMULATION RESULTS

The simulation has been performed for different supply voltage ranging from 0.8V to 1.8V, which allow us to compare the speed degradation and average power dissipation of the reported and newly designed adder topologies. The results of the designed circuits in this paper are compared with a reported standard CMOS full adder circuit. All the circuits are designed in Cadence VIRTUOSO environment using CMOS process design kit. Temperature of operation for circuits is kept at 27^0C. Default values of the channel width (W) and length (L) for nMOS and pMOS in UMC 0.18µm technology are 0.24µm and 0.18µm respectively, and W is varied up to 1µm keeping length constant with proper transistor sizing. By optimizing the transistor size of full adders considered, it is possible to reduce the delay of all the adders without significantly increasing the power consumption, and transistor sizes can be set to achieve minimum *power delay product* (PDP). All adders were designed with minimum transistor sizes initially and then simulated.

Each one-bit full adder has been analyzed in terms of propagation delay, average power dissipation and their products. The value of delay, power and power-delay product of C-CMOS, hybrid and newly designed full adders are measured. The lowest voltage that could work on 10T(4T),SERF and 14T(4T) is 1.4V, 1.2V and 1V respectively. The supply voltage for simulation comparison for C-CMOS, and newly designed adder circuit are 0.8V V_{DD}.

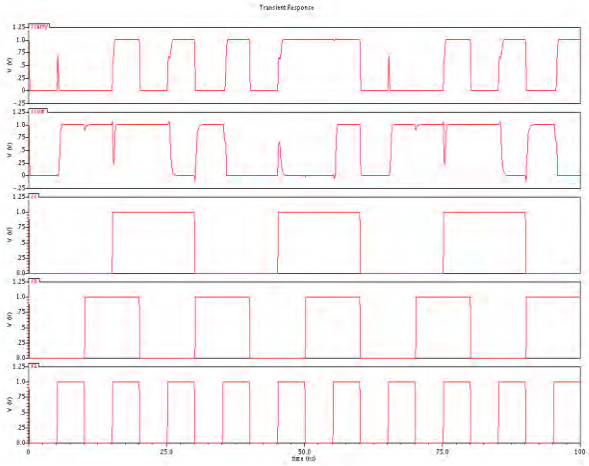


Fig. 9 Simulation snapshot waveforms of designed Full Adder

The simulated snapshot input/output waveforms of designed adder circuit are shown in Figure 9. For each transition, the delay is measured from 50% of the input voltage swing to 50% of the output voltage swing. The maximum delay is taken as the cell delay.

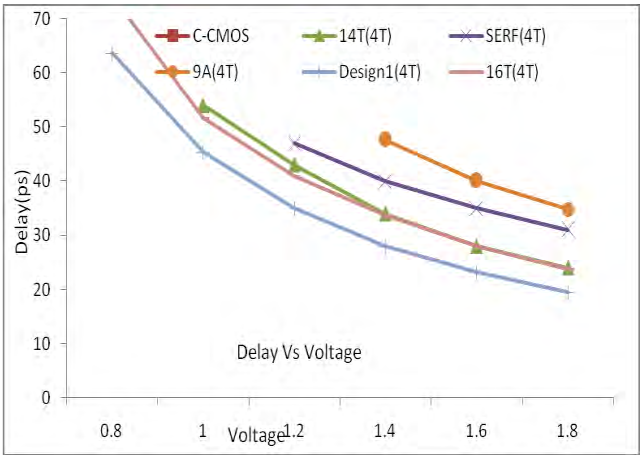


Fig. 10 (a) Delay (ps) comparison of Full Adder cells

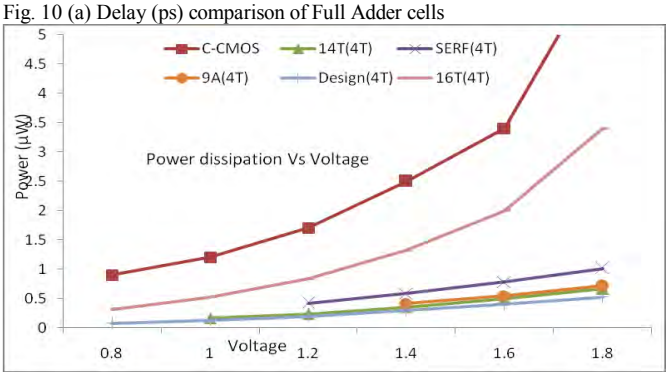


Fig.10 (b) Power (µW) comparison of Full Adder cells

The delay of the designed circuit is compared with the other circuit in Figure 10(a) which shows that the delay of the proposed circuits is very low. Although the circuits proposed in this paper have lower power dissipation than standard CMOS circuits, they have lowest PDP in most cases. The PDP (10^{-18}j) is a quantitative measure of the efficiency and a compromise between power dissipation and speed. Power delay product calculated from production of worst-case delay and average power consumption is given as:

$$PDP = Power_{average} X\ Delay_{worst\text{-}case}$$

A. Immunity to Noise Analysis

In this section we demonstrate that the supply voltage variation noise does not affect the functionality of the circuit. One important factor from the noise perspective that should be taken into consideration is the immunity of the circuit to the ambient temperature. The value of delay and average power consumption for the new designs and some of the conventional adder cells including C-CMOS, TG & Hybrid at different temperatures are shown in Table I. Simulation results shown in Figure 9 to 11 were measured at room temperature at 27^oC but, values of Table I was attained at 0 & 70^oC. As Table I shows, lowering the temperature decreases the power dissipation and speed of circuits, but any increase in the temperature increases these parameters. It is also obvious from simulation results that the design can perform reliably at these temperatures and increasing or decreasing of the delay and power consumption at 0^oC and 70^oC towards 27^oC is acceptable. It means that the design

has an acceptable functionality over a vast temperature range.

TABLE I
SIMULATION RESULT FOR DELAY AND AVERAGE POWER
(V_{DD} for C-CMOS, 14T and newly design circuit is 1V and 10T is 1.4V and SERF is 1.2V respectively)

Design	Temperature (0^0C)		Temperature (70^0C)	
Adders	Delay (ps)	Power(µW)	Delay(ps)	Powe(µW)
C-CMOS	539	0.86	542	0.96
Hybrid	762	1.46	862	1.56
14T	54	0.16	57	0.18
10T(4T)	47.6	0.41	48.2	0.44
SERF(10T)	47	0.42	49	0.44
Design 4T	42	0.12	46	0.14

B. Noise Power Vs Frequency and Temperature Analysis

The proposed full adder design is also analyzed for the noise power analysis with frequency and temperature variation respectively. The noise output response (square output noise voltage) is shown in Figure 11 & 12. Measured noise power is the sum of thermal & flicker noise as a voltage at the output which is calculated in the Cadence VIRTUOSO simulation environment. For the entire noise measurement 0.8V supply source has been taken and others inputs are set to zero. Also the stability of the proposed designs is calculated at the two extreme temperatures which account for noise immunity. Noise analysis shows designed full adder circuit response is constant at high frequency which operates at high frequency and at high temperature satisfactorily.

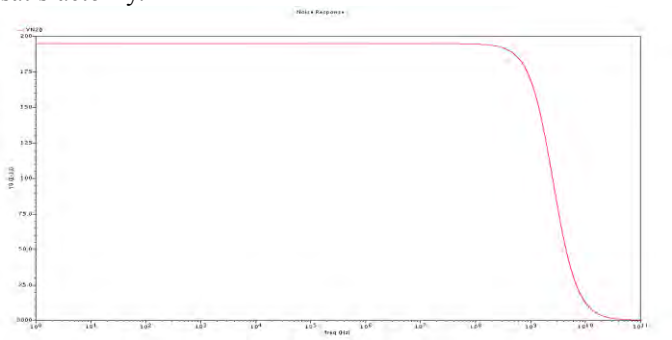


Fig. 11 Noise power Vs Frequency response of newly designed Full Adder.

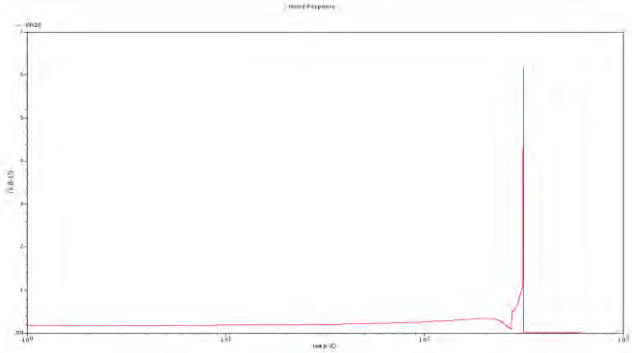


Fig. 12 Noise power Vs Temperature response of newly designed Full Adder.

VI. CONCLUSION

An extensive performance analysis of 1-bit full adder cell has been presented. Different adder logic styles have been implemented, simulated, analyzed and compared. Using the adder categorization and hybrid-CMOS design style, many full adders can be conceived. As an example, newly full adder has been designed using hybrid-CMOS design style with pass transistor are presented in this paper that targets low PDP. The XOR (4T) based hybrid-CMOS full adder shows better performance than most of the other standard full-adder cells owing to the new design modules analysis is discussed in this paper. The compared simulation result shows that the noise performance of the design is superior to other reference design of full adder circuits under different simulation parameters.

VII. REFERENCES

[1] John P. Uyemura, "Introduction to VLSI circuits and systems," Wiley John & Sons, Inc, 2002.

[2] Sung-Mo Kang, Y. Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design," Tata McGraw Hill, 2003.

[3] N. Weste, D. Harris, "CMOS VLSI Design," Pearson Wesley, 2005.

[4] N. Zhuang and H. Wu, "A new design of the CMOS full adder," *IEEE J. Solid-State Circuits*, vol. 27, no. 5, pp. 840–844, May 1992.

[5] A.P. Chandrakasan, S. Sheng and R. W. Bordersen, "Low-power CMOS digital design," *IEEE J. Solid-State Circuits, vol*. 27, pp. 473- 483, April 1992.

[6] Uming Ko, PorasT.Balsara and Wai Lee, "Low-Power Design Techniques for High-Performance CMOS Adders," *IEEE Trans. on very Large Scale Integration (VLSI) Systems*, vol. 3, no.2, pp. 327-333, June 1995.

[7] D. Radhakrishanan, S. R. Whitaker and G. K. Maki, "Formal design procedures for pass-transistor switching circuits," *IEEE J. Solid- State Circuits,* vol. 20, no. 3, pp. 531-536, June 1985.

[8] Reto Zimmermann and Wolfgang Fichtner, "Low-power Logic Styles: CMOS versus pass transistor logic," *IEEE Journal of Solid-State Circuits, vol*. 32, no. 7, pp. 1079-1090, July 1997.

[9] Ahmed M. Shams, and Magdy A. Bayoumi, "A Novel High-Performance CMOS 1-Bit Full-Adder Cell," *IEEE Trans. on Circuits & Systems. II*, Analog and Digital Signal Processing, vol. 47, no. 5, pp. 478–481, May 2000.

[10] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," *Proc. Inst. Elect. Engg. Circuits Devices Systems*, vol. 148, no. 1, Feb. 2001, pp. 19-24.

[11] Sumeer Goel, Ashok Kumar, Magdy A. Bayouni, "Design of Robust, Energy-Efficient Full Adders for Deep-Submicrometer Design Using Hybrid-CMOS Logic Style," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 12, pp. 1309-1321, Dec. 2006.

[12] Ahmed M. Shams, Tarek K. Darwish, and Magdy A. Bayoumi, "Performance Analysis of Low-Power 1-Bit CMOS Full Adder Cells," *IEEE Trans.on Very Large Scale Integration (VLSI) Systems*, vol. 10, no. 1, pp. 20–29, Feb. 2002.

[13] Mark Vesterbacka, "A 14-Transistor CMOS Full Adder With Full Voltage-Swing Nodes," *Proc. IEEE Workshop Signal Processing Systems*, Oct 1999, pp. 713-722.

[14] R. Shalem, E. John and L. K. John "A NOVEL LOW POWER ENERGY RECOVERY FULL ADDER CELL," in *Proc. Great Lake Symp. VLSI*, 1999, pp. 380–383.

[15] Hung Tien Bui, Yuke Wang and Yingtao Jiang, "Design and Analysis of Low-Power 10-Transistor Full Adders Using Novel XOR-XNOR Gates," *IEEE Transactions on Circuits & Systems II: Analog and Digital Signal Processing*, vol. 49, no. 1, pp. 25-30, Jan. 2002.

[16] Chip-Hong Chang, Jiangmin Gu, Mingyan Zhang, "A Review of 0.18µm Full Adder Performances for Tree Structured Arithmetic Circuits," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 13, no. 6, pp. 686-695, June 2005.

[17] Jin-Fa-Lin, Yin-Tsung Hwang, Ming-Hwa Sheu, and Cheng-Che Ho, "A Novel High-Speed and Energy Efficient 10-Transistor Full Adder Design", *IEEE Trans.on Circuits and Systems I*, vol. 54, no. 5, pp.1050-1059, May 2007.

[18] M. Vesterbacka, "A New six-transistor CMOS XOR Circuits with complementary output," Proc. *42nd Midwest Symp. on Circuits and Systems*, Las Cruces, NM, Aug. 1999.

[19] Y. Tsividis, M*ixed Analog-Digital VLSI Devices and Technology*, Singapore McGraw Hill, 1996:.

[20] Shiv Shankar Mishra, S. Wairya, R.K. Nagaria and S. Tiwari, "New Design Methodologies for High Speed Low Power XOR-XNOR Circuits," *Journal of World Academy Science, Engineering and Technology (WASET)*, vol. 55, no. 35, pp. 200-206, July 2009.

[21] S. Wairya **,** P. K. Tripathi , V. Narendar, R. K. Nagaria and S. Tiwari, "A New High Performance Adder-Cell Design and Analysis with minimum Transistors" *1st International Conference on Current Trends In Technology,(NUiCONE–2010)*, Institute of Technology, Nirma University, Ahmedabad, India, pp 1-6, 9th -11th Dec. 2010.

[22] Subodh Wairya, Rajendra Kumar Nagaria and Sudarshan Tiwari, "New Design Methodologies for High-Speed Low-Voltage 1 Bit CMOS Full Adder Circuits", *International Journal of Computer Technology and Application (JCTA)*, Vol. 2, no.3, pp. 190-198, 2011.