Comparative Analysis of Wilson Current Mirror utilizing FGMOS and QFGMOS Technique

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***Abstract*—This paper presents a design of Wilson current mirror using different low voltage and low power design techniques. The techniques utilized for this paper are the Floating Gate Metal Oxide Semiconductor i.e. (FGMOS) and Quasi - Floating Gate Metal Oxide Semiconductor i.e. (QFGMOS) structure. In this paper we will analyze and compare the performance parameters like Input impedance, Output impedance, Bandwidth , Output current vs Input current Characteristics. Performance of the Simple and proposed Wilson current mirror circuit has been operated by using PSpice simulator on 180nm technology at a +0.5 V supply voltage.**

***Index Terms*—Wilson Current Mirror, Floating-Gate MOSFET, Quasi – Floating Gate MOSFET, Output Resistance , Low Voltage, Bandwidth**

I. Introduction

A Current Source is substantially used in VLSI design. In order to design a constant current source which is required in maximum VLSI circuits,current mirror is the good option. The Current Mirror is widely used as a current source .The Current Mirror is a circuit whose function is to copy the current flowing in one active device into different device by keeping current as constant at output terminal regardless what load is applied [1] [2] . Current mirror possess very low input Resistance and very high output Resistance. Current Mirrors are universally exploited in the analog integrated circuits for eg. digital to analog converter, analog to digital converter ,operational transconductance amplifier, Current conveyors ,current mode filter, operational amplifier etc. Current mirror are harnessed as an Active load , dc Current source , Current amplifier and also been widely utilized for biasing purpose in various analog and mixed digital VLSI circuits [3] [3]. To ameliorate functioning of Current mirror many methods have been proposed . various performance enhancement techniques like DTMOS, Voltage Follower ,Level Shifter , FGMOS , QFGMOS are widely used [4] [5], [6] [7]. Simple current mirror has relatively low output resistance and suffers from current mismatch and Channel length modulation effect. Though the cascode current mirror removes drawback of the channel length modulation effect but it suffers from Body effect which ultimately disturbs current at output. .Cascode multiple current mirror configuration provides increased output Resistance and effective open circuit voltage [8] Wilson Current mirror do the same job by utilizing negative feedback configuration. It virtually eliminates the current mismatch of simple current mirror by clinching output current is close to to Input current [9].In Low voltage design the most considerably used methods are FGMOS and QFGMOS .Various types of current mirror,current mode squarer/divider circuit have been designed using FGMOS and QFGMOS technique [7], [8], [9], [10] .To reduce supply voltage requirements and power dissipation Floating gate provides best solution. FGMOS requires effective threshold voltage which can further be reduced by bias voltage . FGMOS suffers from the problem of charge storage which is resolved by QFGMOS. QFGMOS offers better execution in terms of frequency response and the DC offset.This paper is structured in the following manner : commencing from the I The Introduction, II LVLP Design Techniques A. FGMOS B. QFGMOS .III proposed Current Mirror i.) Conventional Current Mirror ii.)FGMOS based Wilson Current Mirror iii.) QFGMOS based Wilson Current Mirror. IV Simulation Results of all the circuits with detailed analyses .V Final Conclusion.

II. LVLP Design Techniques

To achieve desired specifications like High/Low Input Impedance, Low /High Output Impedance , Bandwidth and accuracy the low power design techniques are required .

A. Floating Gate (FG)

The Floating gate Technique is considerably used for low voltage design because by changing bias voltage effective threshold voltage can be reduced. FGMOS and QFGMOS have an advantage to work over lower supply voltage . The input

coupling capacitor divider forces input signal to get attenuated and hence the linearity increases. Linearity is one of the main advantage given by these devices. Though by using Flipped Voltage Follower and Shunt feedback low Input impedance requirement is satisfied. By connecting output impedance with series feedback Low input and output impedance purpose is fulfilled but at the cost of giant supply voltage. The FGMOS possesses capability to perform the weighted sum operation of voltage signals applied at input gate. Another important feature it possess is charge retention capability. Hence FGMOS is widely used as Low Voltage analog circuit such as Rectifier , current mirror , Multiplier and amplifier .

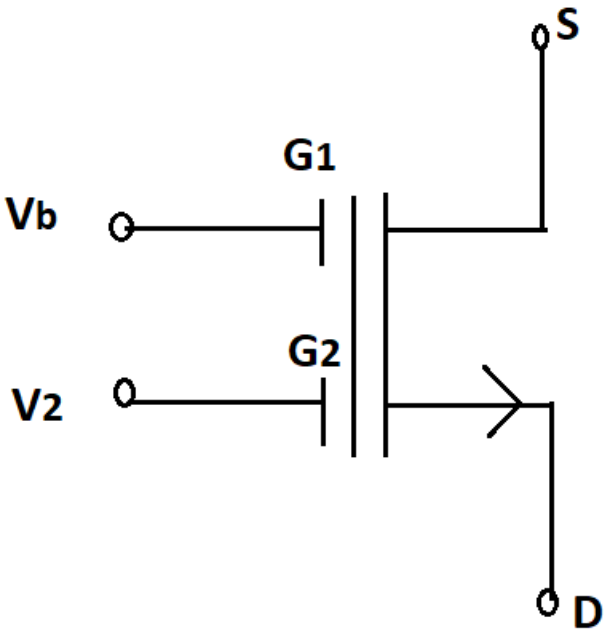

Fig. 1. FGMOS Transistor Symbol

The Fig. 1 shows p channel two input FGMOS transistor symbol and Fig. 2 shows FGMOS transistor equivalent circuit respectively [11]. Vb is the bias voltage applied at gate G_1 and V_2 is the signal input are applied at gate G_2 as seen from Fig. 1. The equation for drain current for p- channel two input FGMOS transistor operating in the saturation region is stated by subsequent equation (1) [11].

$$I_D = \frac{\beta}{2}(V_{FGS} - V_{TH})^2 \tag{1}$$

Where, β is the transconductance parameter,the effective floating gate to source voltage i.e. V_{FGS} is stated by subsequent equation

$$V_{FGS} = \frac{C_1 V_b + C_2 V_{2s} + C_{FGD} V_{DS} + C_{FGB} V_{BS} + Q_{FG}}{C_T} \tag{2}$$

where

$$C_T = C_1 + C_2 + C_{FGD} + C_{FGS} + C_{FGB} \tag{3}$$

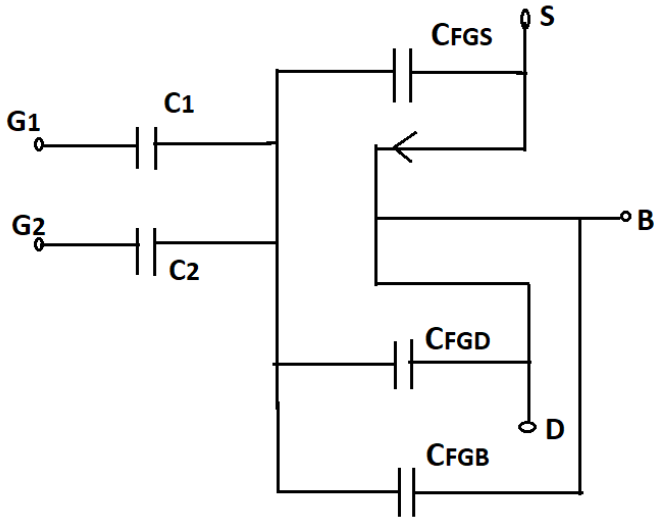

Fig. 2. FGMOS Transistor Equivalent circuit

and C_T represents the total Floating Gate capacitance. C_{FGD} is the parasitic capacitances from floating gate to drain(D),C_{FGS} is the parasitic capacitances from floating gate to source(S) and C_{FGB} is the parasitic capacitances from floating gate to bulk(B).Q_{FG} is the stationary charge present on the floating gate.$V_T H$ is the Threshold voltage , V_{bs} depicts the bias Voltage w.r.t source at $gate(G_1)$, $V_2 s$ is the signal voltage w.r.t source at the gate terminal (G_2) and V_{Bs} is the bulk (B) voltage w.r.t source(S) of FGMOSFET as conveyed in Fig. 1. The drain current expressed can be rephrased as

$$I_D = \frac{\beta}{2}\left[\left(\frac{C_1 V_{bs} + C_2 V_{2s}}{C_T}\right) - V_{TH}\right]^2 \tag{4}$$

Now this equation can be again rewritten as

$$I_D = \frac{\beta}{2}\left(\frac{C_2}{C_T}\right)\left[V_{2s} + \left(\frac{C_1}{C_2}\right)V_{bs} - \frac{C_T}{C_2}V_{TH}\right]^2 \tag{5}$$

The above equation can be repositioned in terms of the effective threshold voltage $V_t eff$

$$V_{teff} = \left(\frac{C_T}{C_2}\right)\left[V_{TH} - \left(\frac{C_1}{C_T}\right)V_{bs}\right] \tag{6}$$

Where,

$$K_1 = \left(\frac{C_1}{C_T}\right) \tag{7}$$

and

$$K_2 = \left(\frac{C_2}{C_T}\right) \tag{8}$$

The Eqn. (6) clearly depicts Floating - Gate Mosfet's the effective threshold voltage demand. This is easily electrically regulated by varying the V_{bs} (bias voltage)and the proportions K_1 and K_2 ,where K_1 and K_2 are capacitances. [11]

B. Quasi-Floating Gate (QFG)

FGMOS has multiple inputs and one of the input terminal is supplied with bias Voltage via attaching a large capacitor, while safeguarding other inputs for the purpose of signal application. This causes lowering in effective threshold voltage . For threshold programmability , the large capacitance is required which ultimately causes many drawbacks like reduction in the effective Transconductance and Gain bandwidth product, degradation in frequency response of sequent circuit , requirement of silicon area also increases , problem of dc offset occurs due to trapping of large amount of charge during fabrication process. These shortcomings are controlled by little modifications in structure hence results in QFGMOS design.

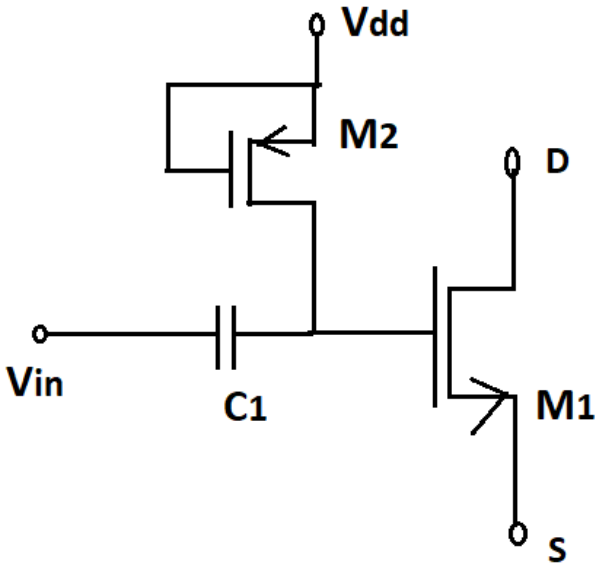

Fig. 3. QFGMOS Transistor symbol

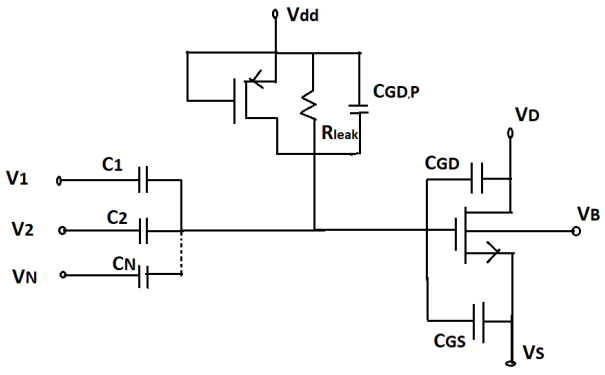

Fig. 4. QFGMOS Transistor equivalent circuit

Fig. 3 represents QFGMOS transistor and Fig. 4 its equivalent circuit. [12] V_{QFG} depicts the Voltage at Gate terminal of Quasi – floating Mosfet as displayed in the Fig. 4 is conveyed as :

$$\mathrm{V}_{QFG}(s) = \left(\frac{sR_{large}C_T}{1+sR_{large}C_T}\right)\left(\frac{\sum_{n=1}^{N} C_n V_n + C_{GS}V_S + C_{GD}V_D + C_{GB}V_B}{C_T}\right) \quad (9)$$

Where

$$C_T = \sum_{n=1}^{N} C_n + C_{GS} + C_{GD} + C_{GB} + C_{(GD,P)} \quad (10)$$

The nth input branch's coupling capacitance is denoted by C_n. C_{GS} is the Gate to Source capacitance , C_{GB} is Gate to Bulk capacitance , C_{GD} is Gate to Drain capacitance , and $C_{(GD,P)}$ is the Gate to Drain capacitance of P- channel Mosfet . The cut off frequency of a high pass filter f_o in transfer function form is depicted in the equation below

$$(f_o) = \frac{1}{2\pi R_{large}C_T} \quad (11)$$

The drain current (I_D) across QFGMOS is produced by applying V_1 voltage at the input terminal of one - input QFGMOS transistor is shown.The Equation for I_D in the Ohmic and Saturation section are described below as [12]:

$$I_D = \beta\left[\left\{\left(\frac{C_1}{C_T}V_1 + \frac{C_{GD,P}}{C_T}V_{DD} + \frac{C_{GD}}{C_T}V_{DS}\right) - V_{TH}\right\} - \frac{V_{DS}}{2}\right]V_{DS} \quad (12)$$

; For Ohmic

$$I_D = \frac{\beta}{2}\left[\left(\frac{C_1}{C_T}V_1 + \frac{C_{GD,P}}{C_T}V_{DD}\right) - V_{TH}\right]^2 = \frac{\beta}{2}{K_1}^2[V_1 - V_{T,eff}]^2 \quad (13)$$

; for Saturation where

$$V_{T,eff} = \frac{V_{TH} - K_2 V_{DD}}{K_1} \quad (14)$$

$$K_{1=}\frac{C_1}{C_T} \quad (15)$$

$$K_2 = \frac{C_{GD,P}}{C_T} \quad (16)$$

$V_{(T,eff)}$ is the Effective Threshold voltage. $V_{(T,eff)}$ has lower value as compared to simple or conventional MOSFET. Therefore its application lies in low voltage requirement .$g_{(m,eff)}$ depicts Effective Transconductance of Quasi – floating Mosfet and which is denoted by the subsequent expression.

$$g_{m,eff} = \left(\frac{C_1}{C_T}\right)g_m \quad (17)$$

where, gm is nothing but the Transconductance of N-channel Mosfet as perceived from quasi-floating gate Mosfet .

III. Proposed current mirror

Fig. 5 shows Conventional or Simple current mirror circuit [13].Where M_1 , M_2 Transistors are part of Simple Current Mirror. The V_{GS} ie. Gate to source voltage across the transistors M_1 and M_2 are akin to simple current mirror .M_3 is added hence local feedback is established due to which output resistance increases. The working principle of Wilson Current Mirror is formed on the Negative feedback concept.I_{in} is a constant current source which possess stable voltage which is further supplied to gate terminal of Transistor M_3.Due

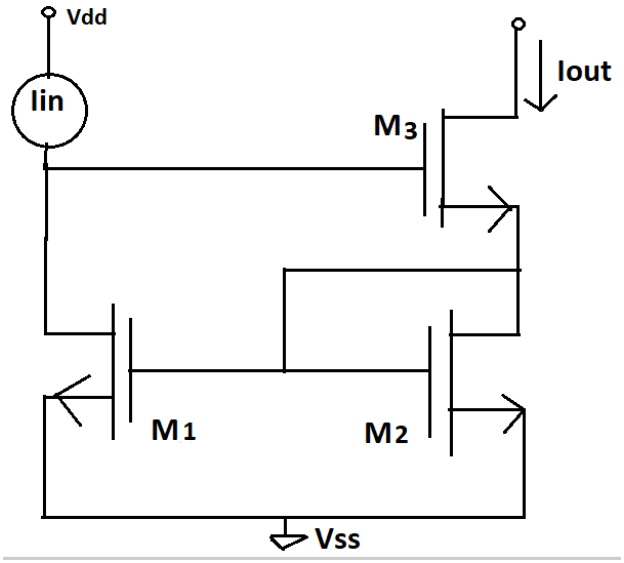

Fig. 5. Wilson Current mirror

to this voltage the drain current through M_3 starts flowing .Hence increase in V_{out} causes increase in I_{out} .Since the gate terminal of M_1 and M_2 transistor are connected with source of M_3 hence current through M_1 and M_2 starts increasing by following current mirror principal .The increase in current in M_1 is compensated as voltage across drain of M_1 drops hence causing reduction in gate voltage at M_3 . This ultimately forces drain current of M_3 to get reduced hence gets steady I_{out}. The FGMOS based circuit implementation of Wilson current mirror is presented in Fig. 6 [14].

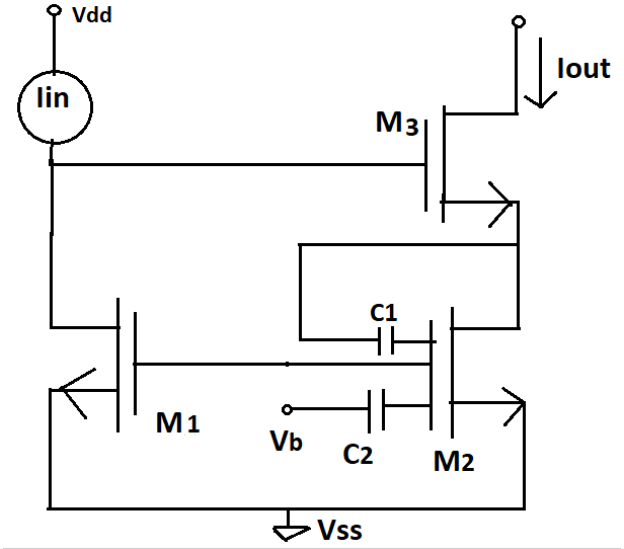

Fig. 6. FGMOS based WCM

The transistor M_2 which is in diode connecting manner is replaced by FGMOS transistor where V_b is the bias voltage whose fucntion is to provide conduction channel and another terminal is used as a normal input gate and is connected with drain of M_2 transistor. The QFGMOS based circuit implementation is shown in Fig. 7

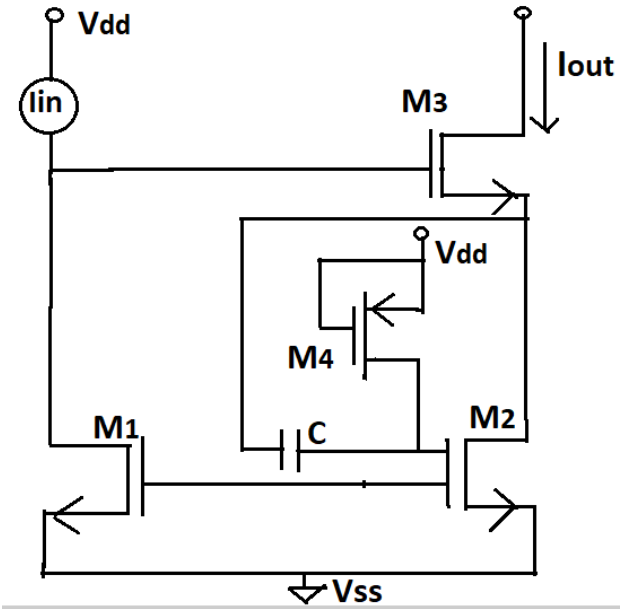

Fig. 7. QFGMOS based WCM

The transistor M_2 of simple Wilson current mirror is replaced by QFGMOS transistor .The Gate terminal of Mosfet M_2 is connected with Drain terminal of Mosfet M_2, while Source terminal of Pmos is connected with V_{dd} (Supply voltage).One of the input gates of transistor M_1 and M_2 are connected such that gate to source voltage of transistor M_1 becomes same as that gate to source voltage of transistor M_2.Wilson current mirror provides high output impedance thus results in improved efficiency of Current mirror.

IV. Simulation and Results

The Current Mirror circuits are displayed in Fig. 5, Fig. 6 Fig. 7 using PSPICE simulator by operating the TSMC 180nm CMOS Technology parameters file . The ±0.5 V as supply voltage has been applied for these simulation purpose . The W/L ratio of Mos transistors used for the designing of Wilson current mirror is in 100.The capacitors C1=C2= 100fF are used for FGMOS and for QFGMOS C=0.001fF. Fig. 8 Represents I_{out} Output current vs I_{in} Input current graph ,where I_{in} is varied from 0mA To 10mA range using I_{in} =10uA .The QFGMOS WCM shows better current linearity as compared to FGMOS and CM Wilson current mirror . Fig. 9 shows current gain characterstics with respect to frequency ,where frequency is varied from 1 hz to 30Ghz. QFGMOS WCM shows higher bandwidth than FGMOS WCM and simple WCM. as shown in Fig. 10 and Fig. 11 represents Input and Output impedance w.r.t frequency. All graphs have been simulated in Pspice simulator only.Comparative analysis of performance parameters of Wilson Current Mirror is shown in Table I

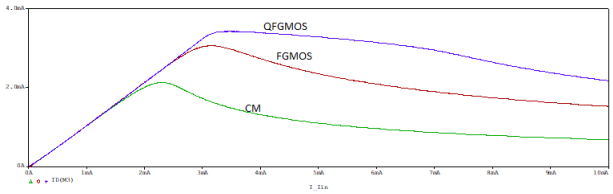

Fig. 8. Output current vs Input current

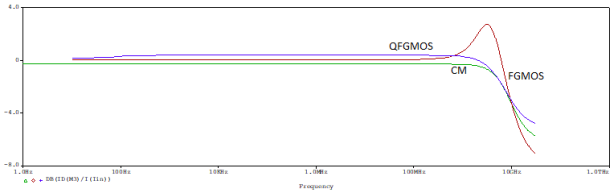

Fig. 9. Current Gain vs Frequency

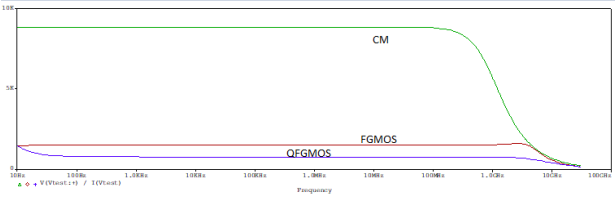

Fig. 10. Input Impedance vs Frequency

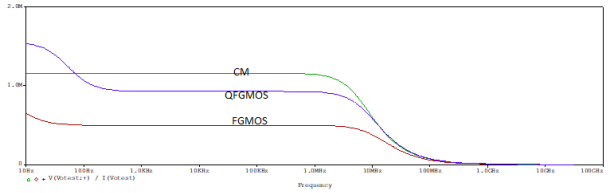

Fig. 11. Output Impedance vs Frequency

V. Conclusion

This paper presents a comparative analysis of the Low voltage and Low power design Techniques namely Floating Gate and Quasi Floating Gate . To verify the advantage and disadvantages of techniques, a Wilson current mirror is used. Among, the discussed approaches, the Quasi - Floating Gate being a low power technique shows much better performance as compared to others. The designs have been implemented using 180nm CMOS technology through PSpice simulator.

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TABLE I
Comparative analysis of performance parameters of Wilson Current Mirror

Technique for WCM	Rin(ohm)	Rout(ohm)	Bandwidth(Hz)
CM	8.85k	1.1M	9.3 G
FGMOS	1.49k	500k	9.8 G
QFGMOS	0.775k	927k	10.79 G

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