Germanium-Source Tunnel Field Effect Transistors with Record High I_{ON}/I_{OFF}

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Abstract

Tunnel field effect transistors (TFETs) with record high I_{ON}/I_{OFF} ratio (>10^6) for low-voltage (0.5V) operation are achieved by using germanium in the source region to achieve a small tunnel bandgap. The measured data are well explained by the theoretical band-to-band tunneling current model. Using the calibrated analytical model, the energy-delay performance of TFET-based technology is compared against that of conventional CMOS technology, at the 65nm node. The TFET is projected to provide dramatic improvement in energy efficiency for performance in the range up to ~0.5GHz.

Introduction

Increasing power density is a challenge for continued MOSFET scaling, due to non-scalability of the subthreshold swing (S) which limits the extent to which the MOSFET threshold voltage (V_T) and hence the supply voltage (V_{DD}) can be reduced, for a given performance target and optimal energy efficiency. To address this issue, alternative transistor designs which can achieve steeper switching behavior (S < 60 mV/dec at room temperature) than the MOSFET have been proposed and demonstrated. These include tunnel FETs (TFETs) [1,2,3] which operate with band-to-band tunneling current that changes with the channel potential more abruptly than thermionic emission current, at low current levels. Accordingly, the best TFETs reported to date show minimum S values <60 mV/dec. However, the average value of S is larger because the subthreshold swing increases as the device turns on, resulting in low ON/OFF current ratio (I_{ON}/I_{OFF} ~ 10^4 for 1V operation) [4]. I_{ON} can be improved by using a smaller-bandgap material such as $Si_{1-x}Ge_x$ [5,6]; however, experimental demonstrations to date have failed to show higher I_{ON}/I_{OFF} for low operating voltages (<1V) [7,8]. We present here a TFET design that utilizes a germanium source region to achieve a small tunnel bandgap and hence large I_{ON}/I_{OFF} ratio (>10^6) for 0.5V operation (**Fig. 1**). An advantage of this transistor design is that it is fully compatible with a standard CMOS fabrication process flow.

Device Fabrication

N-channel TFETs (parameters listed in **Table I**) were fabricated on lightly doped p-type silicon-on-insulator (SOI) wafers as follows. After thermal oxidation to thin the SOI layer down to 70 nm thickness, active areas were patterned using optical lithography and dry etching (**Fig. 2a**), and thermal oxidation was used to grow the gate oxide (3 nm SiO_2). N+ poly-Si gate and low-temperature-deposited oxide (LTO) gate-hard-mask layers, each 150 nm thick, were subsequently deposited and patterned. After the formation of ultra-narrow (8nm-wide) Si_3N_4 gate-sidewall spacers (**Fig. 2b**), masked ion implantation (1×10^{15} As^+/cm^2 @ 70keV, 0° tilt) followed by rapid thermal annealing (10s @ 1000°C in N_2) was used to dope the drain regions heavily n-type (**Fig. 2c**). **Fig. 3** shows a plan-view scanning electron micrograph of a TFET after the drain doping process was completed. Next, an LTO layer was deposited and patterned to selectively expose the source side of the TFETs, before a highly selective and isotropic dry etching process was used to recess the Si in the source regions by ~20nm, undercutting the gate electrode (**Fig. 2c**). Native oxide was then removed in dilute HF (10s in 100:1 H_2O:HF) and boron-doped polycrystalline Ge (poly-Ge) was selectively deposited at 425°C and 400mT in a hot-wall low-pressure chemical vapor deposition (LPCVD) reactor, using GeH_4 (15sccm) and 1%BCl_3 /99%He (35sccm) as the Ge and dopant source gases, respectively (**Fig. 2d**). The sheet resistance of the as-deposited poly-Ge layer was measured to be ~150kΩ/□, which suggests only moderate active dopant concentration (<$10^{18}$$cm^{-3}$). Another LTO (passivation) layer then was deposited (at 400°C) and openings were etched in the LTO to allow for direct probing of gate, source, and drain pads. Device fabrication was completed with a forming-gas anneal (30m @ 400°C) to improve SiO_2 interface properties.

Results and Discussion

Measured I_D-V_{GS} and I_D-V_{DS} characteristics are plotted in **Fig. 4** for a long-channel (5μm) TFET. S is seen to increase with I_D, as expected (**Fig. 5**). The minimum current ("leakage floor") is 0.1pA/μm and the drive current for a 0.5V gate-voltage swing is 0.4 μA/μm, for V_{DS} = 0.5V. The low threshold voltage (<0V) is likely due to a relatively large fixed charge density at the oxide/Ge interface. The drive current does not depend on gate length, as expected (**Fig. 6**). ON/OFF current ratios >10^6 are seen for gate lengths down to 0.4μm, below which the leakage floor increases due to short-channel effects.

Band-to-band tunneling theory predicts [9]

$$I_D = AE_s \exp\left[-\frac{\pi m^{*1/2} E_g^{3/2}}{2\sqrt{2} q\hbar E_s}\right] = AE_s \exp(-B/E_s)$$

where E_s is the vertical electric field at the semiconductor (Ge) surface in the gate-to-source overlap region where the tunneling occurs. A simple expression for E_s is $|V_{GS}+V_{tunnel}|/(4T_{ox})$ where qV_{tunnel} is the minimum energy-band bending needed for band-to-band tunneling to occur, 4 is the ratio of Ge permittivity to SiO_2 permittivity, and T_{ox} is the gate-oxide thickness over the source [10]. The best linear fit for $ln\ I_D/|V_{GS}+V_{tunnel}|$ *vs.* $1/|V_{GS}+V_{tunnel}|$ was found for a V_{tunnel} value of 0.595V (**Fig. 7**), indicating that the effective tunnel bandgap (E_g) is somewhat smaller than this value. This is reasonable, considering that the bandgap of monocrystalline Ge is 0.66eV [11] and that poly-Ge has a high density of defects with associated trap state energy level located ~0.1eV away from the valence-band edge [12], which would effectively lower the tunnel bandgap. Using E_g = 0.56eV and m^* = 0.06m_0 [11], T_{ox} is determined to be 1.9nm from the experimentally measured value of B (2.59 MV/cm, ref. **Fig. 7**).

The energy-delay performance of this TFET technology can be benchmarked against that of CMOS technology using the methodology described in [13]. Using the calibrated analytical model for I_D, with T_{ox} scaled down to 1nm, a comparison is made for the 65nm technology node in **Fig. 8**. The results indicate that this TFET technology offers substantial improvements in energy efficiency, so that it is attractive for low-power applications up to ~0.5GHz.

Conclusion

By employing Ge in the source of an n-channel TFET, record high I_{ON}/I_{OFF} ratio (>10^6) is achieved for low-voltage (0.5V) operation (ref. **Table II**). The TFET can be fabricated using established planar processing techniques, in a CMOS-compatible process flow. TFET I-V characteristics are well modeled by band-to-band tunneling current theory and appear promising for low-power applications over a wide range of performance (up to ~0.5GHz or higher with parallelism).

Acknowledgements

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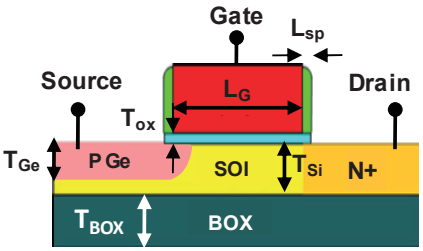

Fig 1: Schematic cross-sectional view of a germanium-source tunneling transistor.

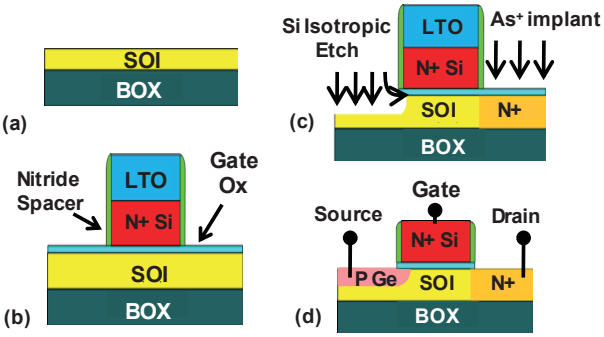

Fig. 2: Process flow used to fabricate TFETs in this work.

Parameter	Value
L_G	0.25-5μm
W	0.25-0.35μm
T_{ox}	3nm
T_{box}	200nm
T_{Si}	70nm
T_{Ge}	21nm
T_{sp}	8nm

Table I: TFET device parameters

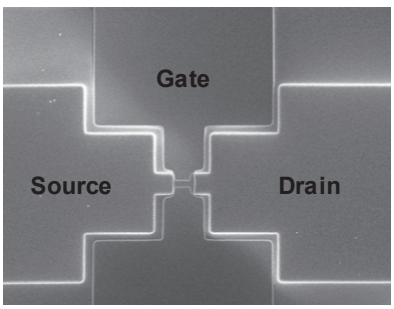

Fig. 3: Plan view scanning electron micrograph of a TFET before Ge source deposition.

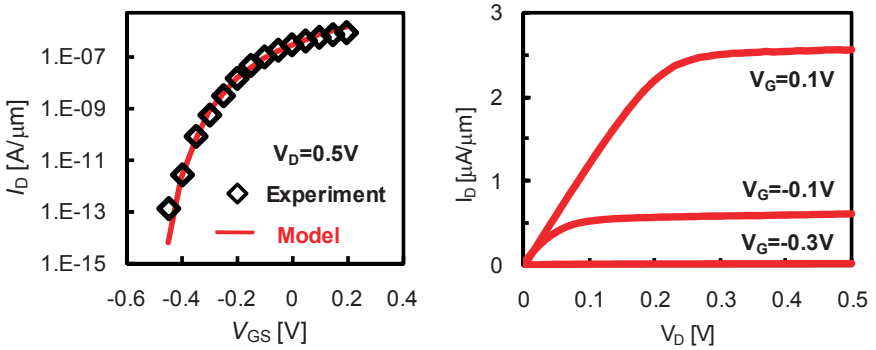

Fig. 4: (a) Measured I_D-V_{GS} and (b) I_D-V_{DS} characteristics for a long channel (5μm) TFET. The measured data show good agreement with the band-to-band tunneling analytic model.

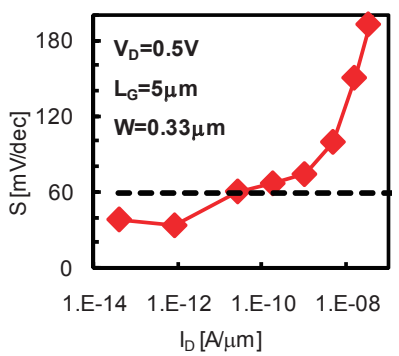

Fig. 5: S *vs.* I_D (from Fig. 4). S increases as I_D increases, as expected for a tunnel transistor.

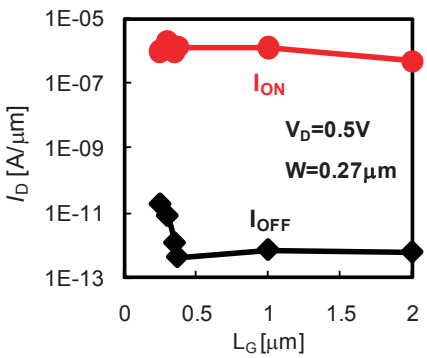

Fig. 6: Measured TFET I_{ON} and I_{OFF} *vs.* L_G. I_{OFF} corresponds to the minimum I_D; I_{ON} corresponds to I_D for 0.5V gate voltage swing.

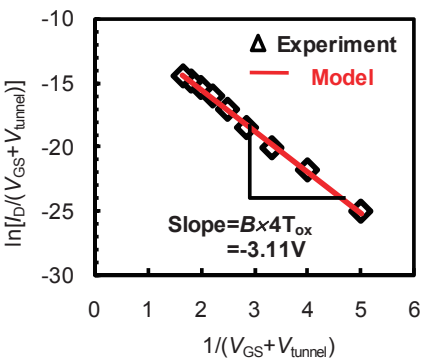

Fig. 7: $ln|I_D/(V_{GS}+V_{tunnel})|$ *vs.* $1/(V_{GS}+V_{tunnel})$ with V_{tunnel}=0.595V, for the TFET of Fig. 4. The tunneling model exponential factor B is extracted to be 2.59MV/cm.

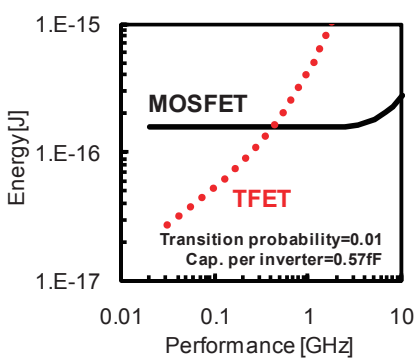

Fig. 8: Simulated Energy-Performance comparison of the MOSFET *vs.* TFET, for a 30-stage FO4 inverter chain. Device parameters are taken from the ITRS, for the 65nm LSTP technology node.

	Ref. [4]	Ref. [7]	Ref. [8]	This Work
Structure	**Si TFET**	**SiGe TFET**	**s-Ge TFET**	**Ge TFET**
T_{ox}(nm)	2(SiO_2)	3(HfO_2)	20(LTO)	3(SiO_2)
L_G(nm)	70	100	1000	5000
@ V_D (V)	1	1.2	0.5	0.5
I_{ON}(μA/μm)	12.1	0.009	0.001	0.42
I_{OFF}(pA/μm)	5400	8	0.3	0.12
I_{ON}/I_{OFF} for V_{DD}=0.5V	6E3	3E3	4E4	3E6

Table II: TFET performance comparison.

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