Performance Comparison of Full Adder Cells in 45nm Technology Node

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***Abstract*—Full Adder (FA) being an integral part of Arithmetic Logic Unit (ALU) of modern integrated circuits (IC) has gained massive research interest by academicians and industrial IC designers. Therefore, a large number of FA cell designs have been innovated, each of them having their respective pros and cons. As a result, it becomes quite necessary to examine the FA cells under a common environment in order to compare their performance parameters which will facilitate IC designers to choose the right FA topology required by the nature of ALU. This paper presents a comparison among 23 different FA cells. Performance comparison of the FAs has been conducted using Cadence design toolkits. The technology node used for the performance analysis and comparison is 45nm.**

Keywords—full adder, 1-bit adder, hybrid adder.

I. INTRODUCTION

VLSI designs which have high degree of efficiency and performance parameters play an important role since modern day electrical and electronic gadgets demand quick calculation utilizing the lowest amount of power [1-7]. FAs are vital part in arithmetic system of advanced ICs. Therefore, FAs design plays a vital role in circuit design of arithmetic systems. As a result, contrasting sorts of FA cells are created throughout the last decade, each bearing some positive and negative sides [8-14].

As there is a large number of FA designs developed by researchers and VLSI designers, it is quite important to simulate, analyze and compare the designs using the same simulation environment which will enable IC designers to pick up the most efficient FA topology required as per system specification [15]. Comparison of FAs conducted in [16] only focused on XOR-XNOR FA designs. However, many other methodologies of FA implementation are required to be analyzed. Comparison of FAs in [17-18] conducted a comparative analysis among FA cells containing various logic methods. However, analysis has been done on 4 FA designs I case of [17]. I case of [18], analysis has been conducted only on 5 FAs. Comparison among FAs done in [19-20] illustrate a large range of FA analysis. However, in ref. [19], technology node has been set to CMOS 180 nm. In case of [20], technology utilized was CMOS 90nm technology. However, Both 180nm and 90nm CMOS processes are considered as outdated. As a result, it is quite important to simulate the circuits in latest available technology node.

This paper introduces a relative investigation on existing FAs utilizing Cadence CAD apparatuses. Favorable sides and downsides of the FA cells are clearly indicated to have a straightforward review on different sorts of full adders.

II. VARIOUS FULL ADDER CELLS

Beginning time of VLSI configuration utilized Pass Transistor Logic (PTL) which utilizes just n-channel CMOS (nMOS) to execute FA cells [21]. PTL FA is quite better in terms of voltage swing. However, it only employs n-channel CMOS transistor (nMOS) which can provide strong logic 0 but unable to provide strong logic 1. Therefore, on account of high power and transistor count, PTL was supplanted by Static CMOS (S-CMOS) logic. S-CMOS utilizes a complementary network of both p-channel and n-channel CMOS (pMOS and nMOS) [22]. FA in [23] employs only 12 transistors. However, the design suffers from threshold voltage drop issue. These 3 FAs in [21-23] falls under conventional domain which only utilizes singe logic style

Transmission Gate FA (TGA) and Transmission Function FA (TFA) came later which use less PMOS and NMOS contrasted with the conventional PTL and S-CMOS strategy [24,25]. While TGA and TFA FA don't experience the effects of voltage degradation, poor capacity of driving is a significant issue in case of TGA and TFA.

FA cells utilizing 16 transistors (16-T) [26], 14 transistors (14- T) [27] and 24 transistors (10-T) [28] likewise utilize different logic styles in order to execute FA function. 24-T FA utilizes a 3 input based XOR logic circuit for computation as opposed to using two separate 2 input XOR gates in series used in conventional designs. In case of 14-T and 10-T adder designs, inputs are passed to XOR gate. As an intermediate block, the XOR gate performs the necessary signals for carry and sum generation. Very low transistors of adders in [23, 27] represents less surface region. But driving ability is a significant concern which restricts their application in high fan-out cases.

Hybrid Pass Static CMOS (HPSC) FA in [29] and New HPSC FA (N-HPSC) utilizes hybrid logic style too. HPSC

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uses PTL to create XOR and XNOR functions. The outermost side comprises of S-CMOS technique. This provides full-swing signals. Double Pass Transistor Logic (DPL) and Swing Restored CPL (SRCPL) Hybrid FAs in [31] produce AND and OR signal to process carry-bit. On the other hand, XOR-XNOR signals are used for sum. Carry input signal is utilized as the select bit of Transmission Gate multiplexers (MUX) in order to deliver output signals obtained from the outputs AND-OR and XOR-XNOR functions.

In view of Gate Diffusion Input (GDI) method, 3 FA structures (denoted as GDI 1, 2, 3) have been designed in [32]. Serious issue related with GDI adders is its degradation of signal. Weak driving capacity is another issue associated with this sort of design methodology. More hybrid FA designs are mentioned in [33-40]. Although FA in [39] used GDI method, the design is not subjected to decline of voltage unlike other GDI based designs due to intelligent combination of GDI and S-CMOS logic. GDI gates are placed for receiving the input and processing the input signals. S-CMOS logic is placed on the output terminals which provide full-swing output voltage levels to the design. Hence, two major problems of GDI design: voltage degradation and low driving power have been solved in this design by smart combination of GDI method and S-CMOS logic. FA in [38] used a combination of TG, S-CMOS and PTL logic.

III. Simulation Result

The FAs mentioned in section II were constructed using Cadence CAD tools. The technology node used was 45 nm. The supply voltage was fixed to 1.0 V. Post-layout simulation has been conducted on the FAs. The results are mentioned in Table I. in addition, transistor count of the individual FA is added in Table I. To have a clear view on the comparison, obtained results are also represented graphically using Fig. 1-3.

FA in [40], known as 10-T FA could not operate properly in the target technology node (45 nm). Therefore, details on performance parameters were not available in Table I [41-50].

IV. Comparative Performance Analysis

Detailed analysis based on simulation results on power, delay and PDP obtained using Cadence has been stated in the following sub-sections.

A. Average Power Comparison:

As per simulation data in Table I and Fig. 1, least power consumption has been achieved by Hybrid 5 FA in [36]. Power consumption of Hybrid FA in [34] was pretty much close to Hybrid 5. Hybrid 7 FA obtained 3rd position in case of power consumption among the FAs listed in Table I.

PTL FA in [21] has very high-power dissipation for which its usage has been highly limited in modern VLSI systems. S-CMOS FA in [22] obtained quite satisfactory performance in case of power dissipation in spite of being one of the oldest FA designs. Although 12-T and 14-T FA in [23, 27] have very low Transistor count (TC), they have high power consumption due to threshold voltage drop issue. Performance of TGA [24], TFA [25], 16-T [26], GDI FA designs [32], Hybrid 1 [33], Hybrid 2 [33], Hybrid 4 [35] and Hybrid 8 FA in [39] were also satisfactory.

B. Propagation Delay:

In case of propagation delay, Hybrid 7 FA in [38] obtained best performance. Hybrid 8 FA in [39] and GDI 2 in [32] are close behind Hybrid 7.

Performance of PTL FA in [21] for propagation delay is quite satisfactory is spite of having very high-power dissipation. S-CMOS FA, which is the most common FA topology has moderated performance compared to the others.

C. PDP:

Hybrid 7 FA in [38] obtained best performance in terms of PDP. GDI 1 in [32], Hybrid 3 in [34] and Hybrid 8 in [39] are close behind Hybrid 7 FA.

PTL FA in [21] has very high PDP dui to its excessive power consumption be in spite of having good performance in delay. S-CMOS in [22], 16-T in [26], GDI 1 and GDI 2 in [32] has satisfactory performance parameters in case of PDP.

TABLE I
FULL ADDER CELLS PERFORMANCE COMPARISON

FA	Ref. no.	TC	Power (uW)	Delay (ns)	PDP (aJ)
PTL	[21]	32	2.75	53.15	146.16
S-CMOS	[22]	28	1.14	64.3	73.3
12-T	[23]	12	1.89	113.6	214.7
TGA	[24]	20	1.01	81	81.81
TFA	[25]	16	0.97	88.2	85.55
16-T	[26]	16	0.92	56.2	51.7
14-T	[27]	14	1.72	105.8	181.98
24-T	[28]	24	1.18	82.65	97.53
HPSC	[29]	22	1.4	54.6	76.44
New-HPSC	[30]	24	1.35	105.7	142.69
SR-CLP	[31]	20	1.26	74.2	93.49
DPL	[31]	22	1.31	60.95	79.84
GDI 1	[32]	18	0.78	47.1	36.74
GDI 2	[32]	22	1.01	42.8	43.23
GDI 3	[32]	21	0.96	53.9	51.74
Hybrid 1	[33]	23	0.87	50.75	44.15
Hybrid 2	[33]	21	0.93	60.85	56.59
Hybrid 3	[34]	16	0.7	52.2	36.54
Hybrid 4	[35]	22	1.09	66	71.94
Hybrid 5	[36]	16	***0.64***	98.7	63.17
Hybrid 6	[37]	24	1.48	79.15	117.14
Hybrid 7	[38]	22	0.83	***38.7***	***32.12***
Hybrid 8	[39]	24	1.03	41.02	42.25

V. Conclusion

A comparative analysis based on various performance parameters of existing FA cells has been conducted in this paper. All the FA cells were simulated using a common environment. Cadence CAD tools were used for simulation and performance evaluation of the FA cells. In case of power, FA in [36] designed by Bhattacharyya et al. achieved best performance. Best performance in delay and PDP has been obtained by FA in [38] designed by Hasan et al. Compared to the previous published papers, this paper presents comparison among a wide range of FA cells. In addition, simulation have been conducted in 45 nm technology node whereas the existing papers conducted simulations in 90 nm technology or above. Hence, the information provided in this paper will enable researchers and VLSI designers to earn a good knowledge on existing FA cells and their respective performance parameters.

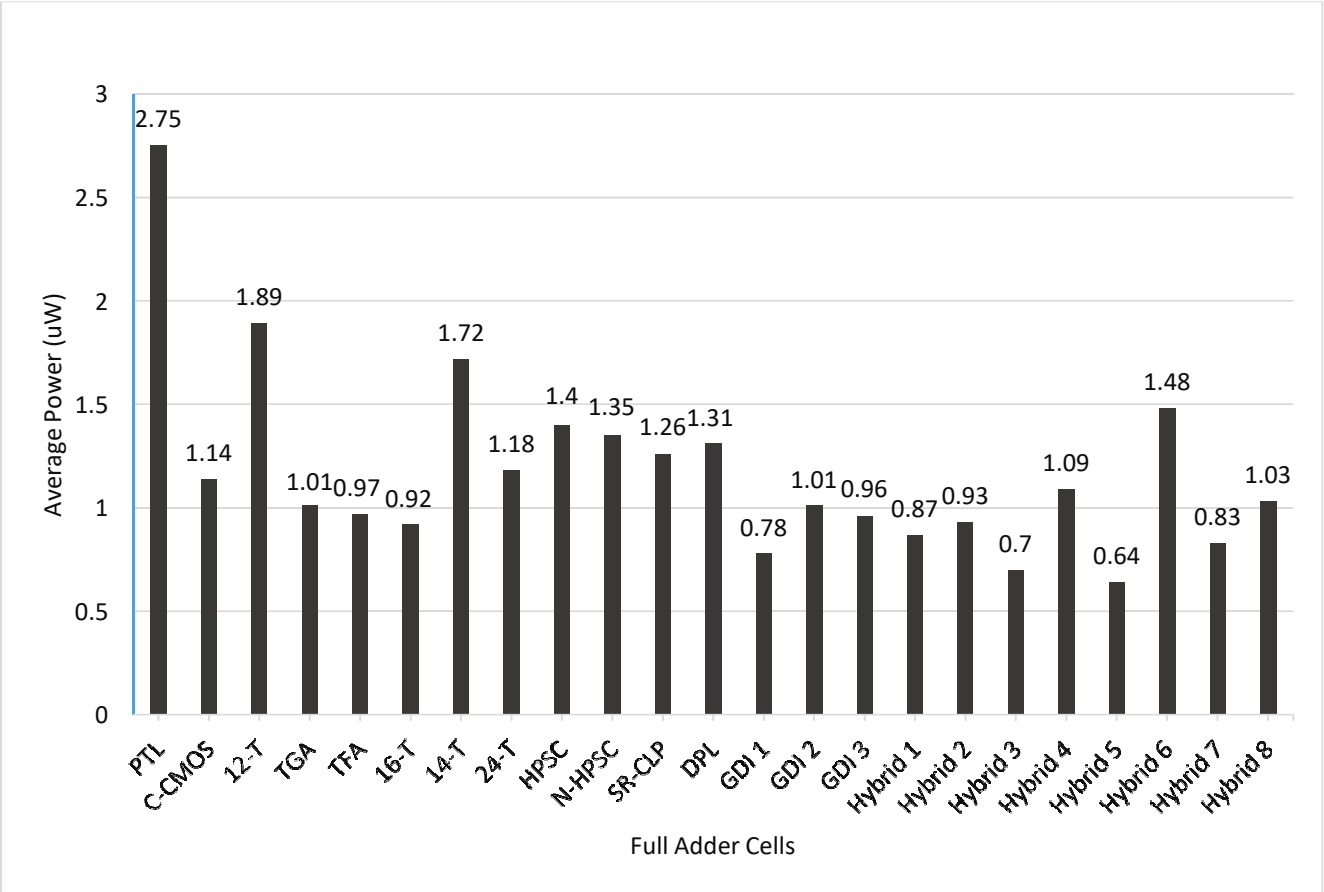

Fig. 1. Power consumption of FA cells.

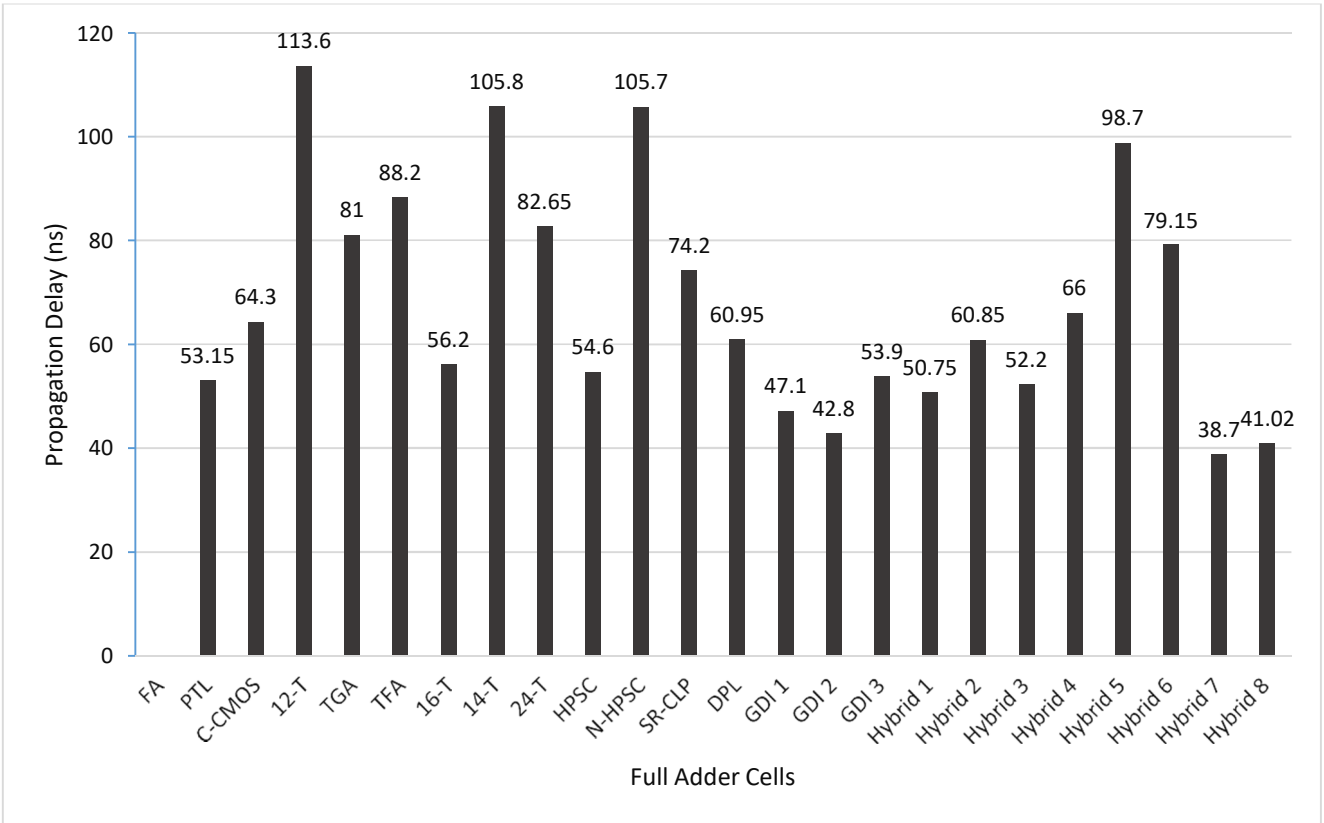

Fig. 2. Delay of FA cells.

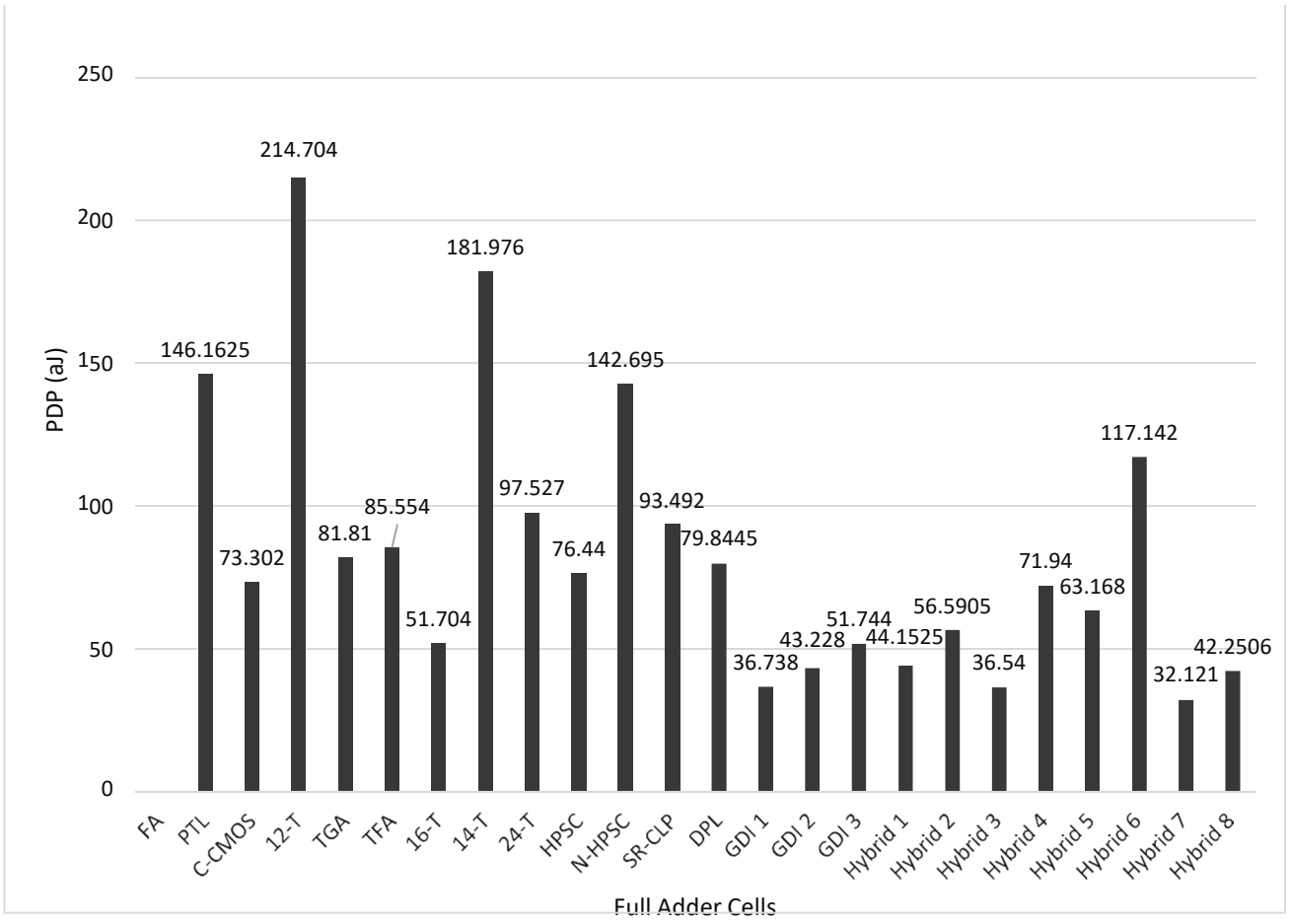

Fig. 3. PDP of FA cells.

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