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ORIGINAL PAPER

TFET performance optimization using gate work function engineering

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Abstract: This work presents main electrical characteristics improvement in a nanoscale tunnel field-effect transistor (TFET) with 50 nm channel length, applying work function engineering techniques. Three different metal gate materials with dedicated work functions are utilized to optimize the TFET performance. By gate work function and length optimization, the main parameters of $I_{on} = 5\times10^{-5}$ A/μm, $I_{off} = 2.5 \times 10^{-15}$ A/μm, $I_{amb} = 3\times10^{-7}$ A/μm, and subthreshold swing = 51.01 mV/decade are obtained in accordance with tunneling barrier shape at source/channel and drain/channel tunnel junctions. The work function engineering techniques, presented in the current work, results in 1.22 times improvement in I_{ON} and 0.99 times improvement in I_{OFF}.

Keywords: TFET; Work function engineering; Planar triple metal gate

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1. Introduction

Tunnel field-effect transistors (TFETs) are highly considered in nanoscale electronics circuits due to low power consumption [1, 2]. TFETs have the ability to work in lower bias voltages [1]. According to the switching energy diagram [3, 4], by scaling the supply voltage, the energy needed for switching will reduce in logic operations [1]. TFET operation is based on band-to-band tunneling mechanism for carrier injection instead of conventional MOSFETs (metal-oxide-semiconductor field-effect transistors) where the thermionic emission of carriers is dominant [1]. TFETs are more preferable in comparison with conventional MOSFETs due to higher speed, lower power dissipation, reduced short channel effects, and higher I_{ON}/I_{OFF} current ratio [5]. Nowadays, MOSFETs need at least 60 mV of the gate voltage to increase one decade of on-state current at room temperature [1–6]. However using TFETs, the subthreshold swing is decreased due to utilizing different carrier injection mechanisms. The subthreshold swing (SS) also defines as the amount of needed gate voltage to alter one decade of drain current measured in mV/decade unit as [2]:

$$\mathrm{SS} = \frac{\mathrm{d}V_G}{\mathrm{d}(\log I_D)}\,[\mathrm{mV/dec}] \tag{1}$$

In addition to TFET, impact ionization MOS (I-MOS) also shows superior subthreshold swing of about 5 mV/dec [6], although I-MOS works in high operating voltages in comparison with conventional CMOS transistors. The low OFF-state current and low supply voltage of TFETs are beneficial in comparison with I-MOS [6].

The two main shortcomings of TFETs are low ON-state current (I_{ON}) and ambipolar current (I_{amb}) [7], where I_{amb} exists according to tunneling occurrence at drain/channel junction in negative gate voltages.

Several solutions are investigated to overcome the mentioned shortcomings. Some researchers have proposed using heterojunctions and III–V semiconductors in source/channel region, to increase the ON-state current of TFETs [8], since heterojunctions reduce tunneling distance and lead to carrier tunneling. Furthermore, the use of high-k dielectric near the source can improve I_{ON} and SS and placing low-k dielectric in the drain vicinity can reduce ambipolar behavior of TFET [9]. In addition, the modification in parameters is focused on controlling the coupling between the gate and tunnel junction at the source/drain side [9].

Work function tuning of metal gate is crucial for adjusting the threshold voltage (V_T) [10]. Different processes are introduced to alter the metal work function such

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as ion implantation usage to change the work function of thin metal films (for example nitrogen ions are used to reduce the Molybdenum work function) [11]. Moreover, changing the annealing temperature can also vary the work function of metal films [11]. It is demonstrated that by arranging a suitable composition of low and high work function metals, the work function of metal alloys can be tuned from 4.16 to 5.05 eV [12]. Furthermore, the two metals stacking can result in metal work function tuning [10].

In this work, enhancing the performance of a TFET structure with work function engineering is demonstrated. The TFET topology which is utilized in this paper is named as planar triple metal gate TFET or PTMG-TFET since the gate consists of three different segments. By choosing appropriate metal work function quantities for each segment, and optimizing the corresponding length, the main electrical parameters of TFET are improved. The optimization approach of the present work is similar to [13].

2. Device topology

Figure 1 shows a *n*-type TFET cross section reported in [14], which is simulated as the basic element of the current work. In this TFET structure, by applying a positive gate voltage, the channel energy bands move downward in energy diagram, so more band bending takes place in the conduction band of channel and source valence band at source/channel junction. In the mentioned condition, electrons can tunnel from the valence band of the source to channel conduction band and then diffuse to the drain side and finally collected by drain electrode. SiO_2-only, HfO_2-only, and the combination of SiO_2 and HfO_2 (hetero-gate-dielectric TFET) have been used as gate dielectric in [14] TFETs.

HfO_2 is considered as gate dielectric material in this paper. The TFET structure characteristics are verified using a commercially available device simulator [15]. Figure 2 demonstrates the effectiveness of the simulation setup in verifying the results of [14]. According to Fig. 2, the TFET

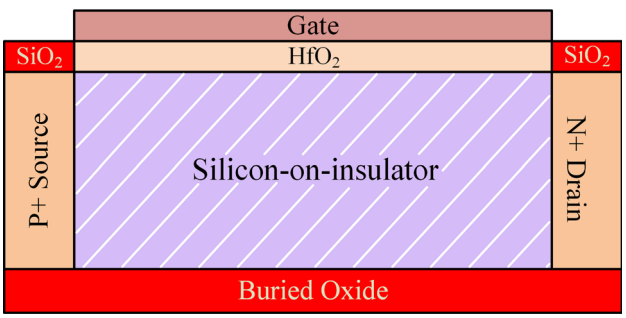


Fig. 1 Regenerated TFET cross section

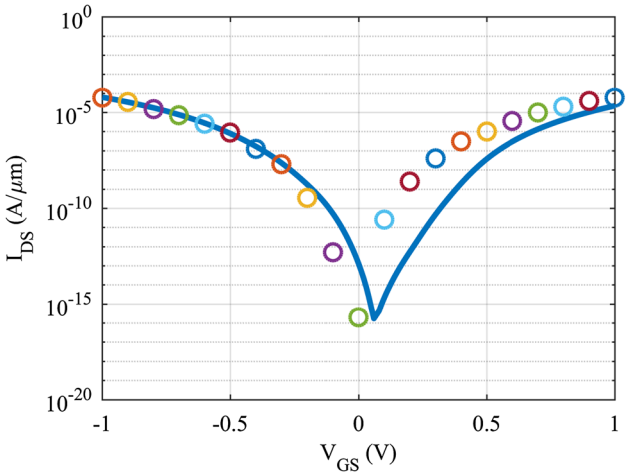


Fig. 2 I_{DS}–V_{GS} verification curve. Circles in this figure are the [14] results, and solid line is the result of regenerated TFET in this work

in [14] suffers from severe ambipolar behavior. In the referenced TFET structure, the value of metal gate work function was 4.37 eV [14]. The mentioned TFET structure characteristics are enhanced by work function engineering in the current work. In this work, the range of work function variation is chosen to be in consistence with the reported work function of [10, 13, 16]. In addition, it has been described that by stacking platinum (Pt) and titanium (Ti) (metal bilayer) as gate metal on HfO_2 dielectric and changing the bottom layer thickness the metal gate work function can change from 3.8 to 4.8 eV continuously [10].

SS is calculated from where the drain current starts to increase to the threshold voltage in the I_{DS}–V_{GS} curve of TFET [17]. Furthermore, the ambipolar current (I_{amb}) and OFF-state current (I_{OFF}) are considered as the drain current (I_{DS}) at $V_{GS} = -1$ V and $V_{GS} = 0$ V, respectively, in this work.

3. Results and discussion

Three separate different sections for the metal gate with various work functions are considered in this paper. One part is placed for controlling the source/channel junction, the other is placed for controlling channel/drain junction, and the middle part is considered for isolating the two mentioned parts. The metal work function near the source is considered as ϕ_1 with the length of L_1, the middle part metal work function is considered as ϕ_2 with the length of L_2, and the metal work function in the drain vicinity is considered as ϕ_3 with the length of L_3 (Fig. 3).

I_{on} of TFET has a direct relation to the tunneling probability [1]. In other words, higher tunneling probability can translate to higher I_{ON}. Due to WKB approximation,

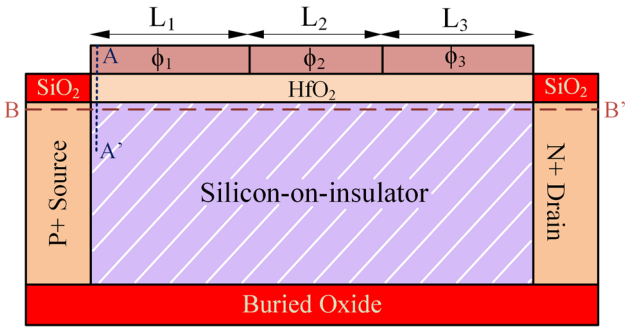


Fig. 3 Planar triple metal gate structure or PTMG-TFET

the band-to-band tunneling probability is determined as [1, 18]:

$$T_{\mathrm{WKB}} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar(E_g+\Delta\phi)}\right) \quad (2)$$

λ is tunneling barrier width or screening tunneling length, m^* is the carrier effective mass in the semiconductor, E_g is the semiconductor bandgap at tunnel junction, $\Delta\phi$ is tunneling window (the energy range which tunneling can occur), q is the electron charge, and $\hbar$ is the reduced Planck's constant in the abovementioned equation. Equation (2) suggests that reducing m^*, E_g, and λ and increasing of $\Delta\phi$ can increase the tunneling probability. In an ideal condition for the maximum tunneling, the tunneling probability (T) should be equal to unity [1].

In the first step of optimization, the values of ϕ_2 and ϕ_3 are considered to be constant and ϕ_1 is varied. The I_{DS}–V_{GS} characteristics and bands diagram (BB′ cutline emphasized in Fig. 3) are shown in Fig. 4. Figure 5 also shows the AA′ cutline emphasized in Fig. 3, (near source/channel tunnel junction) for different values of ϕ_1. According to Fig. 5 with decreasing ϕ_1, more band bending occurs because of higher difference between metal work function and semiconductor work function (higher surface potential (Ψ_s)). Higher band bending can be translated to lower λ and the higher $\Delta\phi$ (tunneling window) which is due to higher band bending of channel conduction band and the valence band of the source. So, in the case of ϕ_1 = 3.8 eV, the highest I_{ON} and according to bands diagram most band bending (lowest λ and highest $\Delta\phi$) is obtained, although resulting in more I_{OFF} simultaneously as shown in Fig. 4. By choosing ϕ_1 as 4.2 eV, in addition to the increment of I_{ON}, some other parameters such as I_{OFF} and SS will decrease. Hence, considering ϕ_1 = 4.2 eV is a suitable choice for the optimization process.

In the second step of optimization process, the values of ϕ_1 and ϕ_3 are considered to be fixed and ϕ_2 changes. Because of the distance between ϕ_2 borders to the entrance of source/drain to the channel, changing ϕ_2 does not have

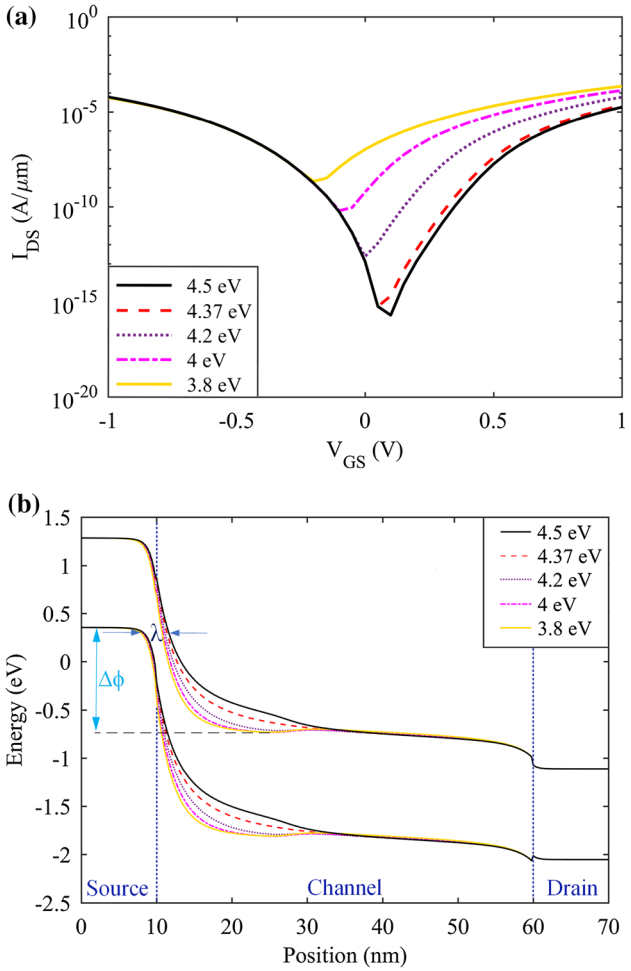


Fig. 4 I_{DS}–V_{GS} characteristic (**a**) and energy band diagrams at BB′ cutline which is illustrated in Fig. 3 (**b**) for fixed values of ϕ_2 and ϕ_3 ($\phi_2 = \phi_3$ = 4.37 eV) with different values of ϕ_1 ($V_{DS} = V_{GS} = +1$ V)

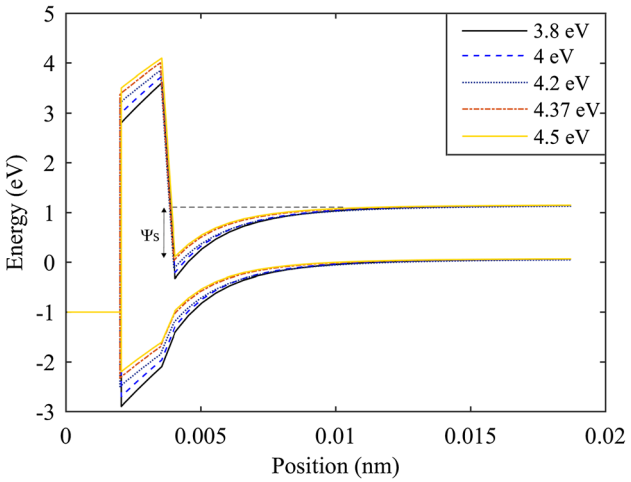


Fig. 5 Conduction and valence bands at AA′ cutline which is illustrated in Fig. 3 for different values of ϕ_1 at $V_{GS} = +1$ V

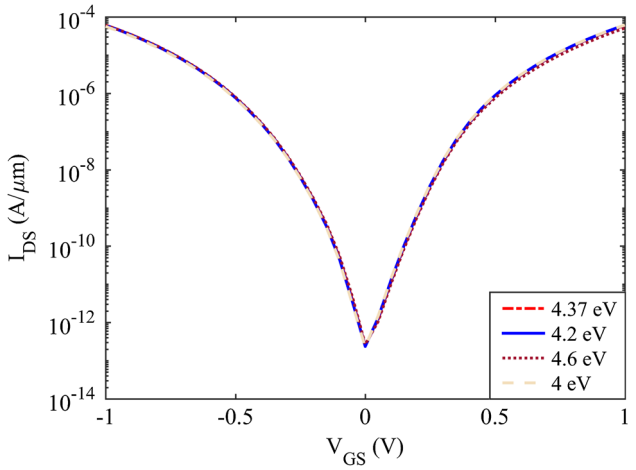


Fig. 6 I_{DS}–V_{GS} characteristic for variation of ϕ_2 for fixed values of ϕ_1 and ϕ_3 (ϕ_1 = 4.2 eV, ϕ_3 = 4.37 eV)

considerable effect for TFET tunneling process. Hence in this condition, ϕ_2 = 4.37 eV is regarded as the initial gate metal work function value (Fig. 6).

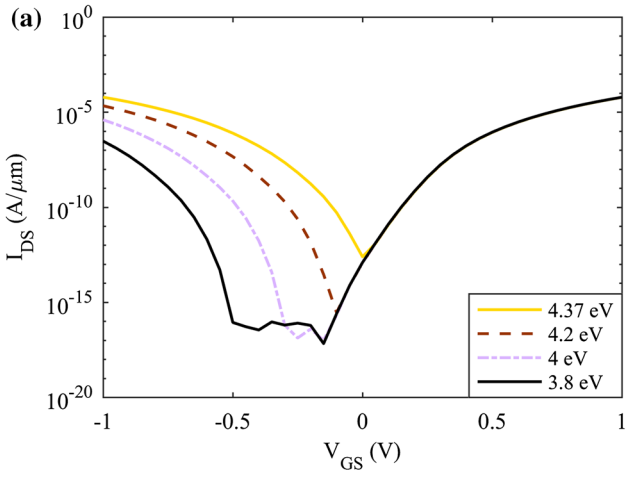
In the third step of optimization process, ϕ_1 and ϕ_2 are considered to be fixed and ϕ_3 changes. λ' is tunneling barrier width and $\Delta\phi'$ is tunneling window at drain/channel junction. In this condition, by decreasing the work function near the drain (ϕ_3) higher λ' and lower $\Delta\phi'$ is obtained. Hence according to Eq. (2), lower tunneling occurs at drain/channel junction which can be translated as lower ambipolar current. According to Fig. 7 for ϕ_3 = 3.8 eV, the lowest I_{OFF} and lowest I_{amb} are obtained.

Ultimately, the optimized values of work function are obtained as ϕ_1 = 4.2 eV, ϕ_2 = 4.37 eV, and ϕ_3 = 3.8 eV. In the mentioned optimization, the initial lengths of ϕ_1, ϕ_2, and ϕ_3 are considered to be 17, 16, and 17 nm, respectively.

In addition, in order to obtain maximum enhancement in the TFET performance, each metal gate length should be optimized. As explained before, the length of each metal parts ϕ_1, ϕ_2, and ϕ_3 are defined as L_1, L_2, and L_3, respectively. In the first step of optimization, L_3 is fixed at 17 nm and L_1 and L_2 are changed. By modifying L_1 and L_2, the I_{ON} and I_{amb} do not change though the SS_{avg} and I_{OFF} change and have a minimum value at L_1 = 5 nm as shown in Fig. 8(a). Hence, the fixed value of L_1 = 5 nm is utilized.

In the second step of optimization, L_2 and L_3 change for the fixed value of L_1 = 5 nm. As shown in Fig. 8(b) as L_2 = 31 nm and L_3 = 14 nm, the minimum average sub-threshold swing and I_{amb} is obtained. In this optimization step, I_{ON} and I_{OFF} have the fixed value and do not change considerably.

In conclusion, the optimized values for length are obtained as L_1 = 5 nm, L_2 = 31 nm, and L_3 = 14 nm. In



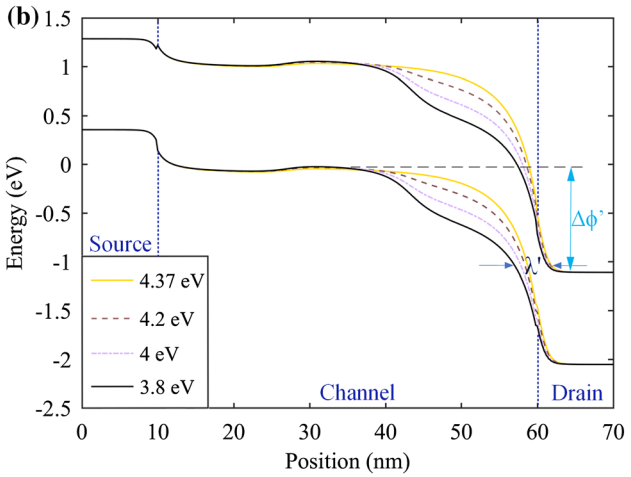


Fig. 7 I_{DS}–V_{GS} characteristic (**a**) and energy band diagrams at BB′ cutline which is illustrated in Fig. 3 (**b**) for fixed values of ϕ_1 and ϕ_2 (ϕ_1 = 4.2 eV, ϕ_2 = 4.37 eV) with different values of ϕ_3 (V_{GS} = − 1 V, V_{DS} = + 1 V)

Fig. 9, the difference between the I_{DS}–V_{GS} behavior of PTMG-TFET and regenerated TFET can be observed. Figure 9 shows that ambipolarity is suppressed completely in the range of − 0.5 V < V_{GS} < 0 V and also ambipolar current is reduced in the range of − 1 V < V_{GS} < − 0.5 V in PTMG-TFET. In addition, the PTMG-TFET has higher I_{ON} and lower I_{OFF} in comparison with the regenerated TFET. Furthermore, Table 1 shows numerical comparison of some of the main electrical parameters of PTMG-TFET with regenerated TFET and other TFETs topologies.

The gate dielectric of HG TFET consists of two different material where the high-k material near the source helps to increase the coupling between gate and tunneling junction at source side (improved I_{ON} and SS) and the presence of low-k material near the drain side reduces the coupling between the gate and tunnel junction at drain side (reduced ambipolar current) [14]. Overlapping gate on drain is an effective way to suppress ambipolar behavior in TFET

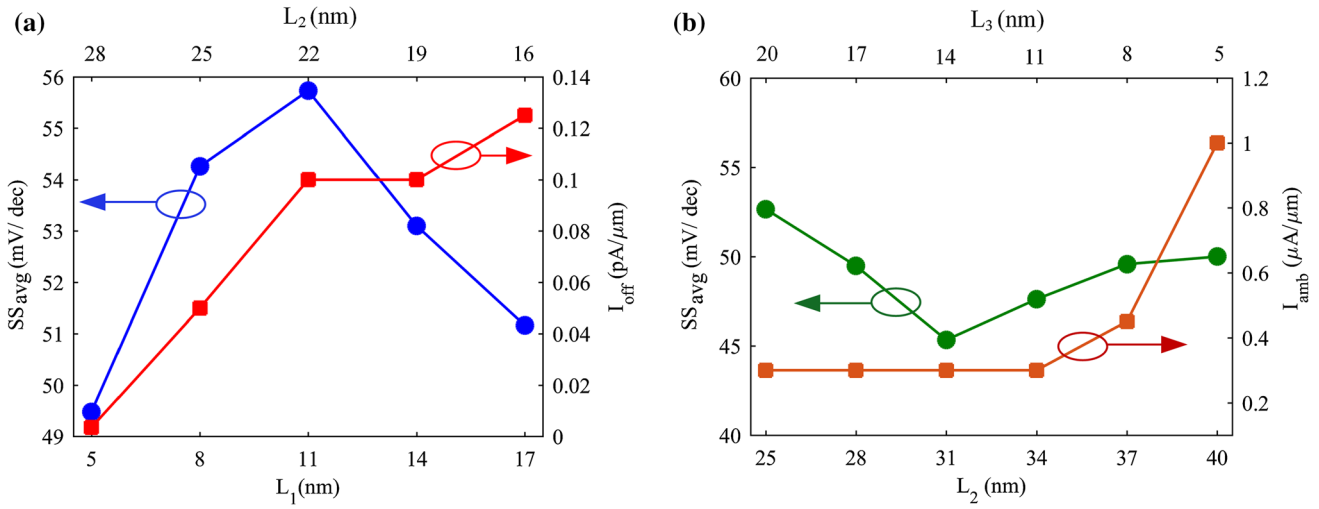


Fig. 8 (**a**) Average subthreshold swing and off-state current versus L_1 and L_2 for fixed value of L_3 = 17 nm. (**b**) Average subthreshold swing and ambipolar current versus L_2 and L_3 for fixed value of L_1 = 5 nm

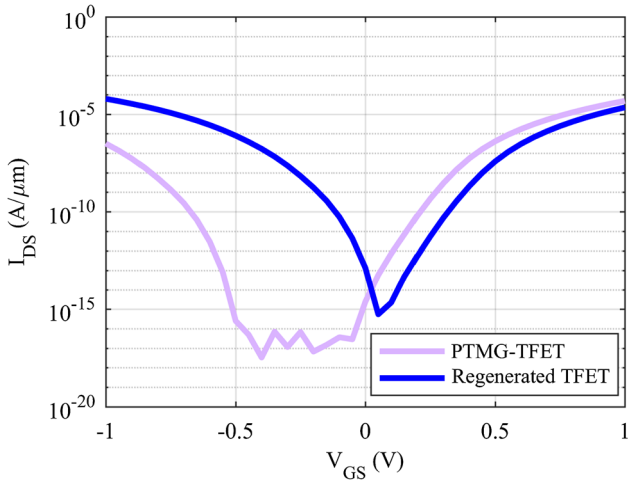


Fig. 9 Comparing the I_{DS}–V_{GS} curves of PTMG-TFET and regenerated TFET

[19]. HDB PNPN TFET or hetero-dielectric BOX (buried oxide) PNPN TFET is designed to reduce ambipolar behavior that uses SiO_2 and HfO_2 above a highly doped ground plane. The BOX (buried oxide) thickness is 25 nm [20]. P-i-n TFET is also a double-gate TFET in which the drain doping is optimized in order to improve the functionality [21].

4. Conclusion

This paper presents a PTMG-TFET with its operation which is a variation of TFET, optimized according to different metal work functions. By changing the work function value of each of the three parts and the corresponding lengths, the main parameters of I_{ON}, I_{OFF} I_{amb}, and SS are optimized. Enhanced I_{ON} and a significant reduction in I_{OFF}

Table 1 Numerical comparison of PTMG-TFET with regenerated TFET and other TFET topologies

	I_{ON} (A/μm)	I_{OFF} (A/μm) (@ V_{GS} = 0 V)	I_{amb} (A/μm) (@ V_{GS} = − 1 V)	Average SS (mV/dec)	I_{ON}/I_{OFF}
Regenerated TFET	2.25×10^{-5}	1.5×10^{-13}	6×10^{-5}	58.85	1.5×10^{8}
PTMG-TFET (This work)	5×10^{-5}	2.5×10^{-15}	3×10^{-7}	51.01	2×10^{10}
HG TFET [14]	9.5×10^{-5}	10^{-16}	2.5×10^{-10}	12	9.5×10^{11}
Overlapping gate-on-drain TFET [19]	4×10^{-7}	2×10^{-15}	10^{-9}	71	2×10^{8}
HDB PNPN TFET [20]	3×10^{-5}	4×10^{-17}	5×10^{-17}	57	7.5×10^{11}
p-i-n TFET [21]	3.5×10^{-5}	5×10^{-14}	3×10^{-16}	30.4	7×10^{8}

and I_{amb} and reduction of about 7.84 mV/dec in SS make this PTMG-TFET as a suitable candidate to be used in digital applications.

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