2020 IEEE International Symposium on Smart Electronic Systems (iSES) (Formerly iNiS) | 978-1-6654-0478-5/20/$31.00 ©2020 IEEE | DOI: 10.1109/iSES50453.2020.00020

Characterization of Charge Plasma-based Junctionless Tunneling Field Effect Transistor (JL-TFET)

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***Abstract*—The steep doping profile associated with conventional Tunneling Field Effect Transistor (TFET) provides significant hindrances from a fabrication perspective despite the obvious merits of the device. Junctionless TFET (JL-TFET) alleviates the problem considerably by introducing a uniform doping profile across the device. In this study, we have looked at several device parameters like gate insulator dielectric constant, gate insulator thickness, silicon body thickness, doping level, and work function of P-gate and source which affect the performance of the device. The analysis is done based on the impact of parameters on subthreshold swing (SS), on-current to off-current ratio (I_{on}/I_{off}), and threshold voltage (V_T). The influence of certain parameters on on-current (I_{on}) has also been looked at. These have enabled us to identify how the tuning of parameters could lead to peak device performance.**

***Index Terms*—Junctionless TFET, Subthreshold Swing, Work Function, Threshold Voltage, Non-local Band-to-Band Tunneling Model**

I. Introduction

Years of aggressive scaling of MOSFET has lead to an unwanted increase in short channel effects, leakage current, and the subthreshold swing is also limited to 60 mV/dec for MOSFET [1]. As a result, research is being carried out extensively to search for alternative devices. Tunneling Field Effect transistor (TFET) is considered one of the most promising of such devices [2]–[4]. Because of the band to band tunneling mechanism, TFET offers much less subthreshold swing compared to MOSFET [5]–[7]. Alongside, TFET also offers lower leakage current, ultra-low power dissipation, and very low off current due to is wide tunneling barrier in the off state. However, fabrication of TFET demands high doping concentration and asymmetric doping structure that imposes a high degree of challenge to our existing fabrication technology [8]. But, such problems can be tackled with junctionless TFET (JL-TFET) in which a uniformly doped silicon structure can attain a P-I-N doping configuration using the charge-plasma concept [9], [10].

Using dual material gate in TFET, improved I_{on}, I_{on}/ I_{off} ratio and suppressed short channel effect has been reported [11]. Moreover, it has also been reported that dual material and dual oxide gate improves its analog characteristics [12]. Raushan et al. in their 2D simulation study of JL-TFET has shown that using dual κ spacer in JLTFET can help it attain subthreshold swing about 40 mV/dec and I_{ON}/ I_{ON} ratio of approximately 10^8 [13].

In this paper, using a TCAD tool, we have designed a silicon JL-TFET with a high κ spacer and appropriately engineered gate work function. We have a varied gate dielectric constant (κ), gate insulator thickness (t_{ins}), silicon body thickness (t_{si}), doping level, P-gate and source work function to investigate primarily how these parameters affect subthreshold swing (point), I_{on}/I_{off}, V_T, and I_{on} in case of some parameters.

II. Device Structure and Simulation Details

Junctionless TFET (JL-TFET) has the basic structure like a conventional TFET, but, instead of the p-i-n doping, a uniformly doped silicon body wafer is used. The p-i-n doping profile is created in the structure by employing work function engineering. As a result, the difficulty and cost associated with doping in the fabrication level can be minimized. The schematic view of the JL-TFET is illustrated below in Fig. 1. The source, gate, drain electrode work function has been set to 5.40 eV, 4.20 eV, and 3.90 eV respectively. Moreover, P-Gate (gate above the source region) has a work function of 5.40 eV. Silicon body thickness is 10 nm, dielectric thickness 3 nm, and a dielectric constant of 7 in gate insulator is used. Silicon body has uniform n-type doping of $10^{18}cm^{-3}$. The above parameters are held fixed while the parameter of interest is varied. It should be noted that 5 nm high-κ spacer (κ=21) is used. P-gate has a length of 20 nm and the control gate has a length of 25 nm. For all types of simulation in this study, V_{DS} has been set to 1 V.

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DOI 10.1109/iSES50453.2020.00020

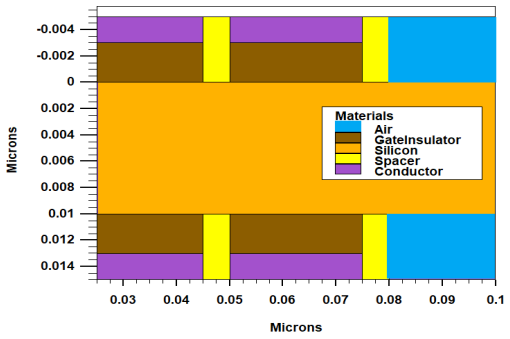

Fig. 1. Schematic of JL-TFET.

In the ON state, the creation of p-i-n region can be observed as shown in Fig. 2. An optimum choice of work function plays a significant role in the performance of JL-TFET [14].

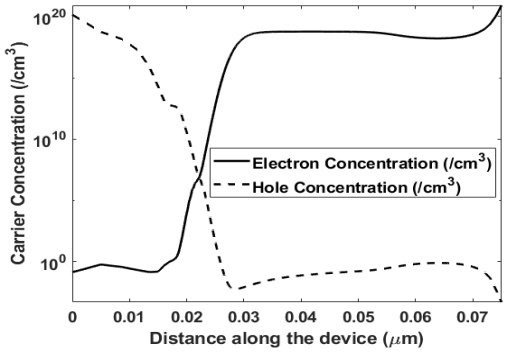

Fig. 2. A plot of carrier concentration (κ=16) in the ON state.

A transfer curve of JL-TFET (κ=16 for gate insulator) is shown in Fig. 3 where V_{GS} is swept from 0 V to 2 V.

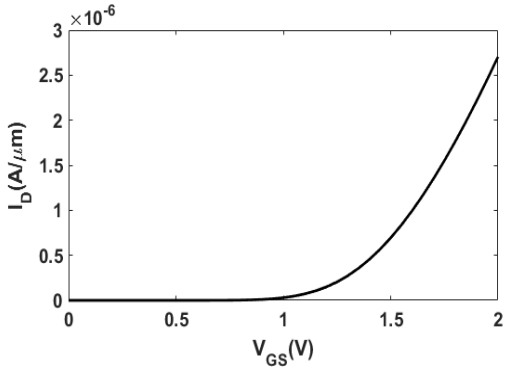

Fig. 3. Transfer curve of a JL-TFET.

III. Methodology

To simulate the device, non-local band-to-band tunneling model is used which considers the inherent non-local nature of the tunneling process. Besides, the following models are used- Fermi-Dirac Statistics, concentration-dependent mobility, bandgap narrowing, trap-assisted tunneling (TAT), Auger recombination, Shockley-Read-Hall recombination (SRH). Fermi Statistics is used to calculate intrinsic carrier concentrations required to evaluate SRH recombination. For numerical solutions of the equations, the Newton method is used.

IV. Results and Discussion

A. Effects of κ on JL-TFET

To observe the effect of κ on JL-TFET, we have varied dielectric constant of gate insulator as follows: SiO_2 ($\kappa = 3.9$), Si_3N_4 ($\kappa = 7$), and Y_2O_3 ($\kappa = 16$). We have found that the subthreshold swing becomes lower when a higher dielectric constant is used which can be seen in Fig. 4. These results are coherent with the findings of Ghosh et al. and Bal et al. in their study in [10] and [14] respectively. These improvements are owing to the greater gate coupling ability of the high-κ insulators. Due to higher gate controllability, I_{on} improves notably when high-κ gate dielectric is used resulting in improvement of I_{ON}/I_{OFF} ratio as illustrated in Fig. 5.

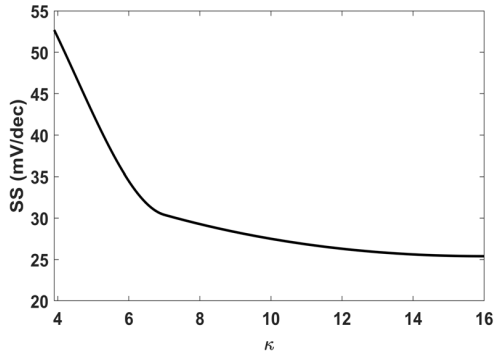

Fig. 4. SS improves as κ increases.

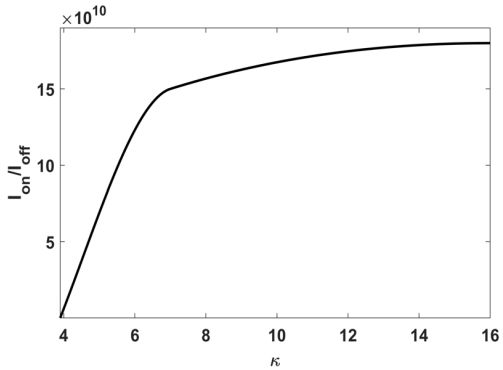

Fig. 5. I_{ON}/I_{OFF} increases significantly with the increase of κ.

We have also observed that threshold voltage improves with increasing κ as referred in Fig. 6. To determine threshold voltage, $10^{-9}A/\mu m$ is taken as the current in the constant

current method considering the remarkable variation of current with respect to changes in some parameters. We can see from

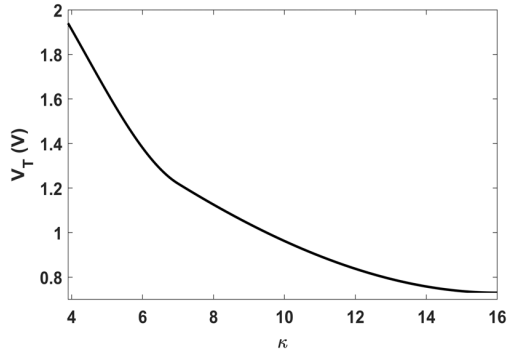

Fig. 6. V_T and κ have negative correlation.

our study that using high-κ materials could lead to improved performance. This is consistent with the study in [15].

B. Effects of t_{ins} on JL-TFET

Fig. 7, 8, and 9 show the behavior of JL-TFET as we have varied the dielectric thickness (1 nm, 2 nm and 3 nm). t_{ins} and SS have positive correlation. I_{on}/I_{off} ratio decrease as we increase t_{ins} because of the falling nature of the on-state current. Also, threshold voltage shows stark improvement when t_{ins} is reduced owing to significant changes in current. These results are consistent with the findings in [10].

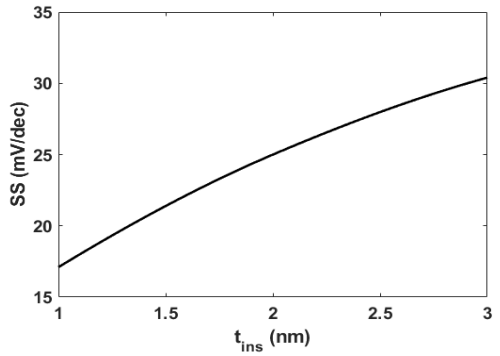

Fig. 7. A reduction in gate insulator thickness results in better SS.

C. Effects of t_{Si} on JL-TFET

Thin channel is desirable as we are continuously trying to design more compact devices. TFET has more tolerance to thin-film short channel effect than conventional MOSFET [14]. As the silicon body thickness of 5 nm, 10 nm and 15 nm are chosen, we can observe that I_{on} falls with an increase in silicon body thickness as shown in Fig. 10. In terms of V_T, performance degrades with bulkier silicon body as shown in Fig. 11 which can be explained by increases in current.

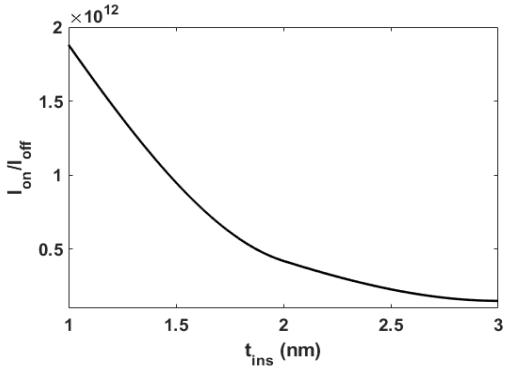

Fig. 8. Reducing t_{ins} results in an increase of I_{on}/I_{off}.

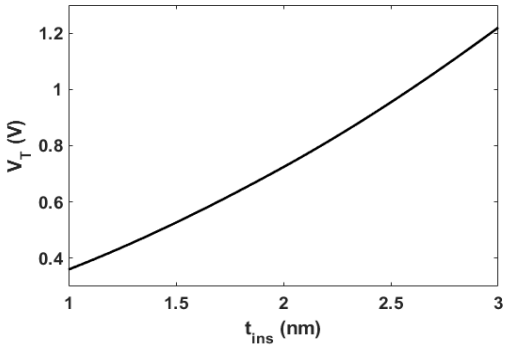

Fig. 9. V_T increases as t_{ins} increases.

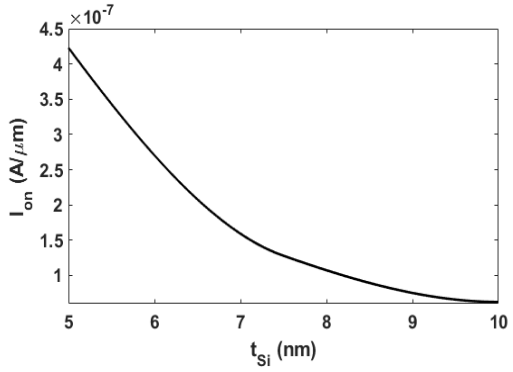

Fig. 10. I_{on} shows falling characteristics when t_{Si} is increased.

D. Effects of doping level in JL-TFET

To investigate the effect of doping level, doping level is varied as shown in Table I. An increasing and decreasing pattern of I_{on} and V_T respectively can be observed respectively with increments in doping level. Even though slight improvements can be observed with higher doping, it must be noted that the effects of doping level are not as substantial as some other parameters. The overall low values on-current is attributed to relatively low value of κ and high t_{ins} used during parametric variation.

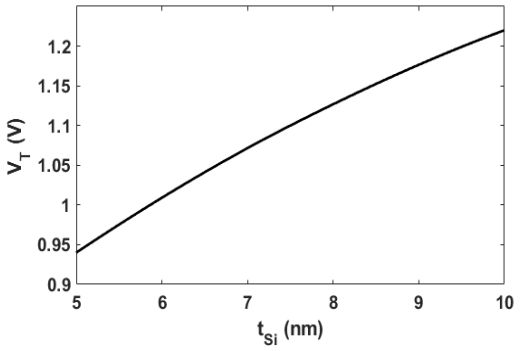

Fig. 11. V_T improves with lower silicon body thickness.

TABLE I
EFFECTS OF DOPING LEVEL ON I_{on} AND V_T

Doping level (/cm^3)	I_{on} $(A/\mu m)$	V_T (V)
10^{15}	4.61×10^{-8}	1.30
10^{16}	4.63×10^{-8}	1.29
10^{17}	4.81×10^{-8}	1.29
10^{18}	6.25×10^{-8}	1.22

E. Effects of P-Gate and Source work function on JL-TFET

We have seen the effects of work function on the performance of the device. A trend in on-current and threshold voltage is noticed with an alteration in work function as shown in Table II. I_{on} increases with higher ϕ which can be explained by Fig. 12 where it can be noticed that there is a reduction in energy barrier width leading to greater tunneling current. Moreover, the threshold voltage exhibits a negative correlation with the work function.

TABLE II
EFFECTS OF P-GATE AND SOURCE WORK FUNCTION ON I_{on} AND V_T.

ϕ (eV)	I_{on} $(A/\mu m)$	V_T (V)
5.40	6.25×10^{-8}	1.22
5.76	5.11×10^{-7}	0.92
5.93	1.02×10^{-6}	0.83

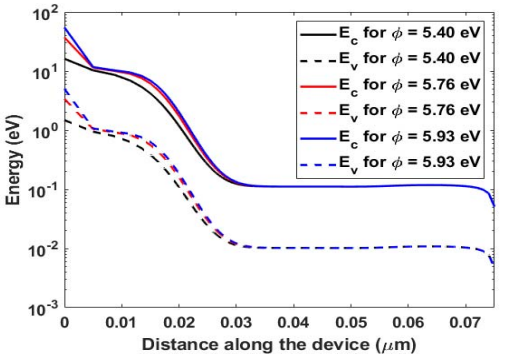

Fig. 12. Band diagram for different work function values.

V. CONCLUSION

JL-TFET is one of the most prominent variations of TFET as it can subside the limitations generally faced by the fabrication of conventional TFET. In this study, we have found that the high-κ gate dielectric enhances the performance of the JL-TFET device. Also, a decrease in T_{ins} improves SS, I_{on}/I_{off}, and V_T. In addition, I_{on} increases, and V_T decreases with a reduction in silicon body thickness. Moreover, improvements in I_{on} and V_T can be seen with an increase in doping level though the effects are not much pronounced. The impact of gate work function engineering is significant on both I_{on} and V_T. Our study can aid in the decision-making process of the choice of parameters to obtain optimum device performance in JL-TFETs.

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