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Doping and Dopingless Tunnel Field Effect Transistor

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***Abstract*—For Low power consumption, an emerging device that depends on lowering the supply voltage with downscaling is proposed which is known as the Tunnel-FET (TFET). In general, MOSFETS (Metal Oxide Semiconductor Field Effect Transistors) is used for the low power transistors. Still, the SS (Sub-threshold Swing) of MOSFET is bounded to 60 mv/decade for further reduction in supply voltage. The dynamic and static power consumption of MOSFETs is increased with the downscaling. Hence, for energy-efficient and low power consumption with improved sub-threshold swing, TFET is auspicious replacement of MOSFETs. The structure of MOSFET and TFET is approximately like each other with a different fundamental working mechanism. TFET is a gated p-i-n diode structure, and current conduction in between the energy bands of the channel and source by switching mechanism of quantum tunneling (band to band tunnel mechanisms) through a barrier. This paper aims to do a literature review of TFET from physically doped TFET to Dopingless TFETs. This survey paper studies and reviews physically doped Double Gate TFET (DG-TFET) available for design. After that, dopingless TFET is studied and shows its dominating performance.**

***Index Terms*—Sub-threshold slope, Ambipolar, Doping, Dopingless, Gate engineering, Drain engineering, Work function, Charge plasma, Random doping fluctuation.**

I. INTRODUCTION

CMOS (Complementary Metal Oxide Semiconductor) has play crucial role in the fabrication of IC's (Integrated circuits) and switches. CMOS technology is used in semiconductor devices because it afforded a possibility of a reduction in supply voltage and increased drive current with low power consumption with down-scaling [1]. But we know, as stated in Moore's law, transistor present on a single chip would be double every 24 months [2]. So, we need the down scaling of semiconductor device to bring down the power dissipation as well as reduced fabrication cost and complexity. To achieve this aim, in the last few years, the scaling of MOSFET reached nanometres, but integrated circuit fabricated with these MOSFETs does not work efficiently at lower power supply. On the other hand, power management becomes more difficult for the further downscaling of the MOSFET [3]. Due to advance downscaling, MOSFET impart several consequences like the lower value of I_{on}/I_{off}(ON-current to OFF-current ratio), short channel effects (Hot carrier effect, DIBL etc.), limited sub-threshold slope value (SS), parasitic as well as coupling effect with high leakage current, etc. [4], [5]. In general, we need a device that potentially replaces the MOSFET. So, to overwhelm the problems of MOSFETs, a novel TFET device is introduced by the T. Baba in 1992 [6]. TFET is the suggesting alternative of the conventional MOSFET, depending on the various operational parameters. Some performance-based advantages of TFET are listed below:

- Possibility for lowering SS value (lower than 60 mv/decade)
- Diminution of the leakage current on account of BTBT (Band -To -Band Tunneling) mechanism
- Used for low power application with lower threshold voltage
- High I_{on}/I_{off} current ratio
- Overcome the short channel effect
- Enhanced switching speed due to tunneling mechanism
- The fabrication process is similar to the MOSFET

The above listed key advantages proven that the TFET has potential to replace the MOSFET. In basic working operation of TFET, the tunnel current flows because of variation in gate voltage (at fixed drain voltage (V_{ds})) and BTBT mechanism [7]. The advisable use of TFETs based on ultra-low power, high speed, energy-efficient, and high frequency application [8]. In this literature survey, we have analysed various doping and dopingless based structures of TFET from the beginning year 2004 to 2020 and elaborate on the performance. Five section are listed in survey paper for literature, Section II assigns for basic device operation, and the physics of TFET, section III is dedicated to the literature survey of doping based TFET, and section IV allocates for different structures and engineering of dopingless TFET.

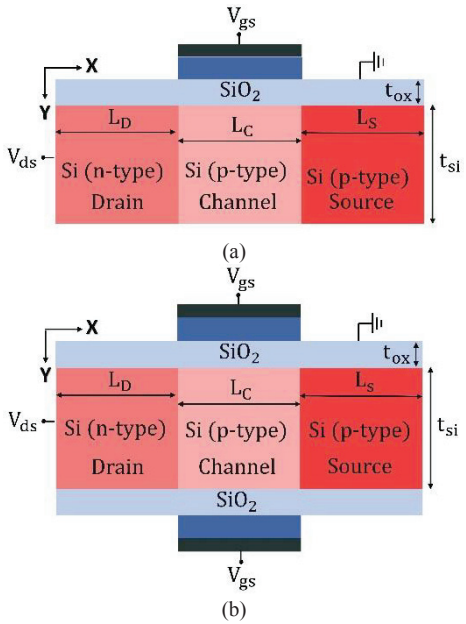

Fig. 1. The general structure of Tunnel Field Effect Transistors (a) Single-gate TFET (SG-TFET) (b) Double-gate TFET (DGTFET) with 3 nm t_{ox} and 10 nm t_{si} [9].

II. DEVICE PHYSICS AND OPERATING PRINCIPLES OF TFET

The device structure of TFET and MOSFET is almost similar except for that drain, and source terminal has opposite type of dopant. Generally, the basic structure of TFET resides abrupt doped p-n junctions, in which potential difference of an intrinsic region controls by the gate contact while operating under the reverse bias condition [9]. According to the majority carrier concentration of source and drain, TFET is divided into two types: (i) n-type TFET (source region p+ type and drain n+ type) and (ii) p-type TFET (source region n+ type and drain p+ type). TFET make use of BTBT as a basic working mechanism. In TFET, between the p-type and n-type regions, intrinsic region of channel is formed. The drain terminal (n-type) work as a sink of majority charge carrier and source terminal (p-type) is a source of majority charge carrier whether gate terminal control the movement of majority charge carrier going from source to drain or vice-versa. In general, gate terminal indirectly controls the drain current. The gate oxide is used to prevents the leakage of current from channel to gate [10].

In OFF-state, a significant barrier potential is present in between channel and source of TFET. Therefore, only leakage current is present [11]. At that point, when a gate voltage (V_g) surpasses the threshold voltage (V_{th}), barrier potential present between the source and channel is diminished. Due to this Conduction Band (CB) of channel region gets aligned with the Valence Band (VB) of the source so that the transition of electron take place from source to channel and current start flowing, it is known as the ON-state of TFET [12], [13]. The general expression of the tunneling transmission probability of carriers is deliberate by using the Wentzel, Kramer's, and Brillouin (WKB) approximation. With the help of WKB approximation phenomena, we can find the tunneling probability through a general barrier potential independent of any type of material and band structure properties. The WKB approximation is given by equation (1) and (2) [14]:

$$T_{wkb} \approx \exp\left[\frac{4\sqrt{2m^* {E_g}^3}}{3q\hbar E}\right] \tag{1}$$

$$T_{wkb} \approx \exp\left[\frac{4\lambda\sqrt{2m^* {E_g}^3}}{3q\hbar[E_g + \triangle\Phi]}\right] \tag{2}$$

Where, E_g is bandgap of material and m^* is effective mass of charge carrier, q is the charge, $\Delta\Phi$ represents the energy window over which tunneling occurs, λ is the screening tunnel length (i.e., tunneling barrier width) which helps to illustrate the depth of transition region at source-channel interface depending on the device dimensions and geometry [12], $\hbar$ is Planck's constant, and E is electric field and measured in Volt/meter. The electric field expressed as $E = (E_g + \Delta\Phi)/\lambda$, which represents the height of triangular barrier potential for the charge carrier to tunnel from the VB of source to CB of channel in the TFET [15]. At constant drain to source voltage (V_{ds}) with step gate to source voltage (V_{gs}), the tunneling barrier width (λ) is reduced with increment in the value of tunneling energy window ($\Delta\Phi$). So, we can conclude that drain current is the strong exponential function of the gate voltage in WKB approximation. For the TFET, one of the key advantages over the conventional MOSFET is the value of SS without any lower limit [16]. The channel cuts higher energy tail of Fermi Distribution Function (FDF), and simultaneously the source cut off the lower energy tail of FDF, by reason of this the tunnel junction near-source and channel behave like a bandpass filter that allows barely charge carriers which can cross the energy window. This filtering concept helps to achieve a lower SS (>60 mV/decade) at the room temperature (300 K) [17]. The SS value obtain by using given equation:

$$SS = \frac{dV_{gs}}{d(\log I_{ds})} \tag{3}$$

Where V_{gs} is voltage across the gate to source terminal, and I_{ds} is the drain current. The general expression of tunneling current for the reverse-biased p-n junction is [18]:

$$I_{rev} = aV_{eff}E\exp\left(\frac{-b}{E}\right) \tag{4}$$

Where E represents the tunnel junction electric field, V_{eff} stands for the biasing of tunnel junction, and a and b are the material coefficient, which depends on the cross-sectional area and material properties of the BTBT device [19]. Both 'a' and 'b' coefficient are given as:

$$a = Aq^3\frac{\sqrt{2m/E_g}}{\hbar^2\pi^2} \tag{5}$$

$$b = \frac{4{E_g}^{3/2}}{3q\hbar}\sqrt{m} \tag{6}$$

by using the equation (3) and (4), sub-threshold slope for BTBT device (TFET) can be expressed as equation (7):

$$SS = \log\left[\frac{1}{V_{eff}}\frac{dV_{eff}}{dV_{gs}} + \frac{E+b}{E^2}\frac{dE}{dV_{gs}}\right]^{-1} \tag{7}$$

From the equation (7), we can see that the kT/q value does not limit SS value of TFET as in conventional MOSFET. The SS value of TFET mainly depends on the two terms (V_{gs} and V_{eff}) of the equation (7). The V_{gs} can efficiently and directly control V_{eff}, which needs high-k gate dielectric or thin device geometry required to make sure the channel can modulate directly with the help of gate bias voltage [20]. To calculate SS value for TFET, the transfer characteristic (output vs. input, i.e., I_{ds}-V_{gs}) is plotted with drain current (I_{ds}, output) on the log scale and gate to source bias (V_{gs}, input) on normal axis. The SS of TFET is defined as two different types:

- Point SS (SS_{pt}): To measure the SS_{pt} of TFET, just look at that point on the I_{ds}-V_{gs} plot at which device depart from its OFF-state and starts flowing the tunneling current [21].
- Average SS (SS_{avg}): SS_{avg} is taken from the I_{ds}-V_{gs} curve, from the ON-point of TFET to threshold voltage (V_{th}) (approximately 0.7 V) [9]. The SS_{avg} is given as:

$$SS_{avg} = \frac{V_{th} - V_{off}}{\log(\frac{I_{th}}{I_{off}})} \tag{8}$$

III. DOPING BASED TFET

The first physical doping-based tunnel transistor presented by the T. Baba [6], known as the surface tunnel transistor (STT), that consist of a minimal length of the gate (≈ 0.1 um) with low performance. Hence to improve the functionality of device, Toshio Baba proposed the second device to achieve steep sub-threshold swing, known as Tunnel FET [22]. In this proposed device, the gate control on channel was enhanced improve tunneling process. For further improvement in the doping based TFET, Kathy Boucart et.al. [9] suggested double gate TFET (DG-TFET) with variation in the gate oxides and prove that with the increment in dielectric strength of the gate-oxide material helps to improve the ON-current and reduced the SS_{avg} (57 mV/dec). The structural representation of single gate TFET (SG-TFET) and DG-TFET is shown in Fig.1. The DG-TFET consists of two gates instead of one gate. The first gate is known as a front gate (at the top), and the second gate known as a back gate (at the bottom). Due to the double gate structure, the controllability of electrostatic potential at the gate terminal is improved on the channel region since electric field lines discontinue from the back gate rather than break off in the channel of TFET and helps to improve the current flow in channel [23]. The effect of dielectric constant on the transfer characteristics has been revealed, which shows that the SS_{avg} is higher at the high value of the dielectric constant [22].

In general, we will consider n-TFET for the observation and analysis in this survey paper. The TFET device has L_S (Length of source), L_D (length of drain) and L_G (gate/channel length) set to 55 nm, 55 nm, and 50 nm with oxides thickness (t_{ox}) is 3nm and 10 nm silicon body thickness (t_{si}). The doping levels for source, drain and channel regions were 1×10^{20} cm^{-3}, 1×10^{18} cm^{-3} and 1×10^{17} cm^{-3} respectively with 4.5 eV contact gate work function [16]-[17]. From the Fig. 2a, we can see that, for ON-state (V_{gs} > 0) the valence band of source get aligned with the channel conduction band because of this electron's movement start from source to channel and current start flowing. However, by considering the above key parameters, I_{on} = 20.14×10^{-6} A/μm, SS_{avg} = 53 mV/decade, I_{off} in the range of 10×10^{-17} A/μm at V_{gs} = 1 V and the transfer characteristic curve of DG-TFET is shown in Fig.2b. For further analysis of DG-TFET with some basic parameter variation like device dimension, body thickness, gate oxide thickness, lower band-gap material used in place of silicon body, and dielectric strength of oxide can be done for improved results like higher ON-current, lower SS value, and high I_{on}/I_{off}.

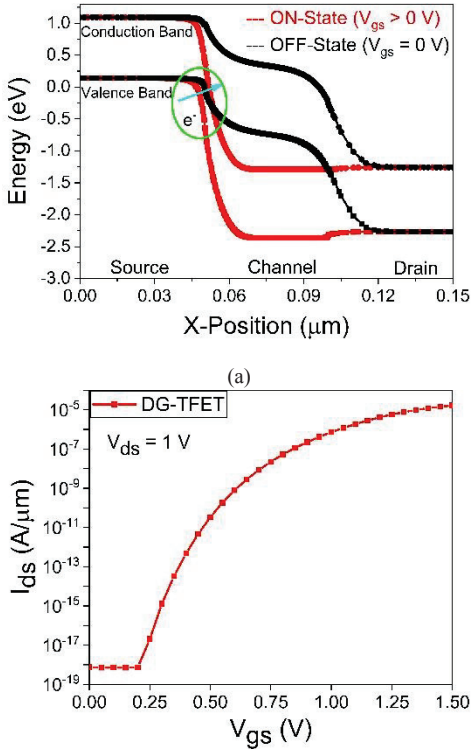

Fig. 2. (a) Comparison of ON-state and OFF- state energyband diagram (EBD) of physically doped DG-TFET **(b)** Transfer characteristics of TFET at V_{ds} = 1 V with variation in V_{gs} from 0.0 V to 1.5 V.

To add advantages related to fabrication complications and to reduce the cost, a dopingless TFET (DL-TFET) is introduced [18]. By using DL-TFET, the fabrication process gets a simple and reduced random dopant fluctuation (RDF) problem as a contrast to conventional physically doped TFET device [24].

IV. DOPINGLESS TFET (DL-TFET)

TFET devices need needle like sharp changes of doping at drain- channel and source- channel junction from a high doping level (10^{20} cm^{-3}) to low doping levels (approximately 10^{18} to 10^{15} cm^{-3}) or vice-versa with complimentary dopant. But an ultra-steep doping profile near the interface is utmost impossible by using ion implantation, diffusion, and thermal annealing process techniques during fabrication [4]. Without forming ultra-steep sharp junction at drain/channel/source interface, important structural variation in the device may lead to an impact on all aspects of device performance. One of these variations, random dopant fluctuation (RDF) is a significant

issue. RDF is caused by the irregularity in charge carrier location and numbers in all the region of silicon body (source, channel and drain) that follow the Poisson distribution rule as well as dimension modification (down scaling) of the device [25]. Due to down scaling, total number of dopants decreases, which leads to many dopant variations related issues and may impact on the basic device parameters like V_{th}, I_{on}, SS etc. Additionally, the random fluctuation and positioning of charge carriers will occur in the actual number of dopant atom present in the channel region. This will become critical in the nanometer device dimension showing a moderate carrier concentration [26].

RDF should be reduced to improve all the aspects of device performance. As we know for a given technology, RDF is directly proportional to the doping concentration of charge carrier in the channel region of the transistor. Therefore, reducing RDF can be obtained by reducing the dopant density. For the ideal case, RDF would be removed completely if the dopant (impurity charge carriers) is zero. So, for a given technology, the TFET device must be optimized to work at the lowest possible carrier /dopant density. For lowest RDF, the threshold voltage reduces and leads to minimizing the static power with unacceptably increase OFF-current [24]. To diminish RDF issue, we need to develop the hole-electron bi-layer TFET on an intrinsic semiconductor (silicon body) without using the doping for p-type and n-type of the source/channel/drain region. In conclusion, doping-less TFET is proposed and expected to be free from the RDF problem with fabrication related benefits. In DL-TFET, by choosing the appropriate work function of metal electrode, "p+" and "n+" type carrier concentration is induced in the intrinsic Si body. It is known as charge plasma concept (CPC) [27], [28]. Due to CPC techniques, the thermal budget is cut down because it will not use the annealing process or ion implantation techniques for doping.

The DL-TFET has potential to grow on a single-crystal silicon substrate by using the low-temperature process. In 2013, M. Jagadesh Kumar et al. [29] propose and investigate the dual-gate DL-TFET (DG-DL-TFET). To achieve appropriate induced carrier and better electrostatic properties, the gap between front and back gate (excluding the oxide layer thickness) in the drain and source region must be kept within the debye length [10]. The mathematical expression of debye length given below:

$$L_D = \sqrt{\frac{\varepsilon_{si} V_T}{qN}} \tag{9}$$

Where V_T represents the thermal voltage, N stands for the carrier concentration of the Si body, ε_{si} is silicon dielectric constant, and q is the elementary charge. In DL-TFET, induced "n-type" drain and "p-type" source regions are created with the help of CPC techniques [30]. The work function is the crucial parameter of the charge plasma concept because variation in the work function of the metal/semiconductor shows the change in induced charge carrier concentration.

To acknowledge the principal of work function, first, we will understand the work function difference of metal and semiconductor ($\Phi_{MS} = \Phi_M - \Phi_S$). Normally, $\Phi_{MS} > 0$ or $\Phi_{MS} < 0$ on varying on work-function of metal (Φ_M) and semiconductor (Φ_S). For the p-type induced region $\Phi_{MS} > 0$, for this condition, the electron can move to metal from semiconductor, and ionized donor atoms at semiconductor interface are generated. Due to this, a negative charge sheet in metal and a positive charge sheet in the semiconductor is created. Same as for the n-type induced region $\Phi_{MS} < 0$ [10].

The work function of silicon, including the oxide contact potential, is 4.8 eV. So, while choosing the drain metal electrode to induced n-type region, we must delimit the metal with work function lower than 4.8 eV. Similarly, for the source metal electrode, the work function is must be higher than 4.8 eV to induce the p-type region. So, for the realization of DLTFET, for drain electrode Hafnium (Φ=3.9 eV) and source electrode, Platinum (Φ=5.93 eV) is used [31].

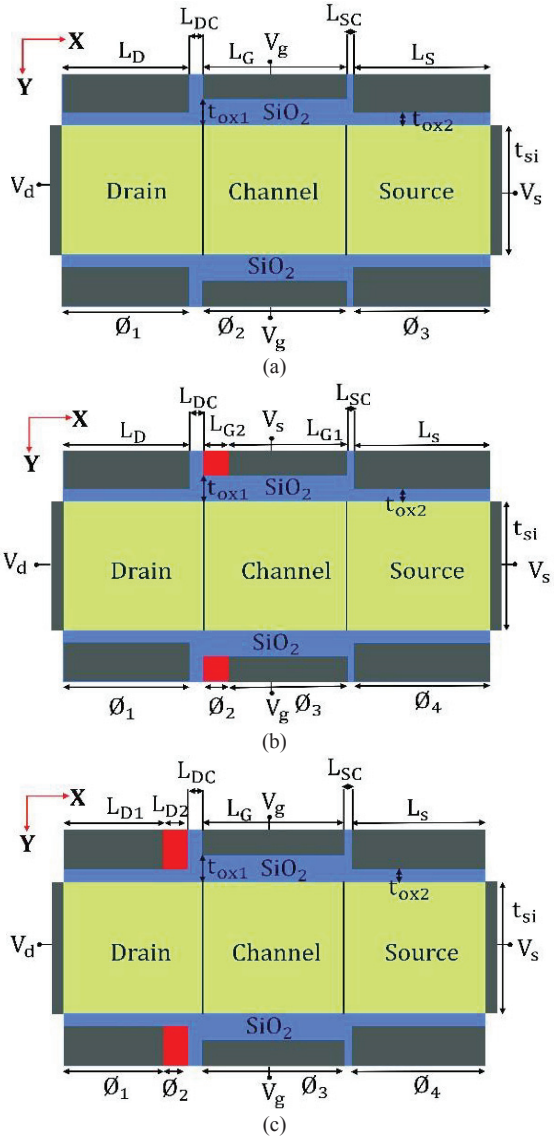

Fig. 3. The graphic of various dopingless TFET structure with different oxide thickness at source/drain (t_{ox2} = 1 nm) and gate (t_{ox1} = 2 nm) **(a)** Conventional dopingless TFET with $L_D = L_S$ = 55 nm , and L_G = 50 nm **(b)** Dual metal gate DL-TFET, L_{G1} = 40 nm, L_{G2} = 10 nm with work functions 4.53 eV and 4.0 eV respectively and **(c)** Drain work function engineering-based DL-TFET with L_{D1} = 45 nm , L_{D2} = 10 nm with work functions 3.9 eV and 4.4 eV respectively [21].

With some benefits, DL-TFET also experiences some critical problems like low ON- current, ambipolar conduction, and poor RF performance [21]. To reduce these problems, an innovative way used to suppress the ambipolar behaviour and to improve the high frequency performance of DL-TFET has been present by B. Ram Raad et al. with the help of Drain Work Function Engineering (DWFE) 27. In DWFE concept, the drain metal electrode is divided into two parts. The first part, near the drain-channel interface, is considered as high work function section (Φ_5) and the remaining part of the drain metal electrode considered as low work function section (Φ_1). In this work, suppressed ambipolar behaviour is achieved by changing the length of high work function part (L_{D1}) of the drain electrode and value of (Φ_1). The device structure and obtain DC characteristic shown in Fig.3 and Fig.4 respectively.

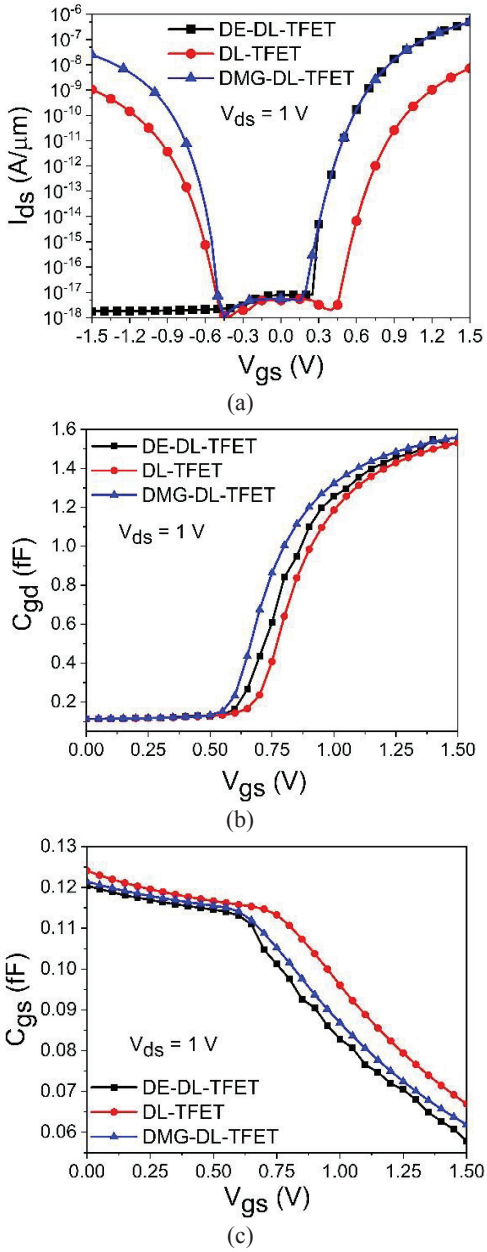

Fig. 4. The comparative analysis of schematic show in Fig.3 w.r.t. **(a)** Transfer characteristics graph **(b)** Gate to drain capacitance (C_{gd}) data plot and **(c)** Gate to source capacitance (C_{gs}) curve of at fixed V_{ds} = 1V.

Furthermore, Yadav et al. [21] proposed gate and drain engineered DL-TFET to achieve suppressed ambipolar behaviour with steeper slop of transfer characteristic curve (loser SS value). By few modifications, an improved SS = 10 mV/decade achieved, and the ambipolar behaviour is suppressed up to 10^{-18} A/μm with threshold voltage 0.65 V. The novel structure, energy band diagram, I-V characteristic and parasitic capacitance curve are shown in Fig. 5 and Fig. 6 respectively. Further, some different structure of DL-TFET is studied, and their I-V (current-voltage) curve obtain for the analysis of ON-current, SS, the Gate to drain capacitance (C_{gd}) and Gate to source capacitance (C_{gs}) which shown in Fig. 6. A comprehensive comparison is performed in between conventional DL-TFET, gate engineering-based DLTFET (DMG-DL-TFET), drain engineering-based DL-TFET (DE-DL-TFET), and with both engineering (gate and drain engineering) based DL-TFET (DE-DMG-DL-TFET) [31].

From the Fig. 4a, we can observe that the drain work function engineered based DG-DL-TFET shows a significant suppression of the ambipolar behaviour. In this structure of DLTFET, the ambipolar conduction suppression occurs because of the high work function of L_{D2} section of drain. Due to the high work function of L_{D2} section, the tunneling barrier increase at the drain/channel interface because this section has higher band energy in comparison to the L_{D1} section of drain region. Further analysis from Fig. 4a say that DMG-DL-TFET and DE-DL-TFET shows higher ON-current in comparison to the conventional DL-TFET. The DEDL-TFET have I_{on}/I_{off} ratio in the range of 10^{11} while the conventional DL-TFET and dual metal gate DL-TFET have in 10^{10} range. From the above analysis, DE-DL-TFET shows the best performance in comparison to various dopingless TFET shown in Fig.3. For further analysis on dopingless TFET, with fixed oxide thickness over the source/channel/drain region, four basic structural design shown in Fig. 5 [21], [31].

The various structures of dopingless TFET with uniform oxide thickness (1 nm) over drain/channel/source are shown in Fig.5 with 10 nm silicon body thickness (t_{si}). For DMGDL-TFET shown in Fig. 5b, the gate electrode divides into two sections L_{G1} = 38 nm and L_{G2} = 12 nm with work function 4.51 eV and 4.3 eV respectively. Similarly, DE-DL-TFET shown in Fig. 5c, drain electrode section divided into two sections L_{D1} = 40 nm and L_{D2} = 10 nm with work function 3.9 eV and 4.4 eV respectively. The structure shown in Fig. 5d is the combination of both gate and drain engineering. The DEDMG-DL-TFET helps to improve the ON-state current and suppress the ambipolar conduction of the device while gate engineering-based DL-TFET helps to analysis the threshold voltage as well as ON-state current [31].

From the Fig.6b, we can see that the drain engineered based dual-metal gate DL-TFET shows the lowest C_{gd} and C_{gs} compare to all other structure of DL-TFET shown in Fig. 5a to 5c. For the improved RF performance low parasitic capacitance required, so DE-DMG-DL-TFET is better than other structure of DL-TFET. For low power application with easy fabrication process, many research techniques and device dimension modification applied on DL-TFET i.e., concerning gate engineering, drain engineering, material engineering with improved device parameters like I_{on}/I_{off}, SS value, threshold voltage, parasitic capacitance etc.

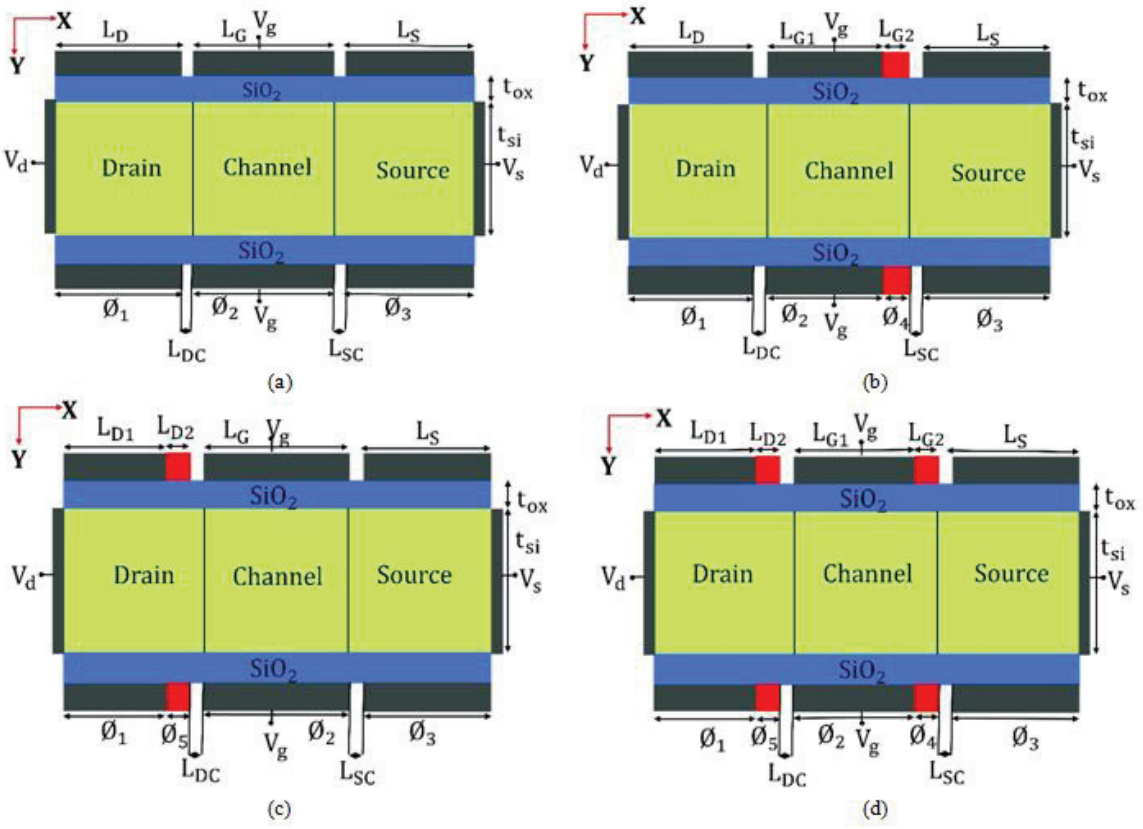

Fig. 5. Schematic of various dopingless TFET structure with fixed oxide thickness at source/drain/gate ($t_{ox1} = t_{ox2} = 1$ nm) **(a)** Conventional DL-TFET **(b)** DMG-DL-TFET **(c)** DE-DL-TFET and **(d)** DE-DMG-DL-TFET with L_D, L_S, L_G, L_{G2} and L_{D2}, 55 nm, 55 nm, 50 nm, 10 nm, and 10 nm respectively [31].

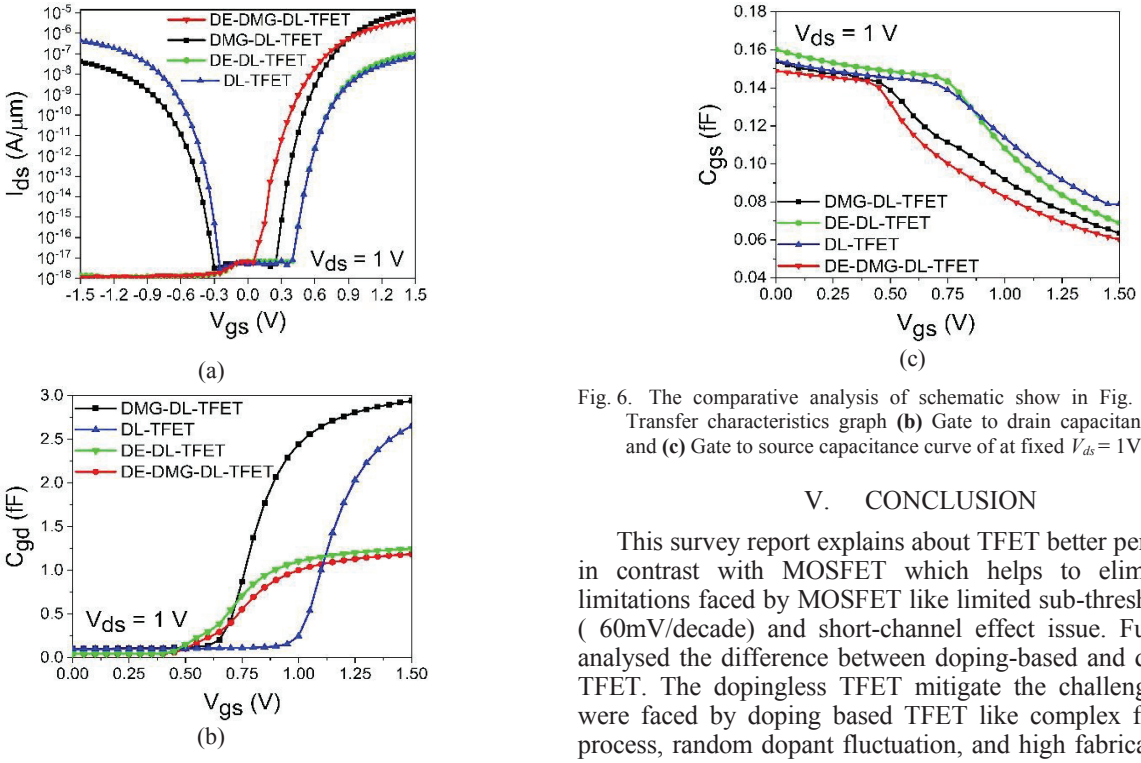

Fig. 6. The comparative analysis of schematic show in Fig. 5 w.r.t. **(a)** Transfer characteristics graph **(b)** Gate to drain capacitance data plot and **(c)** Gate to source capacitance curve of at fixed $V_{ds} = 1$V.

V. CONCLUSION

This survey report explains about TFET better performance in contrast with MOSFET which helps to eliminate the limitations faced by MOSFET like limited sub-threshold value (60mV/decade) and short-channel effect issue. Further, we analysed the difference between doping-based and dopingless TFET. The dopingless TFET mitigate the challenges which were faced by doping based TFET like complex fabrication process, random dopant fluctuation, and high fabrication cost. As well, explain the various type of engineering techniques to

reduce the ambipolar behaviour and SS value with decreased capacitance of DL-TFET. The DL-TFET performance can be further improved with the help of increasing the source/channel interface by modifying the structure and optimized work-function of gate and drain electrode. The TFET has some major application areas like bio-sensing, inverters, and memory devices.

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