DESIGN OF AREA AND POWER EFFICIENT FULL ADDER IN 180nm

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Abstract— **This paper presents a high drivability of full adder with less area and power consumption. This GDI based full adder is implemented by using both gate diffusion input (GDI) technique and pass transistor logic that leads to be a reduced area and power. To reducing the static power, ultralow power diode (ULPD) is used. The leakage current of this diode lies within the range of pA. The comparison has been done between existing systems like CMOS, CPL and hybrid full adders with proposed full adder. All full adders are designed with gpdk 0.18 um in Cadence Virtuoso schematic, and simulations are done in a Spectre Simulator.**

Keywords: GDI technique, UPLD, Hybrid full adder, CMOS and CPL.

I. INTRODUCTION

The adder is a basic building block[1-4] to many digital circuits like a digital signal processor (DSP), microprocessor, and also it plays the major role in array multiplier to add partial products. In arithmetic unit binary addition plays the major role because every arithmetic operations are performed by using an addition operation. So building low power and high performance adders would affect the system performance and also reduce the whole power consumption. That's why to achieving its performance is crucial to improving the whole circuit performance. The proposed full adder is designed with a minimum number of transistors it causes the low power consumption and also less area.

II. REVIEW ON DIFFERENT FULL ADDER TOPOLOGIES

In recent years, there are so many logic styles have been proposed to implement 1-bit full adder cells. The full adders are mainly classified into two types one is static and another one is dynamic full adders. Static full adders consume less power than the dynamic full adders because dynamic logic is a clocked logic. For N-input module, static requires 2N transistors and dynamic requires N+2 transistors. The advantage of using dynamic logic is faster switching speed and less static power dissipation. By combining both logic styles we can achieve hybrid logic style with high performance. We can achieve low area and power by combining two or more logic styles in a single circuit.

2.1 CMOS full adder

The static CMOS full adder follows the regular CMOS structure [5-6], it usually contains one PMOS pull-up network and one NMOS pull-down network as shown in Figure 1.

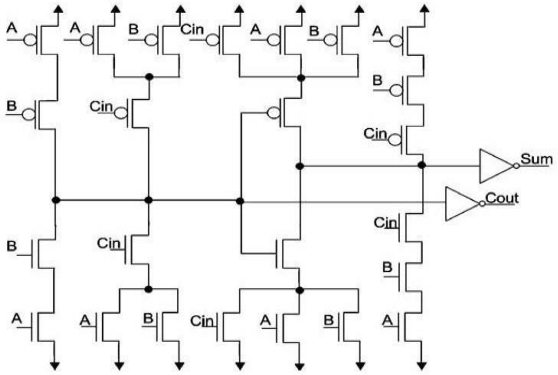
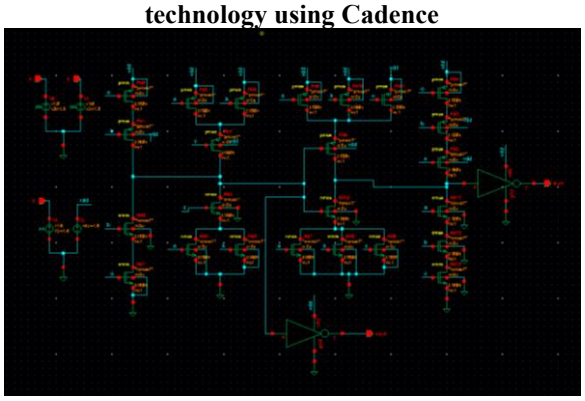


Fig.1 C-CMOS Full adder

Schematic diagram of C-CMOS full adder in 180nm technology using Cadence



In complementary CMOS logic the same function is performing two times, it may cause increasing of area and power. The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing, which are essential

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to provide reliable operation at low voltage with arbitrary transistor size. The disadvantage is driving capability of the circuit is reduced by connecting transistors are in series at the output stage. For suitable rectification buffers are required. Another design style in CMOS is pass transistor logic (PTL) [7, 8]. There are two pass transistor networks, one is PMOS, and another one is NMOS networks. Any one of the pass transistor networks is adequate to design the given logic function. It requires less number of transistors than the CMOS full adder.

2.2 CPL Full adder

The CPL circuits are designed by using NMOS pass transistor network with CMOS inverters at the output stage. The CPL differs from pass transistor logic because source terminal of the pass transistor is not connected to either power supply or ground. It is connected to any one input. The block diagram of a full adder using CPL as shown in Figure-2. The number of transistors to design CPL full adder is less than the CMOS full adder.

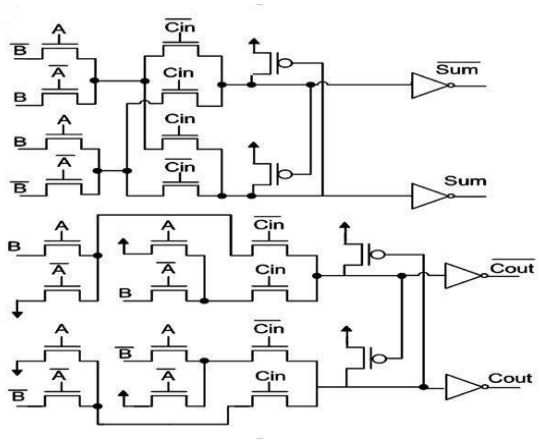
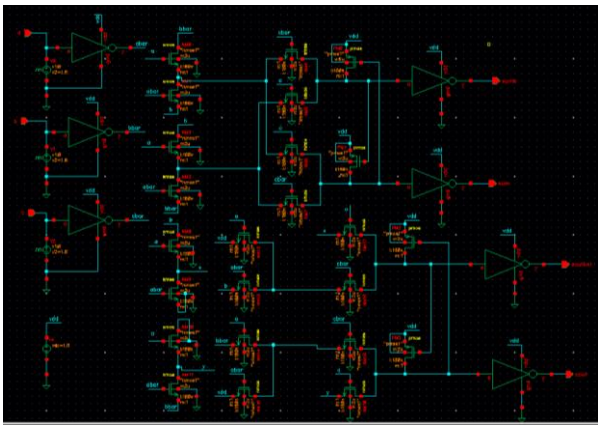


Fig.2 CPL Full adder

Schematic diagram of CPL Full adder in 180nm technology using Cadence



2.3 Hybrid full adder

This hybrid full adder contains Semi-XOR and Semi-XNOR [9, 10] gates instead of normal XOR and XNOR gates. The structures of the Semi-XOR and Semi-XNOR gates as shown in Figure-3. The output of these gates is same as a normal XOR and XNOR gates except 11 in Semi- XOR and 00 combinations in Semi-XNOR gates.

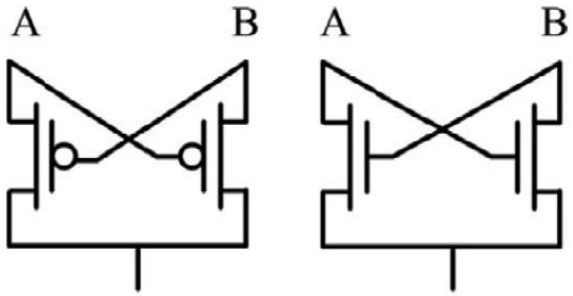


Fig.3 (a) Semi-XOR (b) Semi-XNOR

The truth tables of Semi XOR and Semi XNOR gates as shown in table 1 (**HZ** is high impedance state)

Table 1

A	B	C_{in}	SUM	C_{out}	Semi-XOR	Semi-XNOR
0	0	0	0	0	0	HZ
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	HZ	1
1	0	0	1	0	0	HZ
1	0	1	0	1	1	0
1	1	0	0	1	1	0
1	1	1	1	1	HZ	1

So, one such high impedance state is prevented by including an extra NMOS transistor whose source/drain is connected with input Cin and drain/source connected with SUM.

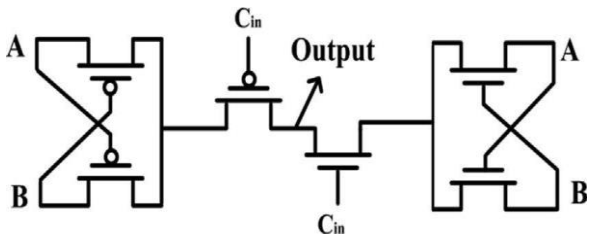


Fig.4 Sum generator cell with incomplete output

This NMOS is conducting in two conditions one is when the output of XNOR gate is one and another one is the SUM is equal to Cin. Another high impedance can be removed by introducing a PMOS with its source/drain connected to SUM

and drain/source to Cin. The complete sum generator cell is as shown in Figure-5

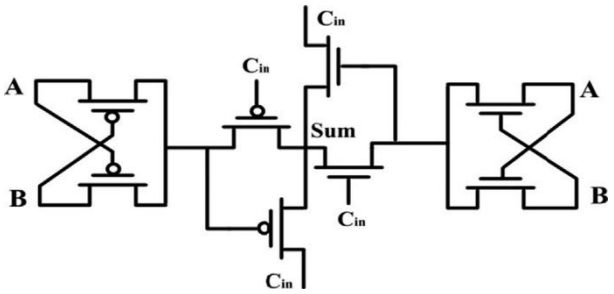


Fig.5 Sum generator with complete output

Similarly for Cout, using Semi XOR-XNOR gates and selector the circuit is designed. To preventing the high impedance states (when both inputs are 1s or both 0s) one extra NMOS and PMOS transistors are added. The source of NMOS is connected to Cout, drain to Vdd and gate to Semi XNOR output and the source of PMOS to Cout, drain to ground and gate to Semi XOR output. To achieving the full swing ULP diode is used. This diode consists of one PMOS and one NMOS transistors as shown in Figure-6.

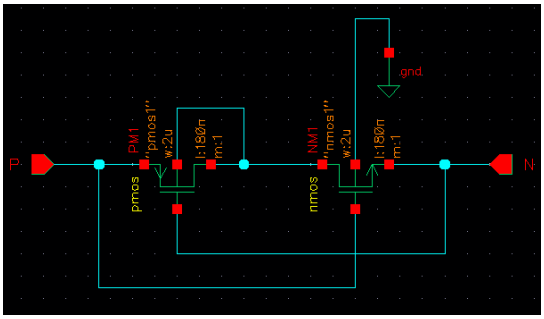


Fig.6 ULP Diode

It reduces the reverse leakage current while maintaining the same forward current in normal CMOS diode. The complete hybrid full adder as shown in Figure-7

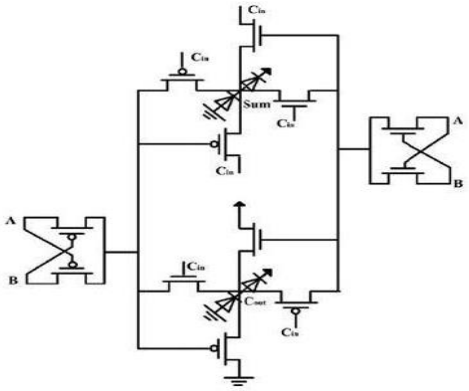
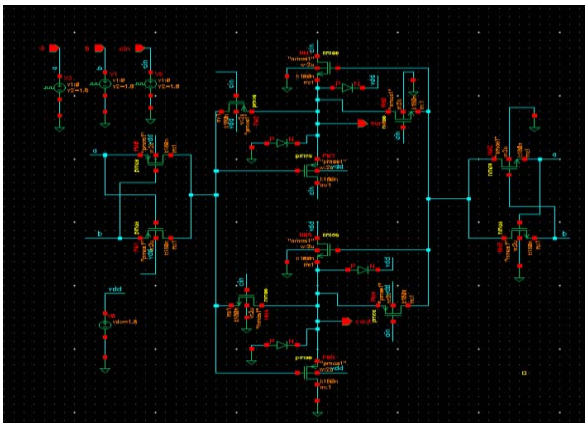


Fig.7 Hybrid full adder

Schematic diagram of hybrid Full adder in 180nm using cadence



3. Proposed Full adder

A new approach to eliminating the use of XOR and XNOR gates in full adder design is full adder using GDI-MUX and pass transistor. Using GDI-MUX technique AND, OR and multiplexer are implemented, by using this gates and pass transistor logic a new full adder is implemented as shown in Figure-8.

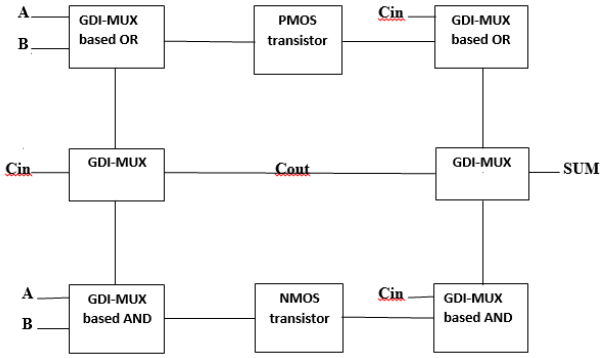


Fig.8 Another logical structure for designing full adder

The GDI (Gate Diffusion Input) cell consists of one PMOS and NMOS transistors. Its look like a static CMOS inverter but it differs because the GDI cell [11] has two extra inputs as shown in Figure-9.

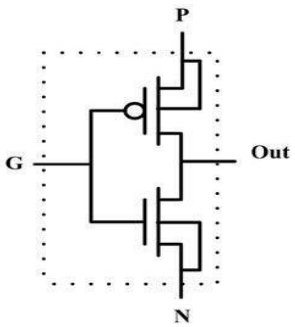


Fig.9 GDI cell

That extra two inputs are P (input to source/drain of PMOS) and N (input to source/drain of NMOS). The source terminals of

PMOS and NMOS are connected to Vdd and ground. The GDI-MUX based OR gate is modeled by connecting source/drain of NMOS (N input) to Vdd, common gate (G input) to A and P input to B. Similarly AND gate is designed by connecting N input to B, G to A and P input to GND. The basic principle is

For **OR** gate based on truth table
If (A==0)
Y= B;
Else if (A==1)
Y= 1 or Vdd

For **AND** gate based on truth table
If (A==0)
Y= 0 or Gnd;
else if (A==1)
Y= B;

From truth table of a full adder, we can consider that when Cin = 0, the full adder Cout is equal to A AND B otherwise it is equal to A OR B. By using multiplexer Cout is selected. As shown in table 3 and 4.

Table 3

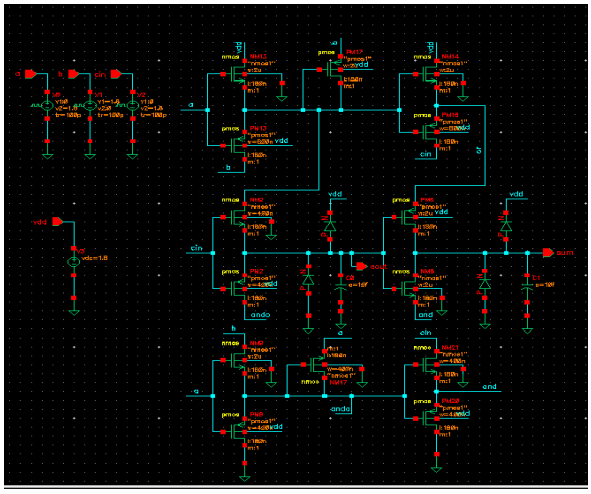
Cin	A	B	Cout = A AND B
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1

Table 4

Cin	A	B	Cout = A OR B
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

When Cout = 0, the sum is equal A OR B OR Cin otherwise sum is equal to A AND B AND Cin. The width and length ratio of PMOS and NMOS transistor in first GDI-MUX and second GDI-MUX based AND gate is 400n:180n. To achieving the full swing the width and length ratio is changed. And also the PMOS and NMOS pass transistors are added.

Schematic diagram of proposed Full adder in 180nm using cadence



4. Simulation and Results

All full adders are designed and simulated by using a Cadence Virtuoso in 180nm gpdk CMOS technology. Power dissipation is measured for different design techniques by varying voltage from 1.5 to 1.8V. The transient response of different full adders as shown in Figure-10 to Figure-1.

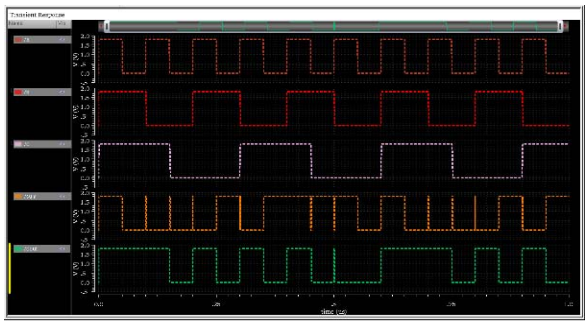


Fig.10 Transient response of C-CMOS full adder

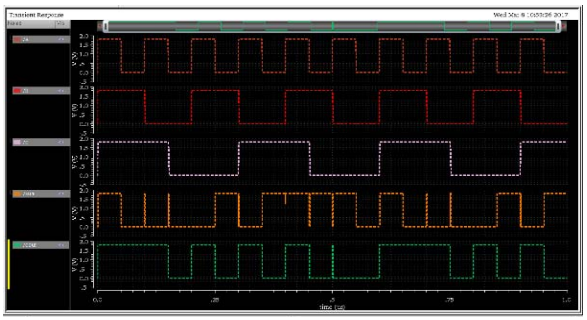


Fig.11 Transient response of CPL full adder

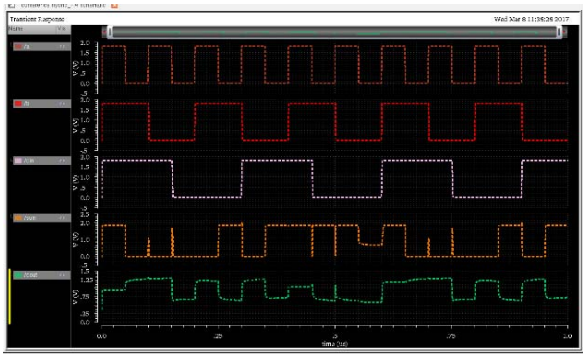


Fig.12 Transient response of Hybrid full adder

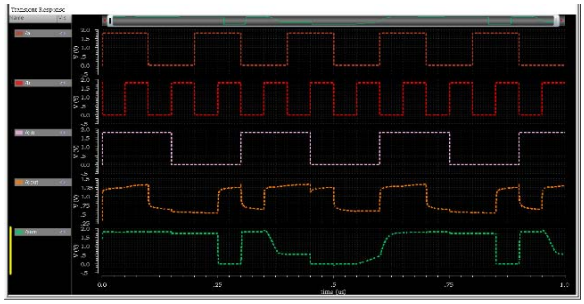


Fig.13 Transient response of proposed full adder

5. Observations

Power dissipation is calculated by varying supply voltage from 1.5 to 1.8V as shown in table-5.

Table 5

Supply Voltage (V)	CMOS (uW)	CPL (uW)	Hybrid CMOS (uW)	Proposed full adder (uW)
1.5	4.55	255.06	2.31	0.404
1.6	5.33	308.33	2.67	0.481
1.7	6.25	366.49	3.07	0.573
1.8	7.26	429.59	3.54	0.678

6. Conclusion

Various types of full adders are designed using different logic styles. These C-CMOS, CPL and hybrid full adders are compared with new proposed full adder. The hybrid and new proposed full adder consist of less number of transistors, because of less number of transistors results in less switching activity and area. Power consumption is increases with increasing supply voltage as shown in table 5.

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