Controlling the Ambipolar current by using Graded drain doped TFET

2023 International Conference on Device Intelligence, Computing and Communication Technologies, (DICCT) | 978-1-6654-7491-7/23/$31.00 ©2023 IEEE | DOI: 10.1109/DICCT56244.2023.10110171

Priyanka Dhiman
Electronics and Communication Engineering
Meerut Institute of Engineering and Technology
Meerut, India
priyanka.dhiman.mtec.2021@miet.ac.in

Kavindra Kumar Kavi
Electronics and Communication Engineering
Motilal Nehru National Institute of Technology Allahabad
Priyagraj, India
kkavi@mnnit.ac.in

Ratneshwar Kumar Ratnesh
Electronics and Communication Engineering
Meerut Institute of Engineering and Technology
Meerut, India
ratneshwar.ratnesh@miet.ac.in

Abhishek Kumar
Electronics and Communication Engineering
Meerut Institute of Engineering and Technology
Meerut, India
abhishek.ec@miet.ac.in

***Abstract*—A Graded Doped Drain TFET (GD-TFET) architecture is proposed in this work to suppress the ambipolar current that exists in Conventional TFET (C-TFET). This graded doping in the drain region improves off-state parameters like off-current, ambipolar current without affecting on-state parameters. The various parameters from different TFET structures like Doping-Less TFET (DL-TFET), Low Doped TFET (LD-TFET), Conventional TFET (C-TFET), and Graded Doping TFET (GD-TFET) are simulated and compared. It has been found that the proposed architecture offers superior suppression of ambipolar current without affecting others parameters. The architecture offers an ambient current of 7×10^{-15} A/µm which is far less than the other structure of 8×10^{-10} A/µm in the case of C-TFET. The structure also offers sub-threshold swing, transconductance, and on-to-off current ratio of 35.0628 mV/decade, 1.44×10^{-05} S and $6.40\times10^{+08}$ A/µm, respectively, which is comparable to C-TFET structure.**

Keywords—Ambipolariy, TFET, Subthreshold Swing, on current, off current, transconductance

I. INTRODUCTION

Moore's law drives the semiconductor industry toward continuous scaling of MOSFET devices. It results in improvement of device performance like power consumption, operating frequency, speed, etc., but it also brings various challenges like short channel effects, increased off current, low driving performance, etc. The increase in off current is due to the Boltzmann tyranny limit of sun 60 mV/decade subthreshold swing [1-15]. This off-current leads to significant static power consumption in CMOS devices.

The tunnel field effect transistor (TFET) is one of the candidates for the replacement of the conventional MOSFET due to its sub 60mV/decade swing (SS) [2]. TFET operation is based on a PIN diode that is sealed from the valence band to the conduction band of the source region . Due to gate-controlled tunneling, TFETs can achieve swings as low as 60 mV/decade. Also, the device has a very low leakage current (off current), making it a suitable device for low current circuits [3].

In spite of various advantages, the circuit suffers from ambipolar current, i.e., when biased with high negative gate voltage, the N-TFET behaves as if it is ON state instead of an off state. This high ambipolar current prevents its application CMOS circuit applications. The high drain current in high negatively biased gate is due to tunnelling from the drain to source region instead of vice-versa in case of N-TFET [4]. This ambipolar current results in the conduction of the circuit in an off condition also and thus must be reduced for proper operation of the circuit.

Various techniques, like gate engineering, spacer, drain engineering etc., are reported to reduce ambipolarity. In gate engineering, an additional gate called a tunnelling gate is used to control tunnelling current [5]. This current can also be controlled by using Underlap Gate-Drain TFET [3], [6] by increasing channel resistance near the drain. These methods require an additional gate/ area near the drain, which limits the scalability of the device [7-9]. The simplest and most popular method to suppress ambipolarity without affecting the scalability of the device is by using drain engineering. Some of the method includes like undoped drain (UD) [9-11], lightly doped drain (LD), pocket near drain [12-15], etc., have been reported. All these methods suppress ambipolarity at the cost of increased subthreshold swing.

A Graded Doped (GD) drain TFET is proposed in this work to suppress the ambient current. The result from the proposed work is also compared with popular drain engineering methods i.e., Undoped (UD) and Lightly Doped (LD) drain. The organization of the work is as follows: First proposed architecture and models used for the simulation is discussed in section 2, followed by the simulation results from the proposed architecture in section 3. The concluded of the work is drawn in section 4.

II. PROPOSED ARCHITECTURE

The schematic of the proposed Graded Drain (GD) structure is shown in Fig.1. The architecture is a double-gated topology with stacked dielectric for better gate control over the channel region. The thickness of silicon dioxide (SiO_2) and hafnium dioxide (HfO_2) is 1nm and 2nm, respectively, for all the simulations. The channel length, source doping, and channel doping are 50nm, 1×10^{20} $cm^{-3}$and 1×10^{10} cm^{-3}, respectively, and are constant for all the simulations except drain doping. The drain region is doped from 1×10^{16} to 1×10^{19} cm^{-3} in case of graded doping (GD-TFET), 1×10^{10} cm^{-3}in case of Lightly Doped (LD-TFET) and without doping in case of Doping-Less (DL-TFET) TFET structures. With positive gate voltage, the graded drain region acts as forward biased and thus allow flow of drain current without restriction. At negatively biased gate voltage, the graded drain acts as reverse biased junction and thus restrict flow of ambipolar current. Each graded region acts as separate reverse biased junction and thus decreases drain

current at negatively biased gate voltage. The various device parameters which are used for the design and simulating TFET is shown in Table.1. The Work function of the metal gate (φ_m) is considered to be 4.7 for the simulation.

The simulation has been done on 2-D ATLAS device simulator. The effect of band-to-band tunnelling is captured by adding a non-local Band to Band Tunnelling (BBT) model. Shockley-Read-hall and Auger recombination models are used for the minority recombination effect in addition to the band gap narrowing model.

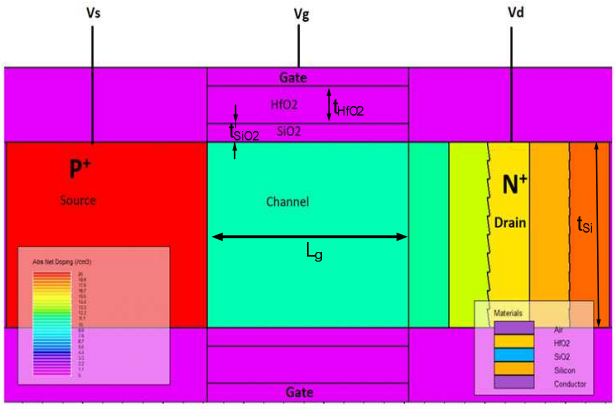

Fig.1. Proposed architecture of GD-TFET

Table 1. Device parameters used for the proposed design

Parameters	***Value***
Channel Length (nm)	50
Source Doping (cm^{-3})	1×10^{20}
Channel Doping (cm^{-3})	1×10^{10}
Drain Doping (Graded) (cm^{-3})	1×10^{16}, 1×10^{17}, 1×10^{18}, 1×10^{19}
t_{SiO2} (nm)	1
t_{HfO2} (nm)	2
t_{Si} (nm)	10
Gate Work-function (ϕ_m)	4.7 eV

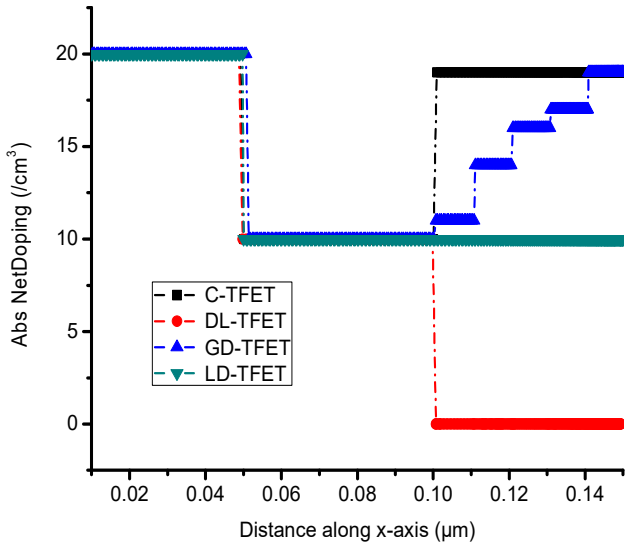

Fig.2. Variation of absolute doping along the x-axis

The variation of doping in different region for different TFET is shown in Fig.2. The doping of source and channel region is the same in the case of Conventional TFET (C-TFET), Doping Less TFET (DL-TFET), Low-Doped TFET (LD-TFET) and Graded Doping TFET (GD-TFET). The drain region is graded doped in the proposed GD-TFET, i.e., the doping is increasing from the channel towards the end of the drain region, which can be inferred from Fig. 2.

III. Results and Discussion

The simulation of all the structures i.e., C-TFET, DL-TFET, LD-TFET, and GD-TFET, has been simulated by using a 2-D ATLAS device simulator with all parameters as constant except drain doping. All the architecture under study uses a double-gated architecture with stacked dielectrics of SiO_2 and HfO_2. The energy band diagram in on condition for C-TFET, DL TFET, LD-TFET, and GD-TFET is shown in Figs. 3, 4, 5, and 6, respectively. From the figures, the tunnelling barrier width is the same in all architectures. Doping of the drain region decreases resistance and thus decreases the energy band at the drain side, which can be inferred from Fig. 3, and Fig. 6. Reducing drain doping increases resistance and energy band at the drain region, which can be visualized from Fig. 4 and Fig. 5.

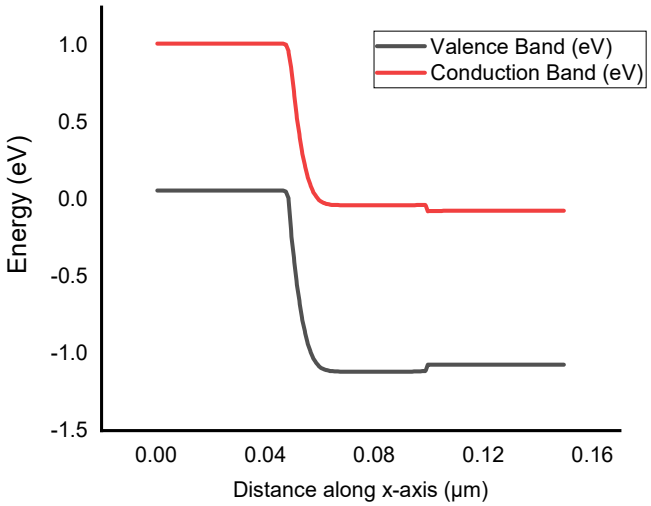

Fig. 3. Band diagram for Conventional TFET in ON condition

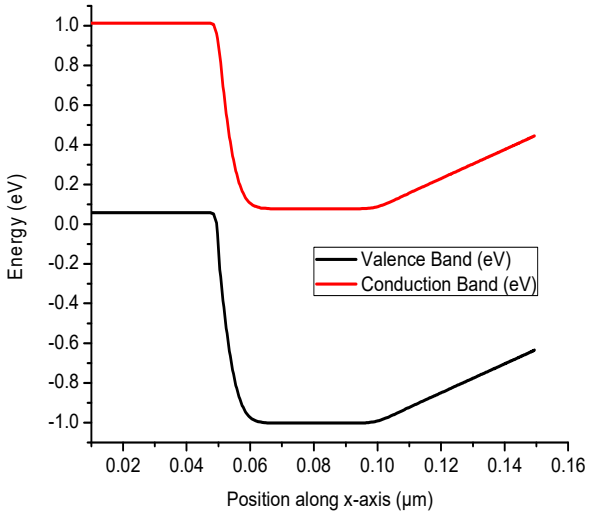

Fig.4. Band diagram for DL-TFET in ON condition

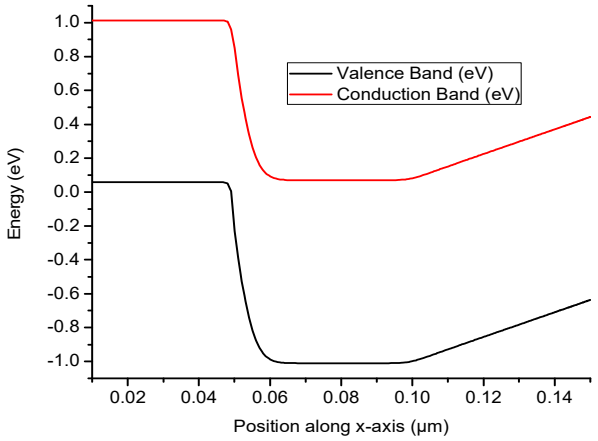

Fig.5. Band diagram for LD-TFET in ON condition

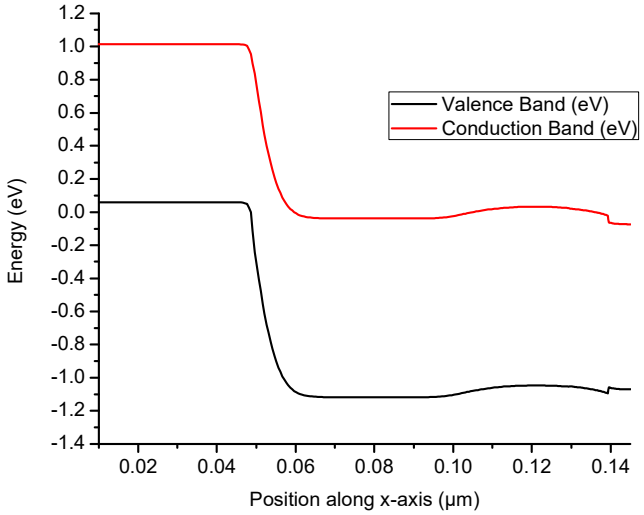

Fig. 6. Band diagram for GD-TFET in ON condition

The variation of drain current with the variation of gate voltage is shown in Fig. 7, and in log scale is shown in Fig. 8. In ON condition and at low voltage below the threshold voltage, the ON current is small but at higher gate voltage results in band to band tunnelling from source to drain region, and this process is same for all structures. In OFF condition or at increasing negative gate voltage, drain current increases due to tunnelling from the drain region, which can be visualized in Fig. 8. This drain current at higher negative gate voltage is called ambipolar current, which must be minimized. This current is minimized in the proposed GD-TFET, as shown in Fig. 8. At the negative-bias gate voltage, the drain is set to act as a reverse-biased junction, thereby limiting the flow of ambipolar current. Each level region acts as a separate reverse-bias junction, thereby reducing the drain current at the negative bias gate voltage. The ambipolar current in the case of GD-TFET is 1×10^{-15} A/μm which is much lesser than the ON current of 1×10^{-10} A/μm or ambient current of C-TEFT i.e., 1×10^{-13} A/μm. The proposed design reduces the ambient current significantly. The variation of the electric field along the length of the device from the source to the drain end is shown in Fig. 9. It is higher in the case of GD-TFET, which results in a higher ON current on a contrary to other designs.

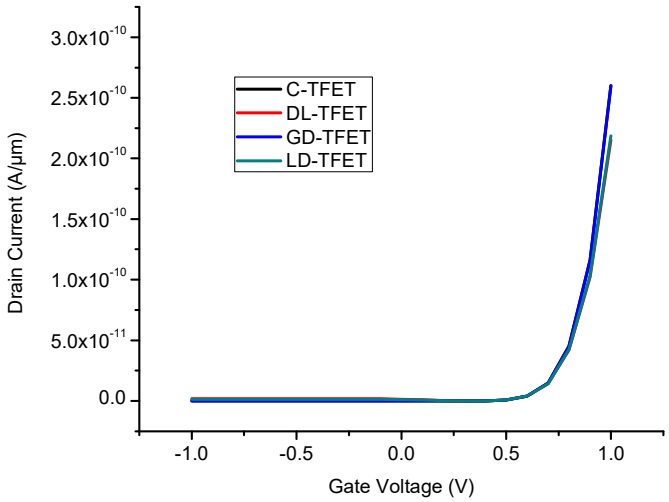

Fig. 7. Drain current with variation of gate voltage

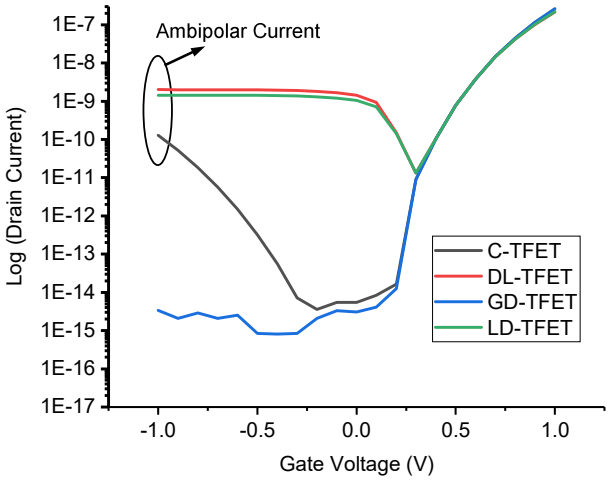

Fig. 8. Drain current with the variation of gate voltage

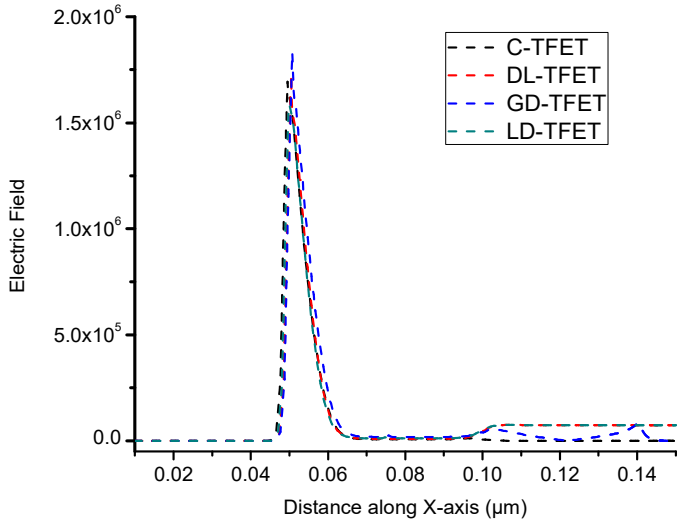

Fig. 9. Electric field along the x-direction

Table.2 Performance comparison for different TFET structures

Parameters	DL-TFET	LD-TFET	C-TFET	GD-TFET
On Current (Ion) (A/μm)	2.15×10^{-7}	2.19×10^{-7}	2.60×10^{-7}	2.60×10^{-7}
Off Current (Ioff) (A/μm)	1.32×10^{-11}	1.32×10^{-11}	8.38×10^{-16}	4.06×10^{-16}
Ion/Ioff	$1.63\times10^{+04}$	$1.66\times10^{+04}$	$3.10\times10^{+08}$	$6.40\times10^{+08}$
sub_vt_slope	17.052915	17.734584	27.3846	28.5203
sub_vt_swing (mV/decade)	58.641	56.387	36.5168	35.0628
g_m (S)	1.13×10^{-05}	1.15×10^{-05}	1.44×10^{-05}	1.44×10^{05}
Vth (V)	0.65	0.65	0.62	0.58

The comparison of different performance parameters for different TFET structures is shown in Table 2. The energy band of all TFET structure is similar and have the same barrier width and electric field from Figs. 3, 4, 5, 6, and 8, so all structures have almost the same ON current, which can be inferred from the performance comparison table. The proposed structure also has the lowest off current, consequently having the highest on-to-off current ratio. It also has the lowest sub-threshold swing of 35 mV/decade among all architectures. Transconductance (g_m) is one of the important parameters which defines the gain of the analog circuit. It should also be high for the device having a higher cutoff frequency. The maximum transconductance of the proposed circuit is also the highest among all the different designs of TFET under study. Thus the proposed circuit is also best suited for analog performance in terms of the gain of the circuit.

IV. Conclusion

A Graded Doped Drain (GD) TFET is proposed to suppress ambient current, which is present in conventional TFET (C-TFET). The proposed structure offers similar ON device parameters like on current, better subthreshold swing and slope, and lower off current. The ambient current of the proposed device is 7×10^{-15}A/μm, which is the lowest among different ambient current reduction methods. The proposed structure also offers a maximum transconductance of 1.44×10^{-05} S. Due to lower subthreshold swing, off current, ambient current, and higher transconductance, the proposed device is best suited for low power digital and analog circuit design and applications.

References

[1] A.Shaker, M.El Sabbagh, and M.M. El-Banna, "Influence of drain doping engineering on the ambipolar conduction and high-frequency performance of TFETs". ieee transactions on electron devices, 64(9), pp.3541-3547, 2017.

[2] Q.Wang, H.Liu, S.Wang, and S.Chen' "TCAD simulation of single-event-transient effects in L-shaped channel tunneling field-effect transistors". IEEE Transactions on Nuclear Science, 65(8), pp.2250-2259, 2018.

[3] K.Nigam, S.Gupta, S.Pandey, P.N.Kondekar and D.Sharma, "Controlling the ambipolarity and improvement of RF performance using Gaussian Drain Doped TFET". International Journal of Electronics, 105(5), pp.806-816, 2018.

[4] N.Bagga, A.Kumar, and S.Dasgupta, " Demonstration of a novel two source region tunnel FET". IEEE Transactions on Electron Devices, 64(12),pp.5256-5262, 2017.

[5] S.Saurabh, and M.J. Kumar, 2010." Novel attributes of a dual material gate nanoscale tunnel field-effect transistor". IEEE transactions on Electron Devices, 58(2) , pp.404-410, 2010.

[6] K.Boucart, and A.M.Ionescu, " Double-gate tunnel FET with high-k gate dielectric". IEEE transactions on electron devices, 54(7), pp.1725-1733 , 2007.

[7] C.K.Pandey, D.Dash, and S.Chaudhury, "Approach to suppress ambipolar conduction in Tunnel FET using dielectric pocket". Micro & Nano Letters, 14(1), pp.86-90, 2019.

[8] M.Saxena, and M.Gupta, "Undoped Drain Graded Doping (UDGD) based TFET design: An innovative concept". Micro and Nanostructures, 163, p.107147 , 2022.

[9] S.Garg, and S.Saurabh, "Suppression of ambipolar current in tunnel FETs using drain-pocket: Proposal and analysis". Superlattices and Microstructures, 113, pp.261-270, 2018.

[10] S.Afzal Ahmad and N.Alam, "Suppression of ambipolarity in tunnel - FETs using gate oxide as parameter: analysis and investigation". IET Circuits, Devices & Systems, 14(3), pp.288-293, 2020.

[11] N.Bagga, N.Chauhan, D.Gupta, and S.Dasgupta, " A novel twofold tunnel FET with reduced miller capacitance: proposal and investigation". IEEE Transactions on Electron Devices, 66(7), pp.3202-3208, 2019.

[12] M.Zhang, Y.Guo, J.Zhang, J.Yao and J.Chen, "Simulation study of the double-gate tunnel field-effect transistor with step channel thickness". Nanoscale Research Letters, 15(1), pp.1-9, 2020.

[13] Kumar, A., "Analog and RF performance of a multigate FinFET at nano scale. Superlattices and Microstructures, 100, pp.1073-1080, 2016.

[14] Kumar, A., "Analytical modelling of subthreshold characteristics of RE-GAA FinFET using center potential", Superlattices and Microstructures, 100, pp.1143-1150, 2016.

[15] Kumar, A. and Singh, S.S.,. "Optimizing FinFET parameters for minimizing short channel effects", In 2016 international conference on communication and signal processing (ICCSP) (pp. 1448-1451). IEEE, April 2016.