Switching Performance Analysis of 3.5 kV Ga_2O_3 Power FinFETs

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***Abstract*— This article presents switching performance analysis of a normally-off 3.5 kV β-Ga_2O_3 power FinFET using Silvaco TCAD simulation platform. The simulated electric field and OFF-state capacitances at a drain voltage (V_D) of 3.5 kV were compared for FinFETs with two different structures: (i) 30-nm-thick Al_2O_3 in the planar regions and partially-filled (PF) inter-fin areas and (ii) 130-nm-thick Al_2O_3 in the planar regions and fully-filled (FF) inter-fin areas. The FF FinFET showed a smaller OFF-state C_{GS} and C_{GD} and the thicker Al_2O_3 significantly reduced peak electric field at the corner of the fin. Therefore, via TCAD device-circuit-integrated model, the impact of electron mobility in the MOS channel, bulk fin and drift region, and the substrate thickness on the device switching performances were investigated on a single-fin FF FinFET structure. The device with 100-μm-thick substrate and ideal drift region and fin mobilities of 180 cm^2/Vs showed 82.6% improvement in the total switching time and 82.2% lower switching losses compared with the device which had thicker substrate thickness (600 μm) and lower electron mobilities in the drift region (130 cm^2/Vs), bulk fin (30 cm^2/Vs), and MOS channel (2 cm^2/Vs). Moreover, the switching performance of multifin FF FinFETs with different fin width/pitch ratio was studied. At a given pitch size of 700 nm, the total power loss of the input power at a frequency of 200 kHz was reduced from 0.83% to 0.61% as pitch ratio reduced from 57.1% to 14.3%. These findings provide helpful insights for design and fabrication of Ga_2O_3 FinFETs with enhanced switching performance for low-waste power conversion applications.**

***Index Terms*— Capacitance, FinFET, Gallium Oxide, power electronics, switching loss, TCAD modeling.**

I. Introduction

POWER converters are widely used in power systems for converting electrical energy from one form to another. Due to the continuous increase in requirements of power density and efficiency in power converters, the state-of-the-art Si-based power devices have reached their performance bottleneck, limited by the material properties. Wide and ultra-wide bandgap materials, such as GaN, SiC, and Ga_2O_3, are emerging as the next-generation semiconductors for high-power applications. Recently, β-Ga_2O_3 has attracted a great deal of attention for ultrahigh power applications, due to the combination of its ultrawide bandgap (4.9 eV), large critical electric field (~8 MV/cm), and large Baliga's figure of merit (BFOM) [1]–[5]. A higher BFOM is equivalent to a lower conduction loss at the same voltage rating, thus is highly preferable for efficient power switching applications. Apart from material properties, the availability of low-cost melt-grown bulk substrates is one of the main advantages of β-Ga_2O_3 that differentiates it from other emerging ultrawide bandgap semiconductors.

Various β-Ga_2O_3 transistors with promising characteristics have already been demonstrated [6]–[10]. For high-power switching applications, vertical device structures are preferred over lateral devices as they need less chip area, increase the number of devices per wafer, and simplify device design including current routing and packaging. Two types of vertical Ga_2O_3-based transistors have been reported to date, including current-aperture vertical electron transistors (CAVETs) [6], [6], [11], [12] and FinFETs [9], [10], [13], [14]. Among these devices, vertical FinFETs are particularly attractive as they do not require p-type doping. Moreover, the doping concentration and fin width can be designed such that fin channel is fully depleted which is desired for normally-off operation [15].

The vertical FinFET structure was first demonstrated in GaAs material system for RF applications by Mishra *et al.* [16], [17]. A vertical GaN power FinFET with submicrometer fin width was demonstrated in 2017 [18]. 1.2 kV vertical GaN power FinFETs were fabricated shortly after the first demonstration, with a record BFOM of 1440 MW/cm^2 and a switching FOM comparable to the state-of-the-art commercial 1.9–1.2 kV Si and SiC power transistors [19], [20]. More recently, a similar structure was adopted in β-Ga_2O_3 material system [13]. Record breakdown voltage over 2.6 kV was demonstrated on β-Ga_2O_3 FinFETs with BFOM of 280 MW/cm^2 [10]. Nevertheless, there is still a lack of knowledge on the switching performance of β-Ga_2O_3-based FinFETs and the extent to which various factors, such as electron mobility in the fin and the drift region, substrate thickness, and design parameters, can affect the switching performance and energy loss of these devices.

The highest electron mobility demonstrated in β-Ga_2O_3, so far, is ~180 cm^2/Vs for carrier density of 2.5×10^{16} cm^{-3}

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in films grown by metal–organic chemical vapor deposition (MOCVD) [21]. This is higher than what has been achieved in halide vapor phase epitaxy (HVPE) grown epi-structure (130 cm^2/Vs for a carrier density of 5×10^{16} cm^{-3}) [22]. Regardless, the electron mobility in the bulk fin is typically much lower (~30 cm^2/Vs) due to dry etch damage and sidewall depletion [13]. The electron mobility in the fin can, however, be significantly improved using techniques such as acid treatment [23] or sidewall regrowth [24]. Substrate resistance is another factor that adds to the device ON-resistance. Currently, commercially available n-type β-Ga_2O_3 substrates are ~600-μm thick with an electron density and mobility of $\sim 3 \times 10^{18}$ cm^{-3} and ~20 cm^2/ Vs, respectively [25], [26]. It is therefore of great importance to fully understand the impact of MOS channel, bulk fin, and drift region mobilities, and substrate thickness on the device characteristics and switching performance to better gauge the full potential of Ga_2O_3 FinFETs. Additionally, in a FinFET structure, the planar areas between fins add significantly to the OFF-state junction capacitances. It is, therefore, important to understand how the fin width/pitch size ratio affects the switching performance of these devices.

In this article, Silvaco ATLAS simulation platform was utilized for dc simulations and C–V analysis of Ga_2O_3 FinFETs. We first compared the peak electric field and OFF-state capacitances in FinFETs with three different structures: (i) 30-nm-thick Al_2O_3 in the planar regions and partially filled (PF) inter-fin areas, (ii) 130-nm-thick Al_2O_3 in the planar regions and PF inter-fin areas, and (iii) 130-nm-thick Al_2O_3 in the planar regions and fully-filled (FF) inter-fin areas. A double-pulse test circuit was then employed for switching analysis via TCAD device-circuit-integrated model [27]. Here, for the first time, the impact of electron mobility in the fin and drift region, substrate thickness, and fin width/pitch size ratio on the OFF-state capacitances and switching performance were studied.

II. Device Design and Simulation Framework

Fig. 1(a) shows the schematic of the first experimentally demonstrated E-mode Ga_2O_3 FinFET which has a 30-nm-thick Al_2O_3 as the gate insulator on the sidewalls and in the inter-fin areas and a PF SiO_2 spacer [9]. A new design is proposed here [shown in Fig. 1(b)], inspired by an earlier work on GaN power FinFETs [28], [29], with the inter-fin region FF by SiO_2, a planar source contact, and a 130-nm-thick Al_2O_3 gate insulator in the inter-fin areas. This new design with low-k dielectric full-filling the inter-fin areas can be fabricated utilizing plasma enhanced chemical vapor deposition (PECVD) or solution-based technique [30]. The thicker Al_2O_3 in the inter-fin area can be achieved by two separate atomic layer depositions (ALD) of Al_2O_3 as well as planarization technique as the following: First, 100-nm-thick ALD Al_2O_3 can be deposited uniformly. Then, a SiO_2 or photoresist planarization process can be performed to selectively etch away the Al_2O_3 on the sidewall and on top of the n+ Ga_2O_3 source and fin sidewalls using tetramethylammonium hydroxide (TMAH), in which the etch of Al_2O_3 with regard to SiO_2 is very selective. After SiO_2 removal, 30-nm-thick Al_2O_3 layer can be deposited by ALD to achieve 130-nm-thick and 30-nm-thick Al_2O_3 in the inter-fin area and sidewalls, respectively.

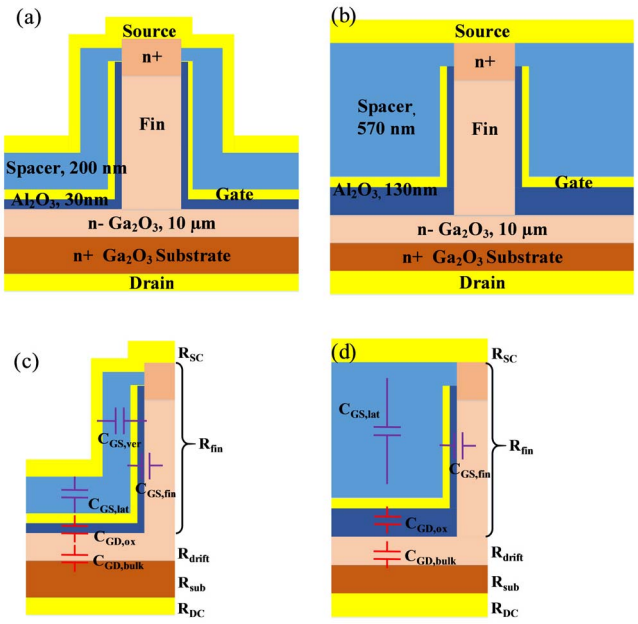

Fig. 1. Schematic cross section of Ga_2O_3 power FinFET with (a) PF interfin, (b) FF inter-fin and thicker dielectric layer in the inter-fin areas. Main capacitances and resistances in each structure are illustrated in (c) and (d). The fin and drift regions were kept identical for both structures with fin width of 100 nm, fin height of 700 nm, and drift region thickness of 10 μm. The "ver," "lat," and "ox" represent "vertical," "lateral," and "oxide," respectively.

TABLE I
PARAMETERS USED IN THE SIMULATION CALIBRATION

Parameters	Values
Average fin electron mobility (cm^2/Vs)	2
Drift region mobility (cm^2/Vs)	33
Bulk Ga_2O_3 electron mobility (cm^2/Vs)	20
Fin width (nm)	330
Fin height (nm)	770
n+ cap thickness (nm)	50
Drift region thickness (μm)	10
Bulk substrate thickness (μm)	600
Doping density (cm^{-3})	1.2×10^{16}

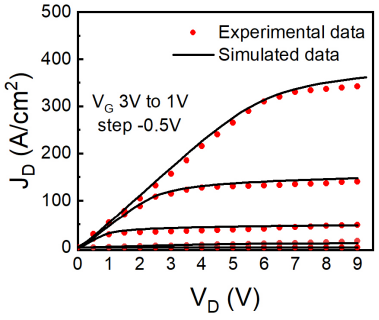

Fig. 2. Comparison of I–V output characteristics of the simulated and fabricated Ga_2O_3 power FinFETs. Copyright 2018 IEEE.

The 2-D TCAD simulations described in this article were performed using the Silvaco ATLAS simulator. The device physical models were established and calibrated based on experimental data in Ref [9]. A good agreement between experimental data and simulated results was achieved as

TABLE II
PARAMETERS USED IN THE PF AND FF FINFET SIMULATION

Parameters	Values
Average fin electron mobility (cm^2/Vs)	30
Drift region mobility (cm^2/Vs)	130
Bulk Ga_2O_3 electron mobility (cm^2/Vs)	20
Fin width (nm)	100
Fin height (nm)	700
Drift region thickness (μm)	10
Bulk substrate thickness (μm)	600
Doping density (cm^{-3})	5×10^{16}

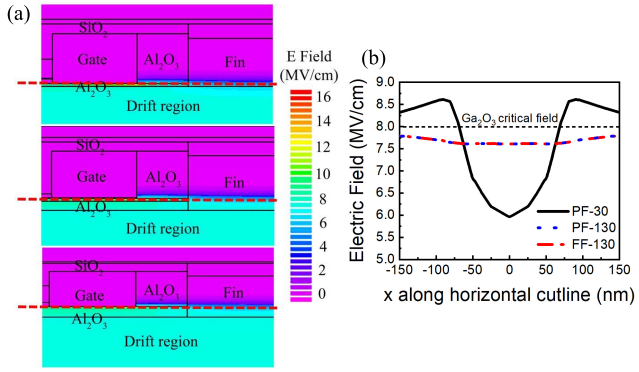

Fig. 3. (a) Simulated contour of electric field in PF-30 (top), PF-130 (middle), and FF-130 (bottom) Ga_2O_3 power FinFET at drain voltage (V_D) of 3.5 kV. (b) Simulated electric field along a horizontal cutline across the fin bottom PF-30 (top), PF-130 (middle), and FF-130 (bottom) Ga_2O_3 power FinFETs.

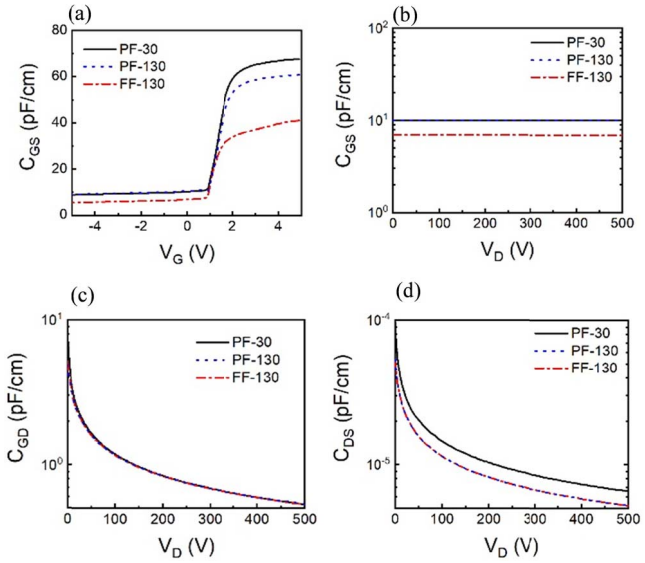

Fig. 4. (a) Gate–source capacitance (C_{GS}) as a function of gate voltage at zero drain voltage. (b) OFF-state gate–source capacitance (C_{GS}). (c) Gate–drain capacitance (C_{GD}). (d) Drain–source capacitance (C_{DS}) as a function of drain voltage at zero gate voltage for PF-30 (black solid line), PF-130 (blue dotted line), and FF-130 (red dash-dotted line) Ga_2O_3 power FinFETs.

shown in Fig. 2. The TCAD model was developed using the parameters depicted in Table I, as given in [9]. The carrier continuity equations and Poisson equations were solved self-consistently, considering carrier generation, drift-diffusion, electron saturation velocity, and complete dopant ionization. In order to simplify the simulation, no thermal models were implemented, as the simulation of electro-thermal effect needs additional consideration of heat dissipation regions and 3-D device periphery geometries. A lower current is expected under a high voltage bias when self-heating effect is included; known as current collapse effect.

PF and FF FinFETs were simulated assuming parameters shown in Table II. Since the fin and drift regions of FF-FinFET were kept identical to PF-FinFET, both devices resulted in a nearly identical ON-state dc characteristics such as threshold voltage (V_T) and ON-resistance (R_{ON}). Fig. 3(a) shows the simulated contour of electric field in Ga_2O_3 power FinFETs at drain voltage (V_D) of 3.5 kV in the OFF-state and Fig. 3(b) shows the corresponding electric field along a horizontal cutline across the fin bottom. The simulated devices include the PF-FinFET with Al_2O_3 gate insulator thicknesses of 30 and 130 nm, named as the PF-30 and PF-130, respectively; the FF-FinFET with 130-nm-thick Al_2O_3 layer in the inter-fin areas, named as FF-130. A thicker Al_2O_3 in the inter-fin areas in both PF-130 and FF-130 devices was found to reduce the voltage held in the Ga_2O_3 and consequently reduce peak electric field in the Ga_2O_3 under the OFF-state operation. The maximum electric field at the corner of fin was reduced from 8.6 MV/cm in the PF-FinFET with 30-nm-thick Al_2O_3 to 7.6 MV/cm in the PF- and FF-FinFETs with 130-nm-thick Al_2O_3. Given the critical electric field of Ga_2O_3 is around 8 MV/cm, the PF-30 FinFET is expected to breakdown at V_D less than 3.5 kV, whereas the peak electric field in the PF-130 and FF-130 FinFET remains under the critical breakdown field at this voltage.

The junction capacitances were also compared for these three different structures to study the impact of thicker Al_2O_3 layer in the inter-fin areas and FF-structure simultaneously. Fig. 4(a) depicts gate-to-source capacitance (C_{GS}) as a function of gate voltage (V_G) at zero drain voltage. C_{GS} plays a vital role as part of the input capacitance during device switching. C_{GS} in the device structure has components in both the inter-fin region and fin channel region [Figs. 1(c) and (d)]. The latter one depends on V_G while the former is only a parasitic component independent of V_G. In the OFF-state, C_{GS} is dominated by capacitance in the inter-fin region; whereas in the ON-state, it depends on both inter-fin region and accumulated electrons formed in the fin region. In both cases, a lower C_{GS} was observed in the FF-130 FinFET compared to the PF-130 and PF-30 FinFETs. When device is turned on, the PF-130 shows smaller gate–source capacitance compared with the PF-30 due to a thicker Al_2O_3 dielectric in the corner of the fin. We also studied the OFF-state C_{GS}, gate–drain (C_{GD}), and drain–source (C_{DS}) junction capacitances in these three structures. Fully filling the inter-fin area by SiO_2 reduced C_{GS} [Figs. 4(b)]. C_{GD} remained almost unaltered by either FF-structure or Al_2O_3 thickness in the inter-fin region. C_{DS} was nearly negligible in all device structures due to the screening effect of gate metal [Fig. 4(d)]. Nevertheless, increasing the Al_2O_3 thickness slightly decreased C_{DS}. Since FF-130 FinFET structure showed larger breakdown voltage and smaller junction capacitances, we focused on this structure for the rest of the studies presented here.

TABLE III
PARAMETERS OF DEVICES USED IN SINGLE-FIN ANALYSIS

Parameters	Values			
	A	B	C	D
MOS channel mobility	2	30	180	180
Bulk fin mobility (cm^2/Vs)	30	30	180	180
Drift region mobility (cm^2/Vs)	130	130	180	180
Bulk Ga_2O_3 electron mobility (cm^2/Vs)	20			
Fin width (nm)	100			
Fin height (nm)	700			
Drift region thickness (μm)	10			
Bulk substrate thickness (μm)	600	600	600	100
Doping density (cm^{-3})	5×10^{16}			

III. SINGLE-FIN ANALYSIS

To study the impact of electron mobility and substrate thickness on the switching performance of FF FinFETs, we simulated a single-fin structure shown in Fig. 1(b). Four devices were studied: For device A, substrate thickness (T_{sub}) and electron mobility in the drift region (μ_{drift}) were assumed to be 600 μm, and 130 cm^2/Vs [22]. Electron mobility in the bulk fin (μ_{fin}) and in the MOS channel (μ_{MOS}) adjacent to the sidewall were set to 30 cm^2/Vs [9] and 2 cm^2/V, respectively. This was to study the impact of sidewall roughness caused by etch damages during the device processing and the interface states at the Ga_2O_3/dielectric interface leading to lower electron mobility [13], [31]. In this case, the majority of the current flows through the bulk fin channel. In comparison, the MOS channel and bulk fin mobilities were both set to 30 cm^2/Vs in device B. Detailed discussion on ON-resistance and mobility analysis of vertical power FinFET can be found in [31]. In device C, electron mobilities in MOS channel, bulk fin, and the drift region were all assumed to be 180 cm^2/Vs which is the highest room-temperature mobility demonstrated for β-Ga_2O_3 [21] with the assumption that the device design and processing are improved to eliminate the detrimental impact of dry etching on electron mobility in the channel. As above-mentioned, the electron mobility in the fin can be significantly improved using techniques such as acid treatment, annealing [23] or sidewall regrowth [24]. For device D, T_{sub} was reduced to 100 μm, while the electron mobility was kept the same as in device C. Substrate thinning is expected to also reduce the self-heating effects although not studied in this article. Table III summarizes the parameters that were assumed in our simulations. A dielectric interface trap density (D_{it}) of 1.5×10^{12} cm^{-2} was assumed in all the presented calculations.

The transfer and output I–V characteristics are depicted in Fig. 5. These calculations suggest that increasing the mobilities, even to a maximum value demonstrated in Ga_2O_3, does not significantly improve the dc characteristic of Ga_2O_3 FinFETs. This is because the maximum electron mobility in β-Ga_2O_3 (180 cm^2/Vs) is much lower than what can be achieved in the drift region in other wide bandgap semiconductors such as GaN or SiC (~1000 cm^2/Vs). On the other hand, thinning the substrate in device D resulted in three times larger current density than that in device A, B, or C at V_G of 3 V. Additionally, a lower knee voltage in device D

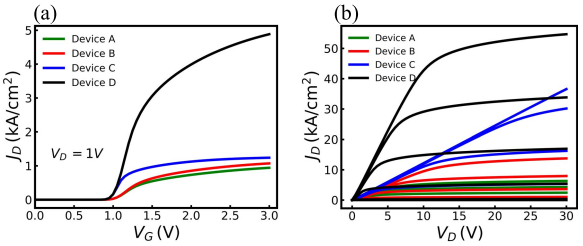

Fig. 5. (a) Transfer and (b) output I–V characteristics in Device A: T_{sub} = 600 μm, μ_{drift} = 130 cm^2/Vs, μ_{fin} = 30 cm^2/Vs, μ_{MOS} = 2 cm^2/Vs, Device B: T_{sub} = 600 μm, μ_{drift} = 130 cm^2/Vs, μ_{fin} = 30 cm^2/Vs, μ_{MOS} = 30 cm^2/Vs, Device C: T_{sub} = 600 μm, μ_{drift} = 180 cm^2/Vs, μ_{fin} = 180 cm^2/Vs, μ_{MOS} = 180 cm^2/Vs, and Device D: T_{sub} = 100 μm, μ_{drift} = 180 cm^2/Vs, μ_{fin} = 180 cm^2/Vs, μ_{MOS} = 180 cm^2/Vs. The gate voltage (V_G) in Fig. 5 (b) was swept from 0.5 to 2 V with a step of 0.25 V.

TABLE IV
COMPARISON OF SPECIFIC ON-RESISTANCE ($R_{ON,SP}$) IN DEVICE A: T_{SUB} = 600 μM, μ_{DRIFT} = 130 CM^2/Vs, μ_{FIN} = 30 CM^2/Vs, μ_{MOS} = 2 CM^2/Vs, DEVICE B: T_{SUB} = 600 μM, μ_{DRIFT} = 130 CM^2/Vs, μ_{FIN} = 30 CM^2/Vs, μ_{MOS} = 30 CM^2/Vs, DEVICE C: T_{SUB} = 600 μM, μ_{DRIFT} = 180 CM^2/Vs, μ_{FIN} = 180 CM^2/Vs, μ_{MOS} = 180 CM^2/Vs, AND DEVICE D: T_{SUB} = 100 μM, μ_{DRIFT} = 180 CM^2/Vs, μ_{FIN} = 180 CM^2/Vs, μ_{MOS} = 180 CM^2/Vs. $R_{ON,SP}$ IS NORMALIZED TO THE DEVICE CELL

	Device A	Device B	Device C	Device D
$R_{ON,sp}$ (mΩ·cm^2)	10.08	8.89	6.37	1.54

can be explained by the reduced substrate resistance, and consequently, a larger portion of the applied voltage being held in the drift region rather than the substrate.

Table IV shows a comparison of specific ON-resistance ($R_{ON,sp}$) in the three above-mentioned devices. $R_{ON,sp}$ was calculated by normalizing to the device cell. $R_{ON,sp}$ was reduced only 36.8% by increasing the electron mobility in the bulk fin, channel, and the drift region to 180 cm^2/Vs. However, $R_{ON,sp}$ reduced 75.8% by reducing the substrate thickness from 600 to 100 μm. These calculations indicate that a thick Ga_2O_3 substrate is not only undesirable because of its low thermal conductivity, but also because it adds significantly to the R_{ON} due to the low electron mobility (20 cm^2/Vs) in the substrate.

A 3.5 kV, 20 A double-pulse test circuit was implemented via Silvaco TCAD simulation framework to study the switching performance of these devices [Fig. 6(a)]. The Silvaco ATLAS device model was incorporated in the SPICE circuit by mixed-mode analysis. To expedite the simulations, the load was modeled as a current source and an ideal freewheeling diode was implemented in the circuit following [32]. The gate resistance (R_G) was set at 1.5 Ω for all the simulations. The gate driver turn-on and turn-off signal level were set at 3 and 0 V, respectively.

Fig. 6(b) shows the switching waveforms during the turn-off transient. In device A, the fall time (t_f) is 184.7 ns, and the turn-off $\Delta v/\Delta t$ is 18.95 kV/μs. The total gate charge is 2.02 μC, including a Q_{GD} of 1.99 μC. In device D, the fall time (t_f) is 33.8 ns, and the turn-off $\Delta v/\Delta t$ is 103.6 kV/μs. The total gate charge was 367 nC, including a Q_{GD} of 362.3 nC. In the device turn-off process, once gate is discharged and reaches the Miller gate plateau voltage, drain starts charging,

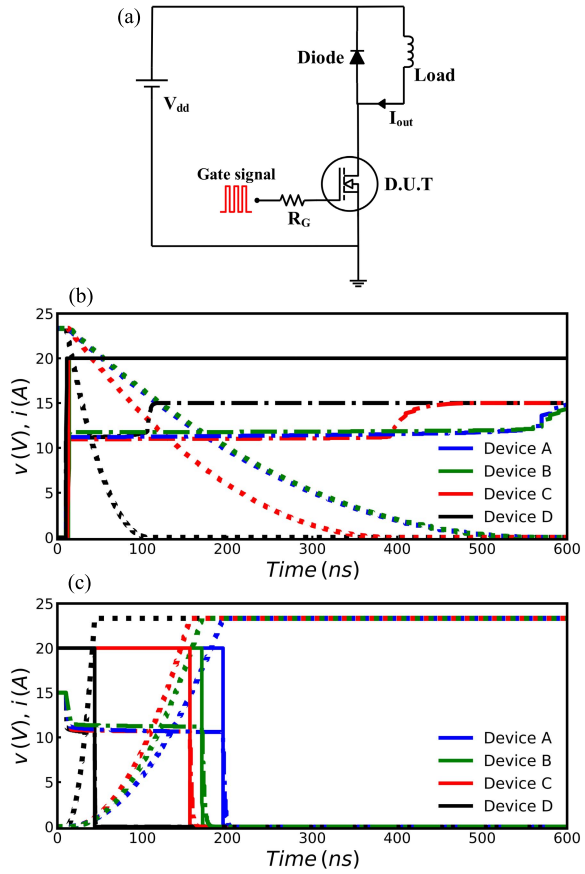

Fig. 6. (a) Schematic of double-pulse circuit implemented in the mixed-mode TCAD simulation. Simulated (b) turn-off and (c) turn-on waveforms in Device A, B, C, and D.

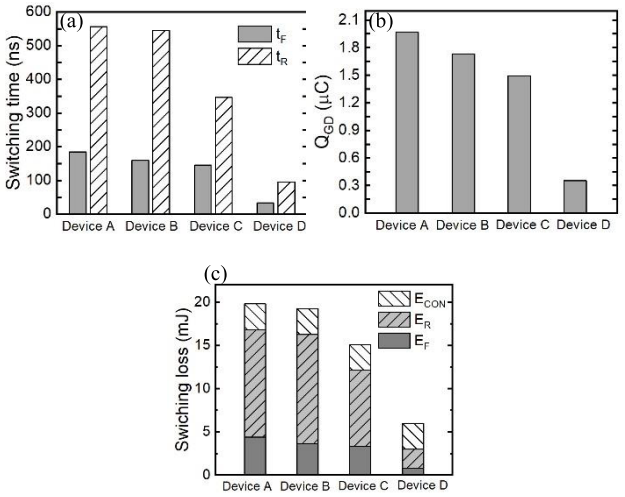

Fig. 7. Key switching metrics extracted from the simulated double-pulse testing waveforms in Device A, B, C, and D, including (a) fall time (t_F) and rise time (t_R), (b) gate–drain charge Q_{GD}, and (c) turn-off energy loss (E_F), turn-on energy loss (E_R), and conduction energy loss (E_{CON}) at switching frequency of 10 kHz.

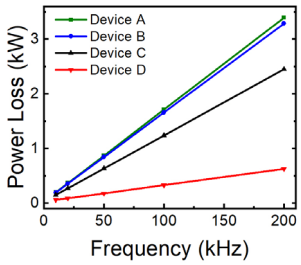

Fig. 8. Power loss as a function of frequency from 10 to 200 kHz in Device A: $T_{sub} = 600$ μm, $\mu_{drift} = 130$ cm^2/Vs, $\mu_{fin} = 30$ cm^2/Vs, Device B: $T_{sub} = 600$ μm, $\mu_{drift} = 180$ cm^2/Vs, $\mu_{fin} = 180$ cm^2/Vs, and Device C: $T_{sub} = 100$ μm, $\mu_{drift} = 180$ cm^2/Vs, $\mu_{fin} = 180$ cm^2/Vs. The input voltage was 3500 V, and the load current was 20 A.

presented by a V_D rise from V_{ON} up to V_{DD} in the Miller Plateau. After the drain is fully charged, the load current decreases to zero and channel is turned off. V_G also continues to decrease and reaches 0 V. The total fall time consists of Miller Plateau time and the time in which load current reaches zero. The Miller Plateau is the major component of switching time and, therefore, switching loss [33]. The reduced Miller plateau time and its corresponding fall time in device C are attributed to a reduced C_{GD} ($t = C_{GD} \times V_D/i_G$) in this device due to higher electron mobility in the fin and drift regions and lower series resistances because of the thinner substrate. A comparison between fall times in device A, B, C, and D shows that substrate thinning is important to reduce the switching time. These steps occur in reverse during the device turn-on process. The turn-on switching waveforms of these three devices are shown in Fig. 6(c). Device D had a total rise time of 95 ns, which is 82.9% lower than that in device A.

Fig. 7 depicts the key switching metrics, including fall time (t_F), rise time (t_R), turn-off energy loss (E_F), and turn-on energy loss (E_R), as well as gate–drain charge (Q_{GD}). The switching frequency was 10 kHz for calculation of energy loss. Device D with 100-μm-thick substrate and ideal drift region and fin mobilities of 180 cm^2/Vs showed 82.6% improvement in the total switching time and 82.2% lower switching losses compared with Device A which had thicker substrate thickness (600 μm) and lower electron mobilities in the drift region (130 cm^2/Vs), bulk fin (30 cm^2/Vs), and MOS channel (2 cm^2/Vs).

Fig. 8 shows the total switching energy loss as a function of operating frequency ranging from 10 to 200 kHz. For a certain power loss, device D yielded four times larger switching frequency compared to that with device A/B/C which has lower electron mobilities and/or thicker substrate. The total power losses of device A, B, C, and D were 4.85%, 4.69%, 3.50%, and 0.89%, respectively, of the input power at a frequency of 200 kHz. It is important to note that in this section the goal was to study the impact of intrinsic parameters on the switching frequency of these devices. Hence, a single-fin structure was employed to enhance the computation speed. Additionally, an arbitrary length (1 μm) was chosen for the planar sections on each side of fin, which contributed significantly to the OFF-state junction capacitances. In Section IV, we studied the impact of fin width/ pitch size ratio on the switching performance of these devices.

IV. Multi-Fin Analysis

A double-fin unit cell (Fig. 9) was implemented to further investigate the impact of fin width/pitch size ratio on the switching performance in the multiple fin systems. For this

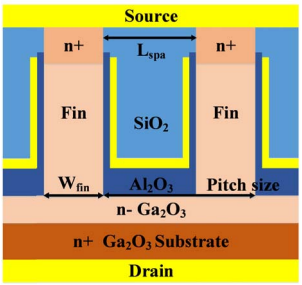

Fig. 9. Schematic cross section of unit cell of Ga_2O_3 power FinFETs.

TABLE V

PARAMETERS OF DEVICES USED IN THE MULTIFIN ANALYSIS. THE DEVICES WITH FIN WIDTHS OF 100, 200, 300, AND 400 NM AT A GIVEN PITCH SIZE OF 700 NM WERE NAMED AS THE W_{FIN}-100, W_{FIN}-200, W_{FIN}-300, AND W_{FIN}-400, RESPECTIVELY. THE INPUT VOLTAGE WAS 3000 V, AND THE LOAD CURRENT WAS 20 A. $R_{ON,SP}$ WAS CALCULATED BY NORMALIZING TO THE DEVICE ACTIVE AREA

Parameters	W_{fin}-100	W_{fin}-200	W_{fin}-300	W_{fin}-400
Fin-to-fin spacing (L_{spa}) (nm)	600	500	400	300
Pitch ratio (W_{fin}/Pitch size)	14.3%	28.6%	42.9%	57.1%
Doping in the fin (cm^{-3})	5×10^{16}	2×10^{16}	8×10^{15}	5×10^{15}
Doping in the drift region (cm^{-3})	5×10^{16}	5×10^{16}	5×10^{16}	5×10^{16}
V_{BR} (V)	>3500	>3500	>3500	>3500
V_T (V)	~1.0	~1.0	~1.0	~1.0
$R_{ON,sp}$ ($m\Omega\cdot cm^2$)	3.76	3.58	3.55	3.54

purpose, the pitch size was fixed at 700 nm for all the simulations. This fixed pitch size ensures the same total die size, and hence, a fair comparison of dc and switching performance between different devices. Therefore, to change fin width/pith size ratio, the fin width and the fin-to-fin spacing were varied as shown in Table V.

Table V shows device parameters and corresponding dc characteristics in devices with various fin widths and fin-to-fin spacings. The substrate thickness was set at 100 μm, and the electron mobility in both fin and the drift was 180 cm^2/Vs. The doping in the fin was reduced as the fin width increased to keep V_T constant and equal to 1 V for a fair comparison, while the doping in the drift region was 5×10^{16} cm^{-3} for all the devices. The doping in the fin can be tuned in practice by epitaxial growth using molecular beam epitaxy (MBE) or MOCVD. Similar R_{ON} and V_T were observed in these devices. It is important to note that, unlike single-fin simulations presented earlier, in this section $R_{ON,\,sp}$ was calculated by normalizing to the total die size to draw a fair comparison between devices with different fin widths. Therefore, $R_{ON,\,sp}$ reported in this section are higher than those reported for the single-fin structure.

The switching performance was studied using the same double test circuit as discussed before. The length of unit cell was adjusted to keep R_{ON} equal to 75 mΩ for all the simulations presented here. The switching frequency was 10 kHz for calculation of energy loss. The input voltage was 3000 V, and the load current was 20 A. As shown in Fig. 10, the total switching time and switching losses reduced 23.3% and 12.7%, respectively, in the device with 400-nm fin width (pitch ratio of 57.1%) compared with that in the device with fin width of 100 nm (pitch ratio of 14.3%). This can be explained by the

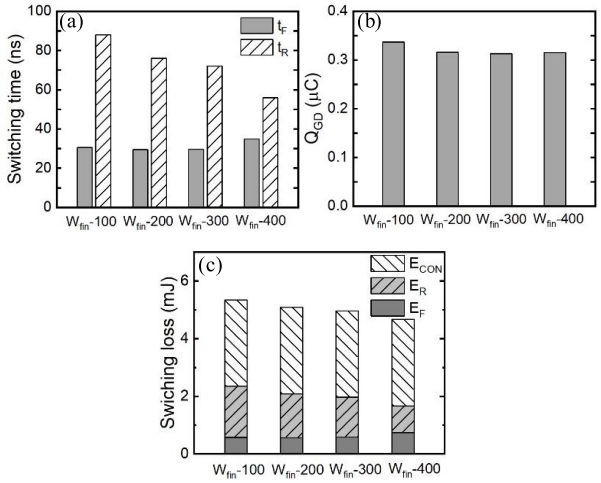

Fig. 10. Key switching metrics extracted from the simulated double-pulse testing waveforms in Ga_2O_3 power FinFETs devices with fin widths of 100, 200, 300, and 400 nm at a given pitch size of 700 nm. The key metrics include (a) fall time (t_F) and rise time (t_R), (b) gate-drain charge Q_{GD}, and (c) turn-off energy loss (E_F), turn-on energy loss (E_R), and conduction energy loss (E_{CON}). The input voltage was 3000 V, and the load current was 20 A.

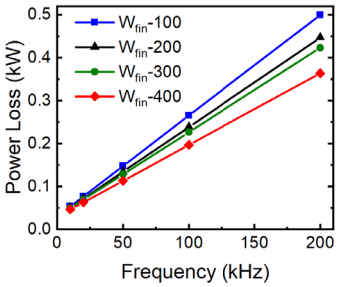

Fig. 11. Power loss as a function of frequency ranging from 10 to 200 kHz in Ga_2O_3 power FinFETs devices with fin widths of 100, 200, 300, and 400 nm at a given pitch size of 700 nm.

reduction in the junction capacitances in the inter-fin region as L_{spa} was reduced in the device with larger fin width.

Fig. 11 shows the total switching energy loss as a function of operating frequency ranging from 10 to 200 kHz. The total power losses of W_{fin}-100, W_{fin}-200, W_{fin}-300, and W_{fin}-400 were 0.83%, 0.74%, 0.70%, and 0.61% of the input power at frequency of 200 kHz, respectively.

Switching FOM ($R_{ON} \cdot Q_{GD}$) of 21.9 nC·Ω was achieved on the Ga_2O_3 power FinFET with 400-nm fin width and 300-nm fin-to-fin spacing operating at 3 kV and 20 A. Currently available state-of-art 3.3 kV SiC devices exhibit switching FOM measured at 1 kV of ~7 nC·Ω (GeneSiC, G2R120MT33J) [34]. At 3 kV one anticipates that the Q_{GD} should increase by a factor of square root three which is ~12 nC·Ω. This highlights that further scaling is necessary to reduce parasitic R_{ON} (further substrate thinning) and parasitic Q_{GD} (tighter fin pitch) to be able to fully access the benefit of Gallium Oxide. This will be a basis of future study.

V. CONCLUSION

In this article, we designed a normally-off β-Ga_2O_3 FinFET with 3.5 kV breakdown voltage. The simulated electric field and OFF-state capacitances at V_D of 3.5 kV were compared using Silvaco TCAD simulation platform for two structures: (i) PF FinFET and (ii) FF FinFET with thicker dielectric in

the inter-fin areas. The FF FinFET showed a smaller OFF-state C_{GS}. Also, the thicker Al_2O_3 in the inter-fin area in this device structure significantly reduced peak electric field at the corner of fin. The switching performance of β-Ga_2O_3 FinFETs was studied, for the first time, on the FF structure. The impact of electron mobility in the fin and the drift region, substrate thickness, and fin width/pitch ratio on the rise/fall time as well as total switching loss was investigated. The device with 100-μm-thick substrate and ideal drift region, bulk fin, and MOS channel mobilities of 180 cm^2/Vs achieved 82.6% improvement in the total switching time and 82.2% lower switching losses in 3.5 kV switching operation. Moreover, the total power loss of the input power at a frequency of 200 kHz was reduced from 0.83% to 0.61% as pitch ratio reduced from 57.1% to 14.3% at a given pitch size of 700 nm. These findings show great promise for β-Ga_2O_3 power transistors and provide helpful insights for design of Ga_2O_3 FinFETs with enhanced characteristics.

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REFERENCES

[1] R. Roy, V. G. Hill, and E. F. Osborn, "Polymorphism of Ga_2O_3 and the system Ga_2O_3—H_2O," *J. Amer. Chem. Soc.*, vol. 74, no. 3, pp. 719–722, Feb. 1952, doi: 10.1021/ja01123a039.

[2] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Lett.*, vol. 10, no. 10, pp. 455–457, Oct. 1989, doi: 10.1109/55.43098.

[3] M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Gallium oxide (Ga_2O_3) metal-semiconductor field-effect transistors on single-crystal β-Ga_2O_3 (010) substrates," *Appl. Phys. Lett.*, vol. 100, no. 1, Jan. 2012, Art. no. 013504, doi: 10.1063/1.3674287.

[4] E. Ahmadi and Y. Oshima, "Materials issues and devices of α and β-Ga_2O_3," *J. Appl. Phys.*, vol. 126, no. 16, Oct. 2019, Art. no. 160901, doi: 10.1063/1.5123213.

[5] A. Jian, K. Khan, and E. Ahmadi, "β-$(Al,Ga)_2O_3$ for high power applications—A review on material growth and device fabrication," *Int. J. High Speed Electron. Syst.*, vol. 28, Mar. 2019, Art. no. 1940006, doi: 10.1142/S0129156419400068.

[6] M. H. Wong, H. Murakami, Y. Kumagai, and M. Higashiwaki, "Enhancement-mode β-Ga_2O_3 current aperture vertical MOSFETs with N-Ion-implanted blocker," *IEEE Electron Device Lett.*, vol. 41, no. 2, pp. 296–299, Feb. 2020, doi: 10.1109/LED.2019.2962657.

[7] S. Sharma, K. Zeng, S. Saha, and U. Singisetti, "Field-plated lateral Ga_2O_3 MOSFETs with polymer passivation and 8.03 kV breakdown voltage," *IEEE Electron Device Lett.*, vol. 41, no. 6, pp. 836–839, Jun. 2020, doi: 10.1109/LED.2020.2991146.

[8] K. D. Chabak *et al.*, "Recessed-gate enhancement-mode β-Ga_2O_3 MOSFETs," *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 67–70, Jan. 2018, doi: 10.1109/LED.2017.2779867.

[9] Z. Hu *et al.*, "Enhancement-mode Ga_2O_3 vertical transistors with breakdown voltage >1 kV," *IEEE Electron Device Lett.*, vol. 39, no. 6, pp. 869–872, Jun. 2018, doi: 10.1109/LED.2018.2830184.

[10] W. Li, K. Nomoto, Z. Hu, T. Nakamura, D. Jena, and H. G. Xing, "Single and multi-fin normally-off Ga_2O_3 vertical transistors with a breakdown voltage over 2.6 kV," in *IEDM Tech. Dig.*, Dec. 2019, p. 12, doi: 10.1109/IEDM19573.2019.8993526.

[11] M. H. Wong *et al.*, "First demonstration of vertical Ga2O3 MOSFET: Planar structure with a current aperture," in *Proc. 75th Annu. Device Res. Conf. (DRC)*, Jun. 2017, pp. 4–5, doi: 10.1109/DRC.2017.7999413.

[12] M. H. Wong, K. Goto, H. Murakami, Y. Kumagai, and M. Higashiwaki, "Current aperture vertical β-Ga_2O_3 MOSFETs fabricated by N- and Si-ion implantation doping," *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 431–434, Mar. 2019, doi: 10.1109/LED.2018.2884542.

[13] Z. Hu *et al.*, "Breakdown mechanism in 1 kA /cm^2 and 960 V E-mode β-Ga_2O_3 vertical transistors," *Appl. Phys. Lett.*, vol. 113, no. 12, pp. 3–8, 2018, doi: 10.1063/1.5038105.

[14] Z. Hu *et al.*, "1.6 kV vertical Ga_2O_3 FinFETs with source-connected field plates and normally-off operation," in *Proc. 31st Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May 2019, pp. 483–486, doi: 10.1109/ISPSD.2019.8757633.

[15] Y. Zhang and T. Palacios, "(Ultra) wide-bandgap vertical power FinFETs," *IEEE Trans. Electron Devices*, vol. 67, no. 10, pp. 3960–3971, Oct. 2020, doi: 10.1109/TED.2020.3002880.

[16] U. Mishra, P. A. Maki, J. R. Wendt, W. Schaff, E. Kohn, and L. F. Eastman, "Vertical electron transistor (VET) in GaAs with a heterojunction (AlGaAs-GaAs) cathode," *Electron. Lett.*, vol. 20, no. 3, p. 145, 1984, doi: 10.1049/el:19840098.

[17] E. Kohn, U. Mishra, and L. F. Eastman, "Short-channel effects in 0.5-μm source-drain spaced vertical GaAs FET's—A first experimental investigation," *IEEE Electron Device Lett.*, vol. 4, no. 4, pp. 125–127, Apr. 1983, doi: 10.1109/EDL.1983.25672.

[18] M. Sun, Y. Zhang, X. Gao, and T. Palacios, "High-performance GaN vertical fin power transistors on bulk GaN substrates," *IEEE Electron Device Lett.*, vol. 38, no. 4, pp. 509–512, Apr. 2017, doi: 10.1109/LED.2017.2670925.

[19] Y. Zhang *et al.*, "1200 V GaN vertical fin power field-effect transistors," in *IEDM Tech. Dig.*, Dec. 2017, pp. 9.2.1–9.2.4, doi: 10.1109/IEDM.2017.8268357.

[20] Y. Zhang *et al.*, "Large area 1.2 kV GaN vertical power FinFETs with a record switching figure-of-merit," *IEEE Electron Device Lett.*, vol. 40, no. 1, pp. 75–78, Jan. 2019, doi: 10.1109/LED.2018.2880306.

[21] Z. Feng, A. F. M. A. U. Bhuiyan, M. R. Karim, and H. Zhao, "MOCVD homoepitaxy of Si-doped (010) β-Ga_2O_3 thin films with superior transport properties," *Appl. Phys. Lett.*, vol. 114, no. 25, Jun. 2019, Art. no. 250601, doi: 10.1063/1.5109678.

[22] K. Goto *et al.*, "Halide vapor phase epitaxy of Si doped β-Ga_2O_3 and its electrical properties," *Thin Solid Films*, vol. 666, pp. 182–184, Nov. 2018, doi: 10.1016/j.tsf.2018.09.006.

[23] W. Li, K. Nomoto, Z. Hu, D. Jena, and H. G. Xing, "Fin-channel orientation dependence of forward conduction in kV-class Ga_2O_3 trench Schottky barrier diodes," *Appl. Phys. Express*, vol. 12, no. 6, Jun. 2019, Art. no. 061007, doi: 10.7567/1882-0786/ab206c.

[24] C. Gupta, S. H. Chan, Y. Enatsu, A. Agarwal, S. Keller, and U. K. Mishra, "OG-FET: An *in-situ O* xide, *G* aN interlayer-based vertical trench MOSFET," *IEEE Electron Device Lett.*, vol. 37, no. 12, pp. 1601–1604, Dec. 2016, doi: 10.1109/LED.2016.2616508.

[25] S.-H. Han, A. Mauze, E. Ahmadi, T. Mates, Y. Oshima, and J. S. Speck, "N-type dopants in (001)β-Ga_2O_3 grown on (001)β-Ga_2O_3 substrates by plasma-assisted molecular beam epitaxy," *Semiconductor Sci. Technol.*, vol. 33, no. 4, Apr. 2018, Art. no. 045001, doi: 10.1088/1361-6641/aaae56.

[26] *Wide Bandgap Ga_2O_3 MOSFET*. Accessed: May 28, 2020. [Online]. Available: https://www.silvaco.com/examples/tcad/section33/example17/index.html

[27] D. Ji and S. Chowdhury, "A discussion on the DC and switching performance of a gallium nitride CAVET for 1.2kV application," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Nov. 2015, pp. 174–179, doi: 10.1109/WiPDA.2015.7369308.

[28] H. Wang, M. Xiao, K. Sheng, T. Palacios, and Y. Zhang, "Switching performance evaluation of 1200 V vertical GaN power FinFETs," in *Proc. IEEE 7th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Oct. 2019, pp. 314–318, doi: 10.1109/WiPDA46397.2019.8998850.

[29] H. Wang, M. Xiao, K. Sheng, T. Palacios, and Y. Zhang, "Switching performance analysis of vertical GaN FinFETs: Impact of inter-fin designs," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, Mar. 12, 2020, doi: 10.1109/JESTPE.2020.2980445.

[30] Z. Liu, X. Zhang, T. Murakami, and A. Fujishima, "Sol–gel SiO_2/TiO_2 bilayer films with self-cleaning and antireflection properties," *Sol. Energy Mater. Sol. Cells*, vol. 92, no. 11, pp. 1434–1438, Nov. 2008, doi: 10.1016/j.solmat.2008.06.005.

[31] M. Xiao, T. Palacios, and Y. Zhang, "ON-resistance in vertical power FinFETs," *IEEE Trans. Electron Devices*, vol. 66, no. 9, p. 3909, Sep. 2019, doi: 10.1109/TED.2019.2928825.

[32] D. Ji, Y. Yue, J. Gao, and S. Chowdhury, "Dynamic modeling and power loss analysis of high-frequency power switches based on GaN CAVET," *IEEE Trans. Electron Devices*, vol. 63, no. 10, pp. 4011–4017, Oct. 2016, doi: 10.1109/TED.2016.2601559.

[33] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York, NY, USA: Springer, 2008.

[34] *GeneSiC, G2R120MT33J*. Accessed: Dec. 6, 2020. [Online]. Available: https://www.genesicsemi.com/sic-mosfet/G2R120MT33J/G2R120MT33J.pdf