Applied Physics A (2019)125:353
https://doi.org/10.1007/s00339-019-2650-5

Applied Physics A
Materials Science & Processing

Dual-material dual-oxide double-gate TFET for improvement in DC characteristics, analog/RF and linearity performance

Satyendra Kumar[1] · Km. Sucheta Singh[1] · Kaushal Nigam[1] · Vinay Anand Tikkiwal[1] · Bandi Venkata Chandan[2]

Received: 3 February 2019 / Accepted: 17 April 2019

Abstract
To overcome the problem of fabrication complexity and to reducei the cost of microelectronic devices, a new concept of dual-material control gate with dual-oxide tunnel field-effect transistor is investigated. A stack gate approach is applied to reduce the width of tunneling barrier at source–channel junction. Use of dual oxides at source–channel interface provides improved capacitive coupling, which enhances the on-state current. The entire gate segment has been partitioned into three parts, namely tunnel gate (M_1), control gate (M_2) and auxiliary gate (M_3) with different work functions such as ϕ_1, ϕ_2 and ϕ_3. In this context, to keep dual-work functionality, the feasible combinations of these work functions are adopted. Technology computer- aided design (TCAD) simulations of these proposed combinations of work functions along with dual oxides provide better results for the combinations of ($\phi_1 = \phi_3 < \phi_2$). In addition, comparison between these combinations on the basis of analog/RF performance is done in this work. This work shows improved analog/RF parameters such as g_m, C_{gs}, C_{gd},f_T and TFP, and linearity parameters including g_{m3}, VIP3, IIP3 and IMD3 for the proposed device DMDODG-TFET (dual-material dual-oxide double-gate TFET). The use of this proposed device structure reduces the ambipolar behavior and subthreshold swing (18.5 mV/deacde), and enhances the on-current [3.6×10^{-5} ($A/\mu m$)] significantly, making it suitable for analog/RF and linearity applications.

1 Introduction

In nano-scale regime, to increase the packaging density of ICs, continuous lowering of chip size has become an important issue. The chip size is being decreased day by day, while increasing the number of transistors on a single chip [1]. In semiconductor industries till now, MOSFET has proved to be most suited transistor in terms of analog/RF performance [2, 3]. However, scaling of MOSFET faces various issues such as static power dissipation, physical limit of subthreshold slope, leakage current and hot carrier effect. To overcome these issues, band-to-band tunneling is being adopted in place of drift–diffusion phenomenon [4–8]. TFET (tunnel field-effect transistor) has emerged as a good alternative to MOSFET to overcome the scaling-related issues. However, according to International Technological Roadmap for Semiconductor requirements (ITRS), some behavioral limitations have been found with TFET too [9]. Some of these include lower on-current and ambipolar behavior, which reduce the device performance. To improve the on-state current, many concepts such as heterostructure TFET, strained-Si, and pocket doping have been proposed by many researchers [10–17]. However, the symmetrical doping of n^+ and p^+ regions has raised the problem of ambipolarity. Use of asymmetric doping profile at source–drain region and large band-gap material on drain side reduces the problem of ambipolarity to a greater extent. But, on the other hand reduced on-current leads to an increase in process complexity [18, 19].

To overcome these issues, two methods have been proposed. First method involves the use of dual-oxide electrically doped TFET and the other method involves the use of work function engineering [20, 21]. Using these two methods, a new device structure of dual-material dual-oxide double-gate TFET (DMDODG-TFET) has been investigated in this work for the first time. The dual-oxide layer

Electronic supplementary material The online version of this article (https://doi.org/10.1007/s00339-019-2650-5) contains supplementary material, which is available to authorized users.

✉ Satyendra Kumar
satyendra.kumar@jiit.ac.in

[1] Jaypee Institute of Information Technology, Noida, India

[2] PDPM-India Institute of Information Technology Design and Manufacturing, Jabalpur, MP, India

Published online: 24 April 2019

enhances the electric field at source–channel interface by improving the capacitive coupling [20]. The use of stack gate oxide(SiO_2 along with HfO_2) has made the reported device more suitable for improved analog/RF and linear performance. This work also includes the dual-work functionality, which is used at dual-metal gate device structure. The comparatively low value of work function at tunnel gate than that of control gate enhances the on-state current [21]. This can be attributed to improved bending of energy bands and probability of tunneling at source–channel interface. However, relatively low value of work function at auxiliary gate diminishes the band bending and electric field at drain–channel interface. In this case, the application of negative gate voltage minimizes the ambipolarity of device. Finally, the improvement of on-state current and suppressed ambipolar behavior make the device suitable for analog/RF and linearity applications. This is shown by investigating the linearity parameters such as voltage intercept point, input intercept point, intermodulation point, and analog/RF parameters such as transconductance, cut-off frequency, and capacitances. These modifications and improvements are very useful for switching, biosensor and low-power applications.

This work is divided into four sections. Section 2 describes the schematic structure of the device, specific parameters and simulation design steps. Section 3 demonstrates the results and the proposed improvements. Section 3 is divided into two subsections, one for DC characteristics and another is for analog/RF and linearity parameters. Finally, the paper is concluded in Sect. 4.

2 Device architecture, description with specification and simulation set-up

Figure 1a shows the schematic device structure of conventional dual-material double-gate TFET (DMDG-TFET) with single SiO_2 layer. The complete cross-sectional view of dual-material dual-oxide double-gate TFET (DMDODG-TFET) with HfO_2/SiO_2-stacked gate oxide is shown in Fig. 1b. The corresponding parameters considered are shown in Table 1. The proposed device structure of DMDODG-TFET has tri-segmented gate electrode with different work functions, while for single-material dual-oxide double-gate TFET (SMDODG-TFET) three metal gates have same work-function values. These electrodes include three metal gates, namely (1) tunneling gate (M_1) (2) control gate (M_2) and (3) auxiliary gate (M_3). The corresponding work functions for the three metal gates are ϕ_1, ϕ_2 and ϕ_3. The values of work function for tunnel gate and auxiliary gate have been taken corresponding to molybdenum (Mo) (4.36 eV–4.95 eV) and aluminum (Al) (4.0 eV–4.26 eV), respectively. A stacked gate oxide layer

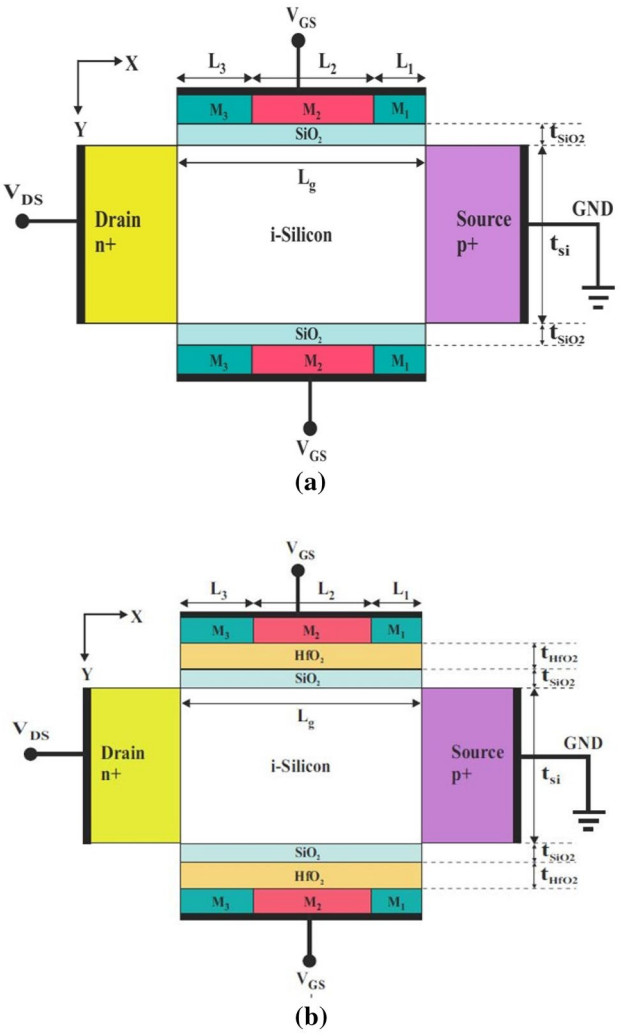

Fig. 1 **a** Schematic of conventional DMDG-TFET with single SiO_2 gate oxide. **b** Schematic of proposed device DMDODG-TFET3 with HfO_2/SiO_2-stacked gate oxide

(HfO_2) + (SiO_2) is implemented between the gate and the channel interface. The difference in oxide layer thickness gives improved on-current and reduced potential barrier width, as it provides better capacitive coupling between the gate and the channel. Length of the gate was considered as 50 nm for better results [20]. Atlast, to further improve the performance quantum tunneling regions have been considered during the simulation. These regions have covered both the interfaces (source–channel and drain–channel interface). Quantum confinement model, band-gap narrowing, Shockley–Read–Hall–Auger recombination and Wentzel–Kramers–Brillouin models have been used for band-to-band tunneling (BTBT), doping concentration, energy of carrier exchange and numerical explanation, respectively [20, 21].

Table 1 Design parameters used in the simulation of device

Parameters	Symbols	Values
Gate length	L_g	50 nm
SiO_2 thickness	t_{SiO2}	0.8 nm
HfO_2 thickness	t_{HfO2}	1.2 nm
Silicon thickness	t_{Si}	10 nm
Channel doping	N_{CH}	1×10^{17} cm^{-3}
Source doping (p-type)	N_S	1×10^{20} cm^{-3}
Drain doping (n-type)	N_D	5×10^{18} cm^{-3}
HfO_2 dielectric constant	k	25
Tunneling gate length	L_1	10 nm
Control gate length	L_2	25 nm
Auxiliary gate length	L_3	15 nm
Tunnel gate work function	ϕ_1	4.0 eV
Control gate work function	ϕ_2	4.6 eV
Auxiliary gate work function	ϕ_3	4.0 eV

3 Results and discussion

3.1 DC parameters

Results of proposed TFET in terms of DC parameters have been presented in two parts. First part deals with the performance of gate oxide stacked SMDODG-TFET (single-material dual-oxide double-gate TFET), while second part deals with the work-function engineering-based DMDODG-TFET.

3.1.1 Stack gate oxide approach for SMDODG-TFET

This section presents the performance analysis of the proposed SMDODG-TFET in terms of surface potential, energy band diagrams and DC characteristics. For the simulation of SMDODG-TFET, the work function of three-material gate has been kept same ($\phi = 4.6$ eV) in Fig. 1b. A comparison has been made between conventional DMDG-TFET with SiO_2 as the oxide layer and SMDODG-TFET, in which the oxide layer consists of SiO_2 and HfO_2 in a stacked fashion. Figure 2a demonstrates the comparison of variation of surface potential of SMDODG-TFET along the channel for different combinations of HfO_2/SiO_2-stacked gate oxide. The variations of lateral (E_X) and vertical (E_Y) electric fields of conventional and SMDODG-TFET along the channel are shown in Fig. 2b, c ,respectively. Both, horizontal and vertical electric fields (E_X and E_Y), are found to be higher for SMDODG-TFET in comparison with the conventional DMDG-TFET. From Fig. 2, it can be noticed that the potential barrier width is reduced at ($V_{GS} = V_{DS} = 1.0$ V) because of using stacked oxide layer. Vertical electric field has been found to be higher using stack gate oxide in comparison with single-oxide layer of lower k dielectric, i.e. SiO_2. The reason for both the improvements is the use HfO_2 and SiO_2

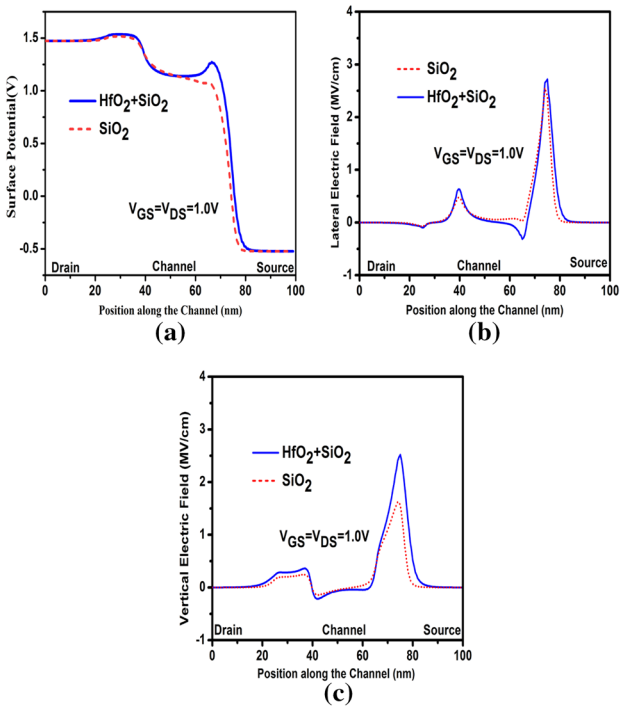

Fig. 2 **a** Surface potential along the channel for different HfO_2/SiO_2 -stacked gate oxide models. Variation of (**b**) E_X and (c) E_Y, along the channel for different combinations of dielectric constant at $V_{DS} = V_{GS} = 1.0$ V of SMDODG-TFET with HfO_2/SiO_2-stacked gate oxide

layers together. The improved horizontal and vertical electric fields provide higher band bending of energy bands. Figure 3a shows the higher band bending in the case of stacked gate oxide layer. This band bending provides better band-to-band tunneling between the source and the channel in the on-state. The variation of difference between two energy bands (L_T^{min}), i.e. tunneling length, for both oxide layers is shown in Fig. 3b. From this figure, it can be concluded that

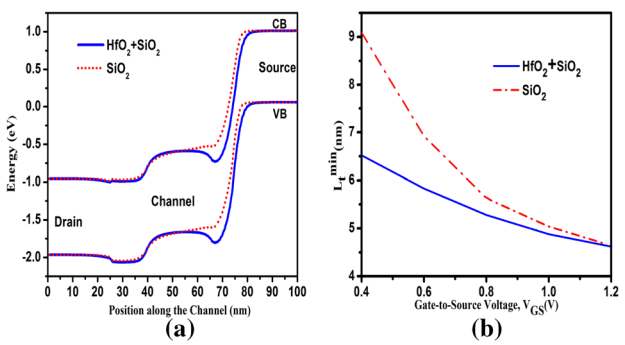

Fig. 3 **a** Energy band diagram in on-state ($V_{GS} = V_{DS} = 1.0$ V) of SMDODG-TFET. **b** Variation of L_t^{min} with V_{GS} for different combinations of SiO_2/HfO_2-stacked gate oxide at ($V_{DS} = 1.0$ V)

tunneling length variation for HfO_2 and SiO_2 is better in comparison with SiO_2.

The DC characteristics of SMDODG-TFET and conventional DMDG-TFET are shown in Fig. 4a. From this figure, a large difference can be noticed between the drain currents of both TFETs, with respect to gate to source voltage (V_{GS}). The stacked gate oxide shows better tunneling current, since the electric field is higher for SMDODG-TFET as shown in Fig. 4. However, the leakage current is higher in the case of SMDODG-TFET. Figure 4b shows the variation of drain current w.r.t. drain to source voltage (V_{DS}) for different values of V_{GS}. This variation has been studied for SMDODG-TFET. According to this variation, it can be observed that drain current increases with the increase in V_{GS}. Large drain current is attributed to band-gap contraction because of better capacitive coupling between source and channel interface.

From all these results, it can be concluded that the dual-gate stacked device SMDODG-TFET shows better performance in terms of higher electric field and higher drain current because of better capacitive coupling compared to conventional DMDG-TFET. So, in the next analysis dual-oxide double-gate structure is considered.

3.1.2 Work-function optimization

To further decrease the leakage and ambipolar currents, work-function engineering has been applied along with stacked gate oxide. For the work-function engineering, three-material gates have been considered. Figure 1 shows the schematic of the proposed device DMDODG-TFET. A comparison is made between different devices, having different values of work functions as shown in Table 2. In this table, different combinations of work functions have been applied to get optimized TFET. In Fig. 5a, two kinds of SMDODG-TFETs with different work functions ($\phi = 4.2\,\text{eV}, 4.4\,\text{eV}$)

Table 2 Device description with different work functions

Possible combinations	ϕ_1	ϕ_2	ϕ_3
SMDODG-TFET	4.6 eV	4.6 eV	4.6 eV
DMDODG-TFET1	4.0 eV	4.6 eV	4.6 eV
DMDODG-TFET2	4.6 eV	4.6 eV	4.0 eV
DMDODG-TFET3	4.0 eV	4.6 eV	4.0 eV

are compared with DMDODG-TFET, in terms of (I_D v/s V_{GS}) characteristics while maintaining $V_{DS} = 1.0\,\text{V}$ constant. From the Fig. 5b, it is observed that DMDODG-TFET shows increased on-current to off-current ratio (I_{ON}/I_{OFF}) for DMDODG-TFET. From this figure, it can be stated that higher on-current can be drawn from DMDODG-TFET. Figure 6a, b shows the energy band diagram of DMDODG-TFET in off-state and on-state by keeping work-function values of auxiliary gate and tunneling gate constant (4.0 eV) and by varying control gate work function. It can be noticed that, with the increase in control gate work function, the width of tunneling region also increases. Because of this increment, overlapping of band-gap at source side decreases which results in lower tunneling current. Whereas, at the drain side lower amount of tunneling was found because of small barrier width at drain–channel interface. In the on-state, no significant difference was recorded for $\phi_2 < 4.6\,\text{eV}$. But, for larger ϕ_2 an increase in band-overlapping was found, resulting in increased tunneling probability. Figure 6c shows the transfer characteristics in the exponential region. For the transfer characteristics, control gate work function has been varied, while auxiliary and tunnel gate work functions have been kept constant. From these graphs, low leakage current and optimum on-current were found for the combination of $(\phi_1 = \phi_3) < \phi_2$.

Further, Fig. 7a, b shows higher value of surface potential and electric field for DMDODG-TFET3 in comparison

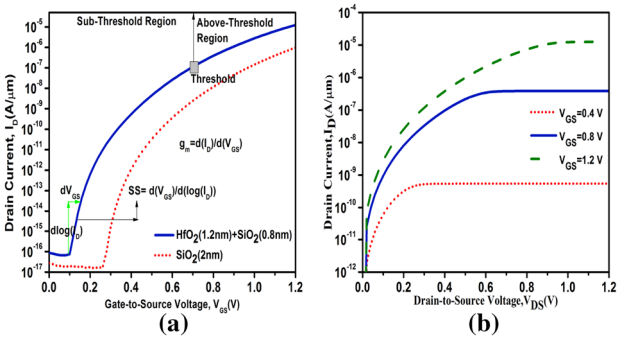

Fig. 4 Variation of I_D **a** against V_{GS} for different combinations of dielectric constant at constant drain voltage ($V_{DS} = 1.0$ V) and **b** against V_{DS} for different values of V_{GS} of SMDODG-TFET with SiO_2/HfO_2 -stacked gate oxide

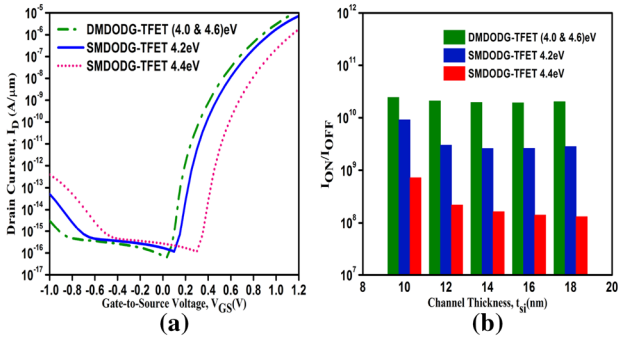

Fig. 5 Variation of I_D **a** against V_{GS} for different combinations of gate work function(φ) at constant drain voltage ($V_{DS} = 1.0$ V) and **b** comparison of I_{ON}/I_{OFF} ratio against t_{si} for different structure DsMDODG-TFET and SMDODG-TFET

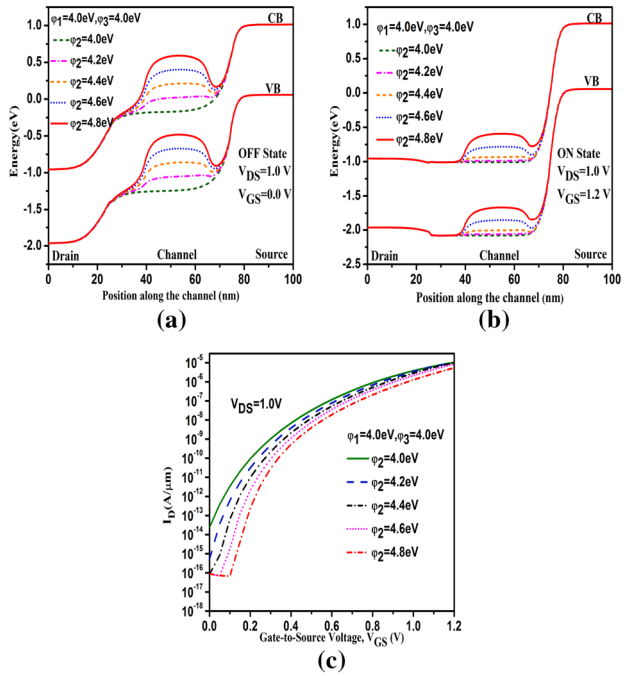

Fig. 6 Energy band diagram of DMDODG-TFET along the X-position in **a** OFF-state ($V_{GS} = 0$ V and $V_{DS} = 1.0$ V) and **b** ON-state ($V_{GS} = 1.2$ V and $V_{DS} = 1.0$ V) at different φ_2 values **c** transfer characteristics of DMDODG-TFET at different φ_2 values

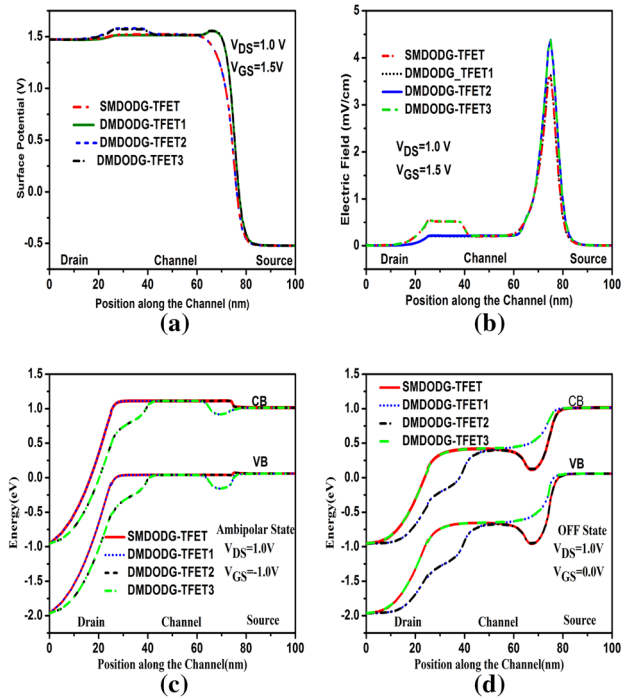

Fig. 7 Comparative plots of **a** surface potential, **b** electric field, **c** energy band diagram in ambipolar state, and **d** energy band diagram in the OFF-state of SMDODG-TFET, DMDODG-TFET1, DMDODG-TFET2, DMDODG-TFET3 along the channel

Table 3 Switching ratio for different structures

Device structure	V_{TH}	I_{on} $(A/\mu m)$	I_{off} $(A/\mu m)$
SMDODG-TFET	1.13 V	3.4×10^{-6}	3.4×10^{-16}
DMDODG-TFET1	0.67 V	3.3×10^{-5}	3.4×10^{-16}
DMDODG-TFET2	1.13 V	3.4×10^{-6}	7.2×10^{-17}
DMDODG-TFET3	0.67 V	3.6×10^{-5}	7.2×10^{-17}

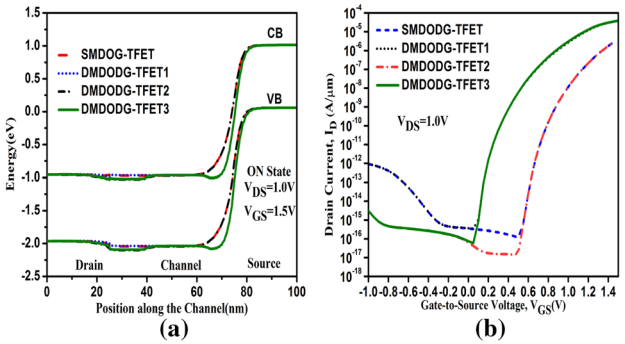

Fig. 8 Comparative plots of **a** energy band diagram along the channel in ON-state; **b** comparative plots of transfer characteristics of SMDODG-TFET, DMDODG-TFET1, DMDODG-TFET2 and DMDODG-TFET3

with other structures. Higher work function at control gate provides large electric field and surface potential. Figure 7c gives the lower value of ambipolar current for the combination of $(\phi_1 = \phi_3) < \phi_2$, i.e. for DMDODG-TFET3 at $V_{GS} = V_{DS} = 1.0\,V$. In the off-state DMDODG-TFET3 has higher band width in comparison with other devices (see Fig. 7 d). From these results, it can be concluded that SMDODG-TFET gives higher leakage current and ambipolar current. DMDODG-TFET1 and DMDODG-TFET2 also do not suppress the ambipolarity to a great extent. The complete analysis of four devices in on-state is shown in Fig. 8a,b. It can be concluded that the presence of lower ϕ_1 at source side reduces the tunneling barrier width, which in turn leads to higher on-current, while the presence of lower ϕ_2 at drain side reduces the ambipolar current. Energy band diagrams in on-state of four devices and transfer characteristics show better performance with the case of DMDODG-TFET3. The impact of work-function engineering for different structures is given in Table 3. It can be concluded that highest on-current and switching ratio can be obtained for DMDODG-TFET3 compared to SMDODG-TFET, DMDODG-TFET1 and DMDODG-TFET2.

3.2 Analog/RF and linearity performance

This section deals with the analog/RF performance of DMDODG-TFET. From the previous analysis, it was

observed that DMDODG-TFET3 shows better DC characteristics along with DMDODG-TFET2, which also shows acceptable results. Further, the comparison between these two kinds of TFETs is presented on the basis of their analog/RF performance. For this comparison, the graphs for analog/RF figure of merits have been analyzed. The parameter transconductance (g_m) is an important parameter to define and explain the terms of analog/RF application. It can be derived by variation in drain current per unit voltage between gate and source (V_{GS}). Higher value of g_m provides significant gain and consequently high analog/RF performance [22]. Figure 9 shows the variation of transconductance with respect to V_{GS}. The value of transconductance for both the TFETs increases up to a fixed voltage and then decreases because of current driven capacity of TEFTs and mobility degradation, respectively. Further, it is noticed from the graph that DMDODG-TFET3 shows better amplification compared to DMDODG-TFET2. For this analysis, 1 MHz frequency has been applied for the small signal analysis. Two types of capacitances, gate to drain capacitance (C_{gd}) and gate to source capacitance (C_{gs}), extracted from small signal analysis can be considered in terms of total capacitance (intrinsic+extrinsic) [26, 27]. Without consideration of overlapping capacitances, the equations for C_{gs} and C_{gd} [28] can be given as follows:

$$C_{gs} = C_{gsi} + C_{fext} + C_{fint}, \tag{1}$$

$$C_{gd} = C_{gdi} + C_{fext} + C_{fint}. \tag{2}$$

Here, C_{fext} is the external fringing capacitance, which is bias independent and C_{fint} is the internal fringing capacitance, which is bias dependent. The fringing electric field between the gate and the channel occurs because of extrinsic capacitances. The fringing electric field is comprised of two components: (1) internal and (2) external. However, the calculation of two fringing capacitances can be done using a substitute approach [29]. According to this approach, the total input capacitance C_{gg} can be calculated as follows:

$$C_{gg} = C_{gs} + C_{gd} = \left| \frac{\mathrm{Im}(Y_{11} + Y_{12})}{\omega} \right|. \tag{3}$$

Here, $\omega = 2\pi f$ and f represents the applied frequency.

Positive gate biasing helps to significantly reduce the potential barrier at drain–channel interface and a slight change in source-to-channel potential barrier [20]. This results in increased gate to drain capacitance (C_{gd}) for positive input gate voltage (See Fig. 10a), but a negative behavior has been observed for gate to source capacitance (C_{gs}). Figure 10b, c shows the cut-off frequency (frequency at unity gain) and device efficiency. Cut-off frequency f_T is given by the following equation [22]:

$$f_T = g_m/(2 \times \pi(C_{gs} + C_{gd})). \tag{4}$$

From the equation of f_T, it can be realized that f_T can be enhanced by having a higher value of g_m and reduced total capacitance. From the curve, it can be observed that DMDODG-TFET3 has large cut-off frequency along with higher efficiency. Another figure of merit to study the analog/RF application is TFP, which is shown in Fig. 10d. TFP (transconductance frequency product) is given as follows [24]:

$$TFP = (g_m/I_D) \times f_T. \tag{5}$$

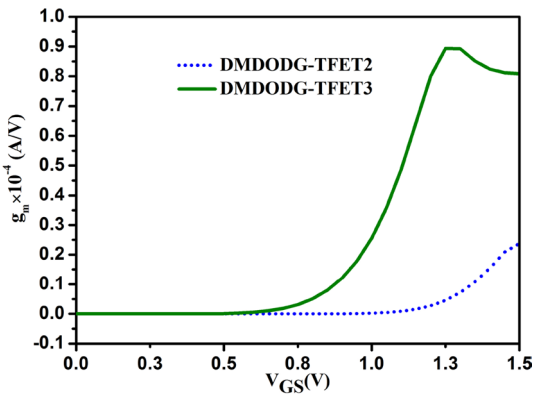

Fig. 9 Comparative plot of the transconductance coefficient g_m of DMDODG-TFET2 and DMDODG-TFET3

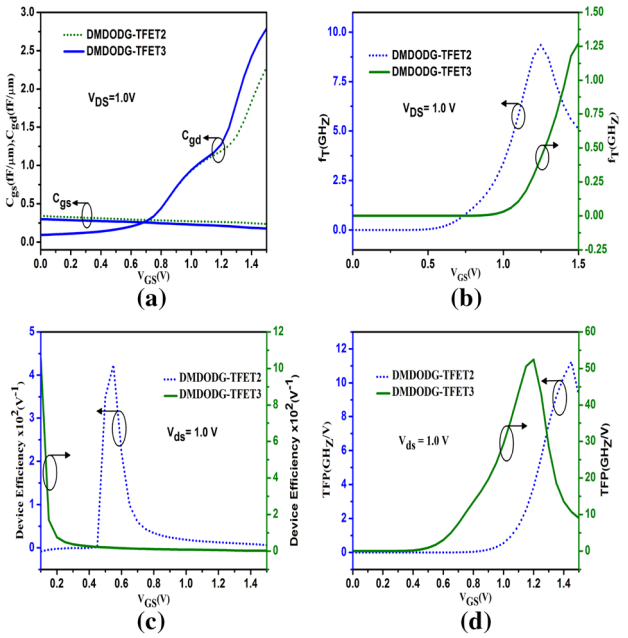

Fig. 10 Comparative plots of **a** C_{gs} and C_{gd}, **b** f_T characteristics, **c** device efficiency, and **d** TFP of DMDODG-TFET2 and DMDODG-TFET3

Due to higher g_m and f_T, TFP is also found to be large for DMDODG-TFET3.

Further, linearity parameters such as voltage intercept points (VIP2, VIP3), input intercept point (IIP3), and intermodulation point (IMD3) were analyzed at 50 ohm [1, 24]. These can be given as follows:

$$\mathrm{VIP2} = 4 \times \left(\frac{g_{m1}}{g_{m2}}\right), \tag{6}$$

$$\mathrm{VIP3} = \sqrt{24 \times \left(\frac{g_{m1}}{g_{m3}}\right)}, \tag{7}$$

$$\mathrm{IIP3} = \frac{2}{3} \times \left(\frac{g_{m1}}{g_{m3} \times R_S}\right), \tag{8}$$

$$\mathrm{IMD3} = [\frac{9}{2} \times (\mathrm{VIP3})^2 \times (g_{m3})]^2 \times R_S. \tag{9}$$

Figure 12 shows the comparative plots of these FOMs with respect to V_{GS}. Figure 11 represents the graph of g_{m3} for both the devices. Third-order harmonic distortion (g_{m3}) is used to derive the linearity parameters because of variability in the values of transconductance. DMDODG-TFET3 gives minimum bias point for third-order transconductance (g_{m3}) compared to DMDODG-TFET2. It also shows significantly higher values of VIP2 and VIP3. Improved VIP2 and VIP3 represent lower distortion and higher linearity [23]. To know the ac non-linearity, IIP3 and IMD3 have been plotted against V_{GS} [23]. To achieve higher linearity, higher values are achieved by IIP3 and IMD3 in the case of DMDODG-TFET3, which is shown in Fig. 12c, d. For low values of V_{GS}, both FOMs attain higher values for DMDODG-TFET3. This indicates that DMDODG-TFET3 is more suitable for analog/RF applications.

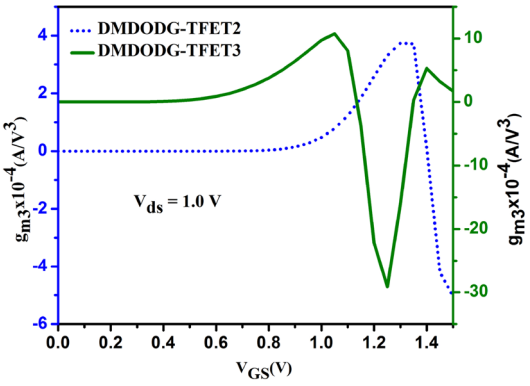

Fig. 11 Comparative plot of the third-order transconductance coefficient of DMDODG-TFET2 and DMDODG-TFET3

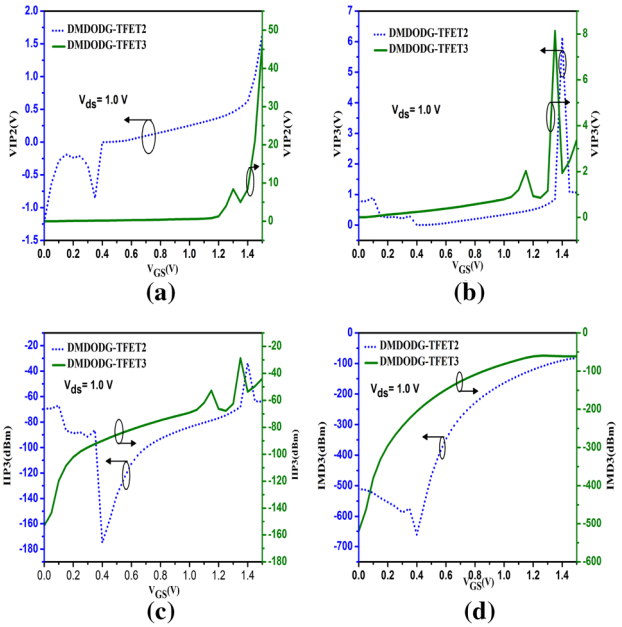

Fig. 12 Comparative plots of **a** VIP2, **b** VIP3, **c** IIP3 and **d** IMD3 of DMDODG-TFET2 along DMDODG-TFET3

A comparison of all parameters in terms of analog/RF and linearity FOMs is presented in Table 4 for DMDODG-TFET2, DMDODG-TFET3 and conventional double-gate MOSFET (DG-MOSFET). The distortion loss found in the case of MOSFET is large compared to DMDODG-TFET3. Analog/RF and linearity parameters investigated in the case of DG-MOSFET are higher but optimum bias point is observed for the case of DMDODG-TFET3 only. Thus, DMDODG-TFET3 is a suitable candidate for good sub-threshold slope, higher switching ratio, better immunity towards short-channel effects and stable bias point [25].

Table 4 Comparison for DMDODG-TFET2, DMDODG-TFET3 and DG-MOSFET in terms of analog/RF and linearity parameters

Parameters	DMDODG-TFET2	DMDODG-TFET3	DG-MOSFET
$g_{m3}\,(A/V^3)$	3.8	10	0.11
$f_T\,(GH_z)$	1.5	8.8	1000
TFP (GH_z/V)	11.2	52.3	4000
VIP2 (V)	1.6	45	138.54
VIP3 (V)	6.12	8.2	27.3
IIP3 (dBm)	−35	−31	25.329
IDM3 (dBm)	−86	−73	41.23

4 Conclusions

In summary, this work presents a dual-oxide (HfO_2 and SiO_2)-based TFET with different work functions at tunnel gate, control gate and auxiliary gate (ϕ_1, ϕ_2 and ϕ_3). The use of dual stack gate oxides improves the on-current and cut-off frequency. The optimum thicknesses of oxide layers improves the linearity FOMs. It can be concluded that DMDODG-TFET3 with work function ($\phi_1 = 4.0\,\text{eV}, \phi_3 = 4.0\,\text{eV}$ and $\phi 2 = 4.6\,\text{eV}$) and gate-oxide thickness ($t_{SiO_2} = 0.8\,\text{nm}$ and $t_{HfO_2} = 1.2\,\text{nm}$) has been proved as best candidate to serve for analog/RF application. This work demonstrates better output for a possible work-function combination of ($\phi_1 = \phi_3 < \phi_2$) in case of DMDODG-TFET3. This combination of work function suppresses the ambipolarity and enhances the on–off-current ratio to 5×10^{11} at $V_{DS} = 1.0\,\text{V}$. Finally, these two approaches of dual oxides and work-function engineering in TFET are useful in analog/RF applications.

References

1. A. Pinczuk, E. Burstein, Raman scattering from InSb surfaces at photon energies near the E_1 energy gap. Phys. Rev. Lett. **21**, 1073–1075 (1968)
2. J.-P. Colinge, C.-W. Lee, A. Afzalian, Nanowire transistors without junctions. Nat. Nanotechnol **5**, 225229 (2010)
3. S.O. Koswatta, M.S. Lundstrom, D.E. Nikonov, Performance comparison between p-i-n tunneling transistors and conventional MOSFETs. IEEE Trans. Electron Device **56**, 456465 (2007)
4. A.C. Seabaugh, Q. Zhang, Low-voltage tunnel transistors for beyond CMOS logic. Proc. IEEE **98**(12), 20952110 (2010)
5. W.Y. Choi, B.G. Park, J.D. Lee, Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec. IEEE Electron Device Lett. **28**(8), 743745 (2007)
6. P.F. Wang, K. Hilsenbeck, T. Nirschl, Complementary tunneling transistor for low power application. Solid-State Electron. **48**(12), 22812286 (2004)
7. A.M. Ionescu, H. Riel, Tunnel field-effect transistors as energy efficient electronic switches. Nature **479**(7373), 329337 (2011)
8. A.M. Ionescu, L.D. Michielis, N. Dagtekin, Ultra low power emerging devices and their benefits for integrated circuits. Proc. IEEE IEDM, 16.1.116.1.4 (2011)
9. The international technology roadmap for semiconductors. http://www.itrs.net
10. M.R. William, A.J. Gehan, Silicon surface tunnel transistor. Appl. Phys. Lett. **67**, 494496 (1995)
11. Q. Zhang, W. Zhao, A. Seabaugh, Low subthreshold swing tunnel transistors. IEEE Trans. Electron Device Lett. **27**, 297300 (2006)
12. K. Boucart, A.M. Ionescu, Double gate tunnel FET with high-k gate dielectric. IEEE Trans. Electron Devices **54**, 17251733 (2007)
13. R.M.I. Abadi, M. Saremi, A resonant tunneling nanowire field effect transistor with physical contractions: a negative differential resistance device for low power very large scale integration applications. J. Electron. Mater. **47**, 10911098 (2018)
14. K. Nigam, S. Pandey, P.N. Kondekar, A barrier controlled charge plasma based TFET with gate engineering for ambipolar suppression and RF/linearity performance improvement. IEEE Trans. Electron Devices **64**, 27512757 (2017)
15. A.M. Ionescu, H. Riel, Tunnel field-effect transistors as energy efficient electronic switches. Nature/em **479**, 329337 (2010)
16. W.Y. Choi, B.-G. Park, J.D. Lee, Tunneling field effect transistor with subthreshold swing (SS) less than 60 mV/Dec. IEEE Electron Device Lett. **28**, 743745 (2007)
17. R.M. Imenabadi, Mehdi Saremi, W.G. Vandenberghe, A novel PNPN like Z-shaped tunnel field-effect transistor with improved ambipolar behavior and RF performance. IEEE Trans. Electron Devices **64**, 47524758 (2017)
18. A. Lahgere, C. Sahu, J. Singh, Electrically doped dynamically configurable field-effect transistor for low power and high-performance applications. Electron. Lett. **51**, 12841286 (2015)
19. K. Nigam, P.N. Kondekar, D. Sharma, A new approach for design and investigation of junctionless tunnel FET using electrically doped mechanism. Superlattices Microstruct. **98**, 1–7 (2016)
20. P.N. Kondekar, K. Nigam, S. Pandey, D. Sharma, Design and analysis of polarity controlled electrically doped tunnel FET with bandgap engineering for analog/RF applications. IEEE Trans. Electron Devices **64**(2), 412–418 (2017)
21. K. Nigam, P. kondekar, D. Sharma, Approach for ambipolar behaviour suppression in tunnel FET by workfunction engineering. Micro Nano Lett. **11**(8), 460–464 (2016)
22. A. Sarkar, A.K. Das, S. De, C.K. Sarkar, Effect of gate engineering in double-gate MOSFETs for analog/RF applications. Microelectron. J. **43**(11), 873882 (2012)
23. J. Madan, R. Chaujar, Interfacial charge analysis of heterogeneous gate dielectric-gate all around-tunnel FET for improved device reliability. IEEE Trans. Device Mater. Reliab. **16**, 227234 (2016)
24. J.H. Huang, Z.H. Liu, M.C. Jeng, A physical model for MOSFET output resistance. Int. Electron Devices Meet. **13**, 569–572 (1992)
25. R. Nagar, M. Saxena, R.S. Gupta, M. Gupta, Linearity and analog performance analysis of double gate tunnel FET: effect of temperature and gate stack. Int. J. VLSI Design Commun. Syst. **2**(3), 186–200 (2011)
26. A. Bansal, B.C. Paul, K. Roy, An analytical fringe capacitance model for interconnects using conformal mapping. IEEE Trans. CAD **25**(12), 2765–2774 (2006)
27. K.M.H. Badami, S. Karmalkar, Quasi-static compact model for coupling between aligned contacts on lnite substrates with insulating or conducting backplanes. IEEE Trans. CAD **31**(06), 858–8674 (2012)
28. S. Ahish, D. Sharma, Y.B.N. Kumar, M.H. Vasantha, Performance enhancement of novel InAs/Si hetero double-gate tunnel FET using Gaussian doping. IEEE Trans. Electron Devices **63**(1), 288–295 (2016)
29. T.C. Lim, Bernard, O. Rozeau, T. Ernst, B. Guillaurnot, N. Vulliet, C.B. Dufournet, M. Paccaud, S. Lepilliet, G. Dambrine, F. Danneville, A charge oriented model for MOS transistor capacitances. IEEE Trans. Electron Devices **56**(7), 1473–1482 (1978)