Theory and Design of Advanced CMOS Current Mirrors

Christoph Tzschoppe, Udo Jörges, Alexander Richter, Bastian Lindner and Frank Ellinger

***Abstract*—In this paper continuous time high-performance current mirrors (CMs) based on series and parallel connected unity sized CMOS transistors suitable for low power applications are presented. It is shown that the proposed implementation techniques allow an increased output resistance, from twice the output resistance of the simple current mirror (SCM) up to more than 50 times of the cascode current mirror's output resistance depending on the chosen topology. A complete theory which describes the concept of using series connected transistors is developed and expressed with analytical equations. Furthermore, it is shown that the advanced current mirror (ACM) and the advanced cascode current mirror (ACCM) exhibit a much higher output resistance compared to the simple and the cascode current mirror (CCM). Spectre simulations of the different current mirror implementations built with transistors of IHP 130 nm CMOS technology verify the analytical solutions.**

***Index Terms*—CMOS integrated circuits, Current mirrors, Low-voltage, Analog integrated circuits**

I. Introduction

In almost every integrated analog circuit design high-performance current mirrors are mandatory to provide bias conditions to single circuit blocks. Especially low power circuitry needs to operate with low supply voltages making the usage of improved current mirrors like cascodes difficult due to the enhancement of the necessary voltage swing while also a high output resistance is very important for many applications. In most publications active feedback circuits [1], [2], [3], [4] and adaptive bias circuits [5] are applied to enable high output resistances and maximum output voltage swing. The drawback is that further bias circuits are required, stability issues have to be investigated [6] and sometimes also multiple supplies are needed [1]. A very suitable and simple solution is the application of current mirrors using series and parallel connected CMOS transistors [7]. Depending on the implementation these CMs offer an increased output impedance while the output voltage swing is only slightly decreased or even equal for cascode implementation. This improvement can be reached when forcing transistors to operate in triode region, which makes an application of these current mirrors possible for aggressively scaled submicron CMOS technologies that can operate only at low voltage supplies because of their low breakdown voltages. All assumptions made in this paper are prepared only for n-MOS transistors, however the same assumptions can be made for p-MOS transistors leading to an equal functionality. In section II-A the theory of series connected CMOS transistors is briefly investigated, followed by section II-B, where an extended current mirror topology is presented to realize an increased output resistance compared to the simple CM. In section II-C the cascode implementation of the ACM is presented including a comparison between single reference CMs, followed by section III which concludes the paper.

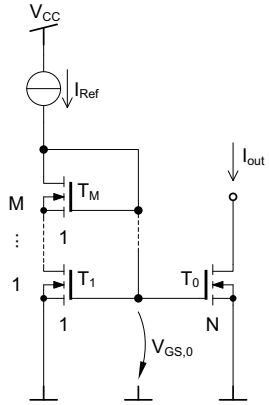
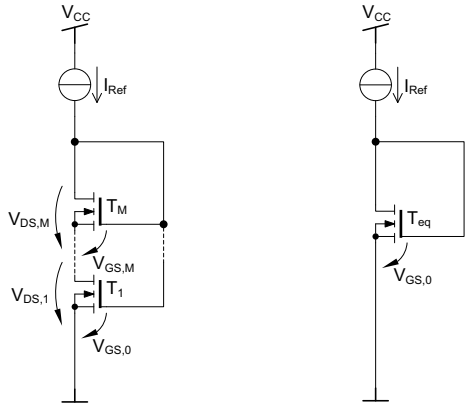


Fig. 1: Advanced current mirror implementation



(a) Series connected transistors (b) Single equivalent transistor

Fig. 2: Transistor conversion principle

II. Advanced Current Mirror Theory

A. Current Mirrors with Series Connected Transistors

This section presents the derivation of the theory for the advanced current mirrors as depicted in Fig. 1. The transistors $T_1 \dots T_M$ are connected in series while the gates are tied together. The voltage $V_{GS,0}$ denotes the gate-source voltage of the transistor T_0, consisting of N parallel connected unity sized CMOS transistors, which is equal to the gate-source

978-1-4673-9492-5/15/$31.00 ©2015 IEEE

voltage of the lower transistor T_1 in the reference path. The transistors in the reference path $T_1 \dots T_{M-1}$ operate in triode region, only T_M operates in pinch-off region, just as the transistor T_0. Every integer mirror ratio $M \times N$ can be realized with this circuit implementation. First we want to investigate two series connected CMOS transistors T_1, T_2 as illustrated in Fig. 2a to transform two series connected transistors to one single equivalent transistor T_{eq}. For all following calculations the channel length modulation effect is neglected ($\lambda \cdot V_{DS} \ll 1$) for all drain current equations, it is only considered for calculations of the output resistance r_{out}. We can set up the drain current equation Eq. 1 for T_1 which operates in triode region.

$$I_{Ref} = \beta \left[(V_{GS,0} - V_{th}) \cdot V_{DS,1} - \frac{V_{DS,1}^2}{2} \right] \tag{1}$$

The transistor T_2 is operating in pinch-off region which leads to Eq. 2. Solving the binomial equation Eq. 2 the reference current can be expressed with Eq. 3.

$$\begin{aligned} I_{Ref} &= \frac{\beta}{2} (V_{GS,2} - V_{th})^2 && (2) \\ &= \frac{\beta}{2} (V_{GS,0} - V_{th} - V_{DS,1})^2 \\ &= \frac{\beta}{2}(V_{GS,0} - V_{th})^2 - \underbrace{\beta \cdot \left[(V_{GS,0} - V_{th}) \cdot V_{DS,1} - \frac{V_{DS,1}^2}{2} \right]}_{= I_{Ref}} && (3) \end{aligned}$$

In Eq. 3 you can observe that the second equation part is equal to I_{Ref} from Eq. 1, thus we can insert it. Solving the resulting equation for I_{Ref} leads to Eq. 4.

$$\begin{aligned} I_{Ref} &= \frac{1}{2} \cdot \frac{\beta}{2} (V_{GS,0} - V_{th})^2 && (4) \\ &= \frac{\beta_{res}}{2} (V_{GS,0} - V_{th})^2 && (5) \end{aligned}$$

with

$$\beta_{res} = \frac{\beta}{2} \tag{6}$$

Eq. 6 proves that two series connected CMOS transistors acts as one transistor (cf. Fig 2b) with a resulting width-to-length ratio $\left(\frac{W}{L}\right)_{res}$ as expressed in Eq. 7.

$$\left(\frac{W}{L}\right)_{res} = \frac{1}{2} \cdot \frac{W}{L} \tag{7}$$

With the gained knowledge it is now possible to develop a theory for M series connected transistors. Each transistor $T_1 \dots T_M$ has a different drain-source voltage $V_{DS,n}$, but for the bottom transistor T_1 Eq. 1 is always valid independently of the number of series connected transistors M. In addition $M-2$ drain current equations for $T_2 \dots T_{M-1}$ can be expressed using a series which is displayed in Eq. 8.

$$I_{Ref} = \beta \left[\left(V_{GS,0} - V_{th} - \sum_{n=1}^{k-1} V_{DS,n} \right) \cdot V_{DS,k} - \frac{V_{DS,k}^2}{2} \right] \tag{8}$$

with $k = 2 \dots (M-1)$

The drain-current equation for the uppermost transistor T_M could be set up in dependence of the number of the series connected transistors M as shown in Eq. 9.

$$I_{Ref} = \frac{\beta}{2} \cdot \left(V_{GS,0} - V_{th} - \sum_{k=1}^{M-1} V_{DS,k} \right)^2 \tag{9}$$

The complete equation set consists of M equations in total. Now we can expand Eq. 9 and insert all $M-1$ triode equations into the expanded pinch-off equation from T_M which leads to the resulting equation Eq. 10 very similar to Eq. 4.

$$I_{Ref} = \frac{\beta}{2} \cdot (V_{GS,0} - V_{th})^2 - (M-1) \cdot I_{Ref} \tag{10}$$

After solving Eq. 10 for I_{Ref} you obtain Eq. 11.

$$\begin{aligned} I_{Ref} &= \frac{1}{M} \cdot \frac{\beta}{2} \cdot (V_{GS,0} - V_{th})^2 \\ &= \frac{\beta_{res}}{2} \cdot (V_{GS,0} - V_{th})^2 && (11) \end{aligned}$$

with

$$\beta_{res} = \frac{\beta}{M} \tag{12}$$

Eq. 12 shows that a series connection of M transistors is equal to one single transistor T_{eq} with a width-to-length ratio $\left(\frac{W}{L}\right)_{res}$ as shown in Eq. 13.

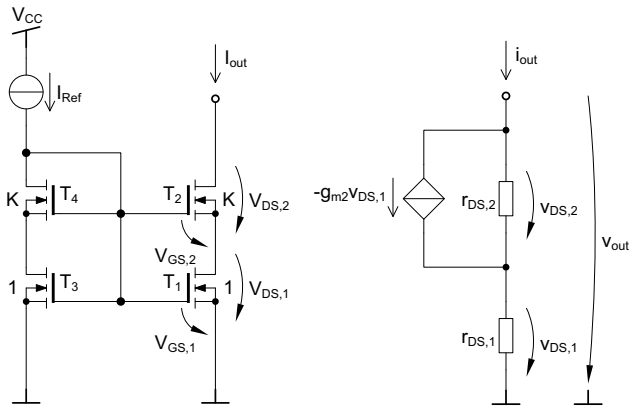
$$\left(\frac{W}{L}\right)_{res} = \frac{1}{M} \cdot \frac{W}{L} \tag{13}$$

B. Increasing the Output Resistance

In this section an advanced current mirror (ACM) implementation with increased output resistance compared to the simple current mirror (SCM) is presented. In Fig. 3a the circuit schematic is depicted. As we know from section II-A, T_1 operates in triode region whereby T_2 is in pinch-off region. From the small signal equivalent model in Fig. 3b we can build the following equation set. Because of the different operation regions $r_{DS,1} \ll r_{DS,2}$, the term $r_{DS,1}$ in the sum of the output resistance has only a small influence, therefore it is negligible.

$$\begin{aligned} v_{DS,1} &= i_{out} \cdot r_{DS,1} && (14) \\ v_{DS,2} &= (i_{out} + g_{m2} \cdot v_{DS,1}) \cdot r_{DS,2} \\ &= i_{out} (1 + g_{m2} \cdot r_{DS,1}) \cdot r_{DS,2} && (15) \end{aligned}$$

With Eq. 14 and Eq. 15 we can calculate the small signal output resistance $r_{out,ACM}$ using Eq. 16.



(a) ACM with increased r_{out} (b) Low frequency small signal equivalent model

Fig. 3: Advanced current mirror

$$\begin{aligned} r_{out,ACM} &= \frac{v_{out}}{i_{out}} \\ &= \frac{v_{DS,1} + v_{DS,2}}{i_{out}} \\ &= r_{DS,1} + (1 + g_{m2} \cdot r_{DS,1}) \cdot r_{DS,2} \\ &\approx (1 + g_{m2} \cdot r_{DS,1}) \cdot r_{DS,2} \end{aligned} \tag{16}$$

The small signal transconductance g_{m2} and the small signal resistance $r_{DS,1}$ can be replaced with the partial derivation of the large signal equations Eq. 17 and Eq. 19 which can be built from the schematic in Fig. 3a.

$$I_{D,2} = \frac{\beta_2}{2} \cdot (V_{GS,2} - V_{th})^2 \tag{17}$$

$$g_{m2} = \frac{\partial I_{D,2}}{\partial V_{GS,2}} = \beta_2 \cdot (V_{GS,2} - V_{th}) \tag{18}$$

$$I_{D,1} = \beta_1 \cdot \left[(V_{GS,1} - V_{th}) \cdot V_{DS,1} - \frac{V_{DS,1}^2}{2} \right] \tag{19}$$

$$\begin{aligned} \frac{1}{r_{DS,1}} = \frac{\partial I_{D,1}}{\partial V_{DS,1}} &= \beta_1 \cdot (V_{GS,1} - V_{th} - V_{DS,1}) \\ &= \beta_1 \cdot (V_{GS,2} - V_{th}) \end{aligned} \tag{20}$$

With the replacement of $r_{DS,1}$ and g_{m2} in Eq. 16 a new equation only depending on β_2 and β_1 for the output resistance $r_{out,ACM}$ is developed in Eq. 21.

$$\begin{aligned} r_{out,ACM} &= \left(1 + \frac{\beta_2 \cdot (V_{GS,2} - V_{th})}{\beta_1 \cdot (V_{GS,2} - V_{th})} \right) \cdot r_{DS,2} \\ &= (1 + K) \cdot r_{DS,2} \end{aligned} \tag{21}$$

Eq. 21 depicts that the output resistance r_{out} is $(K+1)$-times the drain-source resistance $r_{DS,2}$ of the upper transistor T_2 which operates in pinch-off region. The reason is that g_{m2} now takes into account to the output resistance while $r_{DS,2}$ remains constant. With this technique the output resistance can be increased compared to the SCM, as illustrated for different K-factors in Fig. 4. In Table I a comparison between the analytical calculated and the simulated output resistances of the ACMs are given, whereby V_{out} is kept constant with 500 mV. Notice that the relative error between the simulated and the calculated output resistance is maximum 2.5 %.

TABLE I: Calculated and simulated $r_{out,ACM}$ (V_{out} = 0.5 V)

Topology	$\mathbf{r_{out,calc}}$ (Eq. 16)	$\mathbf{r_{out,sim}}$	$\frac{\mathbf{\Delta r_{out}}}{\mathbf{r_{out,sim}}}$ / %
ACM, K=1	$423\,k\Omega$	$433\,k\Omega$	2.3
ACM, K=10	$2.37\,M\Omega$	$2.43\,M\Omega$	2.5

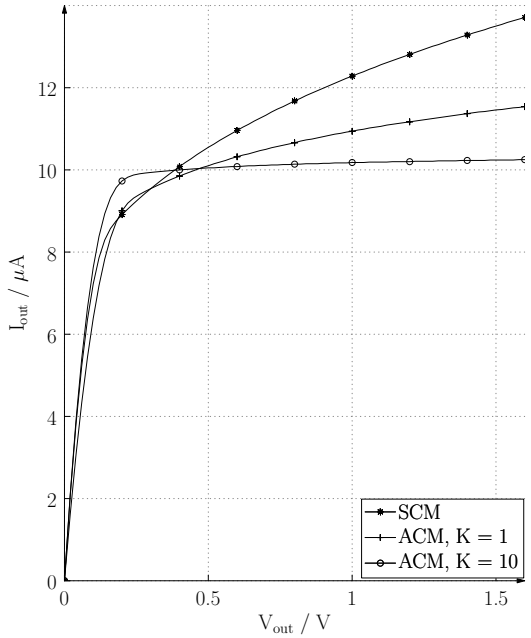


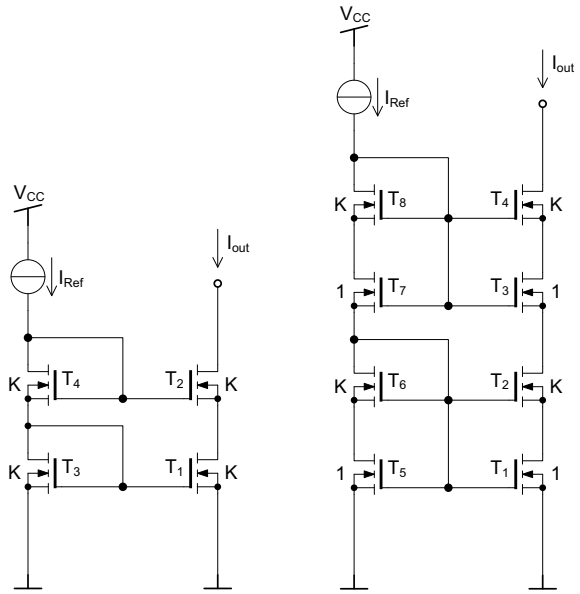
Fig. 4: Current I_{out} of ACM and SCM (W=2 μm, L=1 μm)

C. Cascading of Current Mirrors

To emphasize the benefits of the ACM implementation a comparison of two cascode current mirror topologies with a single reference is given in this section, whereby the Cascode CM (CCM) (cf. Fig. 5a) and the Advanced Cascode CM (ACCM) (cf. Fig. 5b) are chosen. To ensure a fair comparison also the cascode transistors T_2 and T_4 of the CCM are implemented as K parallel connected unity sized transistors, because the gate-source voltage V_{GS} is decreased for parallel connected transistors. This enables an investigation of the necessary voltage headroom for both CM topologies. In Fig. 6 the small signal equivalent circuit model (SSECM) of the ACCM implementation is illustrated. With the given SSECM we can set up the equations for analytical calculation of the output resistance $r_{out,ACCM}$, which is expressed with Eq. 22 - Eq. 25.

TABLE II: Comparison of CM-topologies

Topology	$\mathbf{r_{out}}$	$\mathbf{V_{out,min}}$	No. MOSFETs
SCM	$r_{DS,PO}$	$V_{DS,sat}$	$1+S$
ACM	$(1+K)\cdot r_{DS,PO}$	$V_{DS,sat}+V_{DS,T}$	$(1+K)(1+S)$
CCM	$g_{m,PO}\cdot r_{DS,PO}^2$	$2\cdot V_{DS,sat}+V_{th}$	$2(1+K)$
ACCM	$(1+g_{m,PO}\cdot r_{DS,T})(1+g_{m,T}\cdot r_{DS,T})g_{m,PO}\cdot r_{DS,PO}^2$	$2\cdot V_{DS,sat}+2\cdot V_{DS,T}$	$2(1+K)(1+S)$



(a) CCM (b) ACCM

Fig. 5: Different Cascode CM implementations

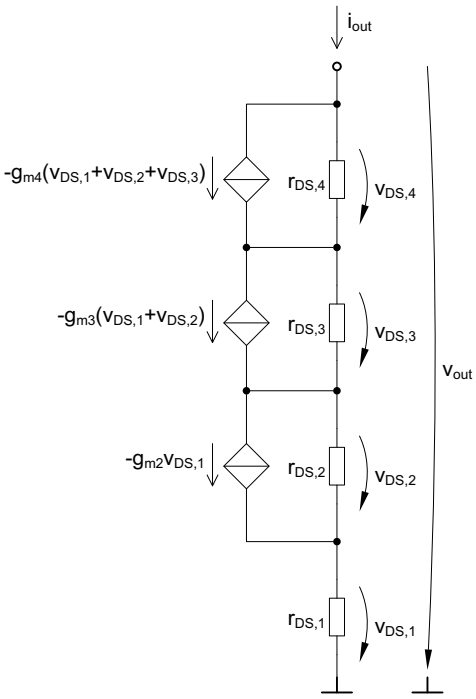


Fig. 6: Low frequency small signal equivalent model of ACCM

TABLE III: Calculated and simulated $r_{out,ACCM}$

Topology	$\mathbf{r_{out,calc}}$ (Eq. 26)	$\mathbf{r_{out,sim}}$	$\frac{\Delta \mathbf{r_{out}}}{\mathbf{r_{out,sim}}}$ / %
ACCM, K=10	$348\,M\Omega$	$373\,M\Omega$	7

$$v_{DS,1} = i_{out}\cdot r_{DS,1} \tag{22}$$

$$\begin{aligned} v_{DS,2} &= (i_{out}+g_{m2}\cdot v_{DS,1})\cdot r_{DS,2} \\ &= i_{out}\,(1+g_{m2}\cdot r_{DS,1})\cdot r_{DS,2} \end{aligned} \tag{23}$$

$$\begin{aligned} v_{DS,3} &= (i_{out}+g_{m3}\cdot(v_{DS,1}+v_{DS,2})\cdot r_{DS,3} \\ &\approx i_{out}\cdot g_{m3}\,(1+g_{m2}\cdot r_{DS,1})\cdot r_{DS,2}r_{DS,3} \end{aligned} \tag{24}$$

$$\begin{aligned} v_{DS,4} &= (i_{out}+g_{m4}\cdot(v_{DS,1}+v_{DS,2}+v_{DS,3})\cdot r_{DS,4} \\ &\approx i_{out}\cdot g_{m4}(1+g_{m2}\cdot r_{DS,1})(1+g_{m3}\cdot r_{DS,3})\cdot r_{DS,2}r_{DS,4} \end{aligned} \tag{25}$$

With the equations Eq. 22 - Eq. 23 we are able to calculate the small signal output resistance $r_{out,ACCM}$ of the ACCM. The small signal drain-source voltages $v_{DS,1}$, $v_{DS,2}$ and $v_{DS,3}$ are negligible because they are only causing an error less than $1\,\%$.

$$\begin{aligned} r_{out,ACCM} &= \frac{v_{out}}{i_{out}} \\ &= \frac{v_{DS,1}+v_{DS,2}+v_{DS,3}+v_{DS,4}}{i_{out}} \\ &\approx \frac{v_{DS,4}}{i_{out}} \\ &\approx (1+g_{m2}\cdot r_{DS,1})(1+g_{m3}\cdot r_{DS,3})\cdot g_{m4}r_{DS,2}r_{DS,4} \end{aligned} \tag{26}$$

For the standard CCM the output resistance is approximately equal to $r_{out,CCM} = g_{m,PO}\cdot r_{DS,PO}^2$, whereby PO denotes that the transistor is operating in pinch-off region. The ACM can also be implemented as a cascode current mirror, as depicted in Fig. 5b which is similar to the well known cascode in Fig. 5a. The benefit of the ACCM is that the output resistance is increased. Thus, also the output resistance of the

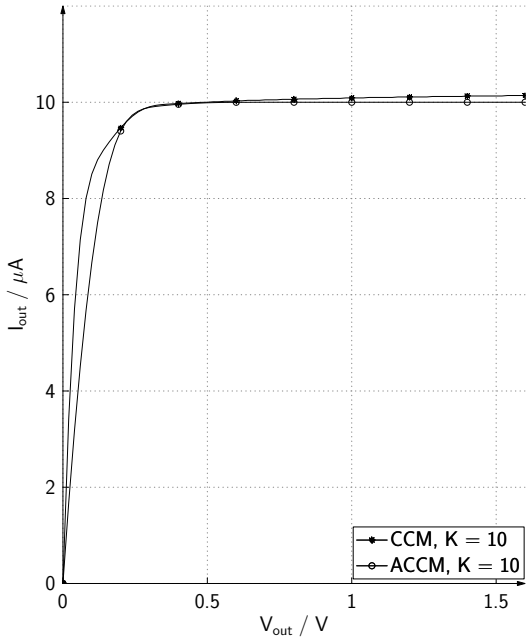


Fig. 7: Current I_{out} of cascode CMs (W=2 μm, L=1 μm)

ACCM can be expressed in terms of the small signal pinch-off and triode parameters with Eq. 27, where T denotes a transistor operating in triode region.

$$r_{out,ACCM} = (1+g_{m,PO} r_{DS,T})(1+g_{m,T} r_{DS,T}) g_{m,PO} r_{DS,PO}^2 \tag{27}$$

Now we can define a factor ϵ between the output resistance of the CCM and that of the ACCM, to quantitatively compare how much higher the value of the ACCM's output resistance is.

$$\begin{aligned} \epsilon &= \frac{r_{out,ACCM}}{r_{out,CCM}} \\ &= (1+g_{m,PO} \cdot r_{DS,T})(1+g_{m,T} \cdot r_{DS,T}) \end{aligned} \tag{28}$$

For the chosen current mirrors in Fig. 5 the calculated value is $\epsilon = 56$, which means that the output resistance of the ACCM is 56-times higher than that of the CCM. By comparing the two curves in Fig. 7 it is seen that the ACCM shows a much higher output resistance compared to the conventional CCM, whereby the voltage swing is kept constant. Only four additional transistors are needed, but this is not always an important design goal. With the gained knowledge of the last sections we can summarize the different current mirror implementations and compare them regarding minimum output voltage, output resistance and number of transistors, which is given in Table II where the mirror ratio should be S. In Table III the analytical calculated and the simulated output resistances of the ACCM are compared, whereby V_{out} is set with 800 mV. You can notice that the relative error between the both output resistances is 7 %.

III. Conclusion

An advanced current mirror topology is presented which enables according to the requirements higher output resistances compared to the conventional simple and cascode current mirror implementation. The proposed circuit implementation is well suited for very large mirror ratios S which is often needed in super low power applications, because a large area reduction is aimed. The advanced cascode current mirror offers an output resistance which is more than 50 times higher compared to the conventional cascode whereby the needed minimum output voltage is nearly constant. For low supply circuits in modern aggressively scaled technologies cascode mirrors should be implemented with the proposed topology for high performance in terms of high output resistances and mirror ratio error, hence it is a good candidate for low voltage high precision applications.

IV. Acknowledgement

This paper was written within the frame of "IKT2020 - Zuverlässige drahtlose Kommunikation in der Industrie" project DEAL funded by the Bundesministerium für Bildung und Forschung (BMBF).

References

[1] X. Zhang, E.I. El-Masry, "A regulated body-driven CMOS current mirror for low-voltage applications," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 51, no. 10, pp. 571-577, October 2004

[2] S. Lee, H. Lee, J.-K. Woo, S. Kim, "Low-voltage bandgap reference with output-regulated current mirror in 90 nm CMOS," Electronics Letters, vol. 46, no. 14, pp. 976-977, July 2010

[3] K. Tanno, O. Ishizuka, Z. Tang, "Low voltage and low frequency current mirror using a two-MOS subthreshold op amp," Electronics Letters, vol. 32, no. 7, pp. 605-606, March 1996

[4] A. Garimella, L. Garimella, J. Ramirez-Angulo, A.J. Lopez-Martin, R.G. Carvajal, "Low-voltage high performance compact all cascode CMOS current mirror," Electronics Letters, vol. 41, no. 25, pp. 1359-1360, December 2005

[5] S.S. Rajput, S.S.Jamuar, "Low voltage, low power, high performance current mirror for portable analogue and mixed mode applications," IEE Proceedings on Circuits, Devices and Systems, vol. 148, no. 5, pp. 273-278, October 2001

[6] J. Ramirez-Angulo, R.G. Carvajal, A. Torralba, "Low supply voltage high-performance CMOS current mirror with low input and output voltage requirements,"IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 51, no. 3, pp. 124-129, March 2004

[7] C. Galup-Montoro, M.C. Schneider, I.J.B. Loss, "Series-parallel association of FET's for high gain and high frequency applications," IEEE Journal of Solid-State Circuits, vol.29, no. 9, pp. 1094-1101, September 1994