Double-Gate Tunnel FET With High-κ Gate Dielectric

Kathy Boucart and Adrian Mihai Ionescu, *Member, IEEE*

***Abstract*—In this paper, we propose and validate a novel design for a double-gate tunnel field-effect transistor (DG Tunnel FET), for which the simulations show significant improvements compared with single-gate devices using an SiO_2 gate dielectric. For the first time, DG Tunnel FET devices, which are using a high-κ gate dielectric, are explored using realistic design parameters, showing an ON-current as high as 0.23 mA for a gate voltage of 1.8 V, an OFF-current of less than 1 fA (neglecting gate leakage), an improved average subthreshold swing of 57 mV/dec, and a minimum point slope of 11 mV/dec. The 2-D nature of Tunnel FET current flow is studied, demonstrating that the current is not confined to a channel at the gate-dielectric surface. When varying temperature, Tunnel FETs with a high-κ gate dielectric have a smaller threshold voltage shift than those using SiO_2, while the subthreshold slope for fixed values of V_g remains nearly unchanged, in contrast with the traditional MOSFET. Moreover, an I_{on}/I_{off} ratio of more than 2×10^{11} is shown for simulated devices with a gate length (over the intrinsic region) of 50 nm, which indicates that the Tunnel FET is a promising candidate to achieve better-than-ITRS low-standby-power switch performance.**

***Index Terms*—Band-to-band tunneling, double gate (DG), gated p-i-n diode, high-κ dielectric, subthreshold swing, tunnel field-effect transistor (FET).**

I. Introduction

As MOSFETs continue to get smaller and run into fundamental performance limitations, there is a renewed interest in exploring devices that use tunneling for their ON-current [1]–[14]. In particular, there is a focus on devices which act as field-effect transistors (FETs), where a change of gate voltage turns the current ON and OFF, but which use band-to-band tunneling in their ON-state, as well as in the transition between the OFF- and ON-states. These devices have the potential for extremely low OFF-current, and present the possibility to lower the subthreshold swing beyond the 60-mV/dec limit of conventional MOSFETs. Therefore, they seem well adapted to be candidates for an ultimately scaled quasi-ideal switch.

One such reported device is the Tunnel FET that incorporates a delta-layer of SiGe at the edge of the p+ region, in order to reduce the barrier width and, thereby, improve the subthreshold swing and ON-current [10], [11]. Another is the carbon-nanotube FET, which uses two independently controlled gates to change the energy bands in the channel [7].

In most of the literature published so far, the experimentally shown ON-currents are unacceptably low for a technology that would like to replace the conventional MOSFET (hereafter, simply referred to as the MOSFET). While OFF-currents are in the range of femtoamperes [7] or picoamperes [8], [9], ON-currents for applied drain and gate voltages of 2 V are still limited to the nanoamperes range [8], [9]. Furthermore, in order to have a CMOS-compatible technology, voltages should be limited even more, to about 1.2 V. While one publication shows ON-currents up to 0.5 mA/μm [13], these devices seem to be hybrid devices rather than pure Tunnel FETs, since their subthreshold slope is constant rather than V_g-dependent.

Looking at the 2005 ITRS [15], the Tunnel FET technology fits best into the Low Standby Power (LSTP) category. For the 50-nm node, an ON-current of 0.612 mA is required with an OFF-current of 10 pA. New Tunnel FET designs will be needed, in order to attain this I_{on} without sacrificing I_{off}. The design we present here, a double-gate (DG) device with a high-κ gate dielectric, is a way of achieving similar improvements (with an ON-current of 0.23 mA, lower than the ITRS requirement, but an OFF-current significantly reduced compared to a conventional MOSFET), while taking advantage of the reduced subthreshold swing possible with this sort of tunneling device. It is important to notice that the results presented here (notably, the ON-current) are not identical with those shown in our earlier report [21], due to a change in the band-to-band tunneling model. The new results, however, qualitatively confirm all initial findings and orders of magnitude (this will be discussed in detail in Section IV).

For reasons of cost and compatibility with already-existing fabrication technology, a process that uses standard CMOS fabrication steps and batch (rather than wafer-by-wafer) processing is preferable. The devices simulated here have been designed to be compatible with this type of processing, to make integration with CMOS possible and to keep costs low. The materials can be deposited with bulk-deposition methods, such as chemical vapor deposition (CVD), rather than expensive techniques, such as molecular beam epitaxy (MBE).

This paper explains the structure of a Tunnel FET and how it functions (in Section II), and discusses subthreshold slope for both MOSFETs and Tunnel FETs (in Section III). Section IV shows how the novel DG design, with an optimized silicon body thickness and a high-κ gate dielectric, results in improved device characteristics in terms of current and subthreshold swing, and discusses the 2-D nature of this device. The effects of temperature are also mentioned.

II. Device Operation and Structure

The investigated device structure is a lateral n-type Tunnel FET in a thin silicon layer, isolated from the substrate by a

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The authors are with the Swiss Federal Institute of Technology, 1015 Lausanne, Switzerland (e-mail: kathy.boucart@epfl.ch).

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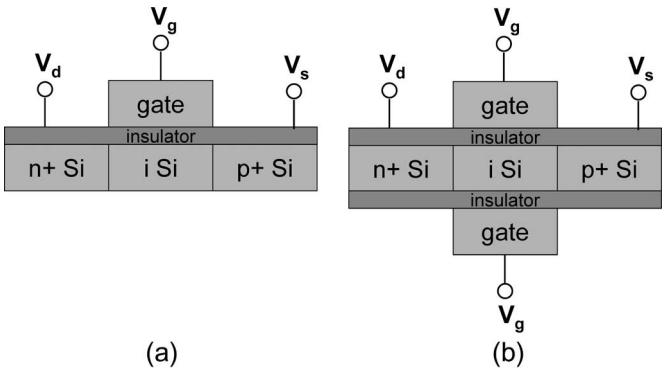

Fig. 1. Simulated Tunnel n-FETs. (a) Single-gate. (b) DG. SiO_2 and high-κ gate dielectrics were studied. $t_{\mathrm{dielectric}} = 3$ nm (physical) and $L_{\mathrm{intrinsic}} = 50$ nm. Drain doping $(\mathrm{n}+) = 5 \times 10^{18}$ atoms/cm^3 and source doping $(\mathrm{p}+) = 10^{20}$ atoms/cm^3.

dielectric layer. The basic design is a gated p-i-n diode. The tunneling takes place in this device between the intrinsic and p+ regions. Schematics of two of the devices simulated are shown in Fig. 1; here, our discussions will primarily focus on the DG device. To operate these devices, the p-i-n diode is reverse-biased—in our simulations, the source is grounded, and a positive voltage is applied to the drain—and a voltage is applied to the gate(s). Without a gate voltage, the width of the energy barrier between the intrinsic region and the p+ region is much wider than 10 nm (the approximate minimum for significant tunneling probability), and the device is in the OFF-state, as shown in the cross section of the device in Fig. 2(a). As the positive gate voltage increases, the bands in the intrinsic region are pushed down in energy, narrowing the tunneling barrier and allowing tunneling current to flow, as shown in Fig. 2(b).

In order to be consistent with MOSFET technology, the names of the device terminals are chosen such that voltages are applied in a similar way for Tunnel FET operation. Since a reverse bias is needed across the p-i-n structure in order to create tunneling and since an NMOS operates when positive voltages are applied to the drain and gate, the n-region is referred to as the drain and the p+ region as the source.

Doping has been optimized in order to create the maximum ON-current, while keeping OFF-current low. As discussed in the study in [8], it is desirable to have a high source doping (around 10^{20} atoms/cm^3 or even higher) but a lower drain doping. For these simulations, the doping levels were 1×10^{20}, 1×10^{17}, and 5×10^{18} atoms/cm^3 for the source, intrinsic, and drain regions, respectively.

The work function chosen for the gate contact is 4.5 eV, corresponding to a metal gate stack. This could correspond to a stack comprised of tungsten (W) and titanium nitride (TiN) [16].

III. Subthreshold Swing

The subthreshold swing of a device is defined as the change in gate voltage which must be applied in order to create a one decade increase in the output current or

$$S = \frac{dV_g}{d(\log I_d)} [\mathrm{mV/dec}]. \tag{1}$$

The subthreshold swing of a MOSFET is limited by the diffusion current physics of the device in weak inversion, such that the minimum possible swing in an ideal device is

$$S_{\mathrm{MOSFET}} = \ln(10)\frac{kT}{q} [\mathrm{mV/dec}] \tag{2}$$

which is about 60 mV/dec at room temperature (300 K).

A Tunnel FET, on the other hand, does not experience the same physical limitation, because the current mechanism relies on the tunneling-barrier width rather than the formation of an inversion channel. Starting from Hurkx's band-to-band tunneling model [17, eq. (12)], as used in Silvaco Atlas [18], the subthreshold slope for a Tunnel FET can be expressed in terms of the gate voltage as

$$S_{\mathrm{TFET}} = \frac{V_{\mathrm{gs}}^2}{5.75(V_{\mathrm{gs}} + \mathrm{Const})} [\mathrm{mV/dec}] \tag{3}$$

where the constant is determined by device dimensions and material parameters. Equation (3) shows that, in Tunnel FETs, the subthreshold slope is highly dependent on the gate voltage, and one should distinguish between the point and the average slopes (the latter being the more important for switch performance). This is an important remark for future benchmarking of new abrupt switch solutions, for which most reports currently point to the optimization of the point slope only.

The benefits of a DG Tunnel FET over a DG MOSFET is shown in Fig. 3, which compares the I_d–V_g characteristics of an optimized asymmetrical DG MOSFET from [19] with those of a simulated DG Tunnel FET, being proposed for the first time in this paper. The two devices have the same dimensions for dielectric thickness (3 nm), channel length (i-region length in the Tunnel FET, equal to 50 nm), and body thickness (10 nm). The optimized DG Tunnel FET uses a high-κ gate dielectric with a dielectric constant of 29, as will be discussed later. It is important to notice the difference between the subthreshold regions in these two types of devices. A MOSFET has a constant slope between the OFF-state and threshold. A Tunnel FET, however, demonstrates a slope that is steeper (smaller swing) closer to the OFF-state and less steep closer to threshold and varies as a function of the gate voltage. Since the threshold voltage of a Tunnel FET cannot be extracted using certain standard MOSFET techniques, in this paper, we use the constant-current method, with a threshold current of 10^{-7} A/μm.

It is clear that the swing for the Tunnel FET in Fig. 3 is lower than that of the MOSFET, whether we look at the point slope or the average slope. The point value of S is defined as the minimum swing value at any point on the I_d–V_g curve. The average S value is calculated between the voltage at which the current begins to increase with increasing gate voltage, and the threshold voltage. These two values are different because S is a function of V_g. Their extraction is shown in the inset of Fig. 3.

A key issue in future DG Tunnel FETs is the simultaneous optimization of $I_{\mathrm{on}}/I_{\mathrm{off}}$ and subthreshold swing. A basic analytical formulation of the tunneling probability $T(E)$, for

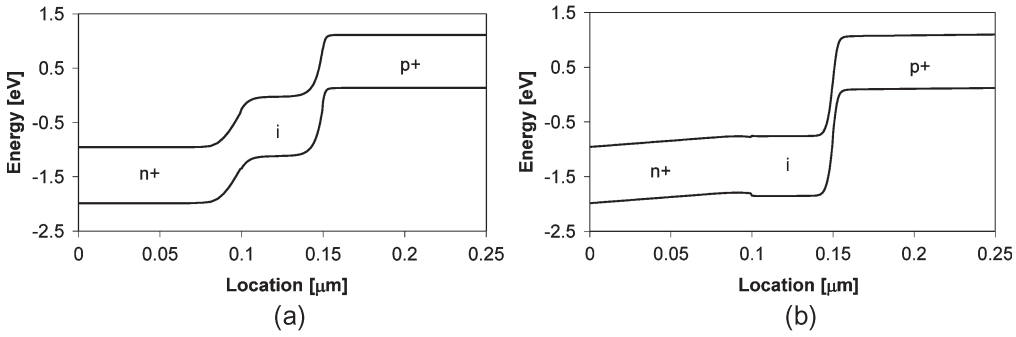

Fig. 2. Device structure corresponds to Fig. 1. (a) Schematic of energy-band diagram of the OFF-state of the Tunnel FET. $V_d = 1$ V and $V_g = 0$ V. In this state, the only current is p-i-n diode leakage current. (b) Schematic of energy-band diagram of the ON-state of the Tunnel FET. In this state, the energy barrier is thin enough that electrons can tunnel from the valance band of the p+ region to the conduction band of the intrinsic region. $V_d = 1$ V and $V_g = 1.8$ V.

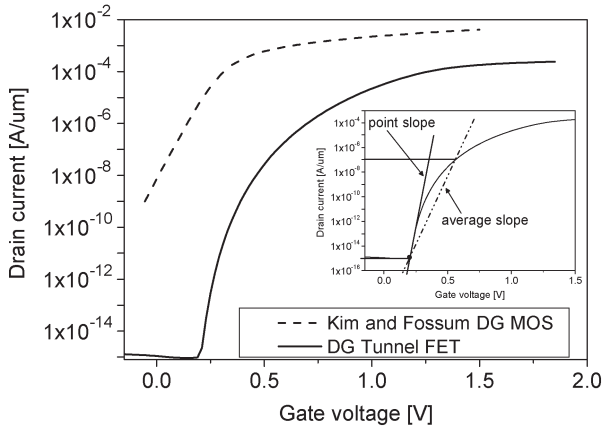

Fig. 3. Comparison of simulated DG-Tunnel-FET characteristics with those of an optimized asymmetrical DG MOSFET (from [13]). While the subthreshold slope is constant for a MOSFET in the subthreshold region, it is a function of V_g for a Tunnel FET. Both devices have $L = 50$ nm, $t_{\mathrm{body}} = 5$ nm, and $t_{\mathrm{dielectric}} = 3$ nm. $V_d = 1$ V. Inset: Extraction of the average slope, and the point at which the point slope is measured.

ultrathin films and gate oxides, has been derived in the study in [20] and shows that

$$T(E) \propto \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3|e|\hbar(E_g+\Delta\Phi)}\sqrt{\frac{\varepsilon_{\mathrm{Si}}}{\varepsilon_{\mathrm{ox}}}t_{\mathrm{ox}}t_{\mathrm{Si}}}\right)\Delta\Phi \quad (4)$$

where m^* is the effective carrier mass, E_g is the bandgap, $\Delta\Phi$ is the energy range over which tunneling can take place, and t_{ox}, t_{Si}, $\varepsilon_{\mathrm{ox}}$, and $\varepsilon_{\mathrm{Si}}$ are the oxide and silicon film thickness and dielectric constants, respectively. Equation (4) suggests that high-κ dielectrics would favor an increased tunneling rate. This comes from the improved electrical coupling between the gate and the tunneling junction due to the increased gate capacitance. In contrast with a MOSFET, the current has an exponential dependence on the square root of the gate capacitance rather than a linear one. Based on this observation, we focus our device optimization on DG Tunnel FETs with high-κ gate dielectrics rather than on the engineering of the material bandgap (as in previous approaches [10], [11] that proposed Tunnel FETs with SiGe).

IV. Results and Discussion

A. Simulation Parameters

All simulations were done in Silvaco Atlas, version 5.11.24.C, which uses a nonlocal Hurkx band-to-band tunneling model [18]. This version of Atlas shows better physical consistency over the version used in a previous publication [21], which used a local band-to-band tunneling (BTB) model. The previously used local model calculates a generation rate at each mesh node from the magnitude of the electric field. In contrast, the currently used nonlocal model works by calculating the tunneling probability from the energy-band diagrams across the device. The simulations use a very fine mesh across the region where the tunneling takes place, from which energy-band profiles and the energies for which band-to-band tunneling is permitted, are determined. The positions for the start and end of tunneling are found for each energy and are used to calculate the current in that energy range. Atlas uses a two-band approximation for the evanescent wavevector and a carefully applied Wentzel–Kramer–Brillouin method.

Gate leakage was neglected in these simulations and can be expected to limit the OFF-current in fabricated Tunnel FETs. Bandgap narrowing was enabled.

B. Double Gate (DG)

In an integrated DG-CMOS/DG-Tunnel-FET process, the Tunnel FETs will benefit from the added gate, such that the current will be at least doubled. In this way, the ON-current is boosted, while the OFF-current, still in the femtoamperes or picoamperes range, increases by the same factor but remains extremely low. It is worth noting that, for ultrathin silicon-on-insulator (SOI) MOSFETs, some reports suggest that this improvement can be even higher when volume inversion takes place [22].

C. High-κ Gate Dielectric

An even higher ON-current and decreased subthreshold swing can be obtained by the careful choice of a gate dielectric. As shown in Fig. 4(a), current increases as the gate dielectric constant increases. Here, Si_3N_4 and two high-κ dielectrics, HfO_2 and ZrO_2, are compared to SiO_2, all with a physical

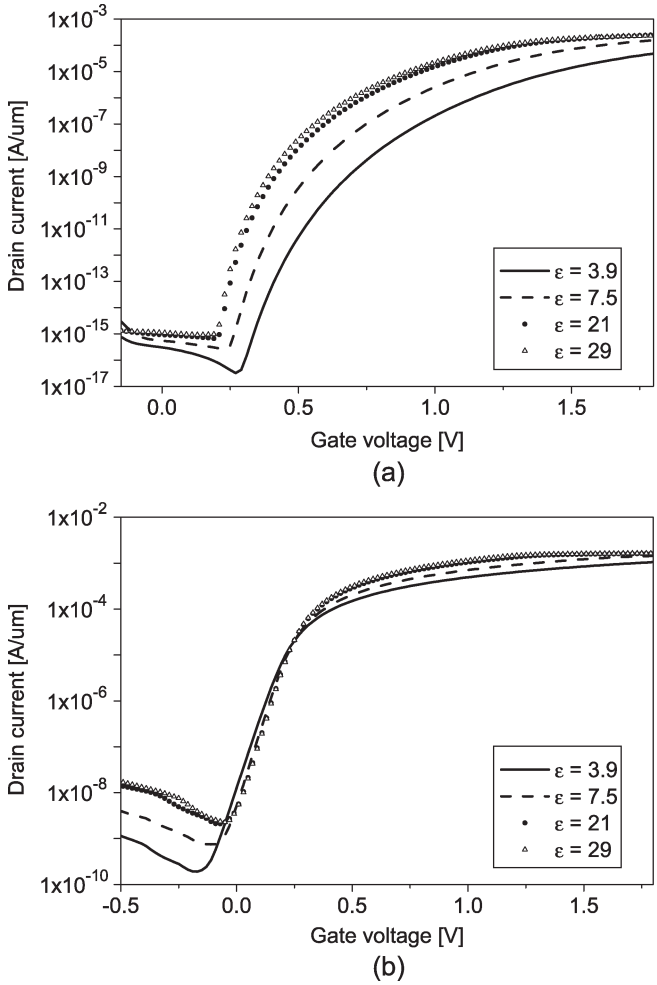

Fig. 4. (a) DG-Tunnel-FET characteristics for various gate dielectrics. $\varepsilon = 3.9$ corresponds to SiO_2, $\varepsilon = 7.5$ to Si_3N_4, $\varepsilon = 21$ to HfO_2, and $\varepsilon = 29$ to ZrO_2. $L_{\mathrm{intrinsic}} = 50$ nm, $t_{\mathrm{dielectric}} = 3$ nm, and $t_{\mathrm{Si}} = 10$ nm. $V_d = 1$ V. (b) Characteristics of a simplified single-gate NMOSFET for various gate dielectrics. Junctions were ideally abrupt, as for the Tunnel FET, with source and drain doped to 10^{20} and the p-type body doped to 10^{17}, $L = 50$ nm, $t_{\mathrm{dielectric}} = 3$ nm, and $t_{\mathrm{Si}} = 5$ nm. $V_d = 1$ V.

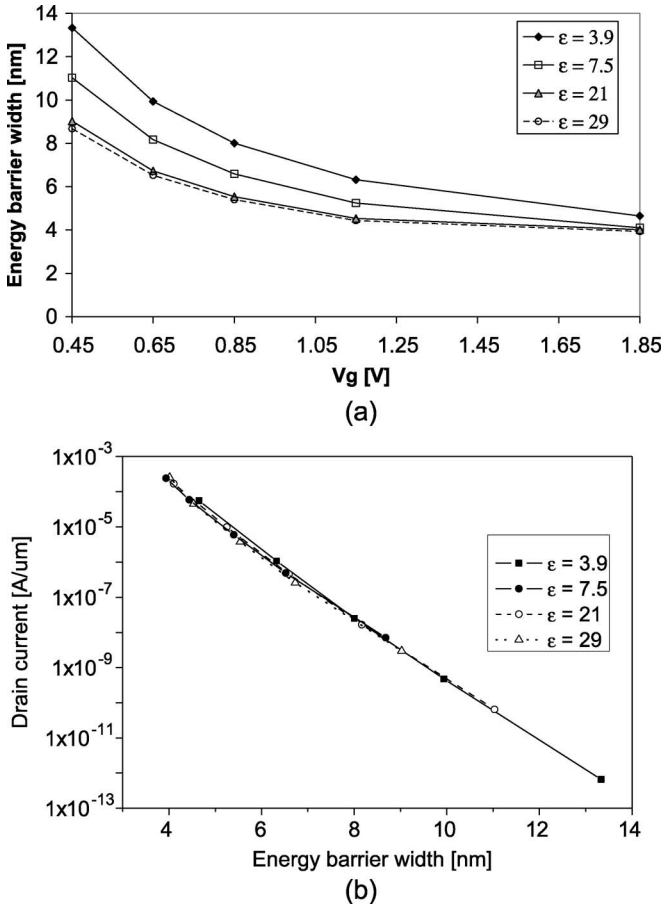

Fig. 5. (a) Width of energy barrier, for band-to-band tunneling, versus V_g, for different values of the gate-dielectric constant. (b) Drain current versus energy-barrier width for different values of the gate-dielectric constant.

thickness of 3 nm. The high-κ materials have dielectric constants of 21 and 29, respectively. The reduced effective oxide thickness provided by these dielectrics offers a solution to the low-ON-current problem experienced by some existing Tunnel FETs at CMOS-compatible voltages. The OFF-current is less than 1 fA.

Interestingly, the ON-current does not increase merely proportionally to the increase in the gate capacitance, as it would for a MOSFET. A simplified MOSFET 2-D structure has been designed for numerical simulation in order to show the difference between the two [Fig. 4(b)]. For Tunnel FETs, as we saw in (4), the improved coupling between the gate and the tunneling barrier has an exponential effect rather than a linear one. The ON-current of a Tunnel FET depends on the width of the energy barrier between the intrinsic and p+ regions, and the current increases exponentially with a reduction in this barrier width. Fig. 5(a) shows the dependence of the energy-barrier width on the gate voltage for the gate-dielectric constants studied. The barrier width was extracted from the simulated band diagrams at a distance of 2.5 nm from the dielectric surface, with 1 V applied to the drain and the source grounded. Fig. 5(b) shows the exponential dependence of the simulated tunneling current on the barrier width. Fig. 6 shows the normalized I_d–V_g characteristics for different gate dielectrics, with each drain–current divided by the gate-dielectric constant of that device. From this figure, it is clear that the improvement in current cannot be simply attributed to a proportional increase of the gate capacitance with the gate-dielectric constant.

In addition to improved I_{on}, both the point and average subthreshold swing improve as the result of the better gate coupling given by a high-κ dielectric. By raising the ON-portion of the I_d–V_g curve [see Fig. 4(a)], we effectively "uncover" a steeper part of the curve in the subthreshold, decreasing the point swing. The average swing is also much improved with a high-κ dielectric, since the threshold voltage falls on a steeper part of the curve. In contrast, the MOSFET swing hits the 60-mV/dec limit [Fig. 4(b)] and cannot improve further.

Fig. 7 shows the linear relationship between $\log(I_D)$ and $\varepsilon_{\mathrm{ox}}^{-0.5}$, which supports what we expected to see from (4).

While high-κ dielectrics have advantages for device characteristics, when put directly in contact with a silicon channel, they can lead to defects at the semiconductor/dielectric interface. Although Tunnel FETs might be less sensitive to changes in channel mobility than MOSFETs, as will be discussed below, standard CMOS fabrication techniques require an interfacial

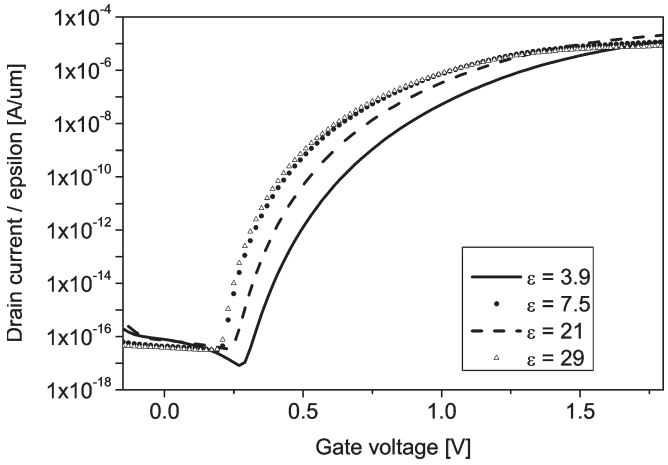

Fig. 6. DG Tunnel FET characteristics, normalized for each gate-dielectric constant (drain current/gate-dielectric constant). $V_d = 1$ V. The increase in drain current is not linearly proportional to the increase in gate capacitance as it would be for MOSFET. Device corresponds to Fig. 1.

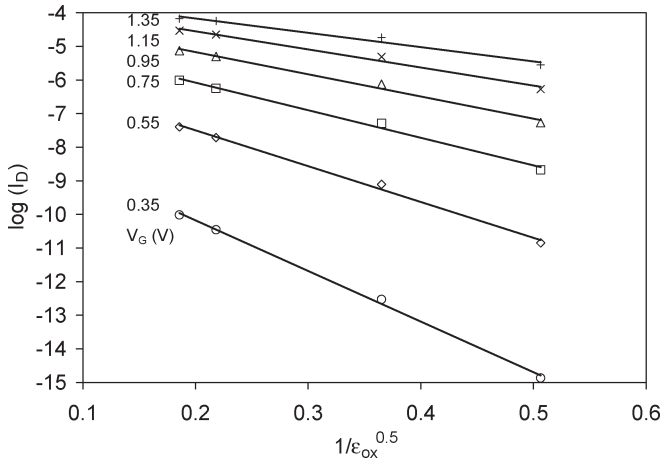

Fig. 7. $\log(I_D)$ versus $1/\varepsilon_{\rm ox}^{0.5}$; the linearity of the plot is in good agreement with the proposed modeling in (4).

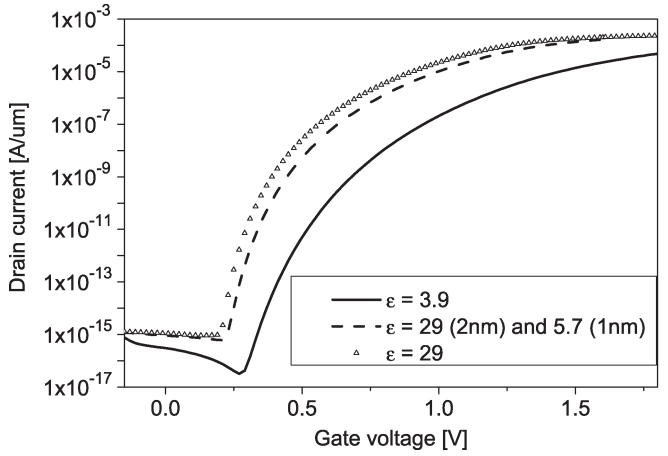

Fig. 8. DG-Tunnel-FET characteristics for a structure with 2 nm of a high-κ dielectric ($\varepsilon_{\rm dielectric} = 29$) with a 1-nm interfacial layer of oxynitride ($\varepsilon_{\rm dielectric} = 5.7$), compared with structures having 3 nm of the high-κ dielectric or 3 nm of SiO_2. $V_d = 1$ V.

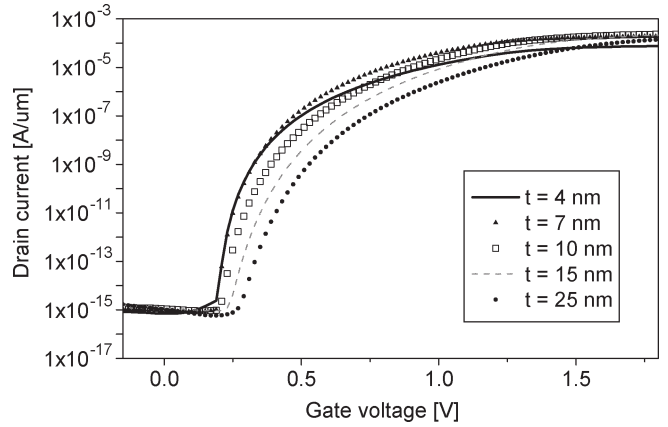

Fig. 9. DG-Tunnel-FET I_d–V_g characteristics for various silicon body thicknesses. $L_{\rm intrinsic} = 50$ nm, $t_{\rm dielectric} = 3$ nm, and $\varepsilon_{\rm dielectric} = 29$. $V_d = 1$ V.

layer between the high-κ dielectric and the silicon channel. A Tunnel FET with a more CMOS-compatible dielectric layer has been simulated, and the resulting I_d–V_g curve is shown in Fig. 8. The simulated device had 1 nm of oxynitride at the silicon surface and 2 nm of ZrO_2. It is clear that even with an interfacial layer, the subthreshold slope and ON-current are very much improved over the device with an SiO_2 gate dielectric.

High-κ dielectrics bring additional challenges such as the limitations of soft and hard dielectric breakdown. Depending on the characteristics of fabricated high-κ dielectric layers, it may be necessary to limit applied gate voltages more than what is reported here. For example, depending on whether the structure of a HfO_2 layer is more tetragonal or cubic, the breakdown field could be 3.9 or 6.7 MV/cm, leading to a breakdown voltage of $V_g = 1.17$ V or 2.01 V [23]. Of course, these voltage numbers would change depending on the high-κ dielectric thickness and/or the existence of an interfacial layer. Although the current simulations aim to stay within optimistic limits, a reoptimization of the design will be needed once the parameters of fabricated materials are known.

D. Thin-Film Structure

SOI and silicon-on-nothing fabrication technology are two fabrication methods currently used to create DG devices. Both of these techniques are commonly used on thin films, down to several nanometers thick. The thickness of a Tunnel FET influences the shape of its I_d–V_g curve, as shown in Fig. 9.

Several trends can be seen in this figure. First, OFF-current, which depends on the cross section of the p-i-n structure, slightly decreases as expected with thickness. As the film gets thinner than 10 nm, ON-current starts to drop, possibly due to the reduced cross-sectional area available for current flow. Due to these trends, the ratio $I_{\rm on}/I_{\rm off}$ will have a maximum when plotted against silicon-layer thickness. Fig. 10 shows that this optimum value occurs when $t_{\rm Si}$ is between 7 and 8 nm, depending on the value chosen for $V_{\rm DD}$, where $I_{\rm on}$ is taken at $V_g = V_{\rm DD}$. The maximum ratio is about 2×10^{11}, and as a comparison, the optimized asymmetrical DG MOSFET from [19] has an $I_{\rm on}/I_{\rm off}$ ratio of 10^6 with $I_{\rm on}$ taken at $V_g = 1.5$ V. The order of magnitude of the $I_{\rm on}/I_{\rm off}$ ratio is not dramatically modified by a variation of the film thickness, which would

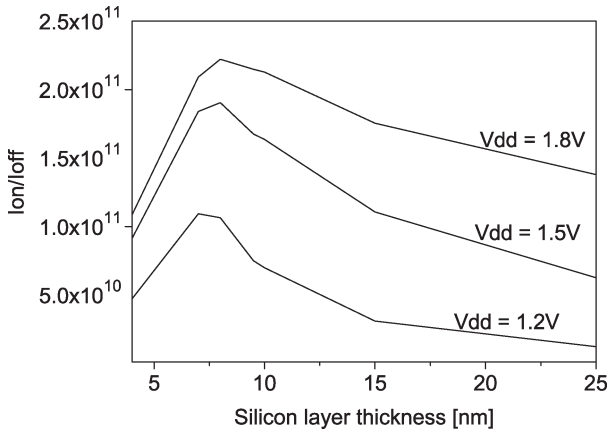

Fig. 10. Ratio $I_{\rm on}/I_{\rm off}$ as a function of the silicon layer thickness, for $\varepsilon_{\rm dielectric} = 29$. A maximum, the optimum point, occurs in the thickness range of 7–8 nm, depending on the value of Vdd used. 1 V was applied to the drain.

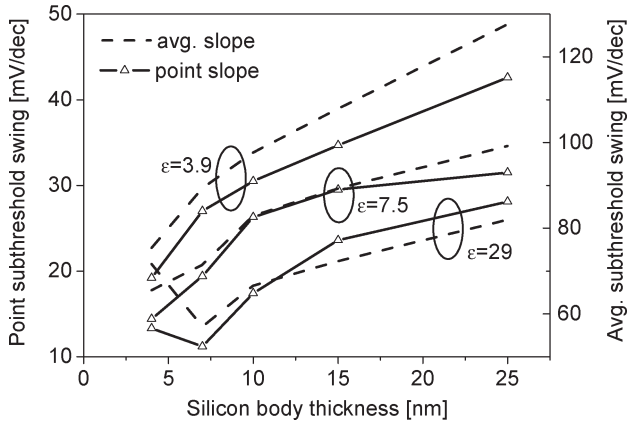

Fig. 11. (Left y axis) Point subthreshold swing and (right y axis) average subthreshold swing as a function of silicon layer thickness for different gate-dielectric constants. $L_{\rm intrinsic} = 50$ nm and $t_{\rm dielectric} = 3$ nm.

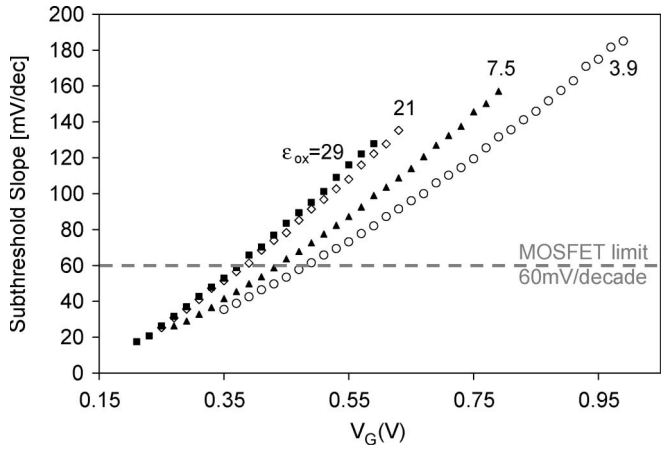

Fig. 12. Dependence of the Tunnel FET subthreshold slope on gate voltage for different dielectric constants, from numerical simulation. Each curve goes up to the threshold voltage of that device. $L = 50$ nm, $t_{\rm dielectric} = 3$ nm, and $t_{\rm Si} = 10$ nm.

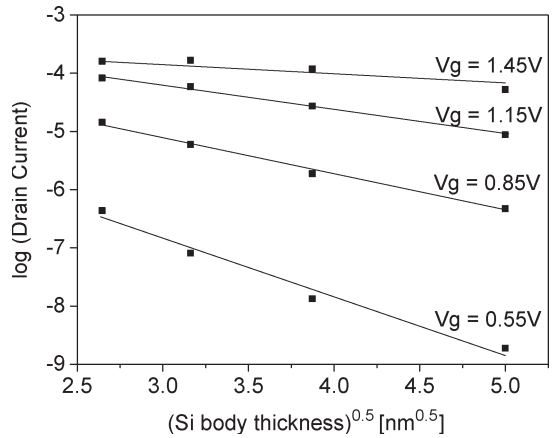

Fig. 13. $\log(I_D)$ versus $1/t_{\rm Si}^{0.5}$ at different gate voltages; the relationship is approximately linear, in agreement with the proposed modeling of (4).

be advantageous if there were variations of body thickness in devices on thin films.

Fig. 9 also reveals that both the average and point values of subthreshold swing become lower as thickness decreases, as shown in Fig. 11. The subthreshold swing also decreases as high-κ dielectrics are used. While the point swing is lower than the 60-mV/dec limit for MOSFETs for all dielectrics and thicknesses simulated, the average swing is lower than this limit only for a high-κ dielectric with a constant of 29 (ZrO_2) and a silicon body thickness of less than 10 nm. The dependence of swing on the gate voltage up to the threshold voltage is shown in Fig. 12, demonstrating that, at low gate voltages, Tunnel FETs have a subthreshold swing under the 60-mV/dec MOSFET limit.

Clearly, these values of the average swing depend upon our chosen definition for the threshold voltage. A lower constant-current value would lower the threshold voltage and, in turn, would advantageously lower the average swing values. It is worth mentioning, however, that qualitatively, all the trends of the curves remain the same.

The relationship between the drain current and the body thickness can be seen in (4): $\log(I_D)$ is linearly dependent on $t_{\rm Si}^{-0.5}$. Fig. 9 shows that this relation may hold true for devices thicker than about 7 nm, but when the silicon body is too thin, the drain current is limited by the reduced body thickness. Fig. 13 shows the extraction of the relationship between $\log(I_D)$ and $t_{\rm Si}^{-0.5}$ for various values of the gate voltage. This behavior will need to be explored further.

Similar results are expected for a p-type device, which has opposite doping from an n-type device [21].

E. Two-Dimensional Simulations

All simulations carried out in Silvaco Atlas were 2-D, and it is informative to look at vertical cross sections of the energy bands of the Tunnel FET, as well as contour plots in two dimensions, in order to understand the functioning of the device. All diagrams are shown for single-gate devices because, with the models currently used, DG devices show identical results, symmetrical for the two halves.

Looking first at the x direction component of the electric field across a device which is ON [Fig. 14(a)], we see that the electric field is close to zero nearly everywhere. Between the intrinsic and p+ regions, where the tunneling takes place, we see a high

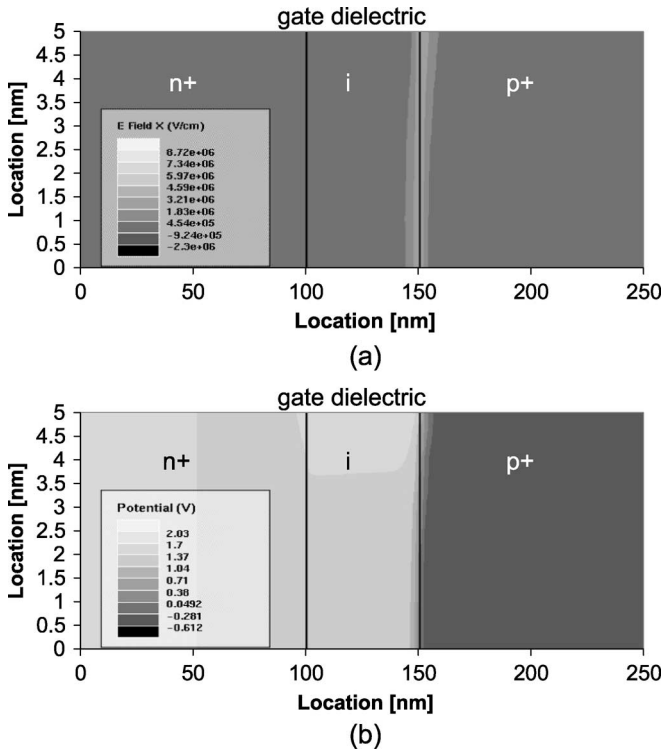

Fig. 14. (a) Contour plot of the x-component of the electric field in a single-gate Tunnel FET biased with $V_d = 1$ V and $V_g = 1.8$ V, in overdrive, with $t_{\mathrm{dielectric}} = 3$ nm and $\varepsilon_{\mathrm{dielectric}} = 29$. (b) Contour plot of the potential of the same device under the same bias conditions.

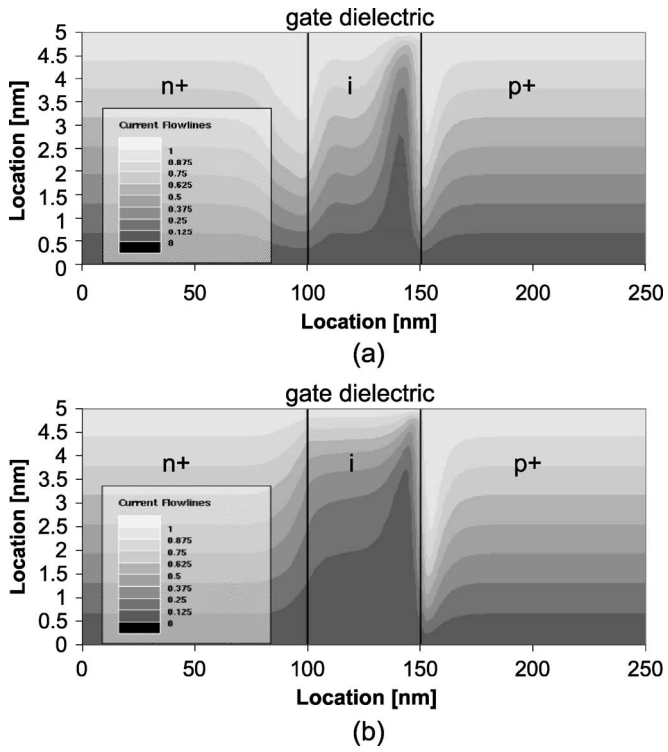

Fig. 15. Current flowlines for the same Tunnel FET as that shown in Fig. 14, with (a) $V_g = V_t$ (obtained using the constant-current technique) and (b) $V_g = 1.8$ V.

positive field throughout the depth of the device. In the potential contour plot for this same device in the same state [Fig. 14(b)], we see that the potential drops abruptly at the tunnel junction, and once again, this holds true for the entire device depth, not just at the surface.

In the diagrams of current flowlines, shown at the threshold voltage [Fig. 15(a)] and in overdrive [Fig. 15(b)], it is clear that the current does not stay close to the gate dielectric as in a MOSFET. As the electrons moves from right to left (source to drain) in the Tunnel FET, they move parallel to the interface through most of the source, then move away from the dielectric interface at about the location of the tunnel junction and, then, attracted by the positive voltage on the gate, flow closer to the interface before spreading back out and passing through the drain parallel to the interface, as they were in the source (electrical contacts are on the sides of the source and drain.)

Inspection of some vertical energy-band cross sections can help in understanding this current flow. Fig. 16(a) shows the energy bands taken vertically at the junction between the source and intrinsic regions, where the band-to-band tunneling takes place. The energy is lower at the dielectric surface than deep in the body, particularly at high V_g, as can also be noticed in the potential contours where we see that the tunnel junction (the abrupt change in potential) is more in the source near the dielectric and more in the intrinsic region deeper in the body. Therefore, just at this junction, electrons will want to go toward the dielectric, to lower energy. Fig. 16(b) shows the energy bands cutting vertically through the very center of the intrinsic region. Here, the bands are nearly flat, and the electrons no longer stay as close to the gate dielectric, as evidenced by the current flowlines.

The current-flow pattern promises to give an advantage over conventional MOSFETs in terms of the effects of surface roughness on device characteristics. Tunnel FETs should be less affected by variations in mobility due to the current being less confined to the surface under the gate.

F. Temperature

The temperature dependence of silicon Tunnel FETs with an SiO_2 gate dielectric has been reported in [9] and [12]. Tunnel FETs with a high-κ dielectric show the same general trends: the OFF-current, caused by the generation of carriers in a reverse-biased junction, increases with temperature, while the ON-current, coming from band-to-band tunneling, changes only slightly, as shown in Fig. 17. The inset of Fig. 17 shows that the subthreshold swing of the Tunnel FET for fixed values of V_g is nearly constant as temperature increases, unlike that of a MOSFET, which degrades proportionally to the increase in temperature, as can be seen in (2). Due to the rising OFF-current, the average subthreshold swing of Tunnel FETs will significantly degrade with increasing temperature, but beyond the leakage level, the current characteristics remain nearly unchanged.

The use of a high-κ dielectric rather than SiO_2 leads to a decrease in the threshold-voltage shift caused by temperature. This is to be expected with the constant-current method of V_t extraction, since with a higher dielectric constant, V_t falls on a steeper part of the I_d–V_g curve. While $\Delta V_t/\Delta T$ is in the range

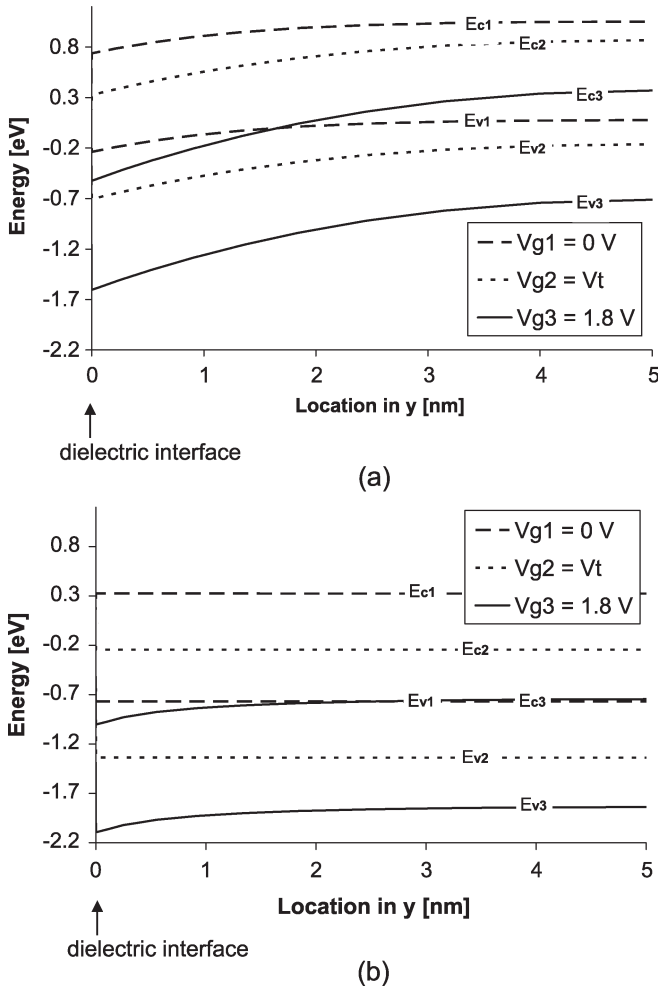

Fig. 16. Cross sections of the energy bands of the same device as that shown in Figs. 14 and 15, taken vertically from the dielectric interface through the body. (a) Cross section at $x = 150$ nm, just at the junction between the intrinsic and p+ regions, where tunneling takes place. (b) Cross section at $x = 125$ nm, at the center of the intrinsic region.

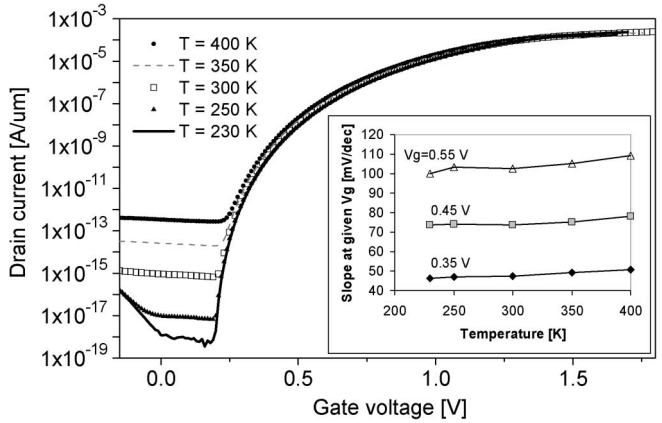

Fig. 17. I_d–V_g characteristics for various temperatures. $V_d = 1$ V. As temperature increases, $I_{\rm off}$ increases, but $I_{\rm on}$ changes very little. Inset: Slope at specific V_g values, versus temperature in Kelvin. We see that these values of slope are only slightly affected by changes in temperature.

of 1–2 mV/K for Si/SiO_2 Tunnel FETs [12] and MOSFETs, we find that $\Delta V_t/\Delta T$ is 0.2–0.3 mV/K for Tunnel FETs with a gate-dielectric constant of 21.

V. Conclusion

We proposed, discussed the basic static operation, and studied by simulation the characteristics of a DG Tunnel FET as a better-than-60-mV/dec current switch. The investigated Tunnel FET showed improved characteristics including higher ON-current and a lower subthreshold swing, after the proposed design modifications: a double gate, a high-κ gate dielectric, and an optimized silicon body thickness. The DG and high-κ dielectric raise ON-current to 0.23 mA at $V_g = 1.8$ V and provide a corresponding improvement in the average subthreshold swing, as low as 57 mV/dec, and a minimum point swing of 11 mV/dec. An optimum silicon body layer thickness of between 7 and 8 nm was found for the studied device with a gate length of 50 nm, maximizing the ratio $I_{\rm on}/I_{\rm off}$ to 2×10^{11}. In addition, the subthreshold swing for fixed values of V_g remains nearly unchanged as temperature increases. The Tunnel FET's promising behavior makes it a strong candidate to complement or replace MOSFET technology, particularly for LSTP applications.

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Kathy Boucart received the B.S. degree in the subject of Radio/TV/Film from the Northwestern University, Evanston, IL, in 1994. She did her undergraduate work in electrical and computer engineering at the University of Texas, Austin, from 1999 to 2001, and received the Master's degree from the Department of Electrical Engineering and Computer Science, University of California, Berkeley, in 2003. She is currently working toward the Ph.D. degree at the Electronics Laboratory, Swiss Federal Institute of Technology (l'Ecole Polytechnique Fédérale de Lausanne).

Ms. Boucart was the recipient of a National Science Foundation (NSF) Fellowship while in the Department of Electrical Engineering and Computer Science, University of California, Berkeley.

Adrian Mihai Ionescu (S'91–M'93) received the B.S. and M.S. degrees from the Polytechnic Institute of Bucharest, Bucharest, Romania, in 1989, and the Ph.D. degree from the National Polytechnic Institute of Grenoble, France, in 1997.

He has held staff and/or visiting positions at LETI-CEA, Grenoble, France, LPCS-ENSERG, Grenoble, France, and Stanford University, Stanford, CA, in 1998 and 1999. Since 1999, he has been a Consulting Expert for the Information Society Technologies (IST) program of the European Commission, Brussels, and was recently appointed as National Representative of Switzerland for the European Nanoelectronics Initiative Advisory Council. From 2002 to 2006, he was the Director of the Laboratory of Micro/Nanoelectronic Devices (LEG-2) and also served as the Director of the Institute of Microelectronics and Microsystems of the Swiss Federal Institute of Technology (l'Ecole Polytechnique Fédérale de Lausanne), Lausanne, Switzerland, where he is currently an Associate Professor. He has published more than 100 articles in international journals and conferences.

Dr. Ionescu was the recipient of three Best Paper Awards in international conferences and of the Annual Award of the Technical Section of the Romanian Academy of Sciences in 1994. He served in the IEEE International Symposium on Quality Electronic Design and International Electron Devices Meeting (IEDM) conference technical committees in 2003 and 2004, and as Technical Program Committee Chair of European Solid-State Device Research Conference (ESSDERC) in 2006.