Design and Performance Assessment of GaSb/Si Heterojunction Vertical TFET with delta doped layer for enhanced DC and AF/RF characteristics

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[[1]](#footnote-1) ***Abstract*—** **In this study, we suggest a novel GaSb/Si Heterojunction incorporated with a delta-doped layer in a Vertical TFET (GaSb-VTFET). The motivation behind the work is to have improved SS with higher ON current and transconductance using Heterojunction structure with delta doped layer. So this device presents a superior performance by enhancing the vertical tunnelling current components and minimising the lateral components. The primary function of including the delta-doped layer in the channel is to diminish the OFF-state leakage components. Various DC characteristics parameters like SS, Vt , ION/IOFF and analogue/RF parameters are also explored for VTFETs with or without heterojunction. The proposed device's comprehensive DC and analogue analysis is compared with a silicon-based source without doped layer (conventional) VTFET (Si-VTFET). The proposed GaSb-based source material with doped layer vertical TFET (GaSb-VTFET) shows enhanced characteristics. The proposed device satisfies the ITRS roadmap guidelines for low standby power by having ION value 6x10-5****A/µm, a standby power IOFF value 10-18 A/µm with SS value 21 mV/decade. So GaSb-VTFET's results suggest that it might be a good contender for ultra-low-power applications.**

Index Terms — Delta doped layer, Vertical TFET, Heterojunction, Tunneling, Ultra low power.

# INTRODUCTION

Conventional MOSFETs are being progressively scaled down to increase their current driving abilities, device density, and analogue performance but at lower costs. [1]. But, the continued miniaturisation affects the device performance by giving rise to complications originating from the shrinking known as short channel effects (SCEs) [2] and owing to these, the current conventional MOSFETs are challenging to be used in low-power applications because their SS is not further scalable at short channel lengths at 300 K. TFETs in this regard come to rescue being able to achieve highly scaled SS, they are very promising [3]. Charge carriers in TFETs undergo band-to-band tunnelling (BTBT), irrespective of thermionic emission as in MOSFETs [4-6]. However, despite the advantages mentioned above, conventional TFETs have low drive current capabilities, making them less suitable for low-power applications [7-8]. Various techniques have been reported in different works presenting ways to improve the drive current in TFET, like using a multi-gate device structure, using buried oxide, and using SOI substrate [9-11]. These schemes result in enhanced ON current and transconductance efficiency with reduced leakage current. Low off-state current requires maintaining low SS at room temperatures, but the SS is constrained to 60mV/decade due to the thermionic emission's working mechanism, which is why SS is a temperature-dependent quantity.

Another inherent attribute of TFETs is ambipolar current [12], which means they function in both positive and negative gate voltage polarities. Because this feature limits the usage of TFETs in many circuit applications, numerous approaches for limiting and reducing the ambipolar current have been developed. Heterostructures and high bandgap materials at the drain side are two regularly utilised approaches for lowering ambipolar current [12-14]. These methods result in an increase in tunnelling width, which reduces the ambipolar current.

It has been recommended to employ GaSb, a low band gap material with a high k gate dielectric. The source-channel interface's staggered heterojunctions based on III-V materials are suitable for low-voltage operation for the best power consumption and performance, according to results [12]. The GaSb staggered heterojunction VTFET's performance with a doped layer and Si VTFET’s performance without a doped layer were evaluated using the TCAD simulation tool[15].The suggested V-GaSb/Si TFET's heterojunction manufacturing capability is established on recent advances in GaSb fabrication on clean Si substrates [3], [4]. GaSb-based highly doped layer tends to serve as a buffer pocket on silicon. In this article, we have studied the analogue, DC and temperature-affected sub-threshold characteristics of the Si & GaSb-VTFET.

In the inquiry, device characteristics and gate work function have been changed to enhance functional performance and decrease ambipolar current. The paper is divided into four sections, the first being introduction where the motivation for the study is discussed, in the second section, we discuss the simulations' device parameters and model specifications, in the third section, results are presented and analysed while in the last section, we discuss the conclusions drawn from the study.

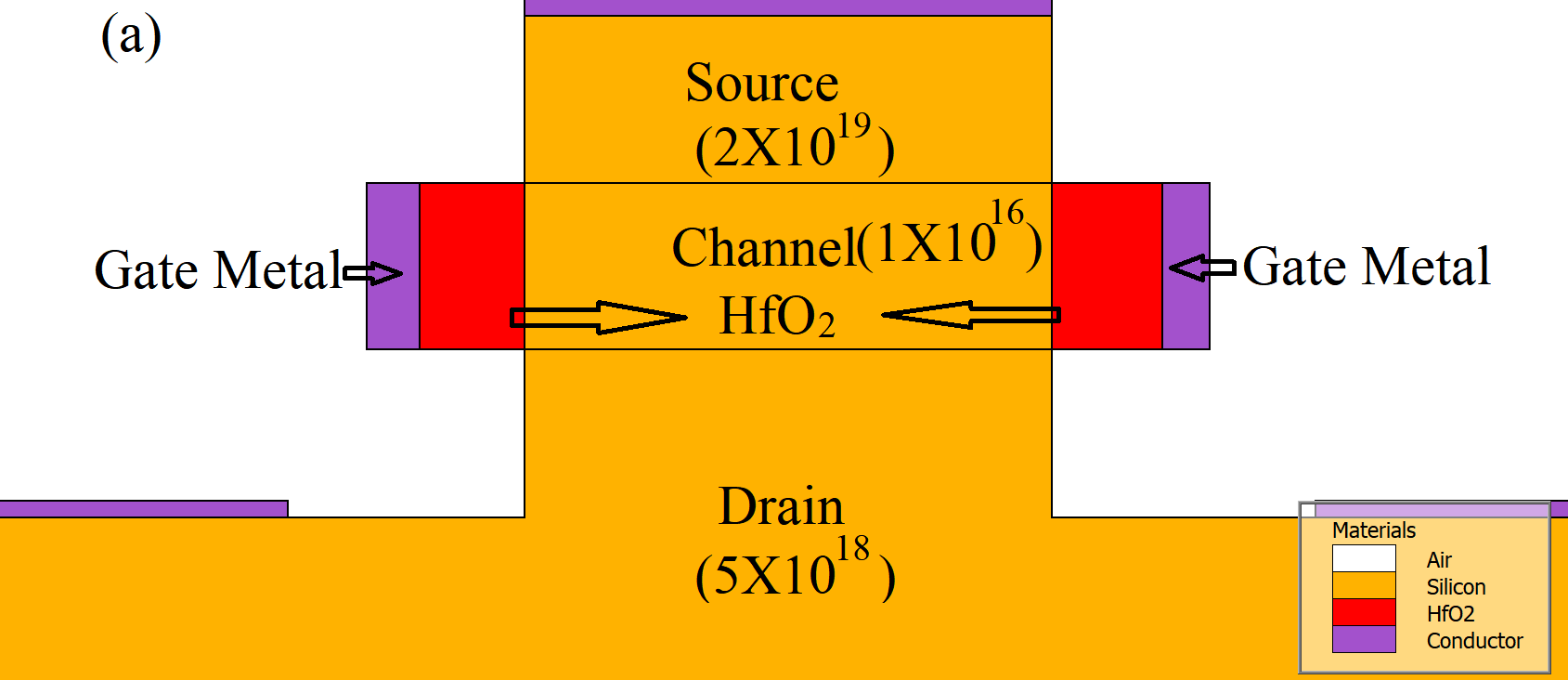
# Device STructure

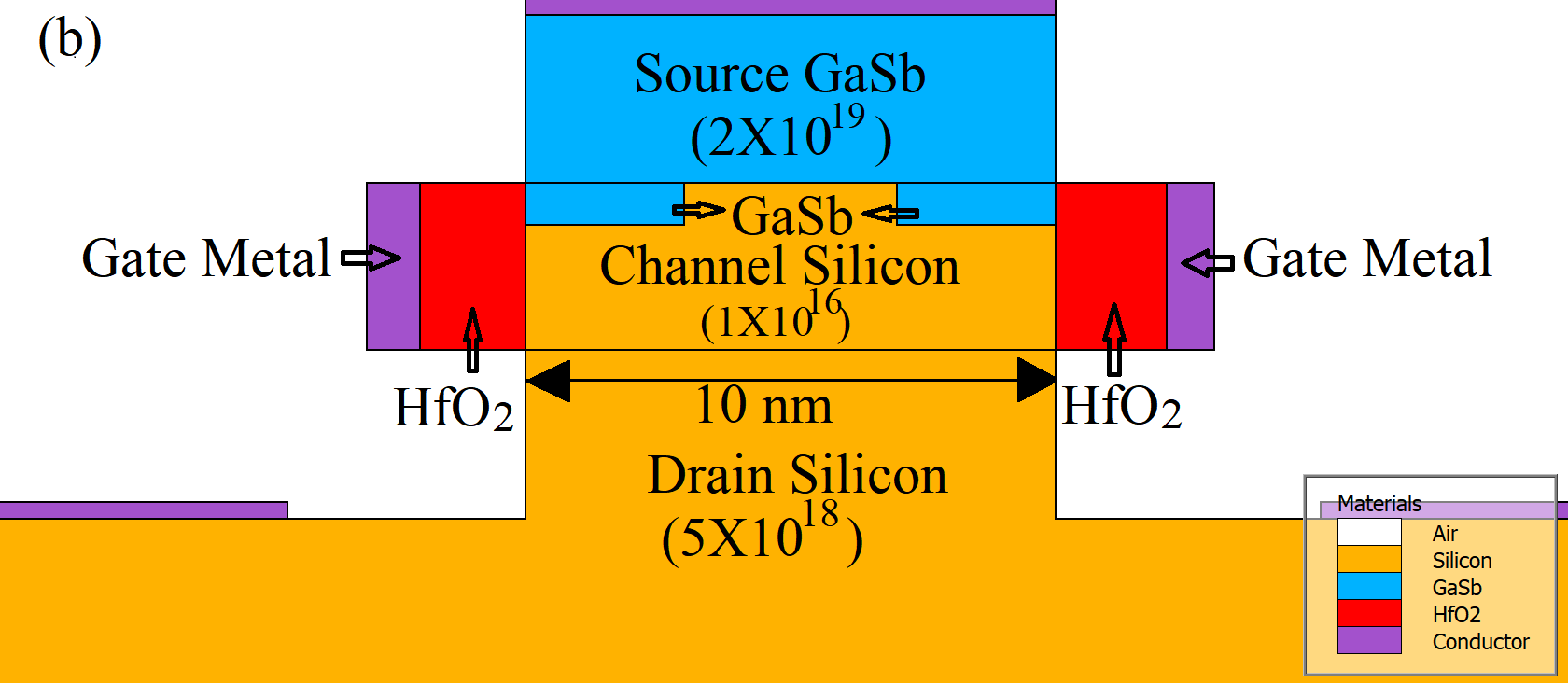
The cross-sectional representation of the GaSb-VTFET and Silicon-VTFET devices is shown in Fig. 1(a) and 1(b). We denote the vertical TFET with no pocket and hetero-material

at source region as silicon-VTFET and the structure with a GaSb delta doped and GaSb in the source region as GaSb-VTFET for the simplicity of discussion. For proper selection of the models needed for the study, calibration has been executed with the reported data of VTFET [16], as shown in Fig 1(c), in which the reported data were extracted using a plot digitiser and compared with the simulated results obtained. The tool used is, as discussed earlier, the Silvaco 2D-ATLAS device simulator. The device design parameters for Silicon-VTFET and GaSb-VTFET are shown in Table I.

TABLE I Design parameters of Silicon-VTFET and GaSb-VTFET

|  |  |  |
| --- | --- | --- |
| **Design parameter** | **Silicon-VTFET** | **GaSb-VTFET** |
| Source Concentration  [p type] (cm-3) | 2×1019 | 2×1019 |
| Channel region Concentration  [p type] (cm-3) | 1×1016 | 1×1016 |
| Drain region Concentration  [n type] (cm-3) | 5×1018 | 5×1018 |
| Metal Gate Length in nm | 20 | 20 |
| Source Length in nm | 20 | 20 |
| Drain Length in nm | 40 | 40 |
| Oxide width ( HfO2) (nm) | 2 | 2 |
| Source Material | Silicon | GaSb |
| Doping Layer Concentration/  Material [n type] (cm-3) | - | 7×1018 GaSb |
| Work function gate metal (eV) | 4.38 | 4.38 |







1. Cross-sectional representation of a) silicon vertical TFET (silicon-VTFET) b) GaSb/Si Heterojunction Vertical TFET with delta doped layer (GaSb-VTFET) (c) Calibrated output characteristic of the simulated Vertical TFET in comparison with the conventional vertical TFET [16]

The SRH (Shockley-Read-Hall) model is considered to be the best for modelling the recombination of charge carriers at the semiconductor-semiconductor and semiconductor-insulator interfaces. The tunnelling of the electrons is explained by non-local BTBT by integrating the probability. This model calculates the generation rate of holes (or electrons) by integrating non-local paths, which depend on the non-local routes formed at the endpoints of the tunnelling path. The numerical solution is then applied using the Newton trap method [17].

**Calibration:** Reported outcomes in [16] have been compared and calibrated in Fig.1 (c). A close similarity between the two outcomes validates the models implemented in the simulation.

# Results And Discussions

In this paper, the SILVACO TCAD tool is used to study and simulate the n-type Silicon-VTFET and GaSb-VTFET. The GaSb/Si heterojunction vertical TFET with delta-doped layer (GaSb-VTFET) and silicon n-channel 2D schematic vertical tunnel field-effect transistor (Silicon-VTFET) are shown in Figure 1. (a and b). We have assigned the device's names A and B to Silicon-VTFET and GaSb-VTFET, respectively. (Table II).

TABLE II  
Device Characteristics

|  |  |
| --- | --- |
| **Device** | **Values** |
| A | Silicon-VTFET |
| B | GaSb-VTFET |

1. *DC Analysis*

The parameters and models used for the proposed device are the same as in the calibration and Table I. At the source-channel intersection, a steep bending of the bands is attained because of high source doping concentration and using low band gap material leads to the enhanced band-to-band generation rate leading to an increased ON-current.



Figure 3. Drain current output characteristics of (a) Silicon-VTFET (b) GaSb-VTFET structure.

## Impact of energy bands:

Fig. 2(a) and 2(b) depict the band energies of Silicon-VTFET and GaSb-VTFET in the ON-state (at Vds = 0.5 V, Vgs = 1.0 V) of operations, respectively. When zero voltage is applied at the gate (thermal equilibrium), the tunnelling width is large enough to forbid the carriers to tunnel through, thus keeping the device in OFF-state. However, as we hike the gate voltage, band energies in the intrinsic region of the FET are reduced, reducing the tunnel width and creating a path for the carriers to travel from the source valance band to the channel conduction band and thus, turning the structure in ON-state.





Figure 2. Band energy variations along the channel for ON state (Vds=0.5 V and Vgs=1.0 V) of (a) Silicon-VTFET (b) GaSb-VTFET structure.

We suggest replacing the greater bandgap silicon at the drain side with the same lower bandgap material GaSb in order to maintain the TFET's traditional operation. By comparison to Silicon-VTFET, this decreases the tunnelling barrier width at the source-channel intersection and increases the generation rate in the proposed device configuration. This results in improved ON state current in the proposed device (GaSb-VTFET) compared to the Silicon-VTFET device.

## Drain Current Analysis

The comparisons of the Id  versus Vgs characteristics of the proposed V-TFETs (Silicon-VTFET and GaSb-VTFET) with and without pockets are shown in Fig 3. The *I*ON/*I*OFF ratios of GaSb-VTFET and Silicon-VTFET are 1.12X1013 and 3.33X1010, respectively.

For the Transfer characteristics, *Vds* is 0.5 V and *Vgs* is varied from 0 to 1 V. The parameters such as ION, IOFF, ION/IOFF, Subthreshold slope and threshold voltage (VT)of the suggested devices with and without hetero-pockets are depicted in Fig. 4 (a-c). The Subthreshold slope with 21.01 mV per decade and 27.38 mV per decade are attained for GaSb-VTFET and Silicon-VTFET respectively. GaSb-VTFET indicates a superior performance than the Silicon-VTFET with improved values like

1. ION/IOFF ratio
2. Threshold voltage (VT)
3. Subthreshold slope

It is because of the improvement in ON-state current in GaSb-VTFET than Silicon-VTFET. Nevertheless, the SS is significantly reduced in the GaSb-VTFET than in the Silicon-VTFET structure. Additionally, no significant difference in the IOFF is observed for the two V-TFETs. Despite having about the same OFF-state current levels, the GaSb-VTFET structure has a superior ION/IOFF ratio than the Silicon-VTFET structure. The GaSb-VTFET outperforms the Silicon-VTFET in subthreshold performance and enhancing its suitability for low-power applications. GaSb-VTFET has a lower threshold voltage (approx. 0.34 V).

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Figure 4 Variation in electrical attributes of proposed structures (Silicon-VTFET and GaSb-VTFET structure) (a) Subthreshold slope (SS) (b) Ion/Ioff ratio (c) Threshold Voltage.

of nanogap is 8 nm at Vds=0 V & Vgs=0.3 V.

1. *AF/RF Analysis*

Now we will comprehend the analogue figure of merits such as transconductance (*gm)*, gate-to-source capacitance (*Cgs)*, and transconductance generation factor (TGF) of both Silicon-VTFET and GaSb-VTFET.

Figure 5 provides a comparative analysis of the transconductance (gm) characteristics of two proposed V-TFETs (Silicon-VTFET and GaSb-VTFET) in (a). In Fig. 5(b), the gate capacitances (Cgg) of the two proposed V-TFET architectures are contrasted. The gm of GaSb-VTFET is considerably greater than that of Silicon-VTFET, as shown in Fig. 6(a). Transconductance *gm* of a device signifies its potential to convert the applied voltage at the gate terminal into the drain characteristic. GaSb-VTFETs have a bigger impact on gm than Silicon-VTFETs do, which allows for improved gate voltage to drain current transformation. This implies that GaSb-VTFET has an improved conversion ability of gate voltage to drain current than the Silicon-VTFET-based device.





Figure 5. Comparison of (a) Transconductance and (b) gate Capacitance of two proposed Vertical TFET structures (Silicon-VTFET and GaSb-VTFET).

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The suggested device's suitability for RF applications is further explored. The parasitic capacitances linked with the device play a critical role in defining its ac behaviour while operating at high frequencies. Circuit oscillation and signal distortion are caused by parasitic capacitances that form a pathway between the output and the input. Because gate-drain capacitance (Cgd) rather than gate-source capacitance (Cgs) dominates a device's overall gate capacitance, decreasing Cgd is critical for RF performance enhancement [5], [6]. Cgd component of the total gate capacitance initiates because of the charge carriers instilling from the drain into the gate region. Also, as the gate voltage increases, an inversion layer gets formed from the drain to the source side, decreasing the potential barrier at the drain side and thus enhancing Cgd. The total gate capacitance of the proposed structures (Silicon-VTFET and GaSb-VTFET) is shown in Figure 5. Studying the total gate capacitance is crucial as it determines the digital systems' transient overshoot and dynamic power dissipation.

The capacity of a structure to convert current into transconductance is measured by device efficiency, often known as the Transconductance generation factor (TGF), which is provided in eq (1). Any TFET device must be chosen between power and high-speed operation. TGF can be obtained from [10].

TGF=/ (1)

The evaluation of TGF as a measure of device efficiency is shown in Figure 6. It's worth noting that the GaSb-VTFET structure is more efficient than the Silicon-VTFET structure. The TCAD results of the said V-TFETs (Silicon-VTFET and GaSb-VTFET) with and without delta-doped are compared in this paper. It is observed that the proposed GaSb-VTFET with a doped layer has improved DC and RF performance parameters than the other proposed VTFET (Silicon-VTFET) device.



Figure 6. Variation of device efficiency or Transconductance generation factor (TGF) of two proposed Vertucal TFET structures (Silicon-VTFET and GaSb-VTFET).

## Conclusion

This paper discusses the DC and analogue/RF analysis of Silicon and GaSb material delta-doped source-based VTFETs. The extensive simulations lead to a conclusion that GaSb-VTFET with GaSb pocketed source has a lesser SS (21.01 mV per decade), reduced threshold voltage (0.34 V), and an enhanced ION/IOFF ratio (1.12 × 1013) than the corresponding values (of 27.38 mV per decade, 0.87 V, and 3.33 × 1010) of the conventional Silicon-VTFET structure. Since the OFF-state current is low, a reasonably well ION/IOFF ratio can be seen in both devices. The suggested GaSb-VTFET is more stable towards temperature variations than the conventional Silicon-VTFET structure. The analogue characteristics report that the GaSb-VTFET device has better transconductance (Gm) and Transconductance generation factor (TGF) than the Silicon-VTFET structure. Using a low band gap source pocket can also aid in lowering the miller capacitance of the device, which can make the device furthermore suitable at the circuit level. Thus, the proposed GaSb-VTFET device can be deemed best for low-power digital applications.

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