Class Test 1

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Q1. $NM_L = ?$
Why Fanout depends on NM_L.
Draw TTL tristate circuit & working.

Q2. Prove Absorption law ~~using~~.
$F(XYZ) = X.\bar{Y} + X.Y.Z + X.(Y + X\bar{Y})$

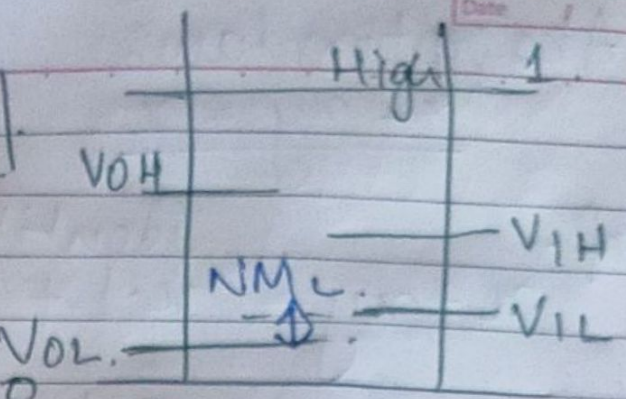
Q3. $F(XYZ) = X.\bar{Z} + \bar{Y}.Z$
(i) SOP. minterms
(ii) POS maxterms.
(i) only NAND gate
(ii) NOR gate.

Q4. Transfer characteristic of cmos of 5V (V_{SS})
$V_{TH} = 1V$, $V_{IH} = ?$
→ at $V_i = V_{IH}$,
what are States of 2 transistor
→ Draw cmos transistor level diagram for Boolean exp in Q3.

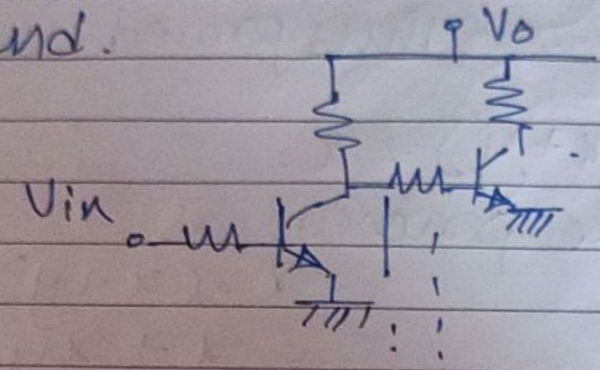
Q10 Ans

$$NM_L = V_{IL} - V_{OL}$$

noise margin.



Fanout:
no. of gates that can be connected to load end.



$N = I_C / I_B$.

$I_C = \frac{V_{CC} - V_{out}}{R_C}$.

$I_B = \frac{V_{out} - V_{BE\,sat}}{R_B}$.

due to involvement of noise margin.

increased.

$V_{out} = V_{IL} + N.M_L$

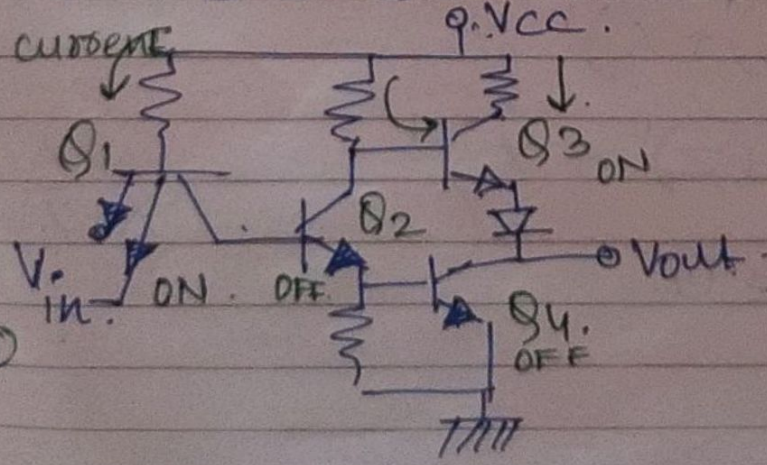
$I_C = \frac{V_{CC} - V_{out}}{R_C}$ ↓ decreased.

$I_B = \frac{V_{out} - V_{BE\,sat}}{R_B}$ ↑ increased.

$N = I_C / I_B$ ↓

(fanout) N decreased.
with increased NM_L.

TTL tristate circuit.



if Vin Vout
0
1.

Q2. Absorption law:

$x + xy = x$.

Proof.

$x + xy = x \cdot 1 + x \cdot y$ (identity) $= x \cdot (1 + y)$ (distributive law).

$= x \cdot 1$ (as $1 + y = 1$)

$= x$

Thus proved.

Similarly, $x \cdot (x + y) = x$.

can also be proved as

$x \cdot (x + y)$

$= x + xy$ (as $x \cdot x = x$)

$= x \cdot (1 + y)$

$= x$.

$F(x, y, z) = \overline{((x \cdot \bar{y} + xyz) + x(y + x\bar{y}))}$

$= ((x \cdot \bar{y} + xyz)' + x \cdot (y + x))'$

$= ((x \cdot \bar{y} + xyz)' + x)'$ (as $y + x\bar{y} = x + y$)

$= ((x \cdot (\bar{y} + yz))' + x)'$ (as $x(x + y) = x$ absorption)

$= ((x \cdot (\bar{y} + z))' + x)'$

$= (x' + (y' + z)' + x)'$ (as $x + \bar{x} = 1$)

$= (1)' = 0$.

Q3. $F(X,Y,Z) = X.\bar{Z} + \bar{Y}.Z$.

(i) SOP.

$= XY\bar{Z} + X\bar{Y}Z + X\bar{Y}Z + \bar{X}\bar{Y}Z$.

$= \Sigma m(6,5,1)$.

	X	Y	Z	m/M	
$\bar{X}\bar{Y}\bar{Z}$	0	0	0	0	X+Y+Z
	0	0	1	1	
	0	1	0	2	
	0	1	1	3	
	1	0	0	4	
	1	0	1	5	
	1	1	0	6	
	1	1	1	7	

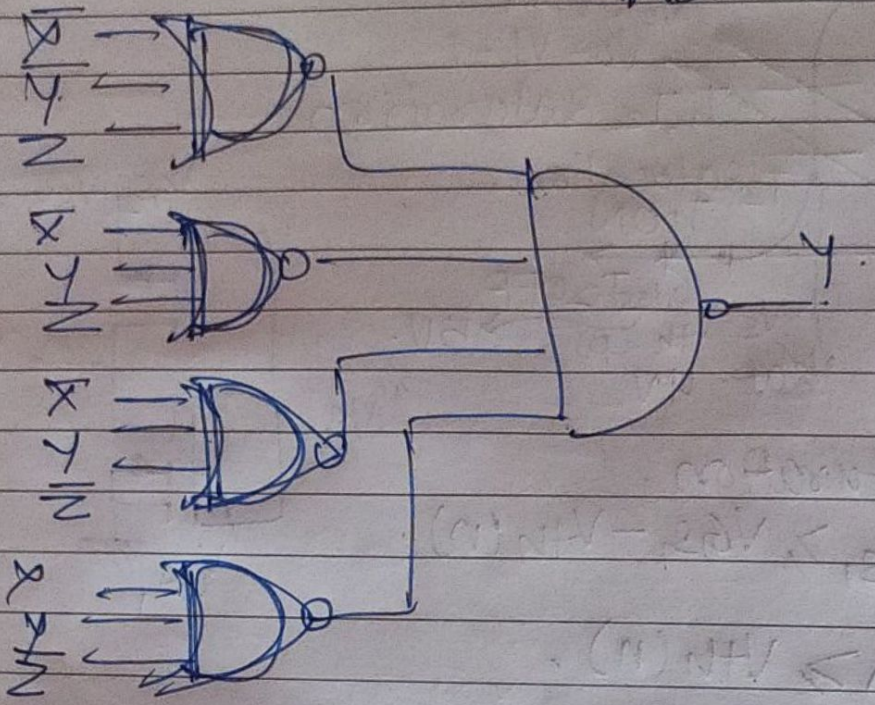
(ii) POS.

$= \pi M(0,2,3,4,7)$.

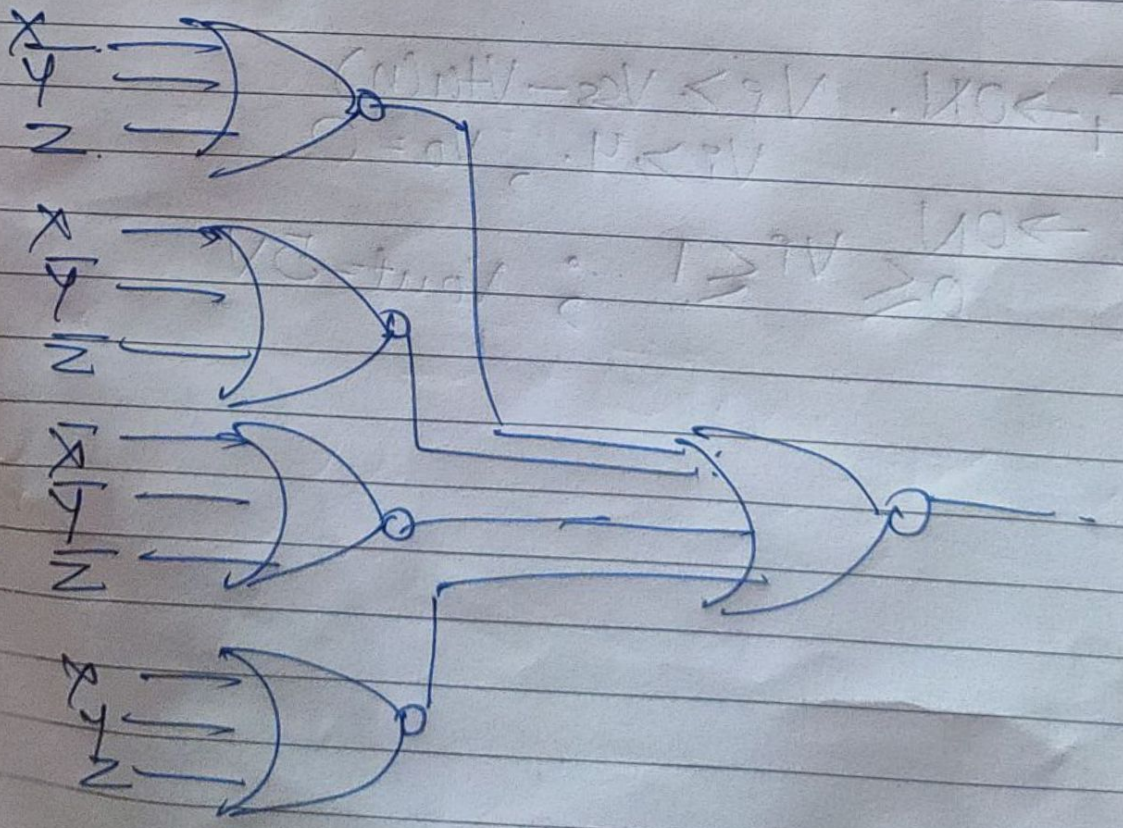
$= (X+Y+Z).(X+\bar{Y}+Z).(X+\bar{Y}+\bar{Z}) . (\bar{X}+Y+Z).(\bar{X}+\bar{Y}+\bar{Z})$.

NAND Degate.

SOP NAND.



POS. NOR gate.



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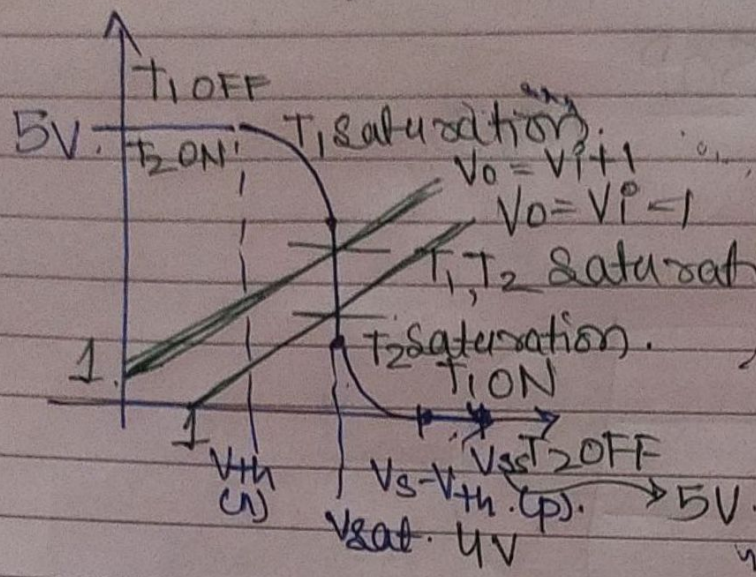
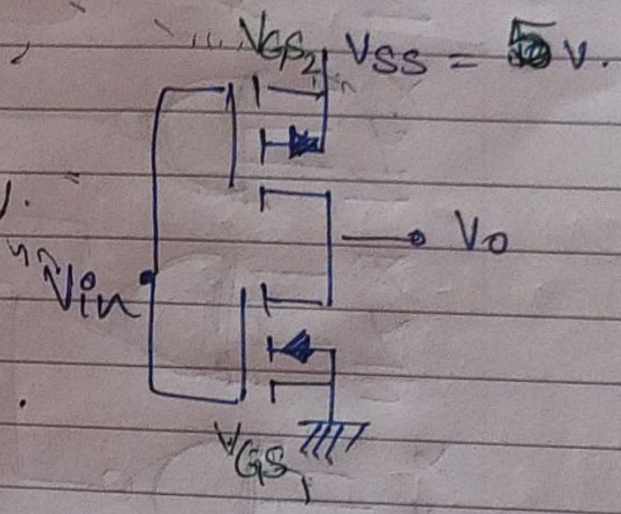
Q4. CMOS transfer characteristics.





T_1 → Saturation.

$V_{GS_1} \geq V_{GS_1} - V_{th(n)}$.

$V_i \geq V_{th(n)}$.

$\therefore V_o \geq V_{in} - 1$

Similarly.

$\therefore$ T_2 will saturate $V_{out} \leq V_{int} 1$

$T_1 \rightarrow ON$. $V_i \geq V_{ss} - V_{th(n)}$

$V_i \geq 4$. $\therefore V_o = 0$

$T_2 \rightarrow ON$

$0 \leq V_i \leq 1$. $\therefore V_{out} = 5V$