POWER ELECTRONICS LAB

Lab Report for **4th** Experiment : Study of single phase AC to DC Converter(Half-Controlled and Full-Controlled)

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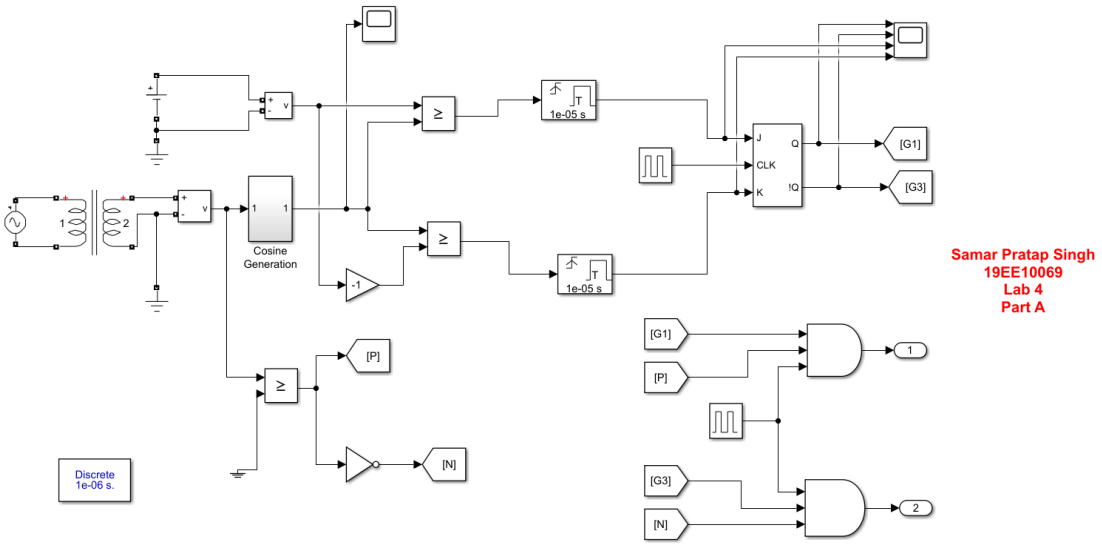
PART - A (Triggering Circuit)

Section 1:

Circuit Diagram :



Given :

$$P_n = 4\,VA, f_n = 50\,Hz, V_1 = 230\,V, R_1 = 6.9\,\Omega, L_1 = 7.1\,mH,$$
$$V_2 = 3.605\,V, R_2 = 1.7\,m\Omega, L_2 = 2.1\,\mu H,$$
$$R_m = 600\,\Omega\,, L_m = 1.145\,H$$

1.

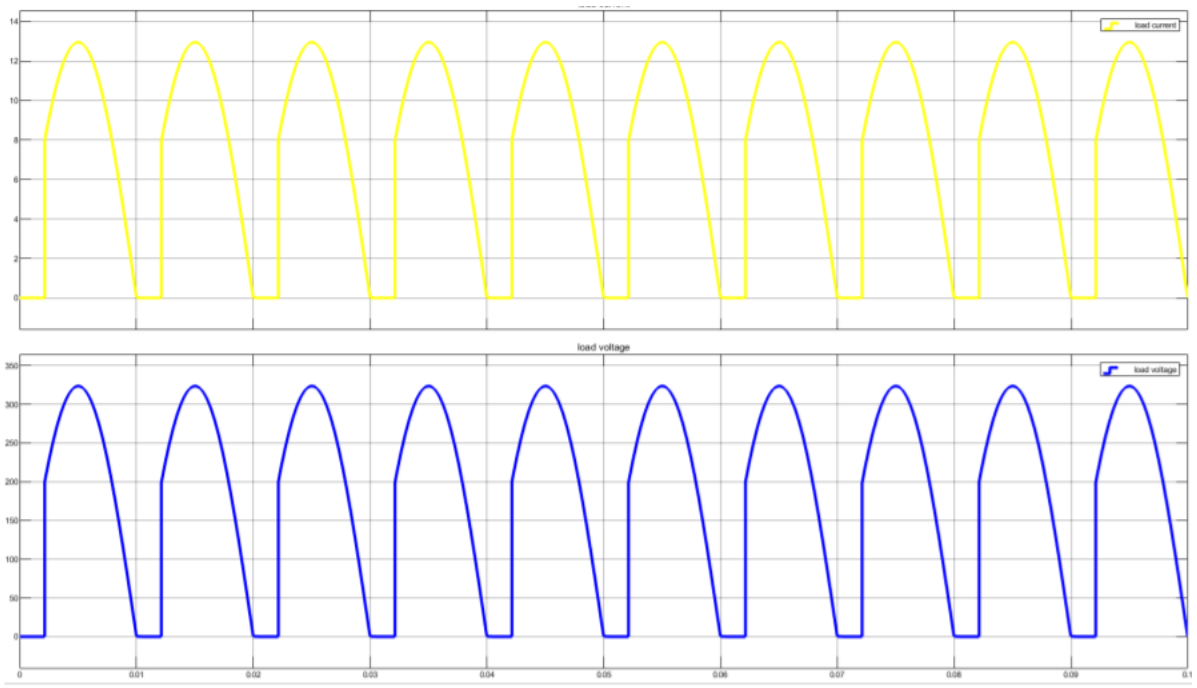
Now, we are using a resistive load in the circuit. So, average output voltage :

V_{out}(avg) = 185 Volts = V_m*(1 + cos(α)) / π

=> On solving, we get the value of α = 38.11°.

So, we get V_{ref} = 3.605*$\sqrt{2}$* cos(α) = 4.107

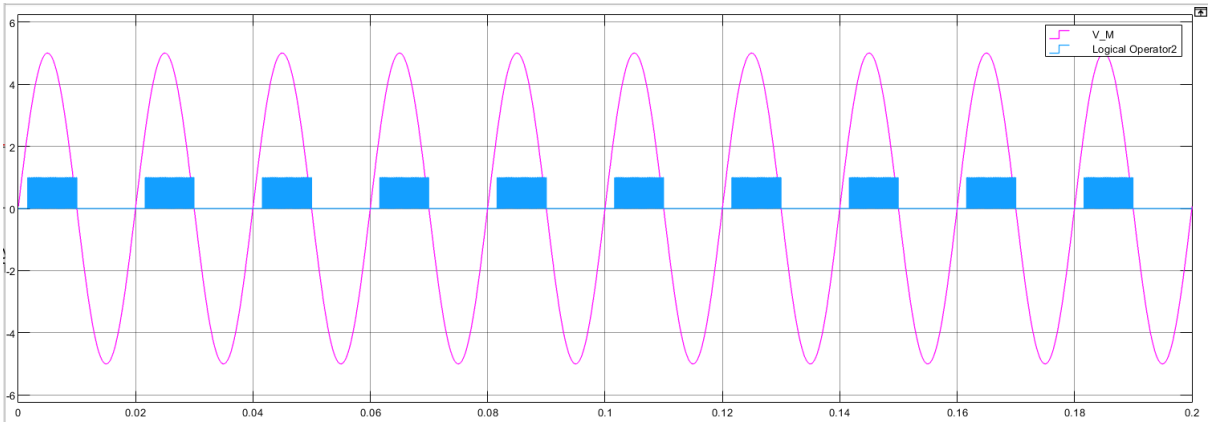
Simulation:



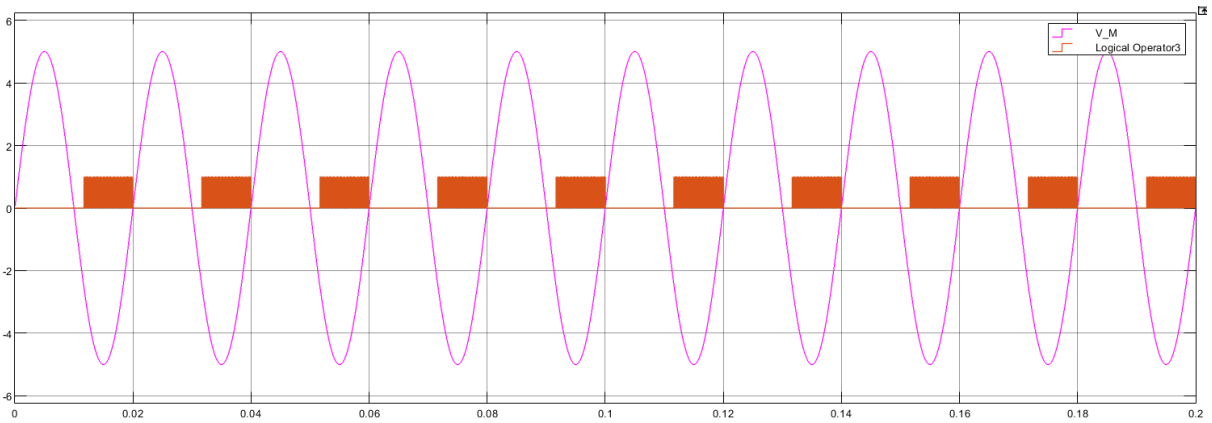
As we can see, that the value of V_{out}(avg) is coming to be 183.8 V.
The value obtained is less than expected due to the forward Volt drop in thyristors.

2.

Gate Pulse 1 w.r.t the cosine and reference signal:



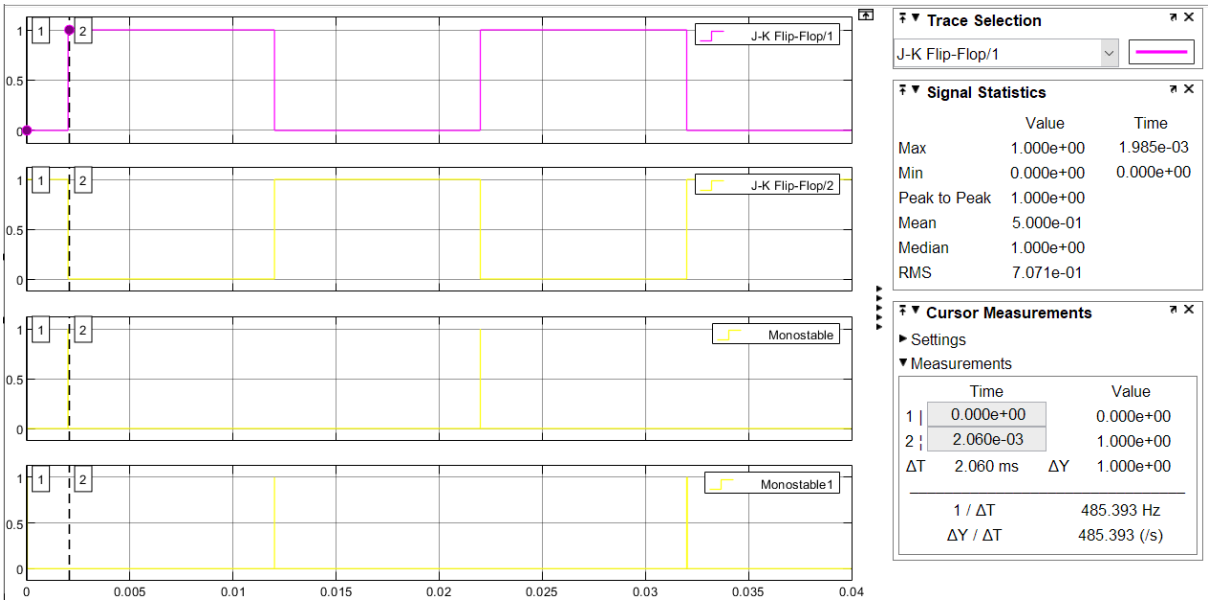
Gate Pulse 3 w.r.t the cosine and reference signal:



Observation from both the gate pulses:

- Thyristor 1 triggers when the input voltage is in the positive half cycle after firing angle α.
- Thyristor 3 triggers when input voltage is in negative half cycle after firing angle α.

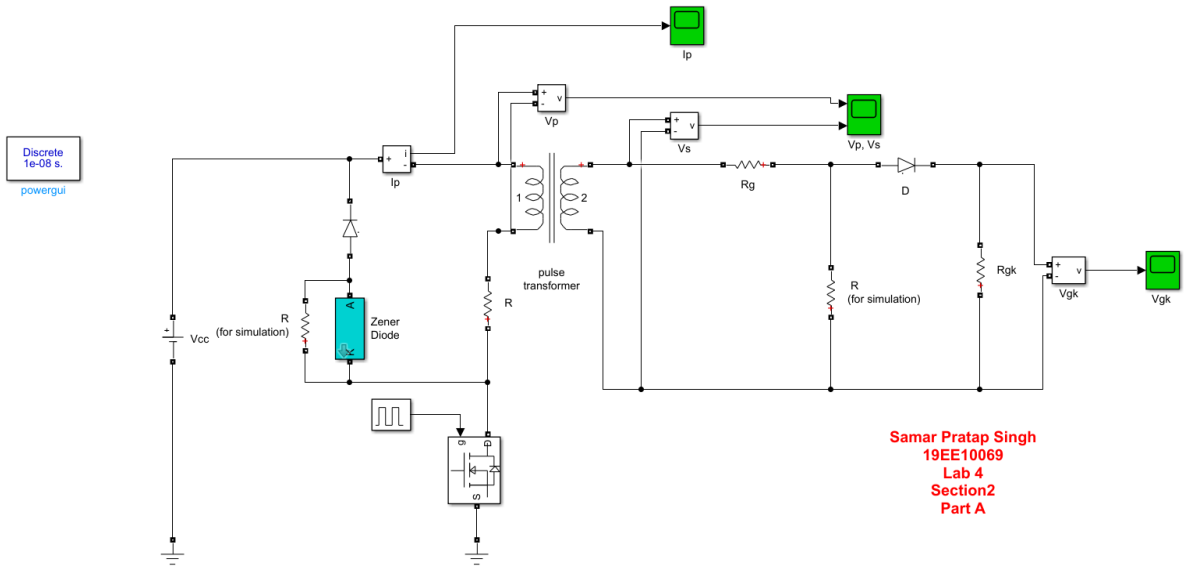
3.



Firing time = 2.060 ms
Firing angle = (360/20)*(2.060)° = 37.08°

Section 2:

Circuit Diagram :



Given :

Pulse transformer specifications: $L_m = 1.5mH$, $L_{lp} = L_{ls} = 20\mu H$, $R_{pri} = R_{sec} = 0.8\ \Omega$, $R_{core} = 400\ \Omega$, $N_1:N_2 = 1:1$

Auxiliaries Specifications: $V_{cc} = 20\ V$, $R_p = 10\ \Omega$, $R_g = 20\ \Omega$, $R_{gk} = 10\ \Omega$

1. Choose zener voltage V_{zener} such that primary winding current is reset to zero within 30% of the pulse duration.

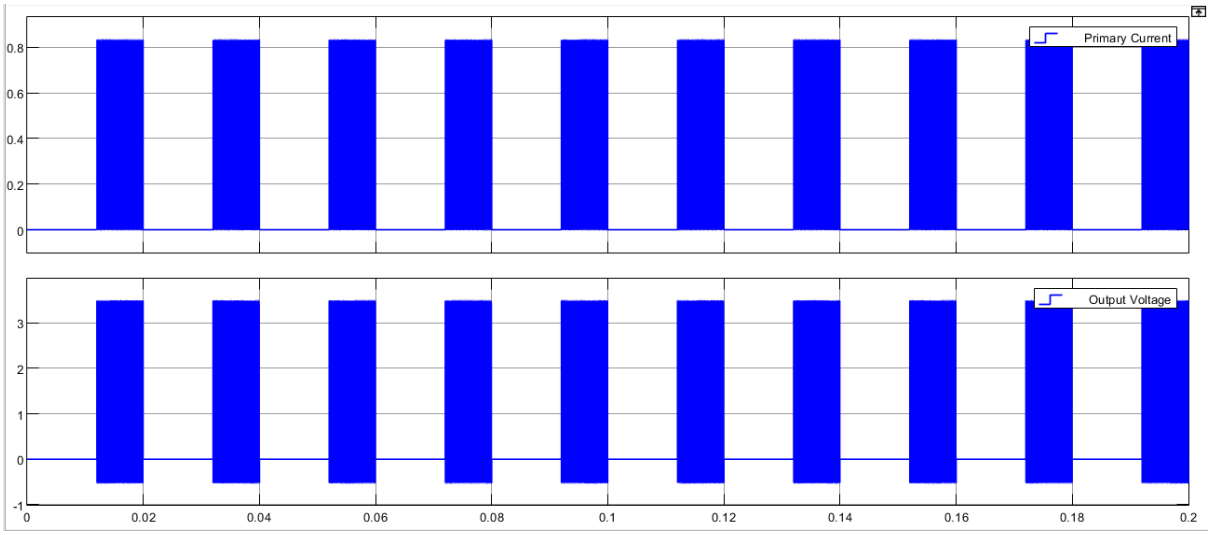
$V_{CC} \times T_{pulse} = V_Z \times T_{demag}$

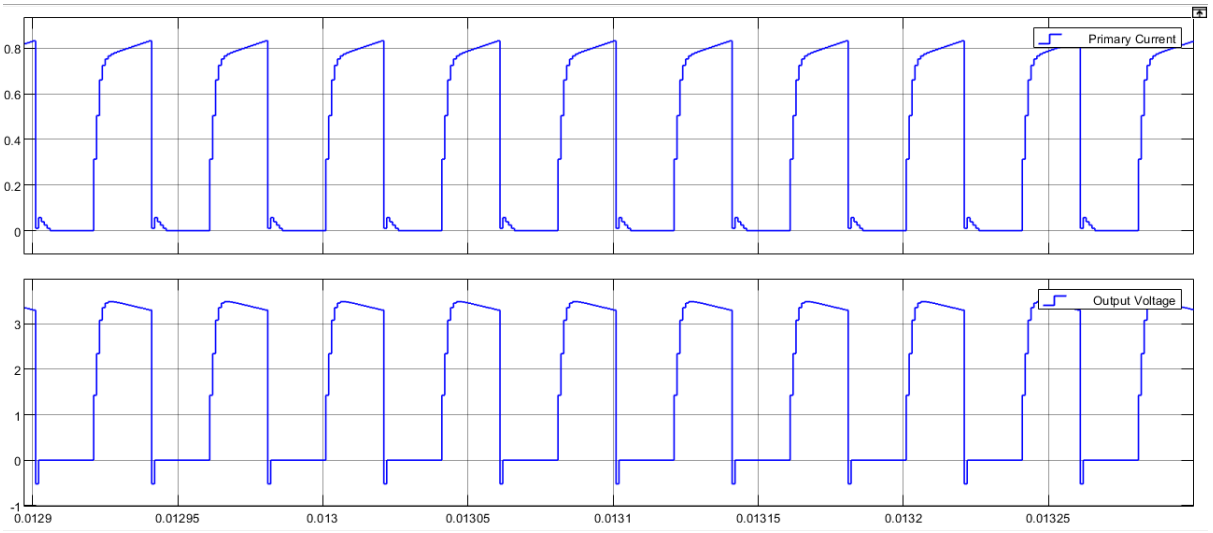
Duration of pulse(T_{pulse}) is 50% of the time period and
Duration of demagnetization of the transformer(T_{demag}) is 30% of the time period of the gate pulse generated by the control circuit.

So, V_{zener}= 33.34V

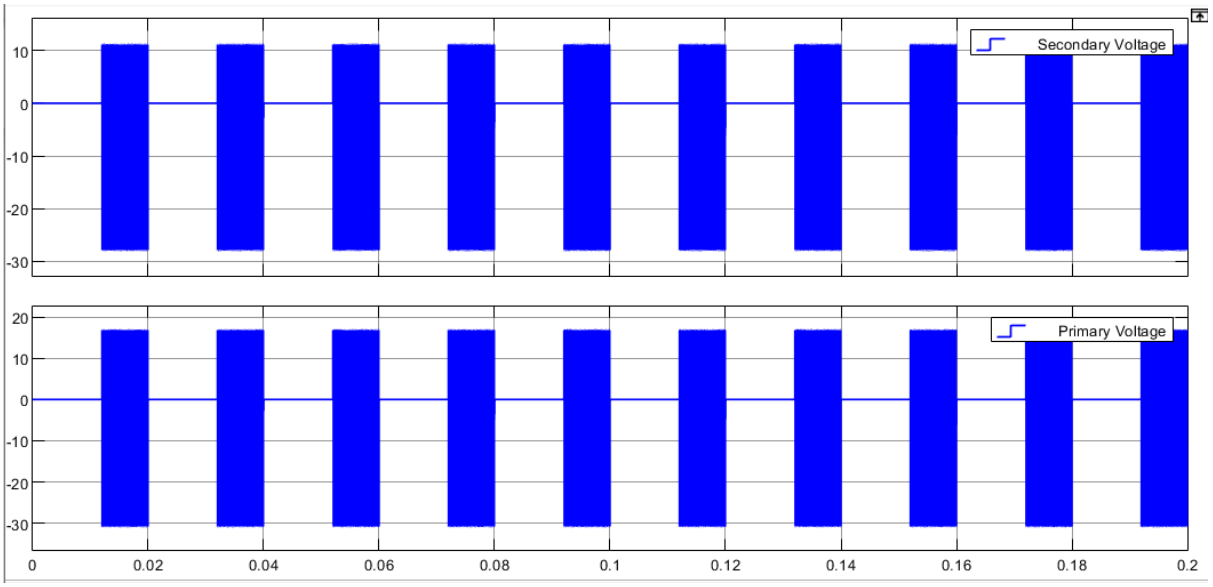
2. Save primary current and output voltage Vgk waveform. Also, save the primary voltage and secondary voltage of pulse transformer together in another plot.

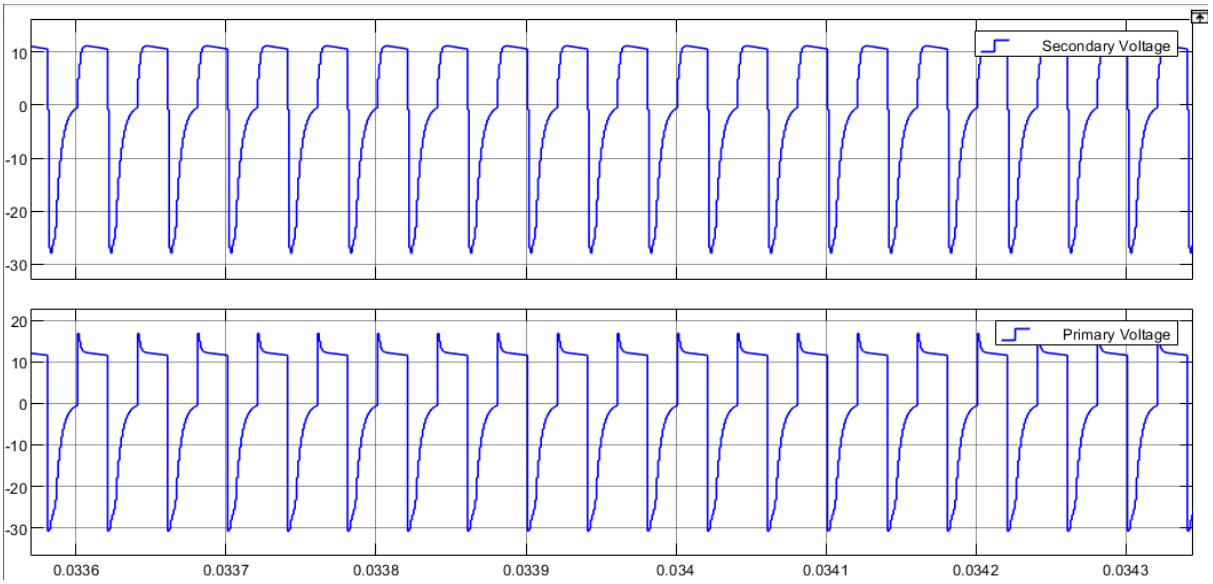
Vgk and Primary Current



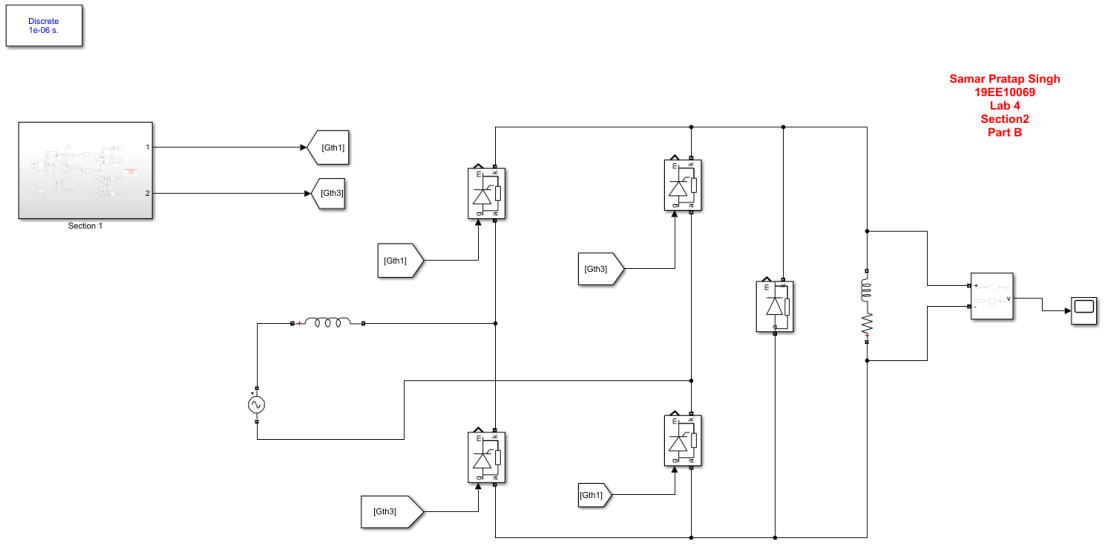


Primary Voltage and Secondary Voltage





PART - B (Full Controlled Converter)



1.

Without source inductance and freewheeling diode for L= 60 mH.

The given value of V_{in} = 230V and α=30,

$$Vout = 2\sqrt{2}\,\pi * 230 * (\cos 30) = 179.33V$$

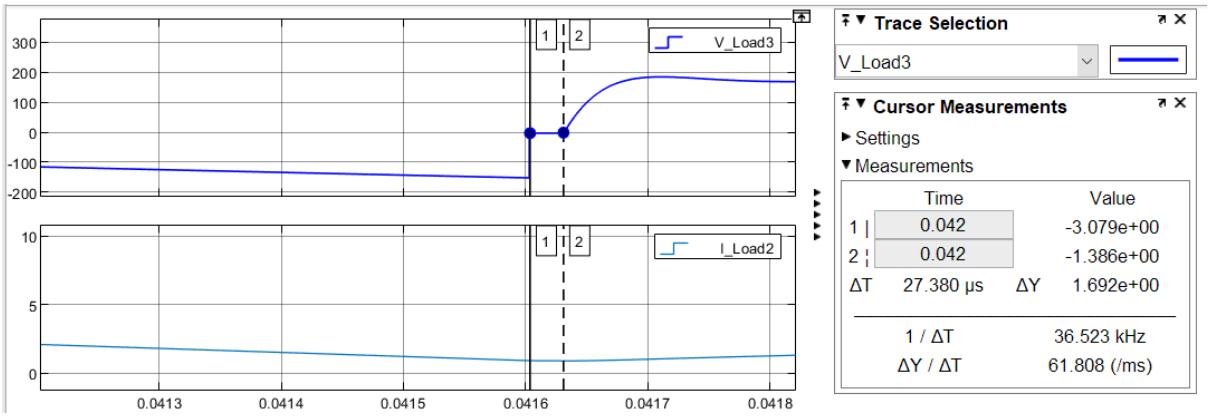
Hence, R_{Load} = $\frac{179.33}{8}$ = 22. 42 Ω

Also, $Vref$ = 3.605 * $\sqrt{2} * cos\ 30$ = 4.414V

Now, **simulating** the circuit,
we get V_{DC} = 183.8V, I_{DC} = 8.32A

2.

With 2.5 mH source inductance,
Simulating the circuit, we get,
V_{DC} = 183.8V,
I_{DC} = 8.32A



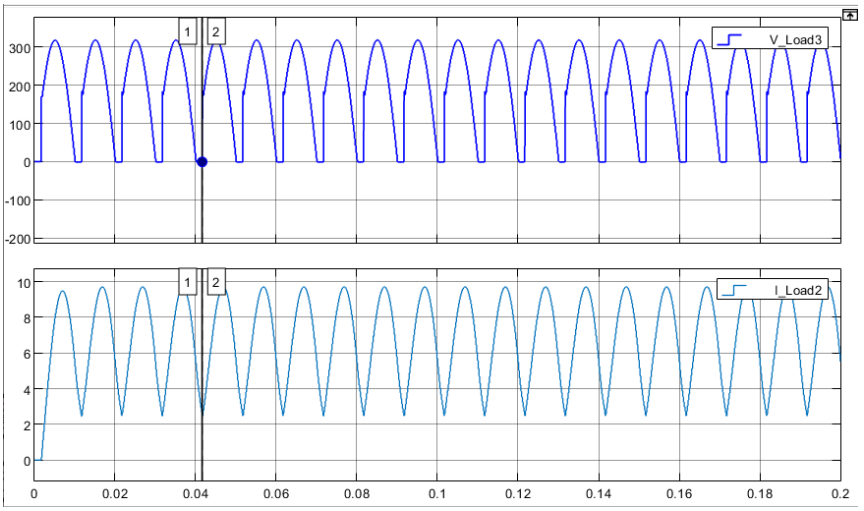
Overlap angle (μ) = (360/20ms)*(27.380us) = 0.493°

3.

Voltage drop due to source inductance: (179.1-177.9) V = 1.2 V

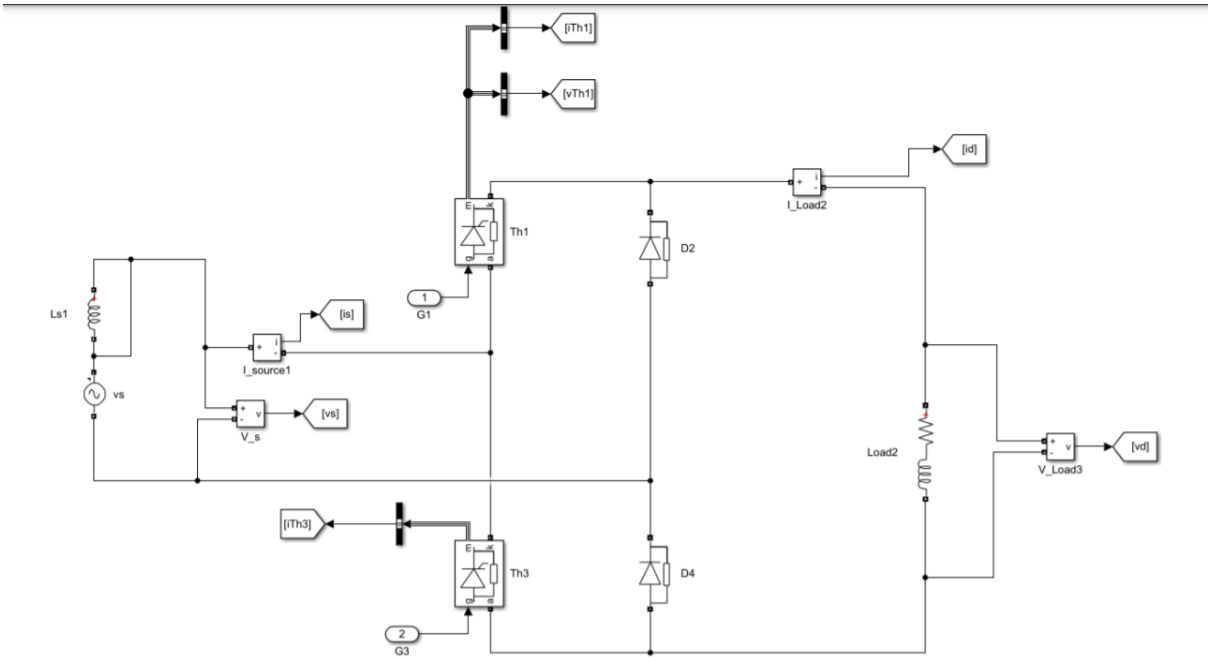
4.

With Freewheeling diode in the same circuit:



Parameter	Load voltage (V) Ideal case	Load voltage (V) with source inductance	Load Voltage (V) with source inductance and freewheeling diode
Firing angle (Degree)	30	30	30
Average load voltage (V)	183.8	183.8	183.8
Average load current (A)	8.32	8.32	8.321
Input RMS current	9.986	9.949	9.945
Fundamental input current	12.28	11.99	12.06
Distortion factor	0.998	0.999	0.999
THD (%)	19.62	18.15	18.18
DPF(Displacement Power Factor)	0.867	0.867	0.867
PF	0.867	0.867	0.867
P_1 (W)	2205.25	2205.24	2205.26
Q_1 (VAR)	997.7	998.89	1028
S_1 (VA)	1972.2	1945.78	2005.14

PART - C (Asymmetric half-controlled converter)



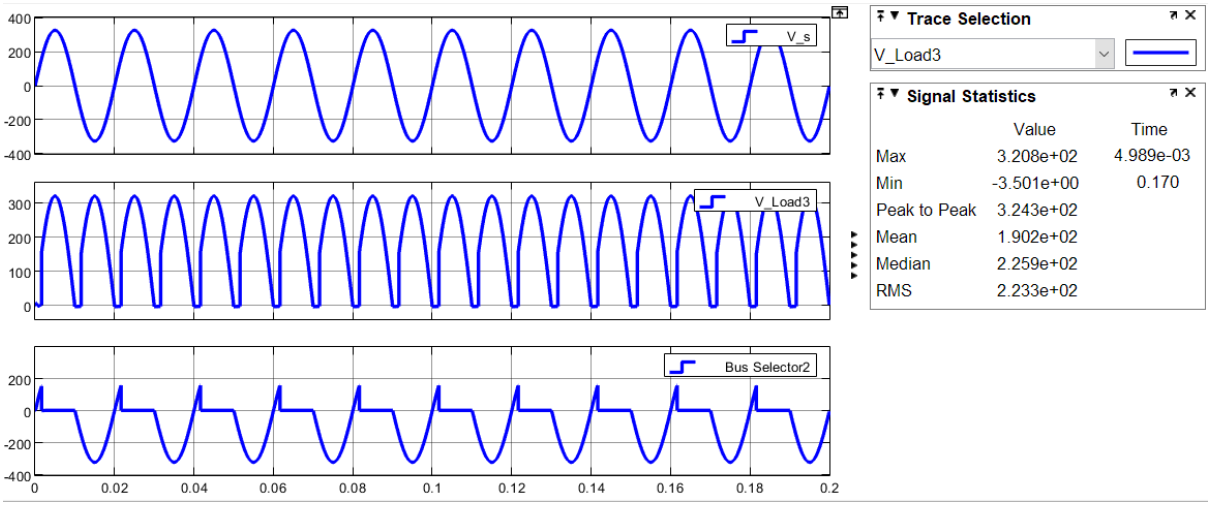
1.

$Vout$ = (Vm / π) (1+cos α) = 193.2V

a)

For firing angle α = 30°,

Simulated average V_{out} =190.2 V



b)

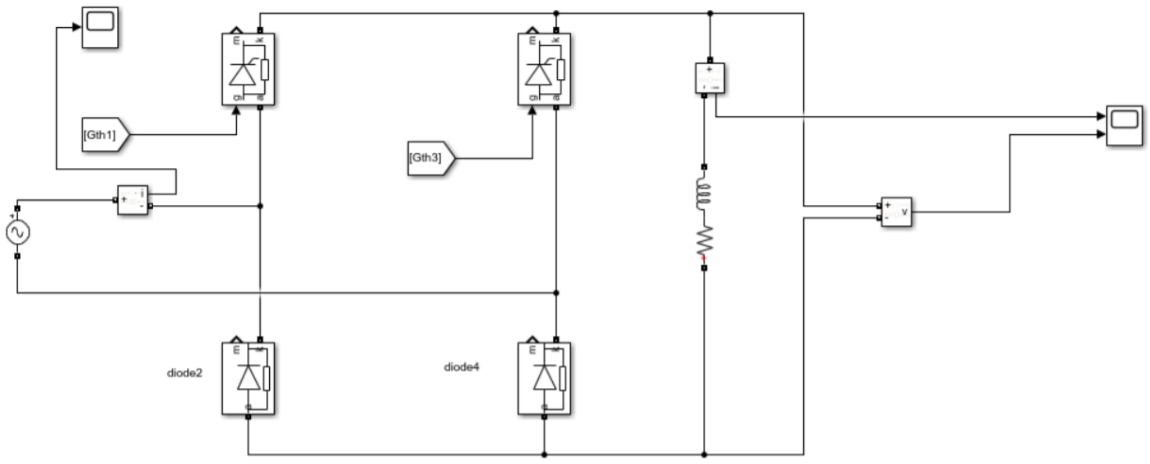
Thyristor 1 (RMS value) = 4.658 A
Thyristor 3 : RMS value = 4.722 A
Diode 2 (RMS value) = 4.855 A
Diode 4 (RMS value) = 4.839 A

c) Considering a source reactance drop of 5% of rated line voltage, find the average output voltage (Vout) for the firing angle α = 30°.

V_m = 0.95*230*$\sqrt{2}$ = 309 V
$Vout$ = (Vm / π) (1+cos α) = 183.54 V

2.

Symmetric Semi-Controlled Converter:



Given : R = 30 Ω, L = 60mH, α = 45°,

Without Free Wheeling Diode :

```
Sampling time      = 1e-06 s
Samples per cycle = 20000
DC component       = 0.02662
Fundamental        = 8.59 peak (6.074 rms)
THD                = 19.19%

      0 Hz   (DC):            0.03    270.0°
     10 Hz                    0.05    254.7°
     20 Hz                    0.05    239.4°
     30 Hz                    0.05    224.1°
     40 Hz                    0.05    208.9°
     50 Hz   (Fnd):           8.59    -28.5°
     60 Hz                    0.04    179.3°
     70 Hz                    0.04    165.2°
     80 Hz                    0.04    151.9°
     90 Hz                    0.04    139.3°
    100 Hz   (h2):            0.03    127.8°
    110 Hz                    0.03    116.2°
    120 Hz                    0.03    105.4°
    130 Hz                    0.03     95.0°
    140 Hz                    0.03     84.7°
    150 Hz   (h3):            0.98     68.3°
    160 Hz                    0.02     64.0°
    170 Hz                    0.02     53.6°
    180 Hz                    0.02     43.1°
    190 Hz                    0.02     32.7°
    200 Hz   (h4):            0.02     23.0°
    210 Hz                    0.02     12.1°
    220 Hz                    0.02      1.9°
    230 Hz                    0.02     -8.1°
    240 Hz                    0.02    -17.9°
```

With Free Wheeling Diode :

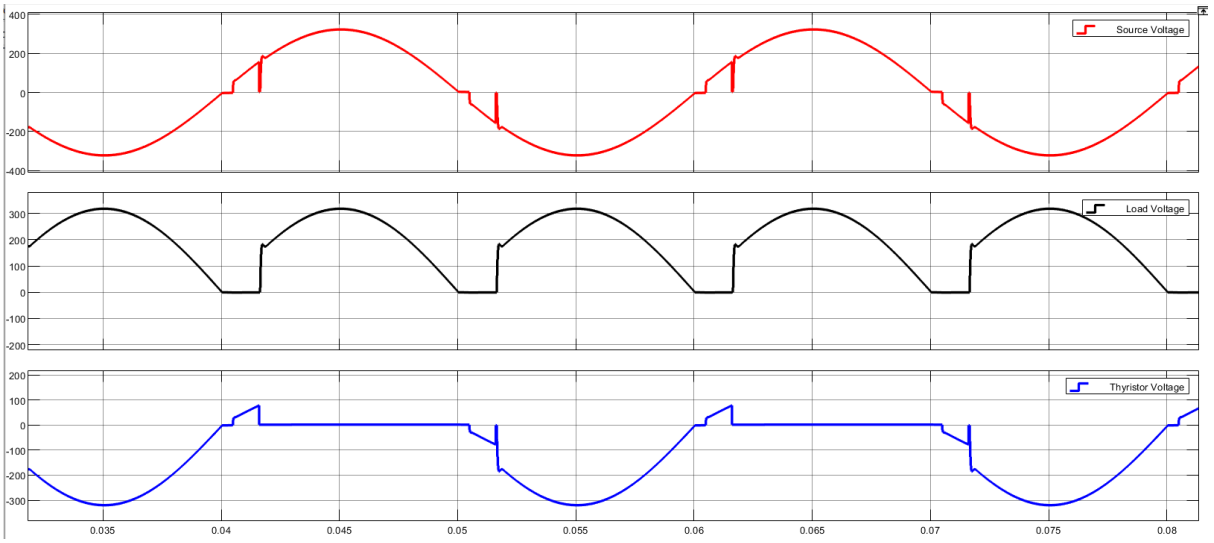
```
Sampling time      = 1e-06 s
Samples per cycle = 20000
DC component       = 0.02701
Fundamental        = 8.584 peak (6.07 rms)
THD                = 19.13%

      0 Hz   (DC):            0.31%    270.0°
     10 Hz                    0.61%    254.7°
     20 Hz                    0.60%    239.4°
     30 Hz                    0.59%    224.1°
     40 Hz                    0.57%    208.9°
     50 Hz   (Fnd):         100.00%    -28.3°
     60 Hz                    0.52%    179.3°
     70 Hz                    0.48%    165.3°
     80 Hz                    0.45%    151.9°
     90 Hz                    0.42%    139.3°
    100 Hz   (h2):            0.40%    127.8°
    110 Hz                    0.36%    116.2°
    120 Hz                    0.34%    105.4°
    130 Hz                    0.32%     95.0°
    140 Hz                    0.30%     84.6°
    150 Hz   (h3):           11.27%     68.3°
    160 Hz                    0.28%     63.9°
    170 Hz                    0.27%     53.5°
    180 Hz                    0.26%     43.0°
    190 Hz                    0.25%     32.6°
    200 Hz   (h4):            0.24%     22.9°
    210 Hz                    0.23%     11.9°
    220 Hz                    0.22%      1.8°
    230 Hz                    0.21%     -8.3°
    240 Hz                    0.20%    -18.1°
```

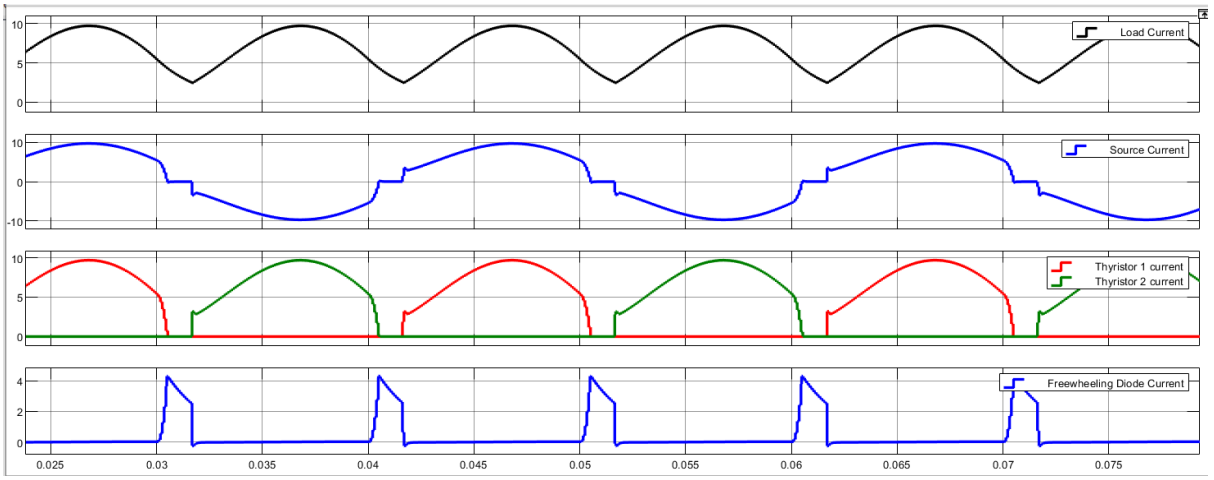
Discussions:

- **Capture (i) source voltage, (ii) load voltage, (iii) voltage across thyristor in one scope for one cycle and also capture (i) load current, (ii) source current (iii) thyristor current (iv) freewheeling diode current in another scope for full-controlled converter.**

  i, ii, iii



  i, ii, iii, iv



- **Make a comparative study between full-controlled and Asymmetric half-controlled converter in terms of load voltage, source current, power factor, THD.**

  Ideal cases considered :

  For a Full controlled converter :

R = 22.4 OHM ,
L = 60mH,
V_{in}(RMS) = 230 V ,50hz,
α=30°

Asymmetric half controlled converter :
R = 22.4 OHM ,
L = 60mH,
V_{in}(RMS) = 230 V ,50hz,
α=30°

Parameters	Full-Controlled	Asymmetric Half Controlled
Load Voltage (AVG)(in V)	179.2	190.8
RMS Source Current (in A)	8.452	8.61
THD (%)	11.55	17.66
Power factor	0.843	0.918
Displacement factor	0.845	0.934

Here we can clearly see that,
Asymmetric Half Controlled gives a greater output voltage and an improved power factor as compared to the Full-Controlled.

- **Why a train of pulses are used to turn on the thyristor instead of a single pulse?**

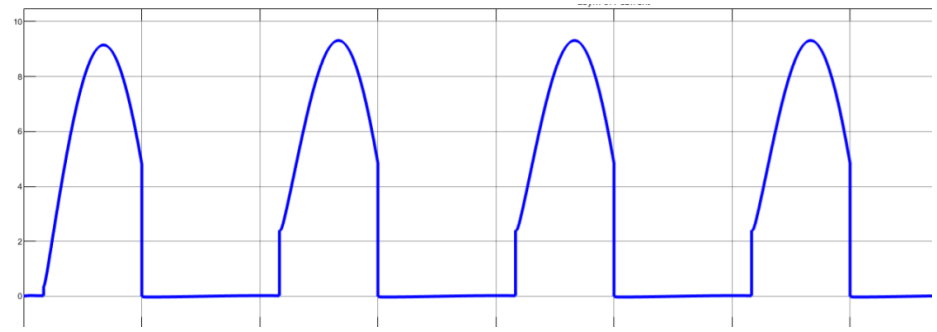
  The following are the reasons we use a train of pulses to turn on the thyristor instead of a single pulse:
  - ➔ If we hold the gate trigger voltage for a longer duration, it will cause huge dissipation of power within the thyristor and thus draw excess power from the circuit.
  - ➔ The thyristor may not latch on with the first firing pulse at the start of a conduction interval, as the current may not reach the minimum holding current. Hence, we need to keep triggering on until it latches on.

- **List key differences between asymmetric and symmetric semi-controlled rectifiers.**

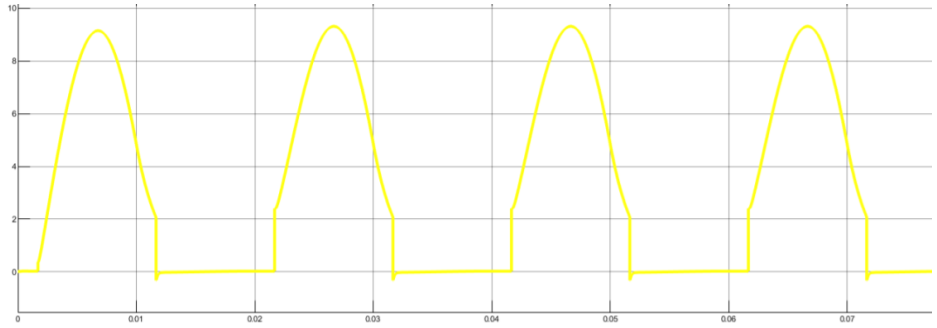
While the load current and the load voltage waveforms comes out exactly the same for both the rectifiers, a difference in the Diode and Load current is observed.

Thyristor Currents:

Asymmetric:

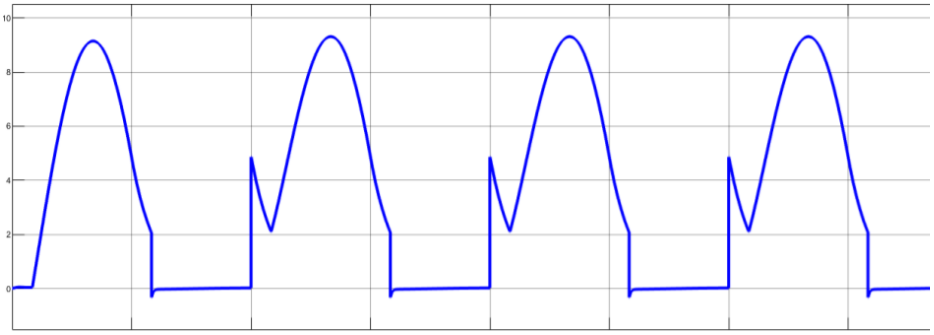


Symmetric:

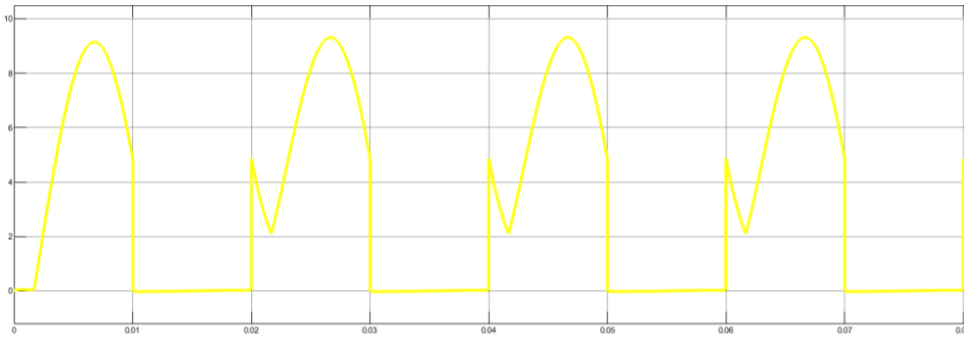


Diode Currents:

Asymmetric:



Symmetric:



Observations:

- ➔ The conduction time for thyristor is more in symmetrical topology, which leads to higher RMS and average thyristor currents.
- ➔ The conduction time for diode is less in symmetrical topology, which leads to lower RMS and average diode currents.

From conduction time periods, we can also say that the average and RMS thyristor current in symmetrical configuration is higher. So SCR current rating should be higher in symmetrical configuration. Also, the average and RMS diode current in asymmetrical configuration is higher. So, diode current rating should be higher in asymmetrical configuration.

The freewheeling path in symmetrical configuration is through a (thyristor-diode) combination, and in asymmetrical configuration is through a (diode-diode) combination. This is because during freewheeling, devices belonging to the same leg will conduct in both configurations.