

# DESIGN DOCUMENT FOR ISOLATED 50W FLYBACK CONVERTER

## POWER SUPPLY SPECIFICATIONS:

Input Voltage Range: 72V DC to 32V DC (48V DC nominal)

Output Voltage: +5V DC

Load: upto 10A

Regulation:  $\pm 2\%$  Over Load and Temperature

This converter is specifically designed to interface with the voltage ranges used in the telecommunications industry.

## FLYBACK TOPOLOGY:

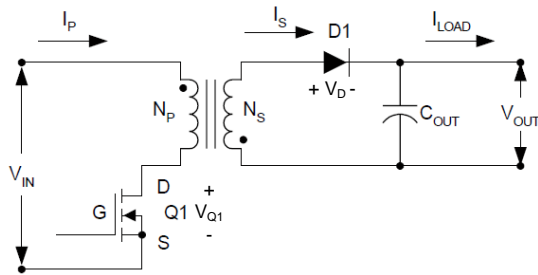
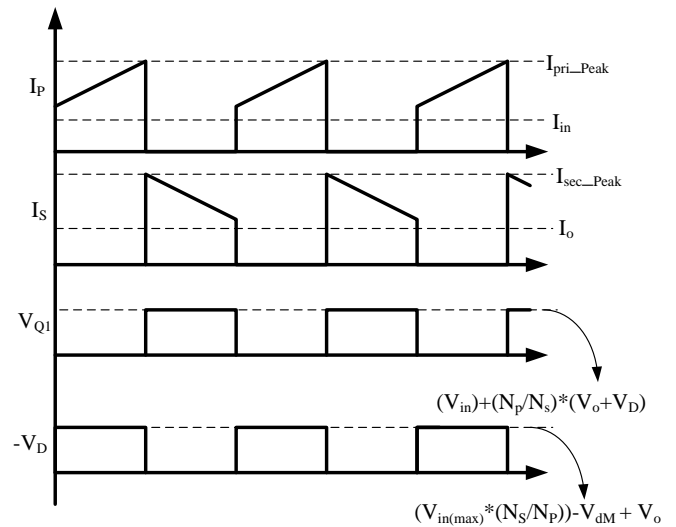


Figure 1: Flyback converter topology



Key waveforms

## MAXIMUM DUTY CYCLE AND TURNS RATIO:

In a CCM flyback converter the maximum duty cycle will determine the turns ratio of the transformer and impact the maximum voltage stress on the switching element.

The DC transfer function of CCM flyback converter is:

$$\frac{V_o + V_D}{V_{in(min)} - V_{Rds(on)}} = \frac{1}{N} \left( \frac{D_{max}}{1 - D_{max}} \right) \dots \dots (1)$$

Here,  $V_o = 5V$  (output voltage)

$V_D =$  Forward voltage drop across the freewheeling diode  $D1 \approx 0.8V$  (worst case)

$V_{in} = 32$  to  $72V$ , maximum duty cycle implies minimum input voltage so,  $V_{in(min)} = 32V$ .

$V_{Rds(on)} =$  ON state voltage drop across the MOSFET Q1 which equal to  $R_{ds(on)} * I_{rms(primary)} \approx 1V$  (worst case)

$N = N_P / N_S =$  Turns ratio,  $N_P =$  number of transformer primary turns

$N_S =$  number of transformer secondary turns

$D =$  Duty cycle

Let us select a maximum duty cycle of 45% (Limiting the duty cycle increase the number of controller ICs to choose from because many controller ICs available today have the maximum duty cycle limitations of 50%)

Substituting all these values in the Eq. (1) gives us a turns ratio of 4.37. The turns ratio is inversely proportional to the peak primary current,  $I_{PEAK}$ , but directly proportional to the voltage stress on the switching element. So, the peak currents will not become unreasonably high and the voltage stress on the MOSFET will be kept as low as possible, the turns ratio is rounded up only to the next integer value, 5, or simply five primary turns for every one secondary turn. Recalculating equation (1) results in actual  $D_{max}$  of 48%.

### **SWITCHING FREQUENCY:**

At higher switching frequencies, the magnetic components and filters will be smaller, but core losses, gate charge currents, and switching losses increase with higher switching frequencies.

At lower switching frequencies peak currents and, consequently,  $I^2R$  losses increases.

A compromise must be reached between component size, current levels, and acceptable losses. For this design, a fixed frequency ( $f_{sw}$ ) of 70kHz was chosen. At  $D_{max}$  equal to 48%,  $t_{on(max)}$  becomes 6.9 $\mu s$ .

### **TRANSFORMER DESIGN:**

When the switch is on, D1 (from Figure) is reverse biased due to the dot configuration of the transformer. No current flows in the secondary windings and the current in the primary winding ramps up at a rate of:

$$\frac{\Delta I_L}{\Delta t} = \frac{V_{in(min)} - V_{Rds(on)}}{L_P} \dots\dots (2)$$

Where  $L_P$  is the primary inductance in Henries and  $\Delta t$  is equal to  $t_{on(max)}$  at  $V_{in(min)}$ .  $\Delta I_L$  is the change in the inductor current which appears as a positive slope ramp on a step in the inductor current waveform.

Based on (2), the primary inductance can be calculated given an acceptable current ripple,  $\Delta I_L$ . Considering 30% current ripple and CCM flyback design, the peak primary current is calculated based on equation (3).

$$I_{peak} = I_L + \frac{\Delta I_L}{2} \text{ where, } I_L = \left( \frac{I_{out(max)}}{N} \right) \left( \frac{1}{1-D_{max}} \right) \dots\dots\dots (3)$$

By replacing  $\Delta I_L$  with  $0.3I_L$ ,  $I_{out(max)}=10A$ ,  $D_{max}=0.48$  and  $N=5$ , we will get peak primary current as 4.42A,  $I_L=3.85A$  and  $\Delta I_L=1.15A$ . The RMS current of a ramp on a step waveform is defined in (4) and calculates to be 2.68A for this application.

$$I_{rms} = \sqrt{\frac{t_{on(max)}}{T} \left( I_{peak}^2 - \Delta I_L I_{peak} + \frac{(\Delta I_L)^2}{3} \right)} \dots\dots\dots (4)$$

Using equation (2),  $L_P$  calculates to approximately 180 $\mu$ H.

Because the inductor (the flyback transformer) is driven in one quadrant of the B-H plane only, a larger core is required in a flyback design. As this converter is operating in the continuous conduction mode at a relatively low frequency, the maximum peak flux density,  $B_{max}$ , is limited by the saturation flux density,  $B_{sat}$ . Taking all this into consideration, the minimum core size is determined by (5).

$$AP = \frac{L_P * I_{peak} * I_{rms}}{J * k_w * B_{max}} \dots\dots\dots (5)$$

Where AP = area product of the core  $A_C * A_W$

$J$  = Current density  $\approx 3 * 10^6$  A/m<sup>2</sup>

$B_{max}$  = Maximum unsaturated magnetic flux density  $\approx 0.2T$

$K_W$  = Window Factor = 0.3

Upon substituting these values in equation (5) we will get the area product as 11845.6mm<sup>4</sup>, based on this area product we have choose the core with the help of the core tables.

COSMOFERRITE EE 3209 core is selected as the core material for this application as its core area product is close to the area product calculated. Refer appendix for datasheet link.

$A_C = C \times F$  = core area for the selected core is  $84.18\text{mm}^2$ ,

$A_w = (B-C) \times E$  = Window area =  $161\text{mm}^2$

AP = Area product =  $13553\text{mm}^4$

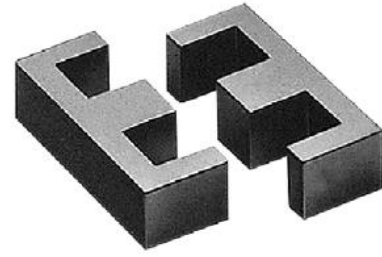
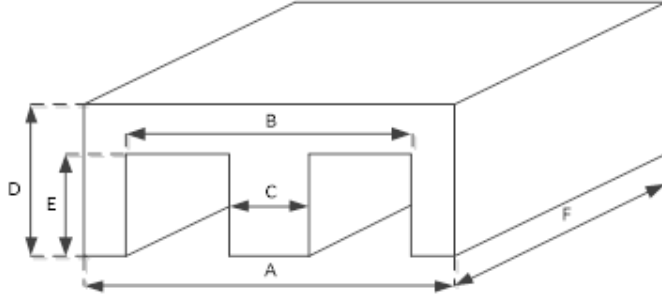


Figure 2: EE cores

The minimum number of primary turns is determined by equation (6).

$$N_P = \frac{L_P \cdot I_P}{B_{max} \cdot A_C} \dots\dots (6)$$

$N_P$  is calculated to be  $\approx 30$  turns, hence the secondary turns  $N_S$  should be 6 to satisfy the turns ratio of 5.

The energy stored in the flyback transformer is actually stored in an air gap in the core. This is because the high permeability of the ferrite material can't store much energy without saturating first. By adding an air gap, the hysteresis curve of the magnetic material is actually tilted, requiring a much higher field strength to saturate the core. The size of the air gap is calculated using the following equation.

$$gap = \frac{\mu_0 \mu_r (N_P)^2 A_C}{L_P} \dots\dots (7)$$

Here,  $\mu_0$  = permeability of free space =  $4\pi \times 10^{-7}$  H/m.

$\mu_r$  = the relative permeability of the gap material (in this case the gap material is air,  $\mu_r = 1$ ).

Substituting all other quantities, gap is found to be 0.053cm and it is evenly distributed between the centre post and two outer legs of the core.

### **WIRE GAUGE SELECTION:**

Required cross sectional area of wire on primary side  $a_p = \frac{I_{P\_rms}}{J} = 8.9 \times 10^{-3} \text{cm}^2$

In order to match this, two strands of 21AWG copper wires are used in parallel.

Required cross sectional area of wire on secondary side  $a_p = \frac{I_{S\_rms}}{J} = \frac{I_{O\_max}}{J \sqrt{(1-D_{max})}} = 46.2 \cdot 10^{-3} \text{cm}^2$ .

In order to match this, six strands of 18AWG copper wires are used in parallel.  
 \*\*These wires should be well twisted in order to have uniform current flow through these wires.

Refer appendix for the selection of wire based on the area calculated.

A proper bobbin is selected based on core that is used and these selected wires are wound on the bobbins in the split primary fashion to reduce the leakage inductance of the transformer. The winding criteria and bobbin and core arrangement is shown in figures followed.

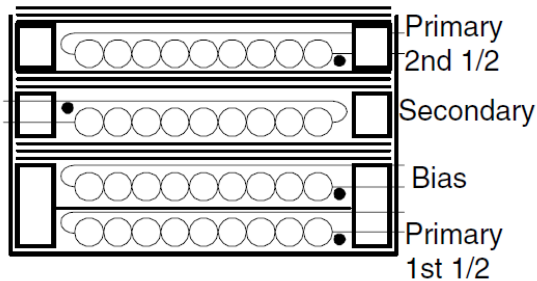


Figure 3: Split Primary winding

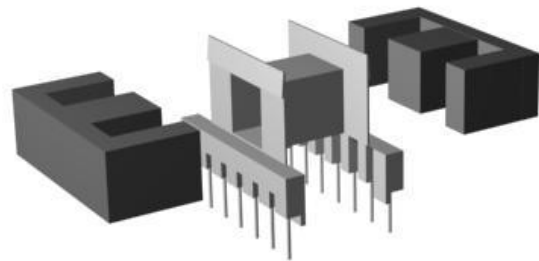


Figure 4: Bobbin and core arrangement

In the split primary winding half of the primary turns which are 15 in this design are wound as first layer, then all secondary (6) turns are wound as second layer and finally the remaining 15 turns of primary winding is wound as third layer.

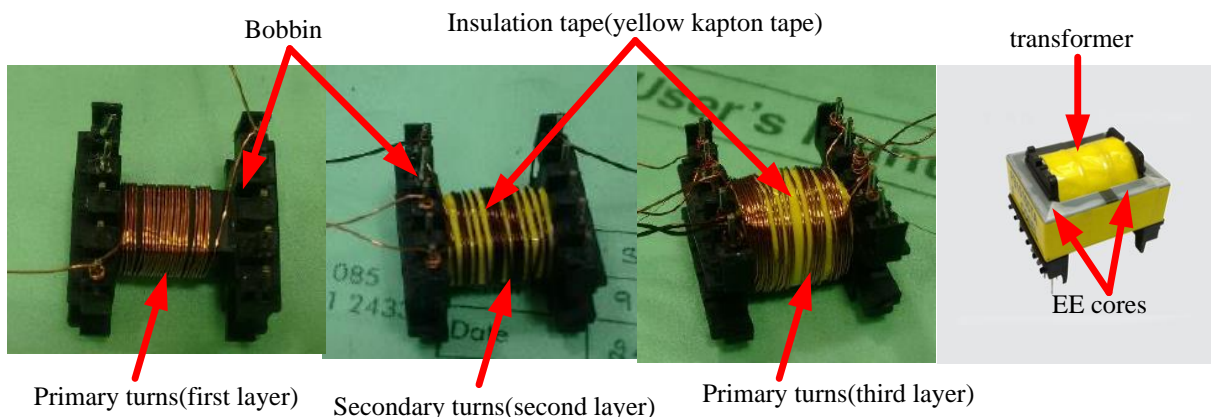


Figure 5: Practical illustration of the winding phenomena.

## **TRANSFORMER LOSSES:**

### **Copper losses:**

Mean Length per Turn (MLT)=  $2(C+F) = 2(9.2+9.15) = 36.7\text{mm}$  for the selected core.

Total length of the wire considering 30 primary turns =  $30 \times 36.7 = 1101\text{mm}$  it will be more considering split primary winding so it is approximated to 1125mm.

Resistance one strand  $R_{dc} = \rho L/A = 2.3 \times 10^{-5} \times 1125 / 411.6 \times 10^{-3} = 0.063 \Omega$

Where  $\rho$  is the resistivity of copper wire at  $100^\circ\text{C}$

Total resistance of the primary winding =  $0.063/2 = 0.0315 \Omega$  (as we are using two strands of copper wire in parallel for primary winding)

Copper loss in primary winding =  $I_{P\_rms}^2 \times R_{dc} = (2.68)^2 \times 0.0315 = 0.226\text{W}$

Similarly, we can find  $R_{dc}$  for secondary side coil/strand which is  $= 0.0053 \Omega$

Total resistance of the secondary winding =  $0.0053/6 = 0.00088 \Omega$  (as we are using 6 strands of copper wire in parallel for secondary winding)

Copper loss in secondary winding =  $I_{S\_rms}^2 \times R_{dc} = (13.87)^2 \times 0.00088 = 0.18\text{W}$

Total copper loss =  $0.4\text{W}$

### **Core loss:**

According to the data sheet core loss for 100kHz operation at  $100^\circ\text{C}$  and considering the maximum peak to peak flux swing of 100mT, is 0.55W/set. In this design the switching frequency is 70kHz, so the loss can be approximated to 0.4W/set.

So total transformer losses are equal to 0.8W.

### **MOSFET SELECTION:**

The switching element in a flyback converter must have a voltage rating high enough to handle the maximum input voltage and the reflected secondary voltage, not to mention any leakage inductance induced spike that is inevitably present. Approximate the required voltage rating of the MOSFET using equation 8.

$V_{ds} = \left[ (V_{in(max)}) + \left( \frac{N_P}{N_S} \right) (V_o + V_D) \right] \times 1.3 \dots\dots (8a)$  neglecting leakage inductance,

$V_{ds} = \left[ (V_{in(max)}) + V_C \right] \dots\dots (8b)$  considering leakage inductance

$V_{ds}$  = the required drain to source voltage rating of the MOSFET,

$V_C$  = the voltage across the clamp capacitor = reflected secondary voltage to primary + voltage spike due to leakage inductance  $\approx 150\text{V}$  (worst case),

and the additional 1.3 factor includes an overall thirty percent margin.

For the flyback converter presented, the required minimum voltage rating of the MOSFET calculates to be 222V considering the leakage.

An FDPF33N25T N-channel power MOSFET was chosen. This device has a voltage rating of 250V, a continuous DC current rating of 20A, and an  $R_{ds(on)}$  of only 94m $\Omega$ . Refer appendix for datasheet link.

### MOSFET LOSSES:

**Conduction loss:**  $P_{cond} = (I_{rms})^2 \cdot R_{ds(on)} @ 100^\circ C = 2.68^2 \times 164.5 \times 10^{-3} = 1.18W$

**Switching Loss:** The switching waveforms of MOSFET during turn ON and turn OFF transitions are shown in the figure 8. Switching losses in the MOSFET are due to high current and high voltage being present in the device simultaneously for a short period. At turn on the drain current begins to flow through the MOSFET when the gate voltage has reached the  $V_{gs}$  threshold. This drain current will continue to rise until reaching its final value. Meanwhile, the drain to source voltage will remain at  $V_{ds}$ , calculated earlier in (8). This voltage starts to fall only after the “Miller” capacitor begins to charge. The charging time,  $t_{ch}$ , for the “Miller” capacitor is a function of the gate resistor,  $R_g$  and the gate to drain “Miller” charge,  $Q_{gd}$ , as given in the datasheet of the MOSFET.

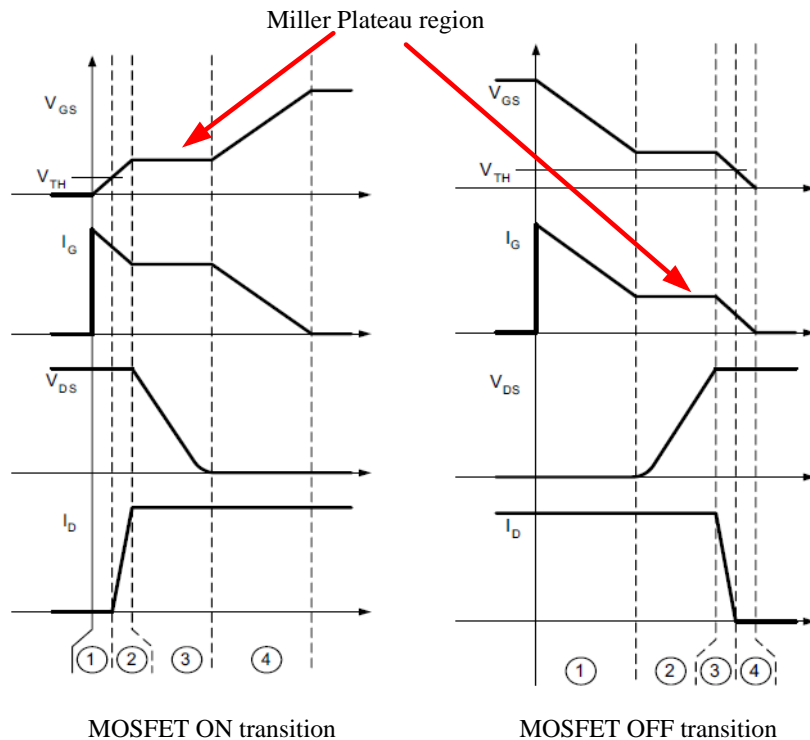


Figure 8: Switching transition of MOSFET

$$t_{ch} = \frac{Q_{gd} \cdot R_g}{V_{drv} - V_{th}} \dots\dots (9)$$

Here  $Q_{gd}$  = Gate-to-Drain ("Miller") Charge = 17nC (from the MOSFET datasheet)

$V_{drv}$  = Gate driver voltage = 15V

$V_{th}$  = gate to source threshold voltage = 3V

$R_g$  = gate resistance = 25  $\Omega$

By substituting these values in equation (9) we will get  $t_{ch}$  = 35.4nS.

The power dissipation of the MOSFET's output capacitance,  $C_{oss}$ , = 330pF for chosen MOSFET, also contributes to the switching losses in the form of  $\frac{1}{2}CV^2f$ . The total switching power loss in MOSFET can be estimated based on the equation (10)

$$P_{SW} = \frac{C_{oss} * (V_{ds})^2 * f_{SW}}{2} + V_{ds} * I_{peak} * t_{ch} * f_{SW} \dots \dots (10)$$

Here  $V_{ds}$  is drain to source voltage of the MOSFET, during operating condition which will be a maximum of 150V depending on the specifications chosen.

Substituting all the values the total switching loss is found to be 1.9W

Total losses in the MOSFET =  $P_{cond} + P_{sw} = 3.08W$

### **DIODE SELECTION:**

Schottky rectifiers have a lower forward voltage drop than typical PN devices, making it the rectifier of choice when considering reducing converter losses and improving overall efficiency. Selecting the appropriate Schottky for a specific application depends mainly on

- the working peak reverse voltage rating,
- the peak repetitive forward current, and
- the average forward current rating of the device.

1. Peak Reverse voltage =  $(V_{in(max)} * (N_S/N_P)) - V_{dM} + V_o = 20V$

2. The maximum average forward diode current is equal to the steady-state load current = 10A

3. The peak repetitive forward current is equal to the reflected primary peak current = 26A

An MBR2535CTL Schottky rectifier from Motorola met the requirements for this design (Refer appendix for datasheet link). This device is a common cathode dual Schottky with a forward voltage drop of 0.47V and a working peak reverse voltage rating of 35V, exceeding the 20V requirement of the chosen design. The average rectified forward current rating is specified at 12.5A per leg, 25A total, and the peak repetitive forward current is rated for 25A per leg, or a total of 50A. Which are more than the design requirement that is 10A total average forward current and 26A total peak repetitive forward current.



## **DIODE LOSSES:**

Power loss in the Schottky is the summation of conduction losses and the reverse leakage losses.

Conduction losses are calculated using the forward voltage drop and the average forward current =  $0.47 \times 10 = 4.7\text{W}$ .

Reverse leakage losses, which are dependent upon the reverse leakage current, the blocking voltage, and the on-time of the MOSFET =  $V_{FD} \times I_{rr} \times D_{\max} = 0.05\text{W}$ .

Total power loss in the diode =  $4.75\text{W}$

## **OUTPUT CAPACITOR DESIGN:**

The output capacitors are also chosen based upon their low equivalent series resistance (ESR), ripple current and voltage ratings, and equation (11).

$$C_{min} = \frac{I_{rms}}{8 \times f_{sw} \times \Delta V} \dots \dots (11)$$

The secondary rms current is  $13.87\text{A}$ , choosing a 2% ripple in output voltage  $C_{min}$  can be calculated to be  $248\mu\text{F}$ .

Ripple current =  $\sqrt{I_{Srms}^2 - I_L^2} = 9.61\text{A}$ .

Four Sanyo OSCON 6SH330M  $330\mu\text{F}$  capacitors in parallel met the requirements for this design when derated for ambient temperature and frequency. Refer appendix for datasheet link.

ESR =  $25\text{m}\Omega$ /capacitor, there are 4 capacitors in parallel so effective ESR =  $25/4 = 6.25\text{m}\Omega$

Power loss in this capacitor =  $I_{rms\_cap}^2 \times \text{ESR}$

$$= \left( I_L \times \sqrt{\frac{2 \times I_{pri\_peak} \times N_P}{3 \times N_S \times I_L}} - 1 \right)^2 \times 6.25\text{m}\Omega = 0.3\text{W}$$

## **CLAMP CIRCUIT:**

Transformer leakage inductance imposes high transients in the switch, requiring a switching device with an excessive voltage rating. The primary side of the converter utilizes a passive polarized voltage clamp (Figure 9) to suppress the voltage overshoot during the turn-off transition of the MOSFET. This circuit limits the peak switch voltage, reducing the power dissipation in the switching device. The total dissipated energy remains the same, but it is now divided between the clamp resistor and the MOSFET.

The parasitic inductance of the transformer is discharged into the capacitor during each switching cycle. The value of the capacitor is selected based upon the amount of energy that this leakage inductance stores plus the initial energy stored in the capacitor from the input voltage and the reflected output voltage. Equation (12) determines the minimum capacitor value.

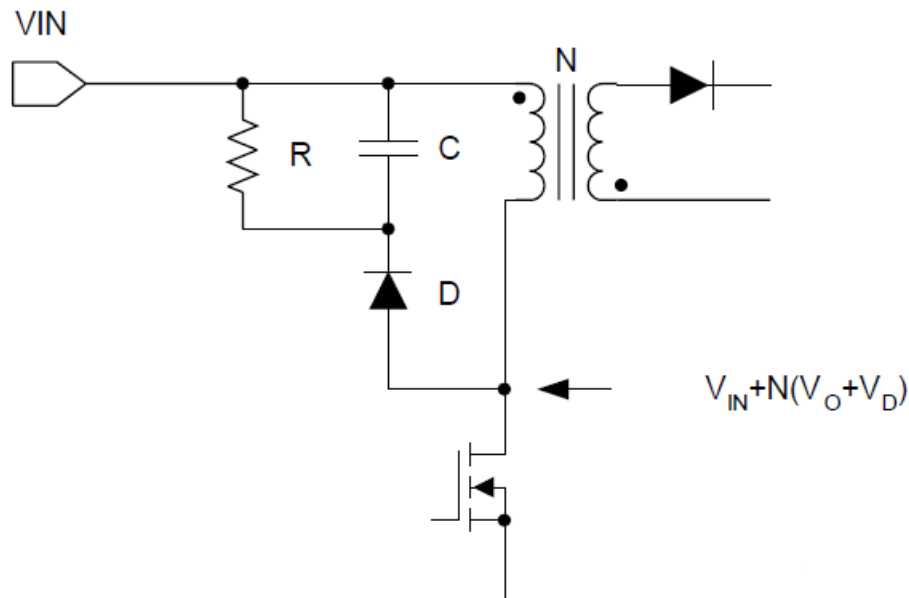


Figure 9: RCD clamp on the primary side suppresses voltage overshoot across the FET

$$C = \frac{L_{lk} * (I_{peak})^2}{\Delta V_c * (\Delta V_c + 2V)} \dots\dots\dots (12)$$

\*This equation is obtained by energy balance i.e, equating the energy stored in the leakage inductor with the energy stored in the clamp capacitor.

- $L_{lk}$  is the leakage inductance of the transformer = 5% of magnetising inductance =  $9\mu H$ ,
- $I_{peak}$  = peak current in the inductor at the time of turn-off,
- $\Delta V_c$  = voltage ripple in  $V_c = 30V$  (considering 20% ripple),
- $V$  = the DC bias across the capacitor which is a result of the DC path through the resistor and diode and the secondary side voltage reflected to the primary and  $= N \cdot (V_o + V_D) = 29V$

Substituting this value in equation (12) will give you the snubber capacitance of  $0.09\mu F$ , so we can choose a capacitor having capacitance =  $0.1\mu F$ .

The power dissipated in the clamp circuit is given by:

$$P_c = \frac{1}{2} \times V_c \times I_{peak} \times t_s \times f_{sw} \text{ where, } t_s = (L_{lk} \times I_{peak}) / (V_c - V)$$

$$P_c = 7.62W$$

$$P_c = \frac{V_c^2}{R} \dots\dots\dots (13)$$

From Eq.(13),  $R=2952\Omega \approx 3K\Omega$ . Here a  $5K\Omega$  resistance should be used to limit the loss in the clamp circuit.

The diode is selected based upon the charging current of the capacitor.

### **HEAT SINK DESIGN FOR MOSFET AND DIODE:**

The FDPF33N25T MOSFET has a junction to case thermal resistance,  $\theta_{JC}$ , of  $3.4^{\circ}\text{C/W}$ . Using a silicone elastomer heat sink pad provides a case to heat sink thermal resistance,  $\theta_{CS}$ , of  $1.26^{\circ}\text{C/W}$ .

$$\theta_{SA} = \frac{T_J - T_A}{P_{con} + P_{sw}} - (\theta_{JC} + \theta_{CS}) \dots \dots (14)$$

Choosing the maximum allowable junction temperature =  $T_J = 150^{\circ}\text{C}$  and ambient temperature =  $T_A = 25^{\circ}\text{C}$ , the  $\theta_{SA}$  is calculated using equation (14) and =  $35.92^{\circ}\text{C/W}$ .

So, a heat sink which provides a maximum thermal resistance,  $\theta_{SA}$ , of  $35.92^{\circ}\text{C/W}$  must be chosen for a use in an ambient temperature,  $T_A$ , of  $25^{\circ}\text{C}$ .

The 577002B00000G, HEAT SINK from AAVID/BOYD can be used here, datasheet link for this heat sink is provided in appendix.

Similarly, the MBR2535CTLG diode has a junction to case thermal resistance,  $\theta_{JC}$ , of  $2^{\circ}\text{C/W}$ , and total loss in the diode is  $4.75\text{W}$ , which is calculated earlier. Keeping remaining parameters as they are the maximum thermal resistance,  $\theta_{SA}$ , provided by the heat sink is calculated to be  $23^{\circ}\text{C/W}$ .

So, a heat sink which provides a maximum thermal resistance,  $\theta_{SA}$ , of  $23^{\circ}\text{C/W}$  must be chosen for a use in an ambient temperature,  $T_A$ , of  $25^{\circ}\text{C}$ .

The PF752, HEAT SINK from AAVID/BOYD can be used here, datasheet link for this heat sink is provided in appendix.

### **EFFECIENCY:**

The total losses = Transformer losses + MOSFET losses + Diode losses + Capacitor loss =  $8.93\text{W}$

Efficiency =  $[\text{output} / (\text{output} + \text{losses})] \times 100 = 85\%$

## **References:**

1. Text book: Course Material on Switched Mode Power Conversion by prof. V. Ramanarayanan.
2. <https://www.ti.com/lit/an/slva086/slva086.pdf>
3. <https://www.ti.com/lit/pdf/slva666>
4. <https://www.ti.com/lit/ml/slup127/slup127.pdf>

# APPENDIX

A. W. G.	DIAMETER	AREA	WEIGHT		LENGTH		RESISTANCE	
B. & S.	Mm.	Sq. Mm.	Kg. per M.	Kg. per Ohm	M. per Kg.	M. per Ohm	Ohms per Kg.	Ohms per M.
0000	11.7	107.2	.953	5940	1.05	6,230	.000168	.000161
000	10.4	85.0	.756	3730	1.32	4,940	.000268	.000202
00	9.27	67.4	.599	2350	1.67	3,920	.000426	.000255
0	8.25	53.5	.475	1480	2.10	3,110	.000677	.000322
1	7.35	42.4	.377	929	2.65	2,460	.00108	.000406
2	6.54	33.6	.299	584	3.35	1,950	.00171	.000512
3	5.83	26.7	.237	367	4.22	1,550	.00272	.000645
4	5.19	21.2	.188	231	5.32	1,230	.00433	.000814
5	4.62	16.8	.149	145	6.71	975	.00688	.00103
6	4.11	13.3	.118	91.4	8.46	773	.0109	.00129
7	3.67	10.6	.0938	57.5	10.7	613	.0174	.00163
8	3.26	8.37	.0744	36.2	13.5	486	.0277	.00206
9	2.91	6.63	.0590	22.7	17.0	386	.0440	.00259
10	2.59	5.26	.0468	14.3	21.4	306	.0690	.00327
11	2.31	4.17	.0371	8.99	27.0	242	.111	.00413
12	2.05	3.31	.0294	5.66	34.0	192	.177	.00520
13	1.83	2.62	.0234	3.56	42.9	153	.281	.00656
14	1.63	2.08	.0185	2.24	54.1	121	.447	.00827
15	1.45	1.65	.0147	1.41	68.2	95.9	.711	.0104
16	1.29	1.31	.0116	.885	86.0	76.0	1.13	.0132
17	1.15	1.04	.00922	.556	108	60.3	1.80	.0166
18	1.02	.823	.00732	.350	136	47.8	2.86	.0209
19	.912	.653	.00580	.220	172	37.9	4.54	.0264
20	.812	.518	.00460	.138	217	30.1	7.23	.0333
21	.723	.410	.00365	.0871	274	23.9	11.5	.0419
22	.644	.326	.00289	.0548	346	18.9	18.3	.0529
23	.573	.258	.00229	.0344	436	15.0	29.1	.0667
24	.511	.205	.00182	.0217	550	11.9	46.2	.0841
25	.455	.162	.00144	.0136	693	9.43	73.4	.106
26	.405	.129	.00114	.00856	874	7.48	117	.134
27	.361	.102	.000908	.00538	1,100	5.93	186	.169
28	.321	.081	.000720	.00339	1,390	4.70	295	.213
29	.286	.0642	.000571	.00213	1,750	3.73	470	.268
30	.255	.0510	.000453	.00134	2,210	2.96	747	.338
31	.227	.0404	.000359	.000842	2,790	2.35	1,190	.426
32	.202	.0320	.000285	.000530	3,510	1.86	1,890	.537
33	.180	.0254	.000226	.000333	4,430	1.48	3,000	.678
34	.160	.0201	.000179	.000210	5,590	1.17	4,770	.855
35	.143	.0160	.000142	.000132	7,040	.928	7,590	1.08
36	.127	.0127	.000113	.0000829	8,880	.736	12,100	1.36
37	.113	.0101	.0000893	.0000521	11,200	.584	19,200	1.71
38	.101	.00797	.0000708	.0000327	14,100	.463	30,600	2.16
39	.0897	.00632	.0000562	.0000206	17,800	.367	48,500	2.73
40	.0799	.00501	.0000445	.0000130	22,500	.291	77,100	3.44

Wire Gauge table

MOSFET datasheet link:

[http://www.farnell.com/datasheets/1876049.pdf?\\_ga=2.23335674.1737564411.1601820746-934437522.1601281899&\\_gac=1.182657492.1601654148.CjwKCAjwn9v7BRBqEiwAbq1Ey88FzK7JRvxIOWaoW6XkYD83Zzpbk9FYZ-Afl9uz76\\_AhYthRbel0RoCqWwQAvD\\_BwE](http://www.farnell.com/datasheets/1876049.pdf?_ga=2.23335674.1737564411.1601820746-934437522.1601281899&_gac=1.182657492.1601654148.CjwKCAjwn9v7BRBqEiwAbq1Ey88FzK7JRvxIOWaoW6XkYD83Zzpbk9FYZ-Afl9uz76_AhYthRbel0RoCqWwQAvD_BwE)

Diode datasheet link:

<http://www.onsemi.com/pub/Collateral/MBR2535CTL-D.PDF>

Output capacitor datasheet link:

<http://pdf.datasheet.live/c901a0a6/semic.sanyo.co.jp/6SH15M.pdf>

Core datasheet link:

[http://www.cosmoferites.com/Downloads/ProductSize/78097ef7-10eb-476e-8649-f8e400047d1a\\_EE3209%20OL\(WS\).pdf](http://www.cosmoferites.com/Downloads/ProductSize/78097ef7-10eb-476e-8649-f8e400047d1a_EE3209%20OL(WS).pdf)

MOSFET heat sink datasheet link:

[http://www.farnell.com/datasheets/2552797.pdf?\\_ga=2.48829926.1737564411.1601820746-934437522.1601281899&\\_gac=1.221523690.1601654148.CjwKCAjwn9v7BRBqEiwAbq1Ey88FzK7JRvxIOWaoW6XkYD83Zzpbk9FYZ-Afl9uz76\\_AhYthRbel0RoCqWwQAvD\\_BwE](http://www.farnell.com/datasheets/2552797.pdf?_ga=2.48829926.1737564411.1601820746-934437522.1601281899&_gac=1.221523690.1601654148.CjwKCAjwn9v7BRBqEiwAbq1Ey88FzK7JRvxIOWaoW6XkYD83Zzpbk9FYZ-Afl9uz76_AhYthRbel0RoCqWwQAvD_BwE)

Diode heat sink datasheet link:

[http://www.farnell.com/datasheets/84564.pdf?\\_ga=2.202425809.1905462968.1601281899-934437522.1601281899&\\_gac=1.224737640.1601379533.Cj0KCQjwtsv7BRCmARIsANu-CQdpQIj0IgWWV1FK-6XeXA7DFp10hqB55nrQrvo8m2yRrkKhr2cGsp4aAsPIEALw\\_wcB](http://www.farnell.com/datasheets/84564.pdf?_ga=2.202425809.1905462968.1601281899-934437522.1601281899&_gac=1.224737640.1601379533.Cj0KCQjwtsv7BRCmARIsANu-CQdpQIj0IgWWV1FK-6XeXA7DFp10hqB55nrQrvo8m2yRrkKhr2cGsp4aAsPIEALw_wcB)