Dec Assignment
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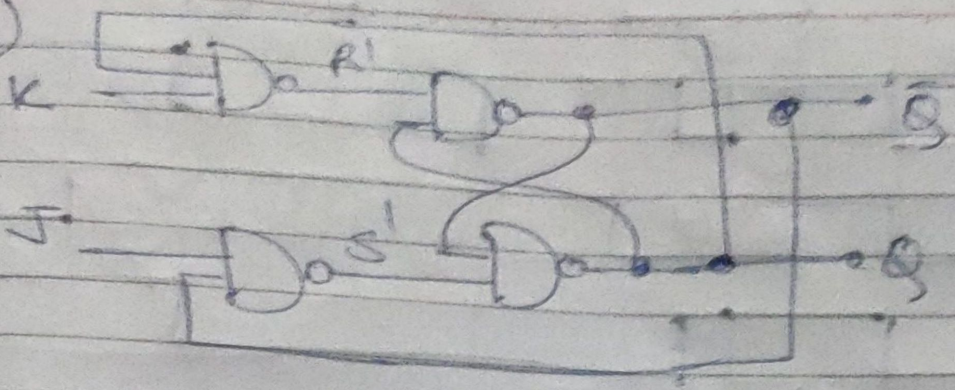
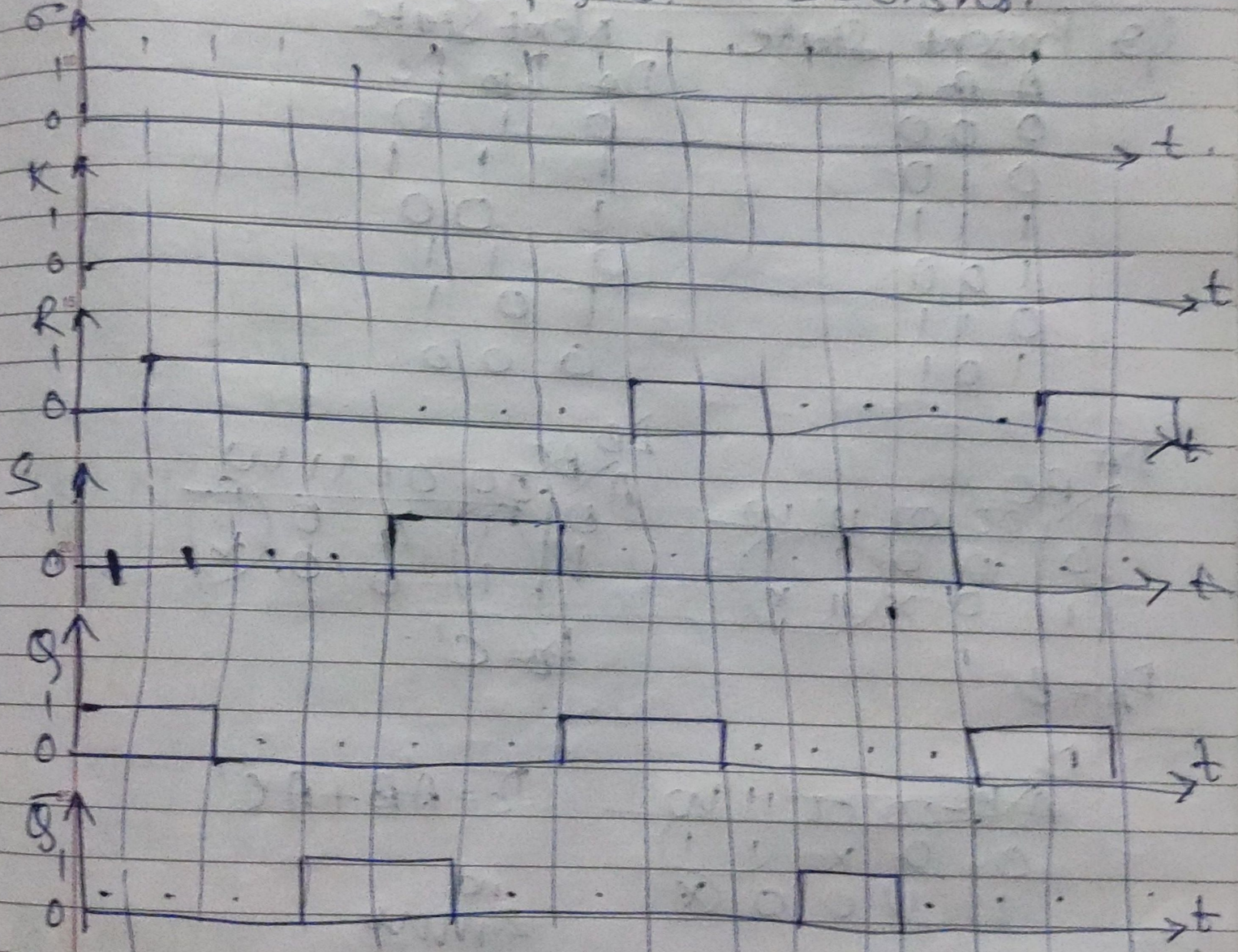
Q1. a)

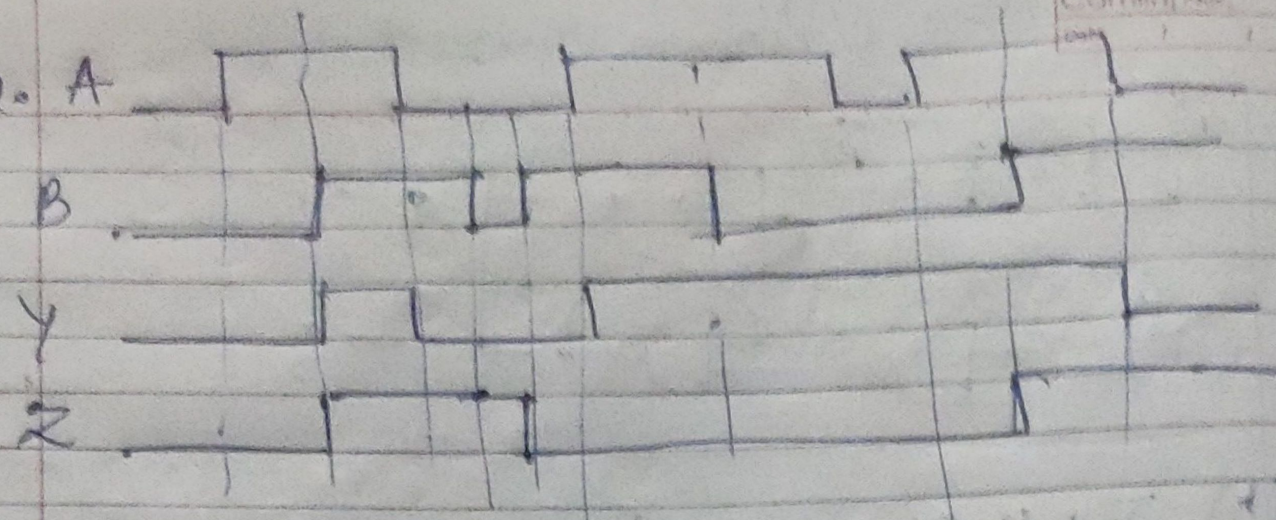


(b) J=1, K=0 → Q=1, Q'=0. τ = 0.5ns.



$$f = \frac{1}{T} = \frac{1}{6 \times 0.5} = \frac{1}{3\ ns} = 333.\overline{3}\ MHz.$$

Q2.



Q3.

Present State			Next State		
A	B	C	D_A	D_B	D_C
0	0	0	0	1	0
0	1	0	1	1	1
1	1	1	1	0	0
1	0	0	0	1	1
0	1	1	1	0	1
1	0	1	0	0	0

D_A

A \ BC	00	01	11	10
0	0	0	1	1
1	0	X	1	X

$D_A = B$

D_B

A \ BC	00	01	11	10
0	1	X	0	1
1	1	0	0	X

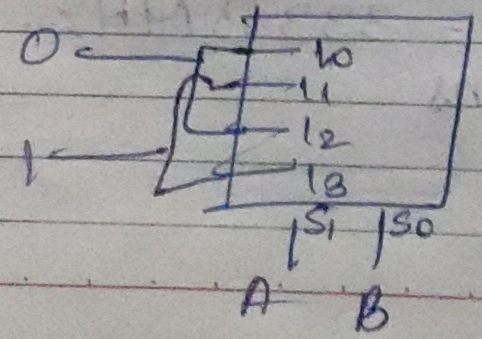
$D_B = C'$

D_C

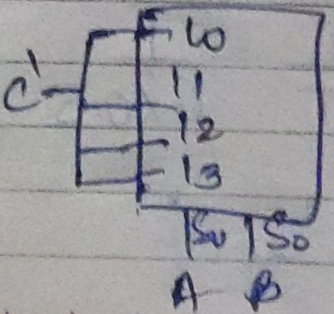
A \ BC	00	01	11	10
0	0	X	1	1
1	1	0	0	X

$D_C = A'B + AC'$

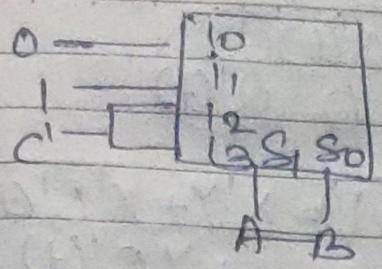
1st mux



2nd mux



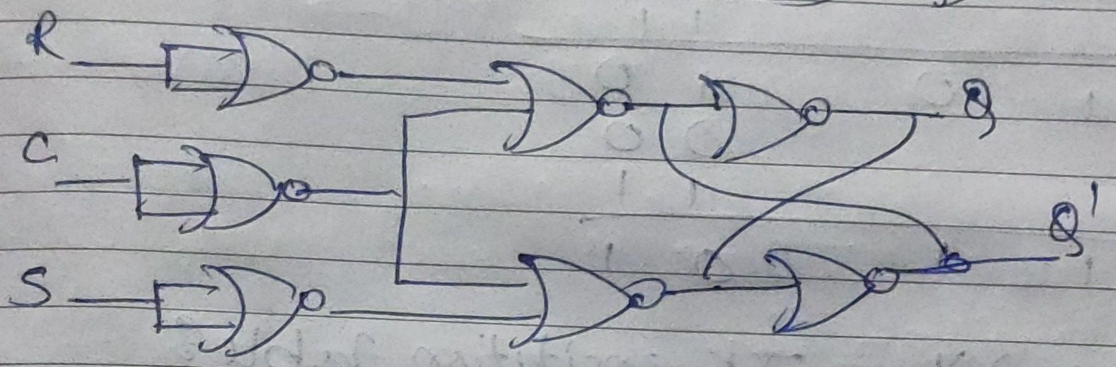
3 MUX



Q4. a) NOR gates:

$Q(t+1) = [(RC + Q')]' = [(R' + C')' + Q']'$

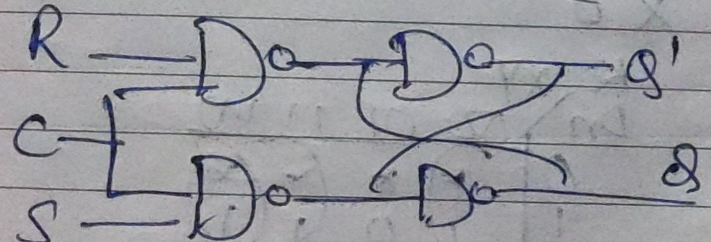
$Q'(t+1) = (SC + Q)' = [(S' + C')' + Q]'$



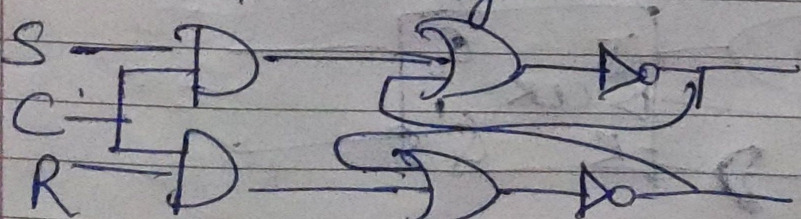
(b) NAND gates

$Q(t+1) = (RC + Q')' = RC]' \cdot Q = (RC)' \cdot (Q')')''$

$Q'(t+1) = (SC + Q)' = (SC)' \cdot Q)''$



(c) AND, OR, Invert gates.



Q. (a)

x	y	Q(t+1)
0	0	Q'(t)
0	1	1
1	0	0
1	1	Q'(t)

x \ y	0	1
0	Q'(t)	1
1	0	Q(t)

$Q(t+1) = x'y + x'Q'(t) + yQ'(t)$.

(b)

Q(t)	Q(t+1)	x	y
0	0	1	0
0	1	0	1
		0	0
		1	1
1	0	1	0
		0	0
		1	1
1	1	0	1

(c) JK to XY: JK excitation table

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Dn \ xy	00	01	11	10
0	1	1	1	0
1	x	x	x	x

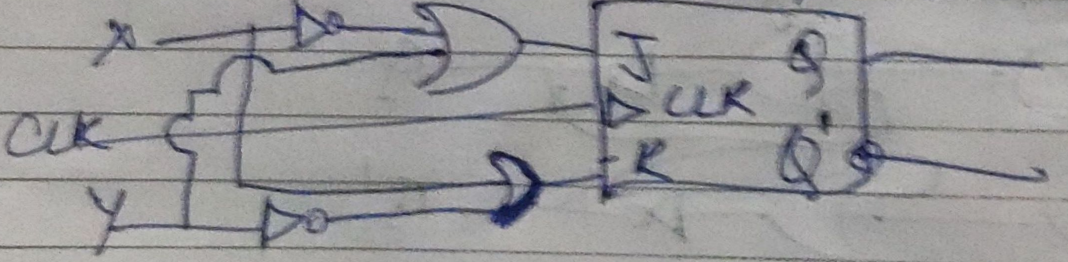
J

Dn \ xy	00	01	11	10
0	x	x	x	x
1	1	0	1	1

K

$J = x'+y$

$K = y'+x$;



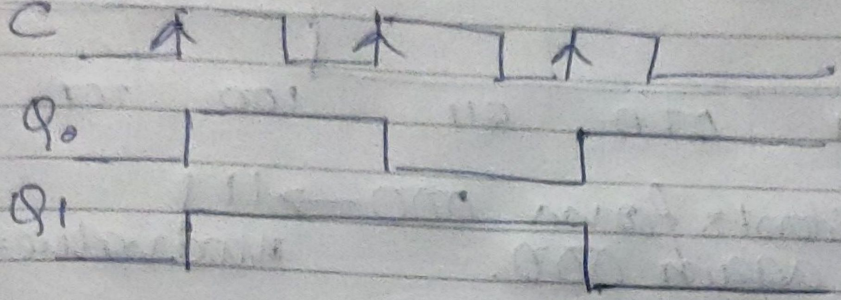
Q6(a) $J = Q'$

$Q(t+1) = JQ' + K'Q = Q'(t)$.

Initially zero, so sequence

0 1 0 1 0 1.

(b) T=1, so output would be complement of prev output.



Q7. $S = (Q \oplus x)'$; $R = (Q \oplus x)$

$Q(t+1) = S + R'Q(t)$

$= (Qx' + Q'x)' + (Qx' + Q'x) \cdot Q$.

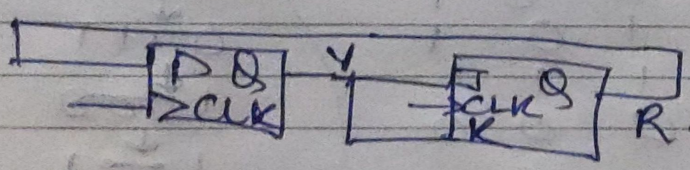
$= (Qx')' \cdot (Q'x)' + Qx'$

$= (Q' + x) \cdot (Q + x') + Qx'$

$= Q'x' + Qx + Qx' = \underline{Q'x' + Qx}$

Q8. When clk goes from 0→1 and x=0, A is 1 and B=0, so Q=0.
When clk goes from 0→1 and x=1 B=1, A=0 and Q=1.

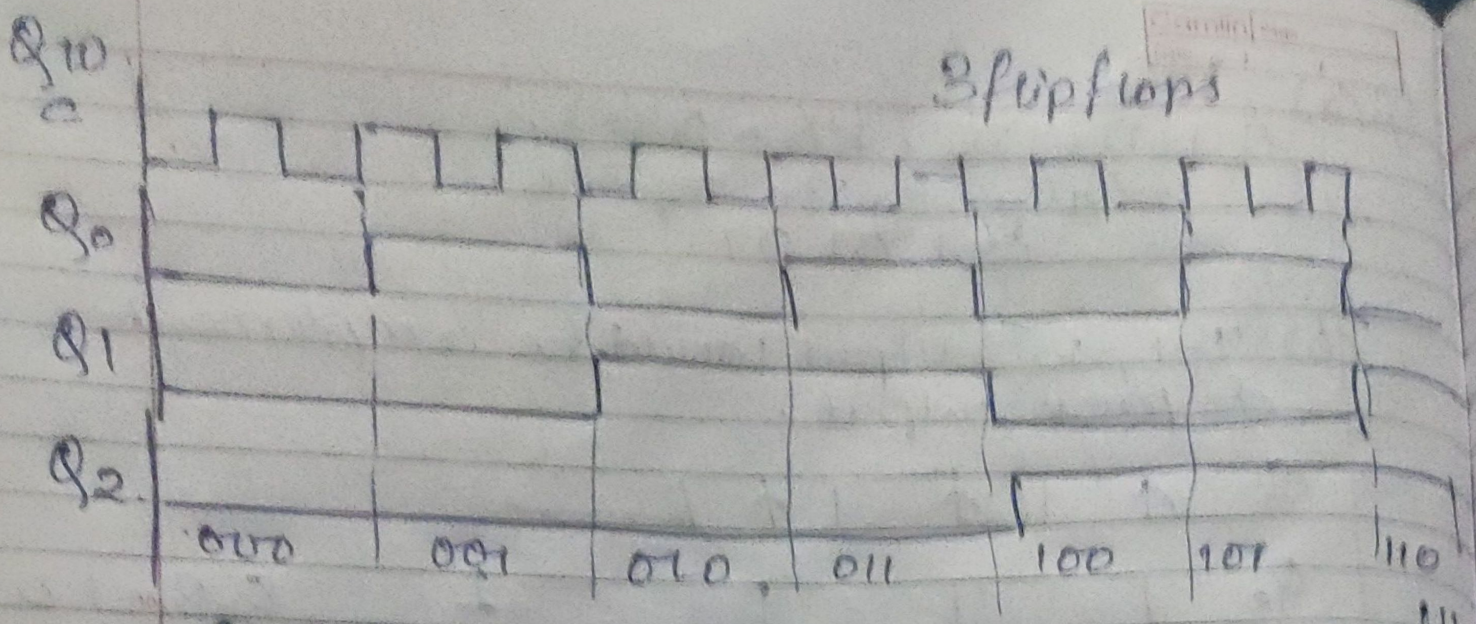
Q9.



Bit sequence at Y
0 1 1 0 1 1 0 1 1

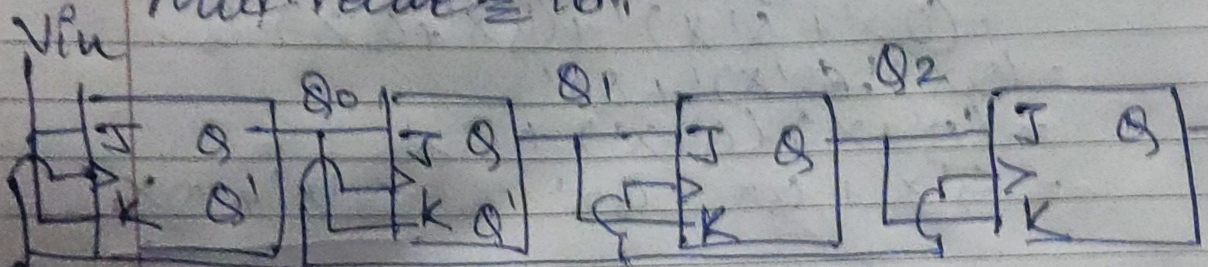
Y	Z	
0	1	
1	1	Y → tells to hold, Z makes Y1
1	0	Y → tells to toggle, Z makes Y1
0	1	Y → tells to toggle, Z makes Y0.
1	0	

clk 1,2 and clk 3



$Q_2Q_1Q_0$ starts from 000 → 111 and then again 000. mod value = 8.

Similarly for 4 such flipflop, Circuit will go from 0000 → 1111 and then 0000. mod value = 16.



CLK	J, K	Q_0	Q_1	Q_2	Q_3
—	1 1	0	0	0	0
1	1 1	1	0	0	0
2	1 1	0	1	0	0
3	1 1	1	1	0	0
4	1 1	0	0	0	1
5	1 1	1	0	0	1
6	1 1	0	1	0	1
7	1 1	1	1	1	1
8	1 1	0	0	0	0

0000 → 0001 → 0010 → 0011 → 1000 → 1001 → 1010 → 1111