

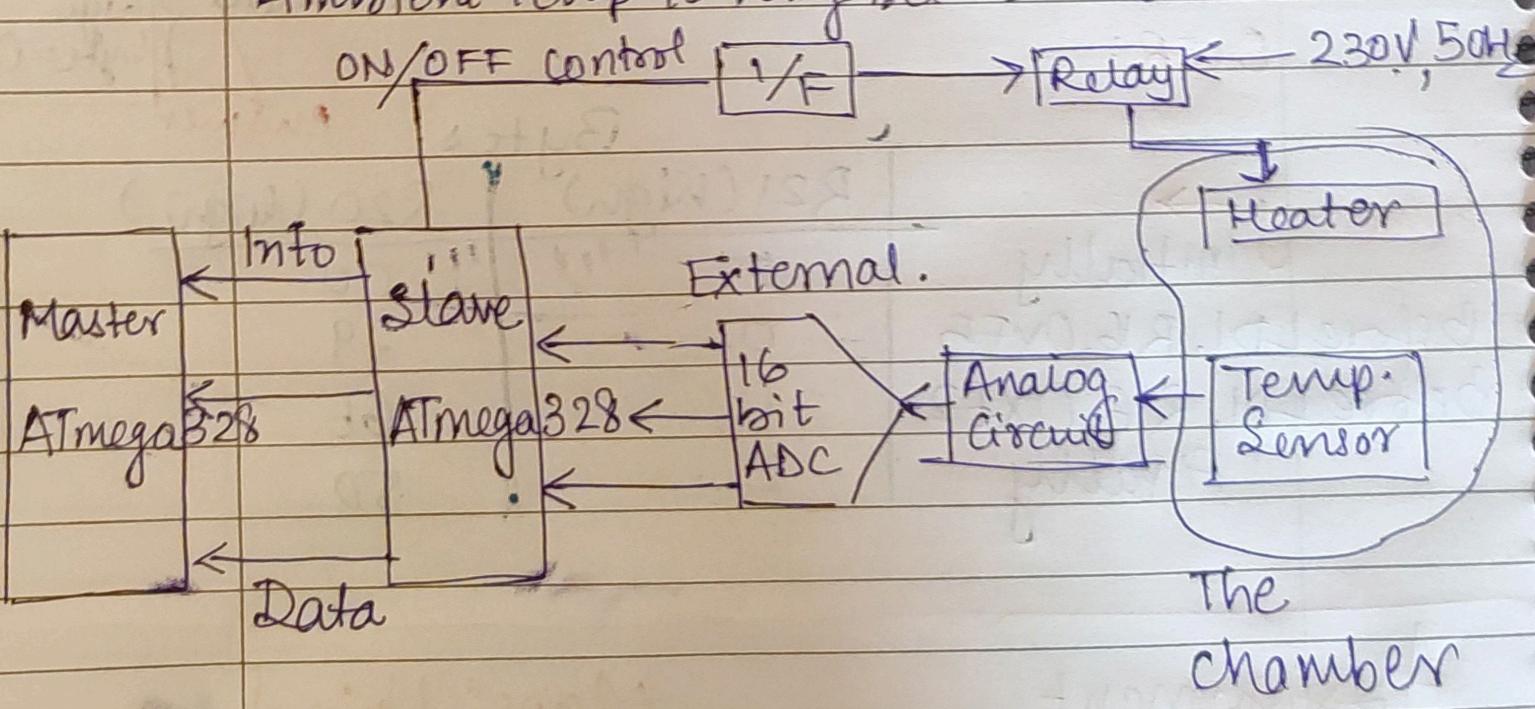
# Embedded Systems - Mansi Uniyal 19EE10039.

Question Design edge computing device to monitor temp. of chamber which is slowly changing and transmit values of master device as depicted.

Sampling time - 1 min. and 16 bit AD converter  
16-bit temp. needs to transmitted only when there is change of temp.  $> 1^{\circ}\text{C}$ .  
 $\therefore$  Change detection algorithm needs to run on slave controller. Master controller is interrupted and data transfer takes place. Subsequently Master controller slaves time and 16 bit temp. values in SRAM.

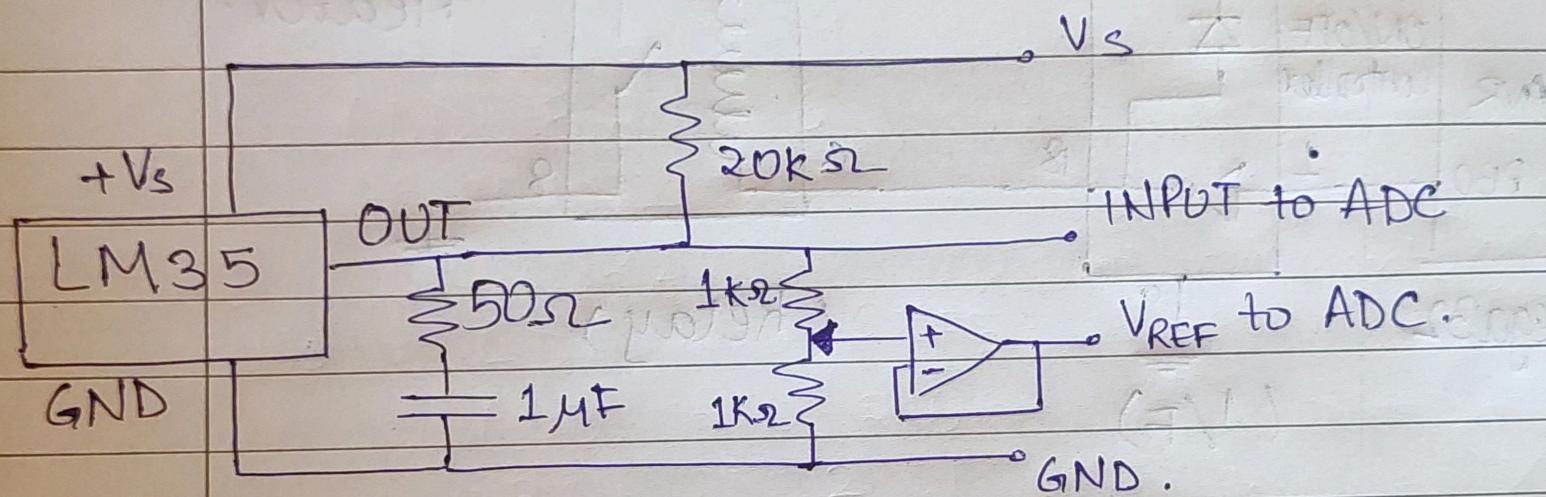
Heater is controlled to maintain temp. at  $25^{\circ}\text{C}$ .

Ambient temp to vary bet  $35\text{-}45^{\circ}\text{C}$ .

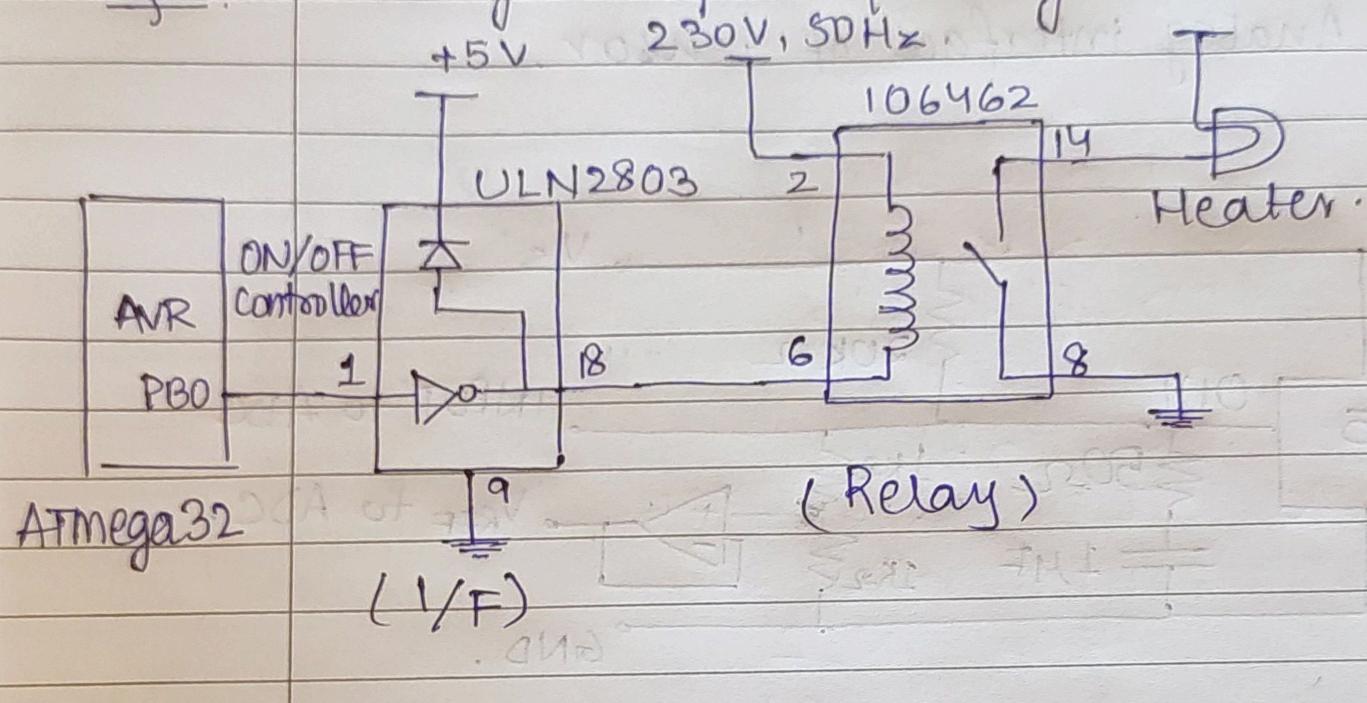


Q10. Circuits.

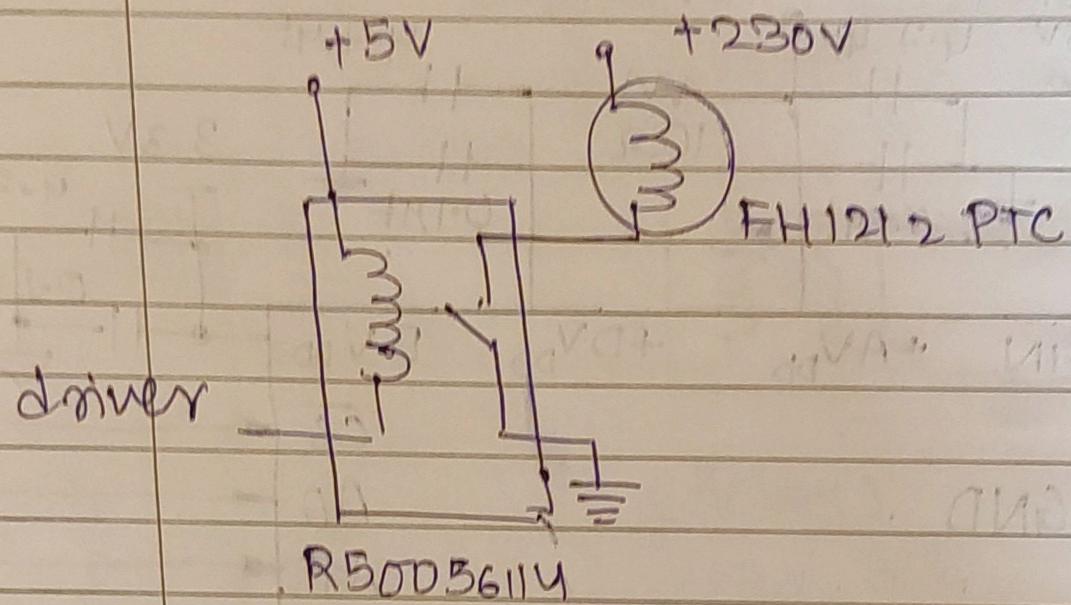
a. Analog interface of sensor.



Q1. b. Analog interface of Relay.



Q10 d. Fleater connection.



Q1.e. Connections between slave & master with all power supplies.

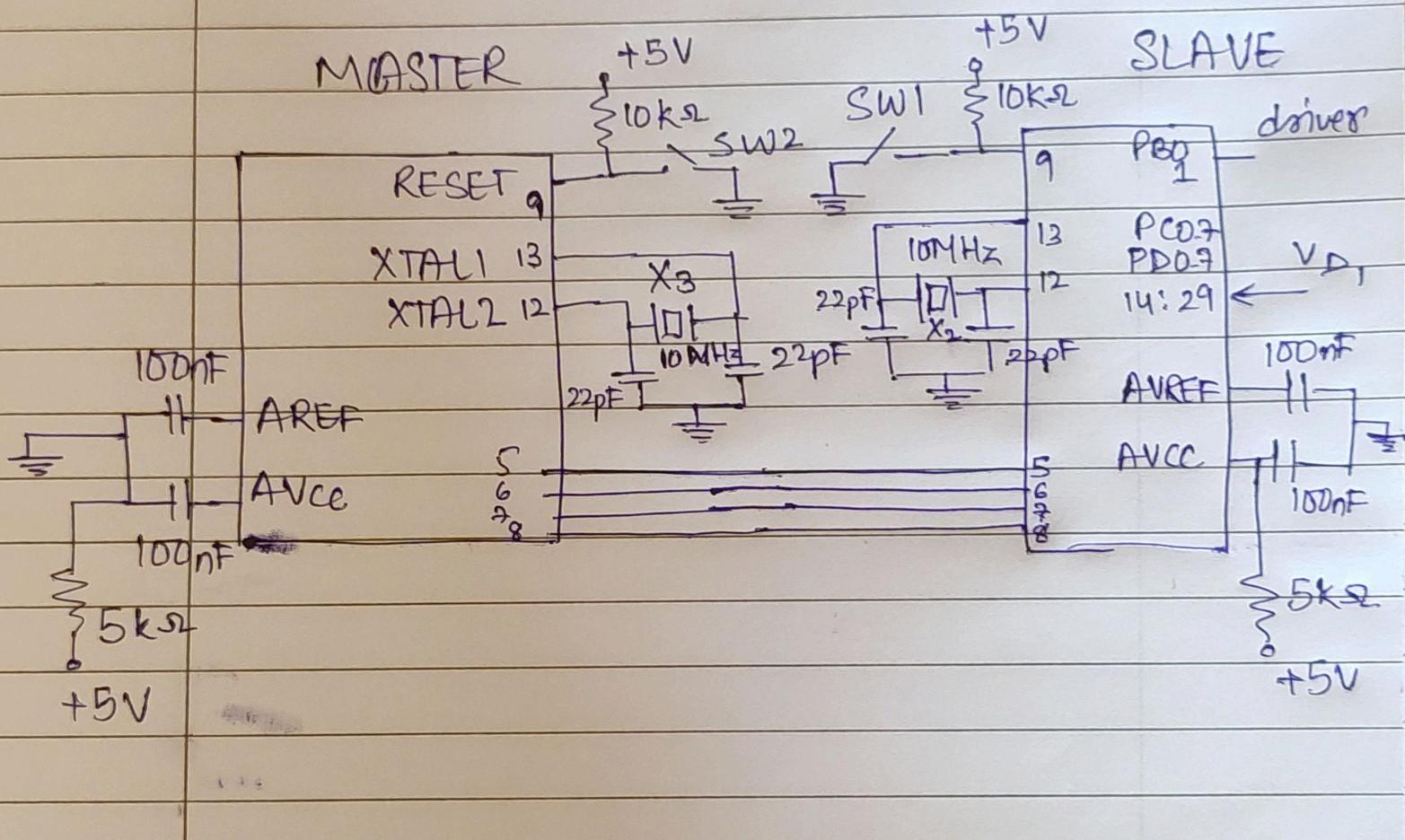
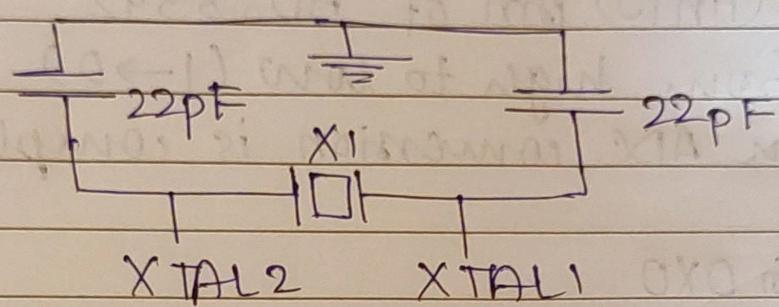


Fig. Connection of clocks  
(10 MHz clock for both controllers)



Q2. a. Slave ADC ISR routine (use interrupt driven data transfer).

Busy (Pin 15) pin of ADS8342 goes from high to low ( $1 \rightarrow 0$ ) when ADC conversion is complete.

CODE:

```
.ORG 0X00
    JMP Main
.ORG 0X02
    JMP EX0_ISR
```

; vector location for  
; External Interrupt 0. }.

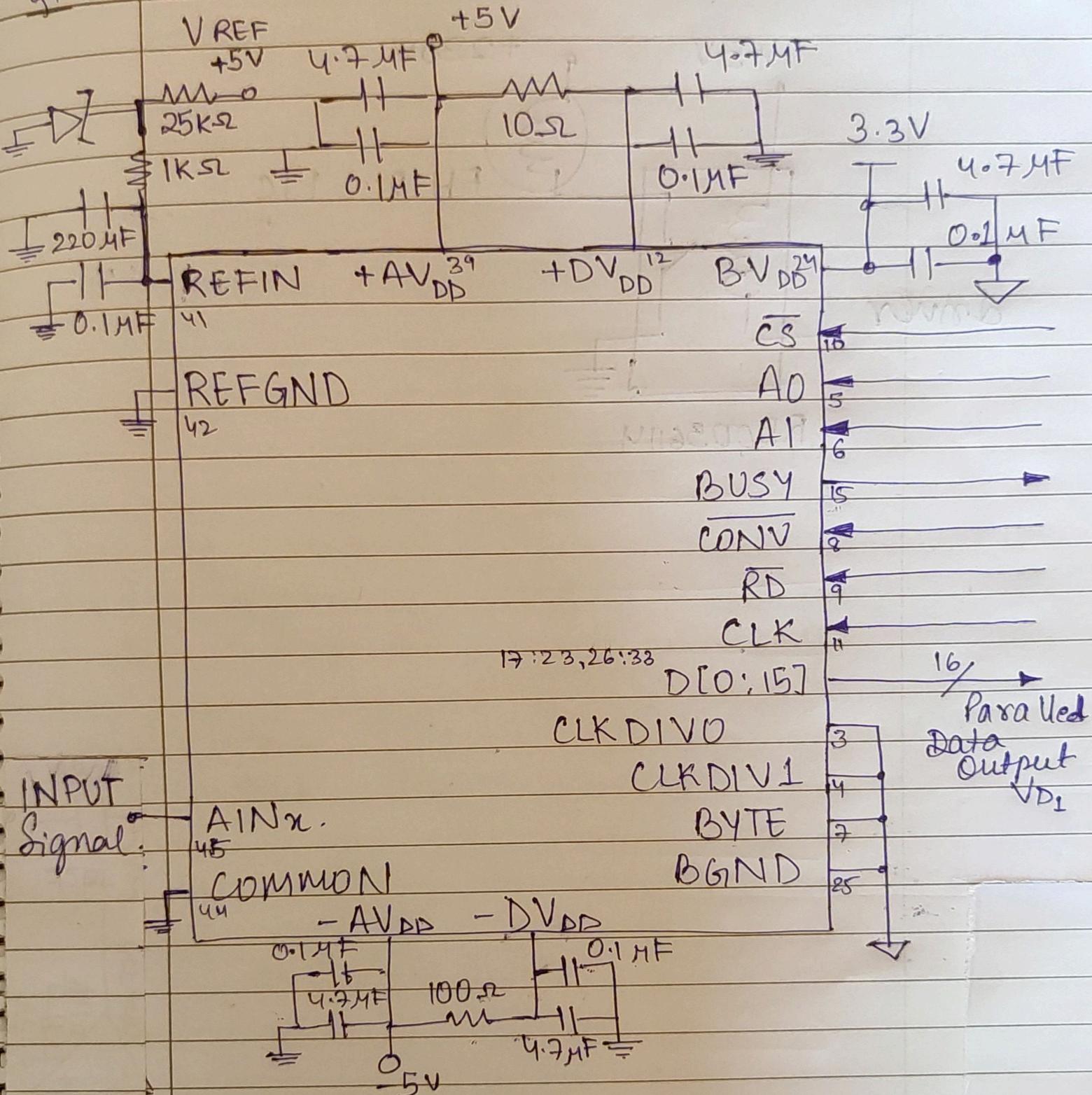
EX0\_ISR:

```
LDI R16,0           ; Make RD low
OUT PORTA,R16        ; store low byte of prev.?
MOV R24,R20          ; temp. value in R24
MOV R25,R21          ; store high byte of prev?
IN  R20,PORTB        ; store low byte of ADC?
                           ; output in R20
IN  R21,PORTC        ; store high byte of ADC?
                           ; output in R21
LDI R16,0xFF
OUT PORTA,R16        ; Make RD high?
```

CALL Detection
RET

; return?.

### Q1. c. ADC connection



Q1. f All pins of each controller needs to be connected and shown in table.

ADS8342 Pin:	Pin name:	Connection
45	AIN0	analog o/p of amplifier
44	COMMON	Ground
42	REFGND	Ground
41	REFIN	power supply
39	+AVDD	5V
42	+DVDD	5V
24	BVDD	3.3V
A:23, 26:33	D[0:15]	digital o/p
3	CLKDINO	Ground
4	CLKDIV1	Ground
7	BYTE	Ground
25	BAND	Ground

Q2. c. Delay routines to generate 1 min-delay

MVI C, 0AH

LOOP:

MVI D, 64H

LOOP1:

MVI E, 0DEH

LOOP2:

DCR E

JNZ LOOP2

DCR D

JNZ LOOP1

DCR C

JNZ LOOP

RET

{ return }.

Q2. d. ON-OFF control routine. ↗ after every delay.

.INCLUDE "M32DEF.INC"  
LDI R16, HIGH(RAMEND); { end of RAM? }  
OUT SPH, R16. { higher 8 bit copied to R16 }  
LDI R16, LOW(RAMEND)  
OUT SPL, R16 { lower 8 bit copied to R16 }  
SBI DDRB, 0. { PB0 → O/P Port }

BEGIN:

SBI PORTB, 0 { PB0 = 1 }  
RCALL DELAY  
CBI PORTB, 1 { PB0 = 0 }  
RCALL DELAY  
RJMP BEGIN { restart BEGIN func" by jumping to start of BEGIN }  
RJMP

DELAY:

LDI R16, 0

LDI R17, 0

LOOP1:

DEC R16 { decrease R16 }

BRNE LOOP1

DEC R17 { branch not equal }

BRNE LOOP1 { check R17 != 0 }

RET { return }

RJMP BEGIN. { return to BEGIN after DELAY func" ends }