

Name: Mansi Sodhani

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e.g. 170001Dept.: CSE
e.g. CSEIndian Institute of Technology Kanpur
CS637 Embedded and Cyber-Physical Systems

Homework Assignment 2

Deadline: October 13, 2023

Total: 50 marks

Problem 1. (10 points) Provide the state-space representation of the dynamics of a DC Motor. Assume that there is no additional load on the motor. Next, Design a Simulink model to capture the dynamics and simulate the model for an input PWM voltage signal with magnitude 1V, frequency 1 kHz and duty cycle 0.1. Assume that the kinetic friction of the motor is negligible. Take the values of the other parameters from Example 7.13 in [LS15]. Provide the plot showing how the angular velocity of the motor varies with time.

[LS15] Edward A. Lee and Sanjit A. Seshia, Introduction to Embedded Systems, A Cyber-Physical Systems Approach, Second Edition, <http://LeeSeshia.org>, ISBN 978-1-312-42740-2, 2015.

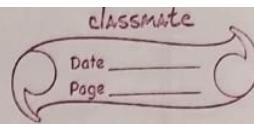
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Sol.1

let Angular Velocity of Motor be $\omega: R \rightarrow R$
 $V(t) = \text{Voltage}$, $i(t) = \text{Current}$, $R = \text{Resistance}$
 $K_b = \text{Back Electromagnetic force constant}$

$$V(t) = R [i(t) + L \frac{d}{dt} i(t)]$$

$$= R [i(t)] + L \frac{d}{dt} i(t) + K_b \omega(t)$$

$$\frac{d}{dt} i(t) = T(t) = K_T [i(t)] - \eta(\omega(t)) - T(t)$$

$K_T = \text{Torque const}$ $\eta = \text{Kinetic friction}$

$T = \text{Torque by Load}$

$$I = 3.88 \times 10^{-7} \quad R = 1.71 \Omega \quad K_b = 2.75 \times 10^{-4}$$

$$K_T = 5.9 \times 10^{-3} \quad \eta = 0 \quad T = 0 \quad L = 1.1 \times 10^{-4}$$

$$\dot{\omega}(t) = \frac{d}{dt} \omega(t) = \frac{K_T}{I} [i(t)] - \frac{\eta}{I} [\omega(t)] - \frac{T(t)}{I} \quad (1)$$

$$V(t) = R [i(t)] + K_b [\omega(t)] + L \frac{d}{dt} [i(t)]$$

The state space representation of dynamic DC motor

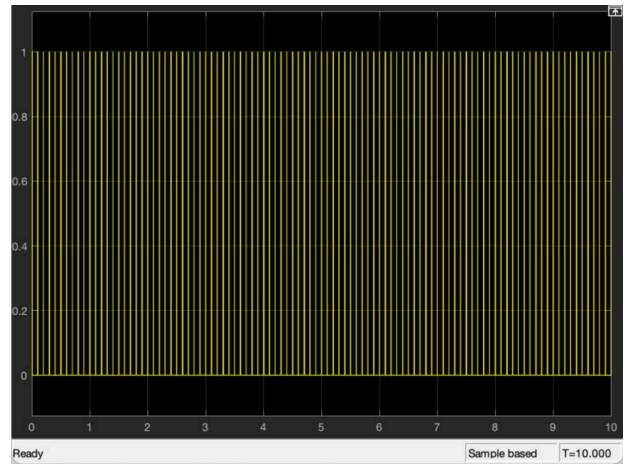
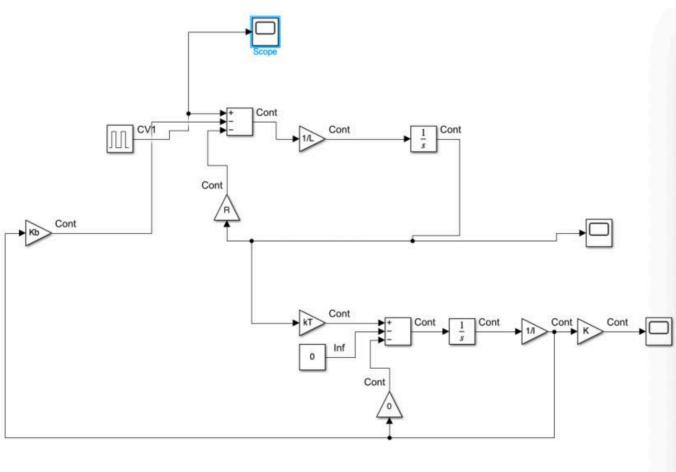
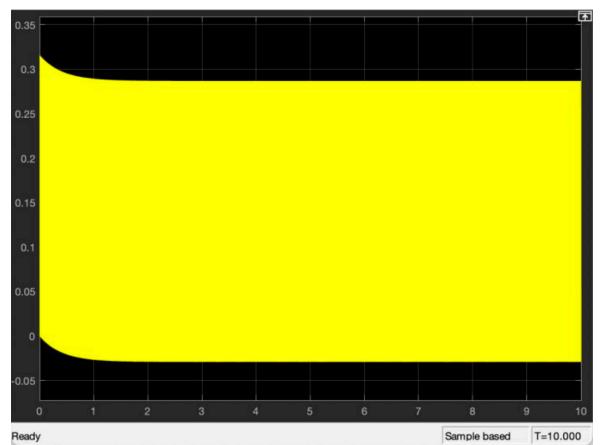
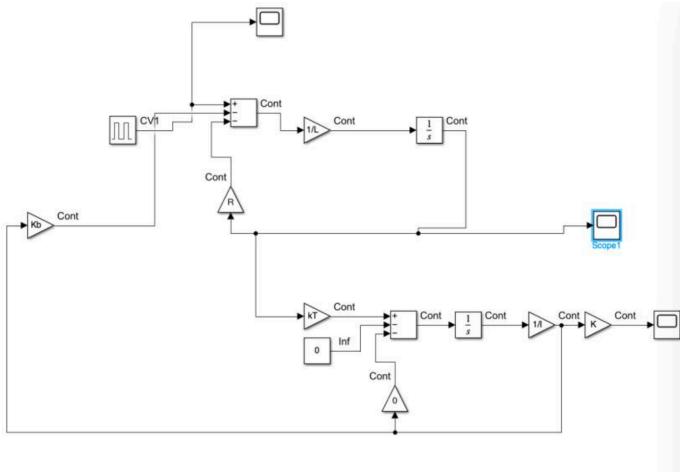
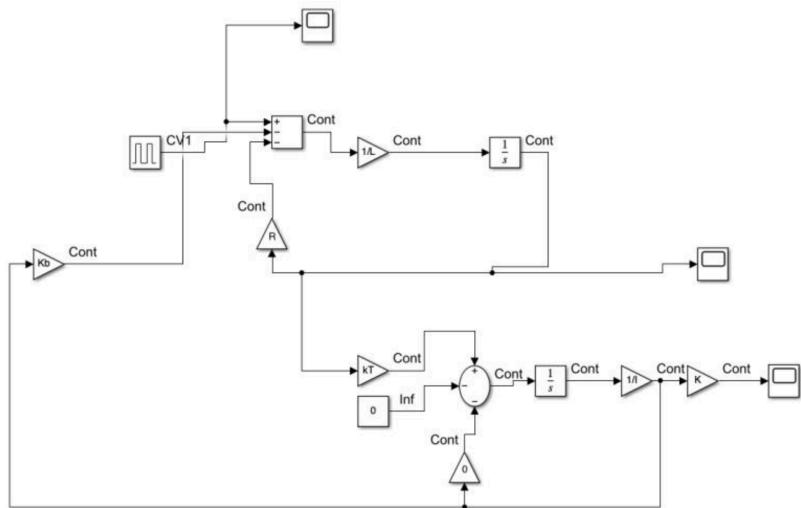
$$L \dot{i}(t) = V(t) - R [i(t)] - K_b [\omega(t)]$$

$$i(t) = \frac{V(t)}{L} - \frac{R}{L} [i(t)] - \frac{K_b}{L} [\omega(t)] \quad (2)$$

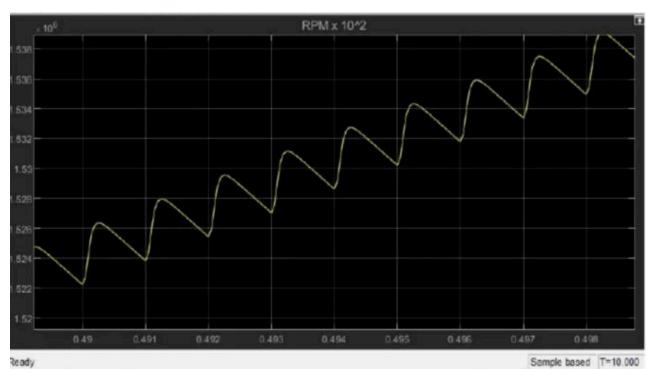
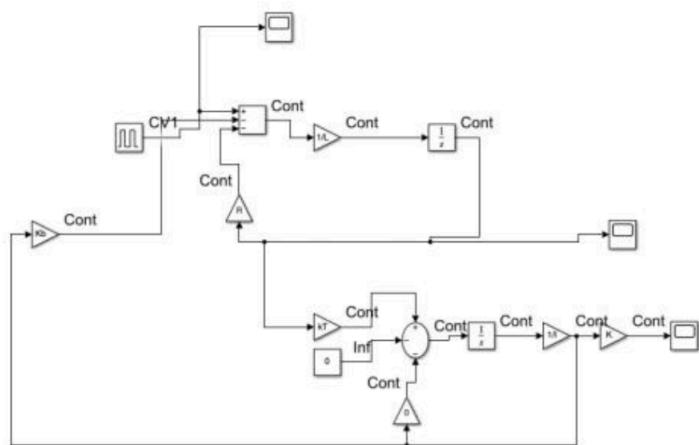
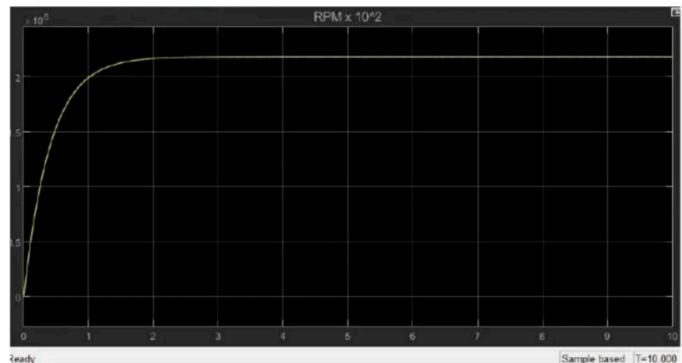
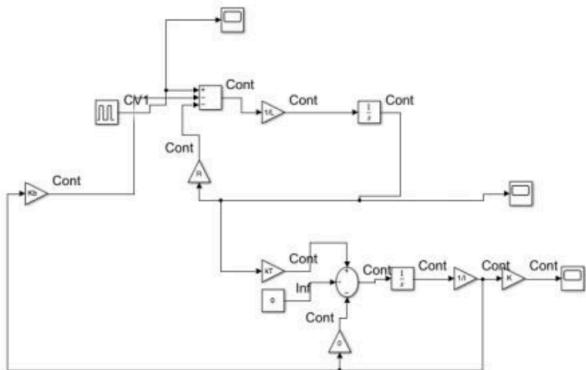
$$\begin{bmatrix} \dot{\omega}(t) \\ \dot{i}(t) \end{bmatrix} = \begin{bmatrix} -1 & K_T/I \\ -K_b/L & -R/L \end{bmatrix} \begin{bmatrix} \omega(t) \\ i(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 1/L \end{bmatrix} V(t)$$

$$y = \begin{bmatrix} 1, 0 \end{bmatrix} \begin{bmatrix} \omega(t) \\ i(t) \end{bmatrix}$$

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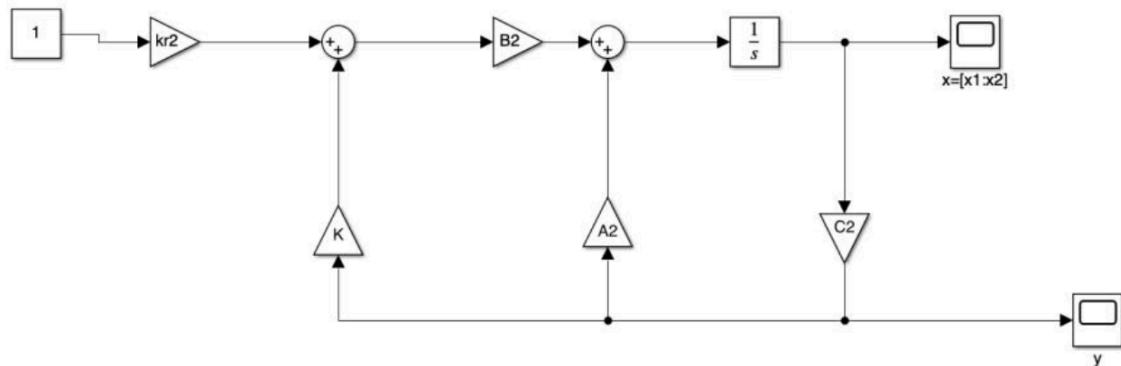
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Problem 2. (10 points) Consider the vehicle steering control problem in Example 6.4 in [AM09]. Assume that $k_1 = 1$, $k_2 = 1.6$, and $k_r = 1$. Model the control system in Simulink using double precision floating point arithmetic. Now replace the model of the controller with the ones that use 16 bit and 8-bit fixed-point arithmetic. In each case, determine the fixed-point data types precisely. Plot the difference between the first state for the floating-point controller and that for the fixed-point controllers. Generate code for both the floating point controller and the fixed-point controllers using different optimization options. Describe the steps you have followed for the code generation.

[AM09] K. J. Astrom and R. M. Murray. Feedback Systems: An Introduction for Scientists and Engineers. Princeton University Press, 2009.

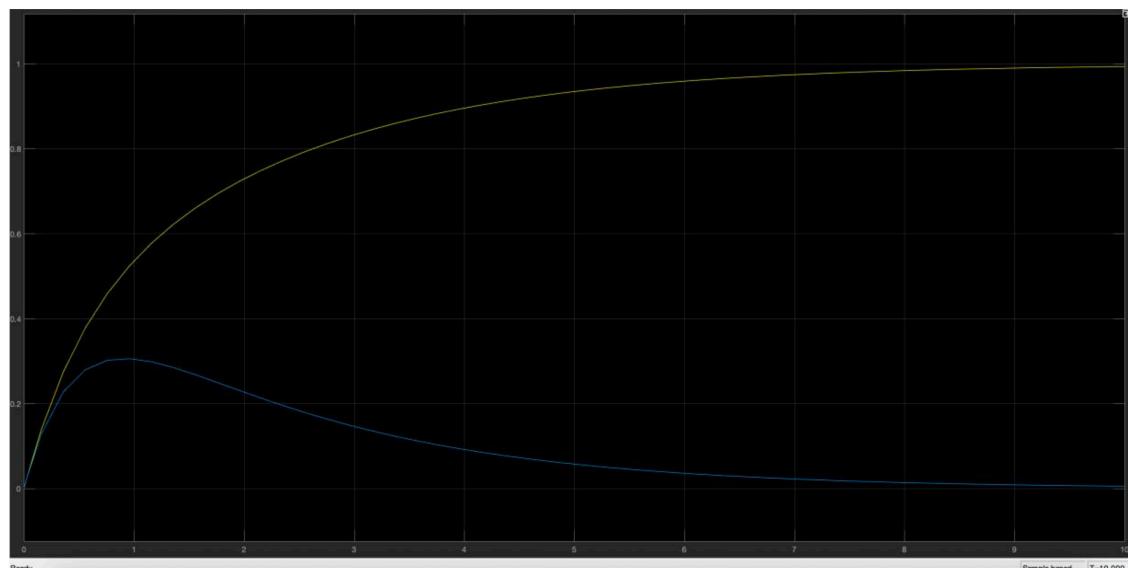
http://www.cds.caltech.edu/~murray/books/AM05/pdf/am08-complete_22Feb09.pdf.

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Double precision floating point arithmetic

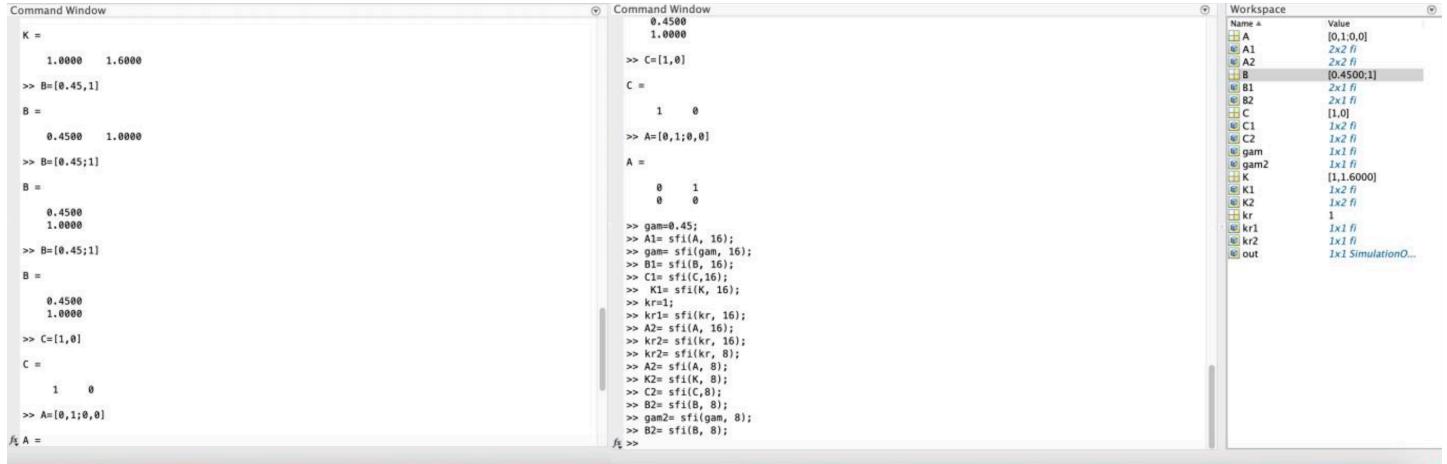
$$x = [x_1 : x_2]$$



y1



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Command Window

```

K =
    1.0000   1.6000
>> B=[0.45,1]
B =
    0.4500   1.0000
>> B=[0.45;1]
B =
    0.4500
    1.0000
>> B=[0.45;1]
B =
    0.4500
    1.0000
>> C=[1,0]
C =
    1     0
>> A=[0,1;0,0]
A =
    0     1
    0     0
>> gam=0.45;
>> A1=sfi(A, 16);
>> B1=sfi(gam, 16);
>> B2=sfi(B, 16);
>> C1=sfi(C,16);
>> K1=sfi(K, 16);
>> kr1=1;
>> krl=sfi(kr, 16);
>> A2=sfi(A, 16);
>> kr2=sfi(kr, 16);
>> kr2=sfi(kr, 8);
>> A2=sfi(A, 8);
>> K2=sfi(K, 8);
>> C2=sfi(C,8);
>> B2=sfi(B, 8);
>> gam2=sfi(gam, 8);
>> B2=sfi(B, 8);
f2>>

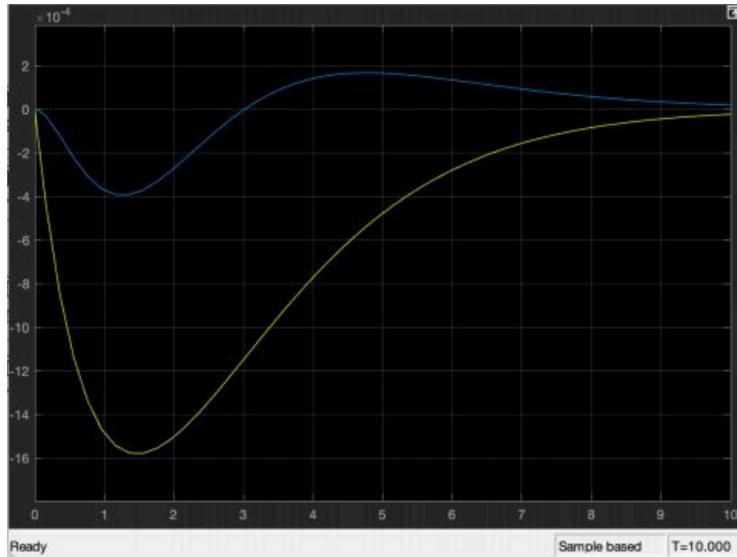
```

Workspace

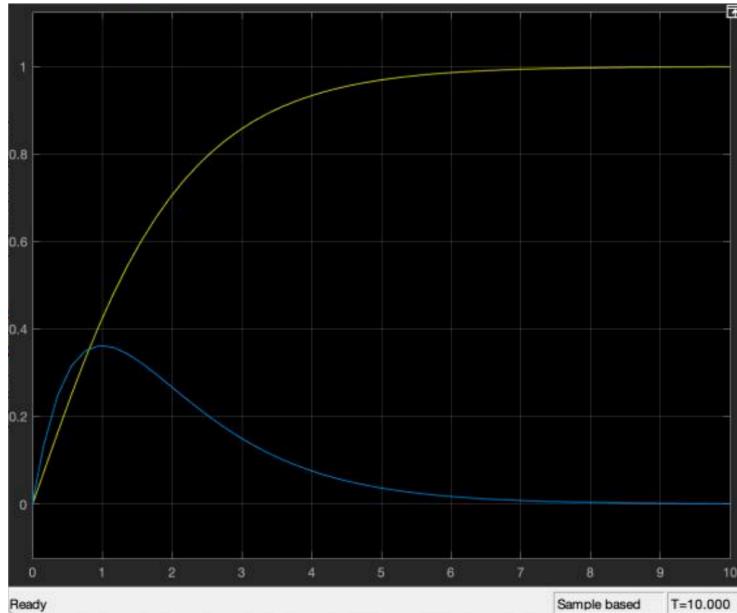
| Name | Type | Value |
|------|----------------------|-----------|
| A | 2x2 fi | [1,0;0,1] |
| A1 | 2x2 fi | [2x2 fi] |
| B | [0.4500;1] | 2x1 fi |
| B1 | 2x1 fi | [0.4500] |
| C | [1,0] | 1x2 fi |
| C1 | 1x2 fi | [1,0] |
| C2 | 1x2 fi | [0,1] |
| gam | 1x1 fi | 0.4500 |
| gam2 | 1x1 fi | 0.4500 |
| K | [1,1.6000] | 1x2 fi |
| K1 | 1x2 fi | [1,1] |
| K2 | 1x2 fi | [1,0] |
| kr | 1 | 1x1 fi |
| kr1 | 1x1 fi | 1 |
| kr2 | 1x1 fi | 1 |
| out | 1x1 SimulationObject | |

Double of the x in floating controller and fixed point controller

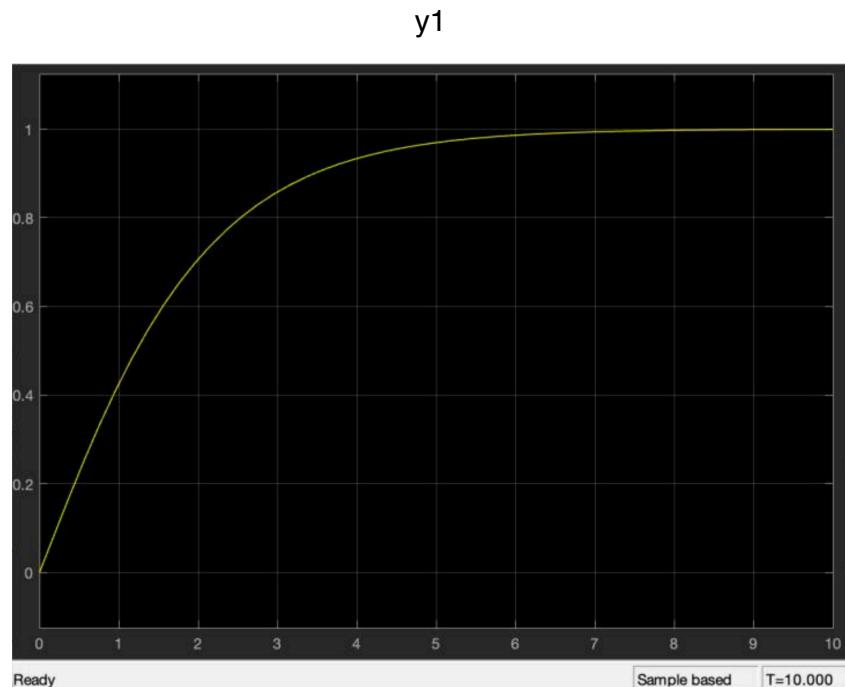
Scope



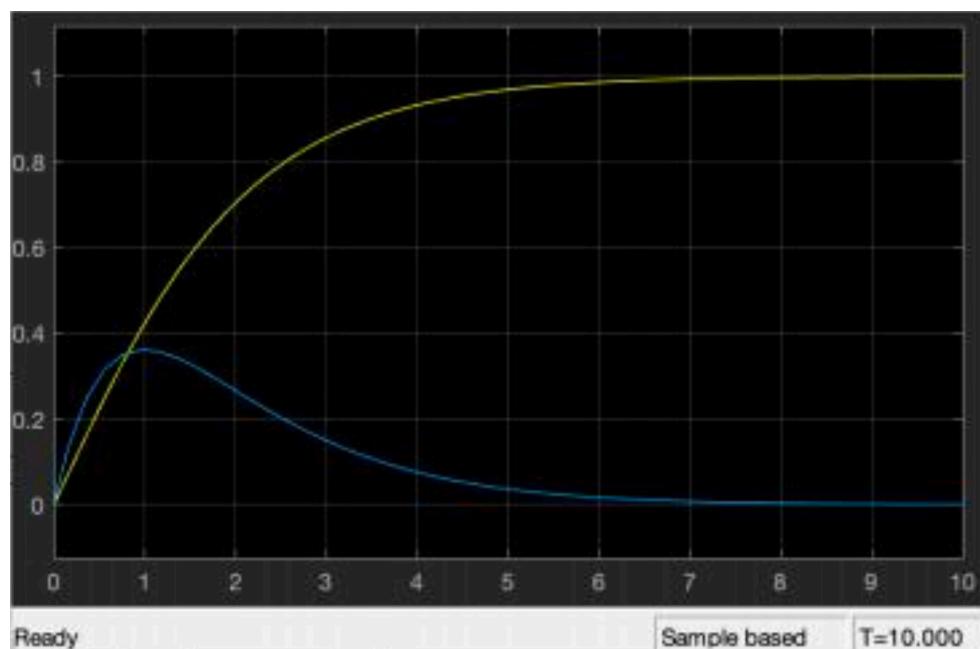
8 bit fixed point arithmetic

 $x = [x1:x2]1$ 

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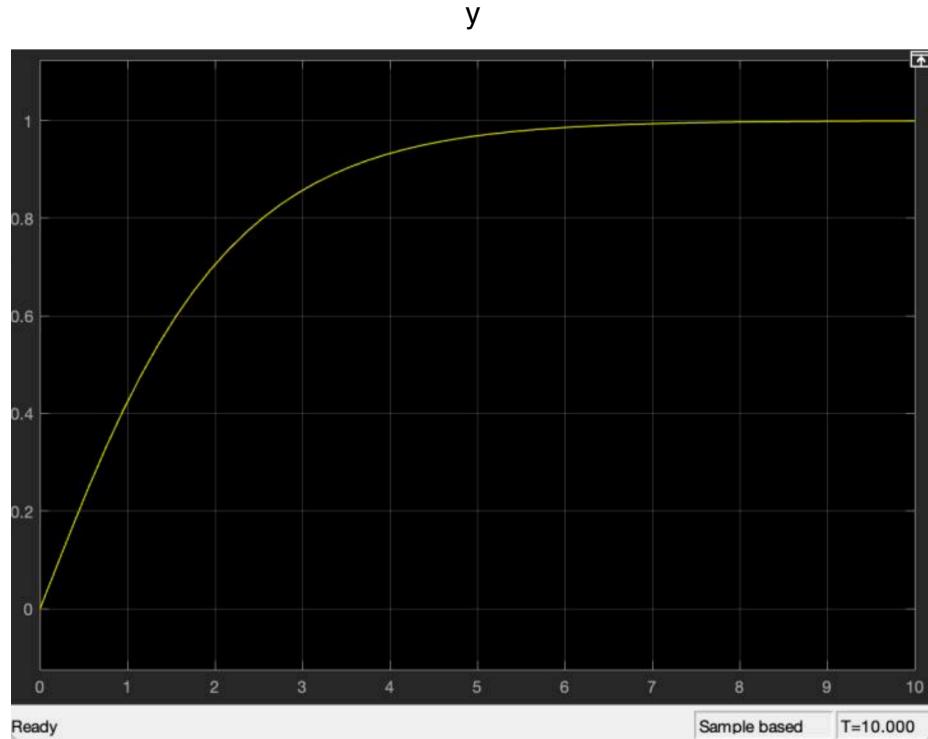
16 bit fixed point arithmetic

 $x = [x_1 : x_2]$ 

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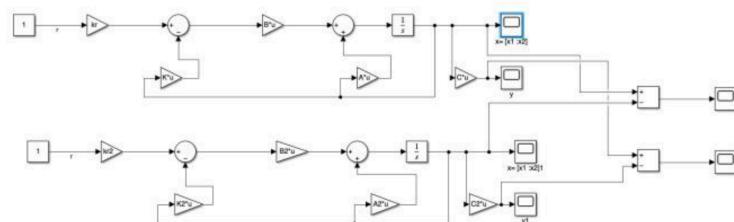
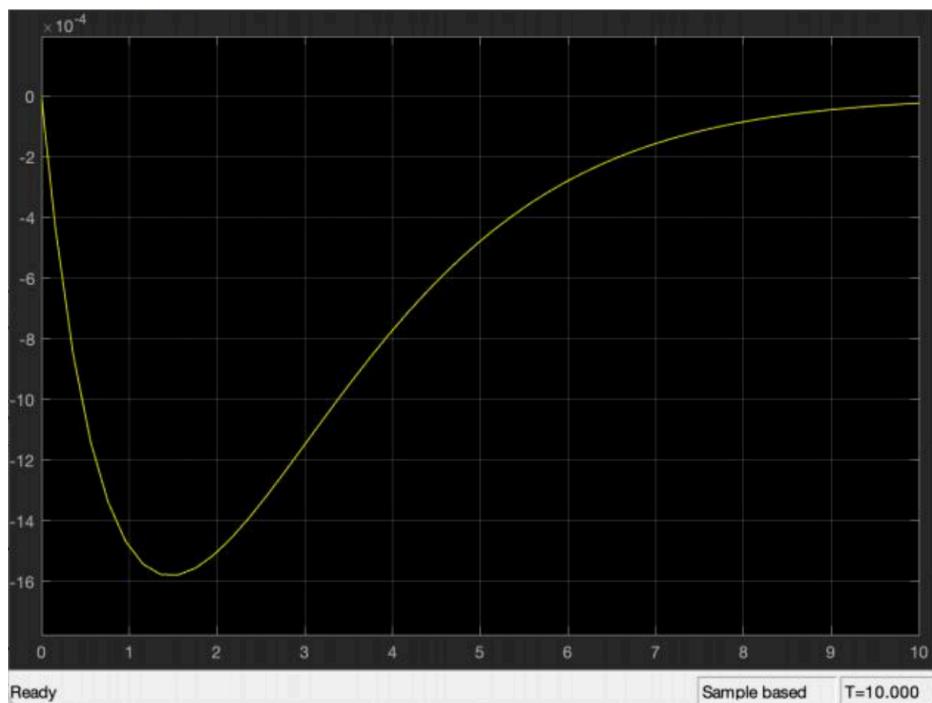
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Double of the y in floating controller and fixed point controller

Scope1



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Problem 3. (10 points) Work out Problem 1 in the Exercises of Chapter 9 in [LS15].

[LS15] Edward A. Lee and Sanjit A. Seshia, Introduction to Embedded Systems, A Cyber-Physical Systems Approach, Second Edition, <http://LeeSeshia.org>, ISBN 978-1-312-42740-2, 2015.

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Sol 3.

Each block stored in the cache is of size 8 bytes. Since each int is 4 byte wide. data[0] and data[1] will lie in same cache block.
 Similarly data[2] and data[3] and so on.

If N = 16

The first loop accesses data[0] to data[15]. Each pair of elements (e.g., data[0] and data[1]) fit in the same cache block. Each time we access a block for the first time, there is a cache miss. After loading a block, both elements in that block are cached. The second loop also accesses data[0] to data[15] again. Since the data is already cached from the first loop, there will be no additional cache misses in the second loop.

The first loop results in 8 cache misses. The second loop results in 0 cache misses.

Total cache misses = 8.

If N = 32,

The first loop accesses data[0] to data[31]. For the first 8 blocks, it will behave the same way as in the previous case, resulting in 8 cache misses. However, after that, the cache will start evicting blocks because we only have 8 blocks in total (direct-mapped). As we load blocks 9-16, they will replace the first 8 blocks, causing additional cache misses. Thus, all 16 blocks will result in cache misses in the first loop. When accessing the data array again, all previously loaded blocks from the first loop would have been evicted due to the direct-mapped nature of the cache. Therefore, the second loop will also result in 16 cache misses, as all blocks will be reloaded. The first loop results in 16 cache misses. The second loop results in 16 cache misses.

Total cache misses = 32.

If N = 16 on a 2-Way Set-Associative Cache,

The first loop accesses data[0] to data[15]. Each integer now occupies its own block. Since we have 16 blocks available and 16 elements to store, each element will occupy one block in the cache, and there will be no evictions during the first loop. Therefore, for N = 16, the first access to each element will result in a cache miss. Hence, there will be 16 cache misses in total during the first loop. The second loop accesses data[0] to data[15] again. Since all data was already loaded in the first loop and the cache can hold all elements (16 blocks), there will be no cache misses in the second loop. The first loop results in 16 cache misses. The second loop results in 0 cache misses.

Total cache misses = 16.

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Problem 4. (10 points) Work out Problem 3 in the Exercises of Chapter 12 in [LS15].

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Sol. 4

(a) RM scheduler is a fixed priority primitive scheduling algo. Tasks with shorter periods, are given higher priority.
Here Task 1 gets higher priority.

$$\begin{array}{|c|c|c|c|c|c|c|c|} \hline 1 & 2 & 1 & 2 & 1 & | & | & | \\ \hline 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 \\ \hline \end{array} \quad u = e_1 + \frac{e_2}{p_1} = \frac{1}{2} + \frac{1}{3} = 0.83$$

$$\text{Utilisation bound} = n \left(\frac{1}{2^n} - 1 \right) = 2 \left(\frac{1}{2} - 1 \right) = 0.828$$

$u > 0.828$ but it still produces a feasible schedule.

$$(b) i) e'_1 = 1 + \Delta t \quad (\text{increase } e_1 \text{ to } e'_1)$$

\because Task 1 is higher priority, it will execute from $t=0 \rightarrow 1 + \Delta t$ & also execute from $t=2 \rightarrow 3 + \Delta t$

for $t < 3$, task 2 gets executed only for $t + \Delta t$ time i.e. not completed.

Hence this schedule is not feasible.

$$e'_2 = 1 + \Delta t \quad (\text{increase } e_2 \text{ to } e'_2)$$

Task 1 will execute from $t=0 \rightarrow 1$ & $t=2 \rightarrow 3$

for $t < 3$, task 2 gets executed for 1 unit time i.e. not completed.

Hence this schedule is not feasible.

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ii) Reduce p_1 to 1.5 gives following schedule which is feasible.

→ Pattern Repeats

| | | | | |
|---|---|-----|---|-----|
| | | | | |
| 0 | 1 | 1.5 | 2 | 2.5 |

Reducing p_1 to less than 1.5 will result in 3rd execution of Task 1 to start execution before $t < 3$. Assume $p_1 = 1.5 - \alpha t$ then Task 2 will get 1st time of execution for $t < 3$ & hence miss the deadline.

This is not feasible.

p_1 can't be reduced to less than 1.5.

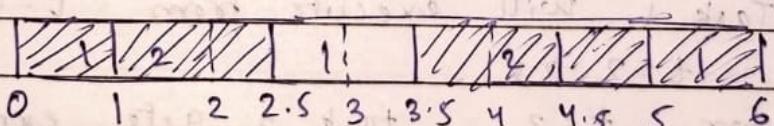
Reducing p_2 to 2 will result in feasible schedule.

→ Pattern Repeats

| | | | | | | |
|---|---|---|---|---|---|---|
| 1 | 2 | 1 | 2 | 1 | 2 | 1 |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 |

So p_2 can't be reduced further because it's already at 100% utilisation.

c) EDF scheduler:



∴ deadline of all tasks are met
feasible schedule $u = 100\%$

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Problem 5. (10 points) Work out Problem 6 in the Exercises of Chapter 12 in [LS15].

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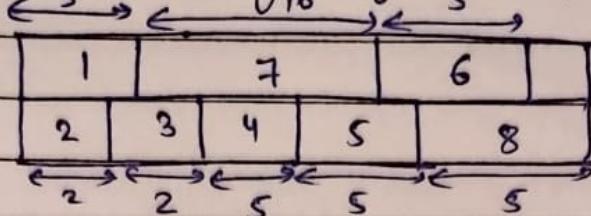
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Sol. 5

(a)

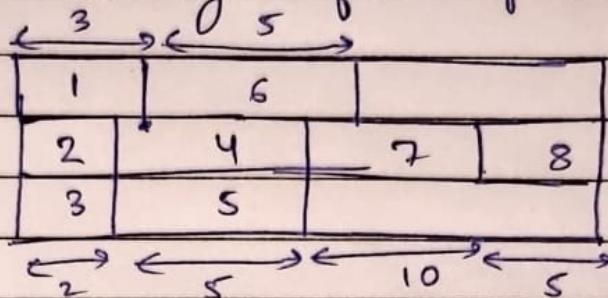
Scheduling of 2 processors



$$\text{Total Makespan} = 19$$

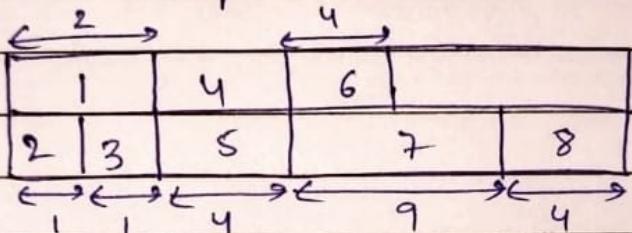
(b)

Scheduling of 3 processors



$$\text{Total Makespan} = 22 > \text{Total Makespan (a)}$$

(c)



$$\text{Total Makespan} = 19 = \text{Total Makespan (a)}$$

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