Slovenská technická univerzita v Bratislave
Fakulta informatiky a informačných technológií

FIIT-3028-52076

**Martin Dinja**

# Simulator for instruction pipelining

Bakalárska práca

Vedúci práce: Ing. Ján Hudec PhD.

May 2025

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Študijný program: Software Engineering

Študijný odbor: 9.2.5 Software Engineering

Miesto vypracovania: Institute of Informatics and Software Engineering, FIIT STU, Bratislava

Vedúci práce: Ing. Ján Hudec PhD.

May 2025

# Declaration

I hereby declare that I have completed this work independently, based on consultations and using the cited literature.

In Bratislava, 21.05.2025

.....

Martin Dinja

# Acknowledgment

I would like to express my gratitude to my supervisor, Ing. Ján Hudec PhD., for his guidance, support, and patience throughout the course of this thesis.

# Annotation

Slovak University of Technology Bratislava
FACULTY OF INFORMATICS AND INFORMATION TECHNOLOGIES
Degree Course: Software Engineering

Author: Martin Dinja
Diploma Thesis: Simulator for instruction pipelining
Supervisor: Ing. Ján Hudec PhD.
May 2025

The aim of this thesis is to address the problem of outdated and difficult to use simulators for instruction pipelining by introducing a new simulator. It is designed to be used by students and teachers to better understand the concept of instruction pipelining and its inner workings. This thesis analyzes the instruction pipelining concept, the existing simulators, their shortcomings, and proposes a new simulator that addresses those shortcomings, and describes its implementation. The new simulator is implemented using modern web technologies and is designed to be user friendly and easy to use. The simulator is evaluated by students and teachers to determine its usability and effectiveness in teaching and learning instruction pipelining.

# Anotácia

Slovenská technická univerzita v Bratislave
FAKULTA INFORMATIKY A INFORMAČNÝCH TECHNOLÓGIÍ
Študijný program: Informatika

Autor: Martin Dinja
Bakalárska práca: Simulator na prúdove spracovanie inštrukcií
Vedúci bakalárskej práce: Ing. Ján Hudec PhD.
Máj 2025

Cieľom tejto práce je vyriešiť problém zastaraných a ťažko použiteľných simulátorov pre prúdove spracovanie inštrukcií zavedením nového simulátora. Je navrhnutý tak, aby ho mohli používať študenti a učitelia na lepšie pochopenie koncepcie prúdoveho spracovania inštrukcií a jeho vnútorného fungovania. Táto práca analyzuje koncept prúdoveho spracovania inštrukcií, existujúce simulátory a ich nedostatky. Navrhuje nový simulátor, ktorý tieto nedostatky rieši, a opisuje jeho implementáciu. Nový simulátor je implementovaný pomocou moderných webových technológií a je navrhnutý tak, aby bol užívateľsky prívetivý a ľahko použiteľný. Simulátor je hodnotený študentmi a učiteľmi s cieľom určiť jeho použiteľnosť a účinnosť pri výučbe a učení sa pipelingu inštrukcií.

# Contents

**1 Introduction** **1**

**2 Analysis** **5**

2.1 Instruction Pipelining . . . . . 5

2.1.1 Introduction . . . . . 5

2.1.2 Instruction Pipeline Stages . . . . . 6

2.1.3 Pipeline Hazards . . . . . 6

2.1.3.1 Structural Hazards . . . . . 7

2.1.3.2 Data Hazards . . . . . 7

2.1.3.3 Control Hazards . . . . . 8

2.1.4 Pipeline Stalls . . . . . 8

2.1.5 Pipeline Performance Metrics . . . . . 8

2.2 Existing Solutions . . . . . 9

**3 Solution Proposal** **1**

**4 Implementation** **5**

**5 Solution Verification** **7**

**6 Conclusion** **11**

6.1 Summary . . . . . 11
6.2 Future Work . . . . . 13

**A First Appendix** **27**

**B Contents of Included CD–ROM** **29**

# Chapter 1

# Introduction

Instruction pipelining is an intrestingly simple concept... But to truly understanding this idea of parallelism can be challenging. It feels like reading music without ever hearing a song. The flow, the stalls, the hazards—they were words without a melody. And many tools that try to help with visualizing these notes are outdated in today's day and age. This thesis was born out of a desire to transform that silence into a beautiful symphony, crafting an instrument that would allow learners to not just see, but experience the song of instruction pipelining.

In contrast to how a non pipelined processor works, a pipelined processor executes multiple instructions simultaneously. One at each stage of the pipeline. This allows for a higher throughput of instructions, but also introduces a new set of challenges.

The problem is that there is no modern, user-friendly tool that allows for the visualization of instruction pipelining in a way that is easy to understand. Most tools are either outdated, or too complex to use, which makes it difficult for students to learn about this interesting topic.

To bridge the gap. This thesis aims to analyze existing solutions, identify their limitations, and propose a comprehensive solution in the form of a web-based instruction pipeline simulator The paper is organized as follows: Chapter 2 provides an analysis of existing solutions, Chapter 3 presents the proposed solution, Chapter 4 describes the implementation of the solution, Chapter 5 discusses the verification of the solution, and Chapter 6 concludes the paper with a summary and future work.

# Chapter 2

# Analysis

## 2.1 Instruction Pipelining

### 2.1.1 Introduction

In the 1970s and 1980s in response to the increasing complexity of CISC(Complex Instruction Set Computer) processors researchers realized that simplifying the instruction set could lead to better performance. This insight is how the first RISC(Reduced Instruction Set Computer) projects were developed[1]. And almost simultaneously, the concept of pipelining was introduced. Pipelining is a method used to enhance a processor's throughput by overlapping the execution phases of multiple instructions. By dividing the execution of an instruction into several stages and executing multiple instructions concurrently, the processor can handle several instructions simultaneously, thereby increasing its throughput[3]. Figure 2.1 illustrates the concept of pipelining.

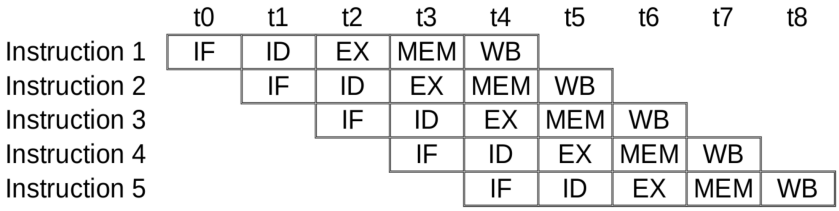


Figure 2.1: Pipelining

### 2.1.2 Instruction Pipeline Stages

The classical RISC pipeline consists of five stages: instruction fetch, instruction decode, execute, memory access, and write-back [6].

- **Instruction Fetch (IF)**: Fetches the instruction from memory using the program counter, which is then incremented.
- **Instruction Decode (ID)**: Decodes the instruction to determine the operation and fetches operands from the register file.
- **Execute (EX)**: Performs the operation on the fetched operands.
- **Memory Access (MEM)**: Accesses memory for load/store instructions; otherwise, bypassed.
- **Write-back (WB)**: Writes the result back to the destination register.

[2]

### 2.1.3 Pipeline Hazards

A hazard is a condition that occurs when the pipeline cannot execute the next instruction in the cycle. There are three types of hazards: structural, data, and control hazards.[3]

#### 2.1.3.1 Structural Hazards

Structural hazards occur when the hardware cannot support the combination of instructions in the pipeline. For example, if two instructions require the same hardware resource, such as the memory unit[4]. This stalls the pipeline or corrupts a result.[5]

#### 2.1.3.2 Data Hazards

Data hazards occur when an instruction depends on the result of a previous instruction. There are three types of data hazards: read-after-write (RAW), write-after-read (WAR), and write-after-write (WAW).

- **Read-After-Write (RAW)**: Occurs when an instruction reads a register before a previous instruction writes to it.
  - **Solution**: Use techniques such as forwarding (or bypassing), where we add extra paths to the pipeline to allow the result of an instruction to be forwarded to the next instruction that needs it.
- **Write-After-Read (WAR)**: Occurs when an instruction writes to a register before a previous instruction reads from it.
  - **Solution**: This hazard is rare in RISC architectures due to the use of register renaming, which ensures that each instruction has a unique destination register.
- **Write-After-Write (WAW)**: Occurs when two instructions write to the same register.
  - **Solution**: Similar to WAR hazards, register renaming can be used to avoid WAW hazards by ensuring that each write operation targets a unique register.

[4]

#### 2.1.3.3 Control Hazards

Control hazards occur when the pipeline makes a decision based on a previous instruction that has not yet completed. For example, a branch instruction may change the program counter before the next instruction has been fetched. This can lead to incorrect execution of instructions.[4]

### 2.1.4 Pipeline Stalls

Pipeline stalls occur when the pipeline cannot proceed due to a hazard. Stalls can be resolved by inserting no-operation (NOP) instructions or by forwarding data to the next instruction. However, these solutions can reduce the performance of the pipeline.[4]

### 2.1.5 Pipeline Performance Metrics

There are several metrics used to evaluate the performance of a pipeline, including throughput, speedup, and efficiency.

- **Throughput**: The number of instructions completed per unit of time.
- **Speedup**: The ratio of the execution time of a non-pipelined processor to the execution time of a pipelined processor.
- **Efficiency**: The ratio of the speedup to the number of pipeline stages.
- **IPC (Instructions Per Cycle)**: The average number of instructions executed per clock cycle.
- **CPI (Cycles Per Instruction)**: The average number of clock cycles required to execute an instruction.

- **Cycles Per Second (CPS)**: The number of clock cycles per second.
- **Clock Rate**: The frequency at which the processor operates.
- **Latency**: The time taken to complete a task.
- **Throughput**: The number of tasks completed per unit of time.
- **Bandwidth**: The amount of data that can be transferred in a given time.
- **Response Time**: The time taken to respond to a request.

[4]

## 2.2 Existing Solutions

# Chapter 3

# Solution Proposal

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# Chapter 4

# Implementation

# Chapter 5

# Solution Verification

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# Chapter 6

# Conclusion

## 6.1 Summary

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## 6.2 Future Work

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# Appendix A

# First Appendix

# Appendix B

# Contents of Included CD–ROM

CD–ROM included to the thesis contains following files:

- `/file1` — First file
- `/file2` — Second file