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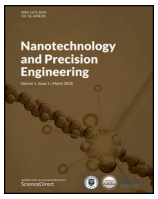

Surface defects in 4H-SiC homoepitaxial layers

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ABSTRACT

Although a high-quality homoepitaxial layer of 4H-silicon carbide (4H-SiC) can be obtained on a 4° off-axis substrate using chemical vapor deposition, the reduction of defects is still a focus of research. In this study, several kinds of surface defects in the 4H-SiC homoepitaxial layer are systemically investigated, including triangles, carrots, surface pits, basal plane dislocations, and step bunching. The morphologies and structures of surface defects are further discussed via optical microscopy and potassium hydroxide-based defect selective etching analysis. Through research and analysis, we found that the origin of surface defects in the 4H-SiC homoepitaxial layer can be attributed to two aspects: the propagation of substrate defects, such as scratches, dislocation, and inclusion, and improper process parameters during epitaxial growth, such as in-situ etch, C/Si ratio, and growth temperature. It is believed that the surface defects in the 4H-SiC homoepitaxial layer can be significantly decreased by precisely controlling the chemistry on the deposition surface during the growth process.

1. Introduction

Owing to the recent progress in the growth and device technologies of wide-bandgap semiconductors, these materials are now considered realistic candidates for advanced power devices that outperform Si-based devices. Among these materials, silicon carbide (SiC), due to its wide bandgap, high electric breakdown field, high thermal conductivity, and high carrier saturation velocity, is a potential semiconductor material that can be extensively applied in different fields with high power, high voltage, high temperature, and high frequency.[1] In addition, SiC has the following advantages: p- and n-type doping control in a wide range by either in-situ doping during growth or ion implantation, availability of a native oxide, and relatively long carrier lifetimes for bipolar devices due to its indirect band structure.[2,3]

Since the first production of SiC Schottky barrier diodes in 2001 and SiC power metal–oxide–semiconductor field-effect transistors (MOSFETs) in 2010, the market of SiC unipolar power devices (mainly 1 kV class) has gradually been growing, demonstrating remarkable energy efficiency in real electronic systems.[4,5] Currently, the commercialized 650–1700 V SiC Schottky barrier diodes have been widely applied in many fields, such as consumer electronics with power adaptors and battery chargers.[6,7] SiC MOSFETs have been used in a few systems in the industrial filed, but they are still at the beginning stage of development. Moreover, high-voltage and high-current devices are still being developed because of the inhibitions of factors, such as high cost, poor quality of epitaxial wafers, and low process technology. In recent years, we have witnessed a growing market of high-voltage particle accelerators for medical applications, where the voltage of power supply reaches 3.3–30 kV. Generally, the device structures are realized by epitaxial growth on 4H-SiC substrates, so high-quality epitaxial wafers are essential for the development of high-performance power electronic devices.[8] In the past 10 years, the growth process of the 4H-SiC homoepitaxial layer has been significantly improved. The introduction of chloride precursors, epitaxial growth on large-area substrates with low defect densities, improvement of the surface morphology, the understanding of the chemical vapor deposition (CVD) reactions, and epitaxial mechanisms by advanced simulations are just the main recent research areas and development progress obtained in the 4H-SiC homoepitaxial process.[9–11] Aside from these, the high cost of 4H-SiC is an important problem, and its price is 4–6 times that of silicon devices. Indeed, for a 1.2 kV Schottky diode, the cost of this process reaches 25%–30% of the total device cost. Therefore, the cost reduction of 4H-SiC homoepitaxial layer is a future research focus.

In this work, several common surface defects in the 4H-SiC homoepitaxial layer are reported. These surface defects are discussed, including the origin, morphology feature, characterization, and reduction method. The findings show that a low surface defect density of the 4H-SiC epitaxial layer can be obtained by carefully controlling the surface chemistry of the CVD process.

2. Growth process

4H-SiC homoepitaxial wafers were grown on 6-in. 4° off-axis Si-face 4H-SiC substrates through the CVD method.[12] Commercial-production-grade 6-in. 4H-SiC substrates were used. The structure of the epitaxial

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wafer is shown in Fig. 1. Silane (SiH_4), trichlorosilane (TCS), ethylene (C_2H_4), and propane (C_3H_8) are usually used as silicon precursors and carbon precursors during growth process. The carrier gas was hydrogen (H_2), and the n-type doping gas was nitrogen (N_2).[13] The growth temperature and pressure are 1500–1650 °C and 50–150 mbar, respectively. Fig. 2 shows the process sequence used for the 4H-SiC homoepitaxial growth process. The growth process of 4H-SiC homoepitaxial wafers considers the ramp temperature, in-situ etch, epitaxial growth, and cool-down, as shown in Fig. 2. In-situ etching was primarily performed before the drift layer growth using pure H_2, HCl/H_2, hydrocarbon/H_2, or SiH_4/H_2 at high temperatures of 1500–1650 °C.[13,14] The purpose of in-situ etching is to remove the subsurface damage due to substrate polishing and to obtain regular step structures. The proper process parameter of the drift layer growth is extremely important to obtain high-quality epitaxial wafers. These parameters include the growth temperature, pressure, C/Si ratio, and Cl/Si ratio. The C/Si ratio is an extremely important parameter, and the good surface morphology is obtained under a fixed range. When the C/Si ratio is too low, the surface suffers from the formation of severe macrosteps and Si droplets. By contrast, surface morphological defects, such as triangle defects, are easily generated when the C/Si ratio is too high.[2,15]

3. Defects in the 4H-SiC epitaxial layer

The drift layer, as an important part of power electronic devices, directly influences the performance of devices. Thus, it is very important that a high-quality drift layer can be obtained for the development of high-performance power electronic devices. Currently, the quality of the epitaxial layer is evaluated by two parameters: uniformity and defect density of the epitaxial layer. The distribution of the breakdown voltage of devices in wafer depends on the uniformity of the epitaxial wafer with thickness and doping concentration, and the typical values of uniformity for the thickness and doping concentration are not more than 1.5% and 6.0%, respectively. The thickness of the epitaxial layer was determined through a Fourier transform infrared spectrometer (Thermo Scientific, Nicolet iS50), and the doping concentration was obtained through a capacitance–voltage measurement using a Hg Schottky contact (Semilab Corp., MCV-530). The edge exclusion is 5 mm in the measurement process.

The defect in the epitaxial layer has a negative effect on the performance of SiC power electronic devices, such as low breakdown voltage, high leakage current, and poor stability. Morphological defect distribution was measured and counted using an inspection tool (LaserTec Co., SICA88) or the same precision-level inspection tool. Meanwhile, the surface defect density of the 4H-SiC epitaxial layer can be carefully controlled at approximately 1 cm^{-2}. Although the quality of the current 4° off-axis 4H-SiC epitaxial layers has been obviously improved in recent years, they still cannot satisfy the requirements of high-voltage devices above 6.5 kV due to their extremely low yield. Thus, further defect reduction in epitaxial layers is still one of the research focuses. The common morphological defects in the epitaxial layer include triangles, carrots, pits, step bunching, stacking faults, dislocations, downfalls, and downfall triangles, and these defects have different influences on the performance of the device.[16,17] The defect origin of the epitaxial layer can be divided into two aspects. First, the defect is generated during the epitaxial process, or the so-called process-induced defect. Second, some defects come from the substrate, or the so-called extended defects. In the paper, several morphological defects are discussed to decrease the defect density in the 4H-SiC epitaxial layer.

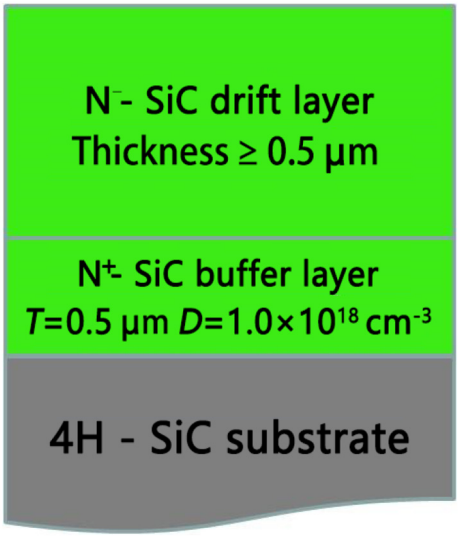

Fig. 1. Structure chart of the 4H-SiC homoepitaxial wafer.

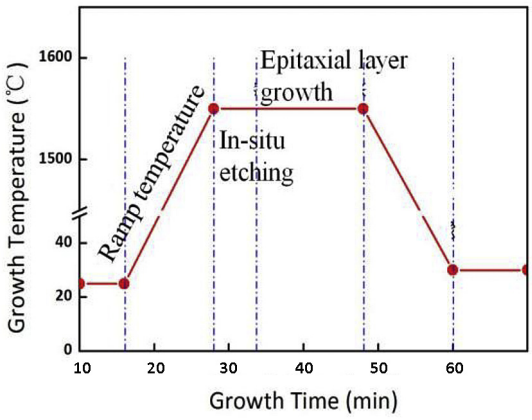

Fig. 2. Process sequence of the 4H-SiC homoepitaxial layer using CVD.

3.1. Triangle defects

The triangle defect is one of the most common surface defects in the 4° off-cut 4H-SiC epitaxial layer. This kind of defect gives rise to negative and serious impacts on the yield ratio and reliability of a device, or the so-called killer defects.[18] Hence, systematic investigations on the origins and morphologies of the triangle defects are necessary. The morphology of triangle defects can be clearly seen using an optical microscope with high magnification. Fig. 3(a) and (b) show the different morphologies of triangle defects using an optical microscope. The formation mechanism of triangle defects in the 4H-SiC epitaxial layer is presented in Fig. 3(c). The formation of triangle defects is believed to be ascribed to the two-dimensional (2D) nucleation on terraces, which affects the growth of the step flow.[19,20] Through a morphological observation of Fig. 3 (a) and (b), it is found that triangle defects can be divided into two types: obtuse triangle and acute triangle. Many reports have attributed the origin of obtuse triangle defects to surface scratches, foreign materials, and micropipes. These defects can be effectively reduced by improving the substrate surface and operation environment. Another type of acute triangle defects is ascribed to the improper parameters of the growth process, and shallow profiles can be observed using optical microscopy. In recent years, several ways have been studied to further reduce acute triangle defects. The triangle defects in the 4H-SiC epitaxial layer can be effectively controlled through the adjustment of the growth process parameters of the temperature and C/Si ratio. Generally, the triangle defect density of the 4H-SiC epitaxial layer can be reduced to 0.39 cm^{-2} with increasing growth temperature, as shown in Fig. 4. The reasons for the reduction of the triangle defect density are

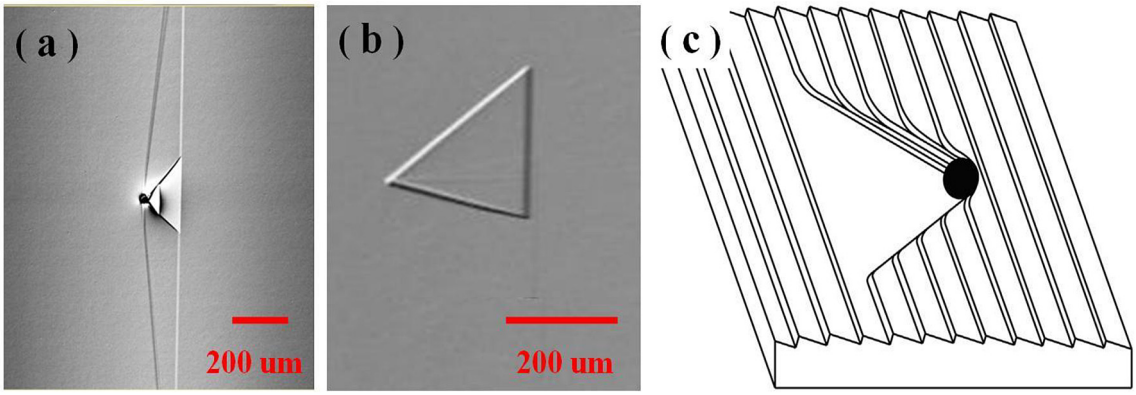

Fig. 3. General types (a-b) and formation mechanism (c) of the triangle defect in epitaxial layers.

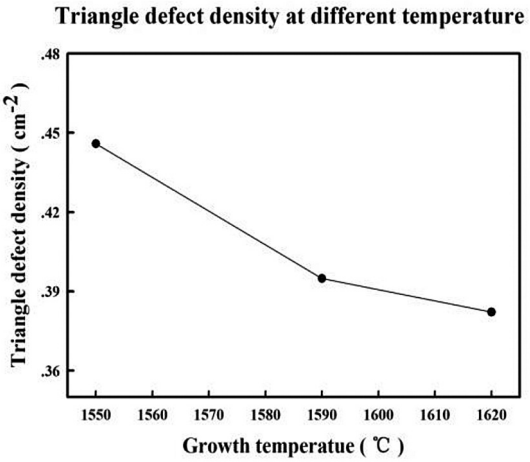

Fig. 4. Triangle defect density of epitaxial wafers at different growth temperatures.

as follows: First, the migration rate of an adatom on the deposition surface is increased, which effectively inhibited the 2D nucleation on the terraces. Second, the effective C/Si ratio on the deposition surface is reduced under a higher temperature, which enhances the step flow growth during the epitaxial growth. Therefore, the low triangle defect density of the 4H-SiC epitaxial layer can be obtained through the optimization of the substrate surface and growth process.

3.2. Carrot defects

The carrot defect is one of the major surface morphological defects that appear in as-grown epitaxial layers, and it was reported to increase the reverse leakage current of 4H-SiC Schottky and p–n junction diodes.[21,22] The different structures and origins of the carrot defect have been proposed in many papers.[21,23] The carrot defect is extended along the step-flow direction in the epitaxial layers. Fig. 5(a) shows the morphology of the carrot defect in the 4H-SiC epitaxial layer. It can be seen that the carrot defect consists of ridges. To further analyze the formation of carrot defects, the 4H-SiC epitaxial layer was etched using molten KOH at 500 °C for 30 min. The microscopic images of the carrot defect after molten KOH corrosion is shown in Fig. 5(b). By using the molten KOH etching method, it is found that the carrot defect consists of a threading screw dislocation (TSD)-related etch pit as the starting point and a pair of basal plane dislocation (BPD)-related etch pits as the terminating point, and the starting and terminating points are connected by a typical stacking fault intersecting the epitaxial layer surface. Meanwhile, the different origins of the carrot defect have been presented in previous reports, such as dislocations with TSDs and BPDs, dislocation slip bands, and substrate surface scratches.[24,25] Based on these reasons, their densities can be effectively reduced using the following methods. First, the significant decrease in the density of carrot defects was observed using the in-situ etching prior to the epitaxial growth.[24] The reduction of the carrot defect density is ascribed to the morphological improvement of the substrate surface. In addition, the formation of the carrot defect density can be

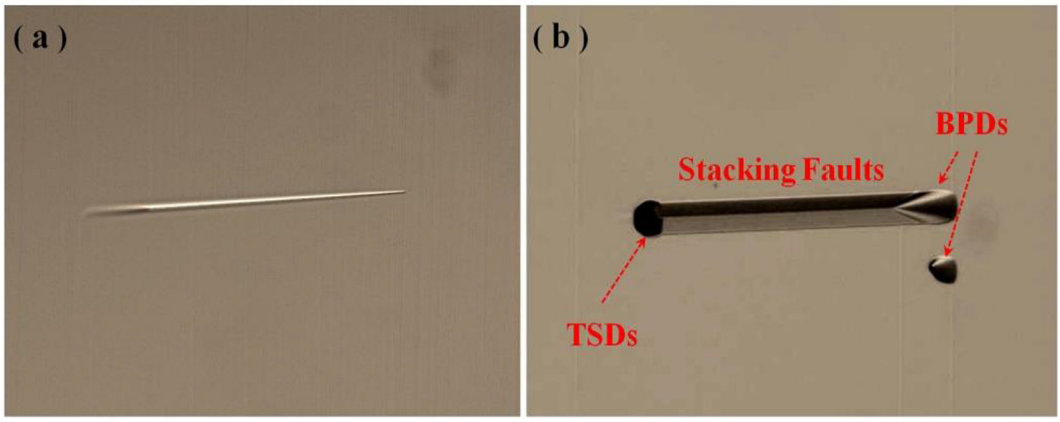

Fig. 5. Microscopic images of the carrot defect: (a) morphology on the epitaxial surface; (b) etched by molten KOH.

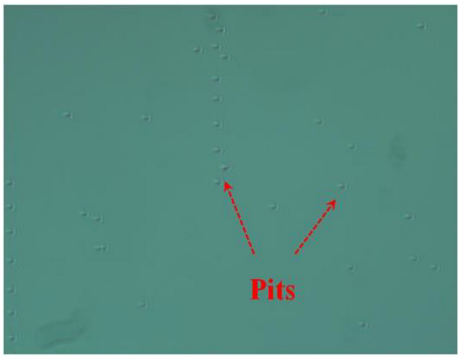

Fig. 6. Morphology of surface pits using the optical microscope.

avoided under Si-rich conditions due to the resulting improvement in the growth of the step flow.

3.3. Surface pits

With the development of industrial technology, surface pits have become a new issue due to their very high density. The surface pits of the epitaxial layer can cause the occurrence of a local electric field crowding, resulting in negative effects on the device performance.[26,27] In many previous reports, the morphology and origin of surface pits have been studied in depth using the selective etching method and synchrotron reflection X-ray topography. The microscopic images of the surface pits are shown in Fig. 6. Currently, it was demonstrated that the surface pits can be originated from the threading screw dislocations and threading edge dislocation (TED) sites during the epitaxial growth of 4H-SiC.[28,29] The observed dislocation-induced surface pits according to their shape are classified into two types. One is deep pits, whose typical lateral size is a few μm with a depth of a few tens of nm, and the other is shallow pits, whose typical lateral size and depth are approximately 1 μm and a few nm, respectively.[30] The difference of the pit shape originates from the improvement of the kinetics of the step-flow growth and the controllability of the ingredients supplied to the substrate surface. By analyzing the shape of the surface pits, the deep pits had an effect on the leakage current of the Schottky barrier diodes and lifetime of the metal–oxide–semiconductor capacitor. The influence of the process parameters on the formation and reduction of surface pits on the 4H-SiC epitaxial layer has been investigated, such as C/Si ratio, pre-etching prior to the growth process, growth temperature, and growth rate.[31,32] Chen et al. revealed that a lower surface pit density can be prepared using a lower C/Si ratio even though a substrate may have a high dislocation density. Generally, the different shapes of surface pits depend on the C/Si ratio for the epitaxial growth, and the shape of surface pits gradually becomes a deep pit under a high-C/Si-ratio condition. The surface pits of epitaxial layers can be reduced using the following factors: First, the origination of surface pits can be reduced by the quality improvement of the substrate, such as low TSDs and TEDs. Second, the optimized growth conditions can effectively eliminate defects generated during the epitaxial growth, such as lower C/Si ratio and growth rate.

3.4. Step bunching

Step bunching is another kind of morphology defect. The step bunching defect occurs on the surface of the 4H-SiC epitaxial layer, and its profile can be observed using an optical microscope. Step bunching can induce a crucial problem in high-power devices where the rough junction interface causes electric field crowding, resulting in the reduction of blocking voltages. In addition, it has an important effect on the channel mobility or the oxide breakdown characteristics in MOSFETs.[33] The morphology of step bunching is perpendicular to the primary orientation flat shown in Fig. 7. Although various explanations of the formation of step bunching have been provided, the formation mechanism has not been aptly explained until now. At present, the free step bunching of the 4H-SiC epitaxial layer is achieved by the improvement of process parameters, namely, in-situ etch, growth temperature, and C/Si ratio.[34] Fig. 7 presents the effect of growth temperature on step bunching in the growth process. The formation of step bunching is attributed to the different growth rates with [1−100] and [11−20] orientations.[35] The growth rate with [1–100] and [11–20] orientations is gradually the same when the growth temperature is decreasing. Therefore, the formation of step bunching on the 4H-SiC epitaxial layer can be avoided by carefully controlling the chemistry temperature on the deposition surface during the growth process.

3.5. BPDs

Generally, there are three different dislocations in commercial 4H-SiC substrates: TSDs with a typical density of 300–500 cm^{-2}, BPDs with a typical density of 500–1000 cm^{-2}, and TEDs with a typical density of 2000–5000 cm^{-2}. These dislocations in the substrate can propagate into the epitaxial layer during the epitaxial growth due to the growth mode of the step flow.[36] Almost all TSDs and TEDs in the substrate are replicated in the epitaxial layer, and it is hard to eliminate them using the epitaxial method. However, most (>90%) BPDs in the substrate are converted to TEDs within a few micrometers of an initial epitaxial layer without any special treatment, and the rest is propagated in a SiC epitaxial layer along the basal plane during epitaxial growth. The

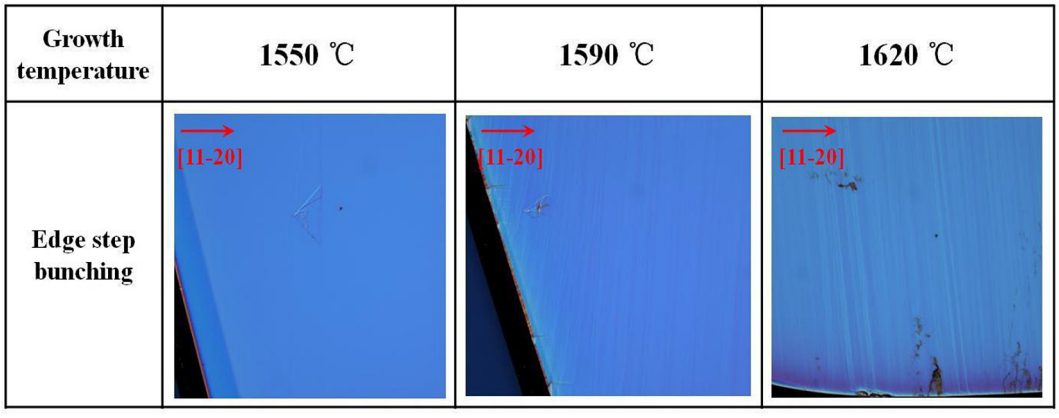

Fig. 7. Step bunching of the surface for 4H-SiC epitaxial wafers at different growth temperatures.

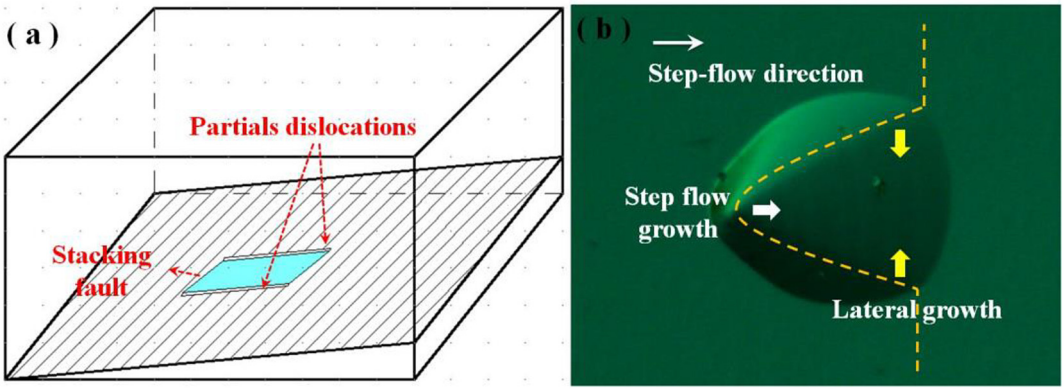

Fig. 8. Decomposition schematic (a) and conversion process (b) of BPDs.

TSDs and TEDs have no evident influence on the performance of Schottky barrier diode devices, but the BPDs in the epitaxial layer are considered the source of stacking faults that lead to the performance degradation of bipolar devices with a forward voltage drift and reverse leakage current.[36] Therefore, decreasing the density of BPDs in epitaxial layers is a key issue. A BPD in 4H-SiC can be dissociated into two partial dislocations with a stacking fault enclosing between them, as shown in Fig. 8(a).[37]

The step flow growth in the down-step direction and lateral growth perpendicular to the step flow direction can simultaneously take place during the epitaxial growth.[37] The growth mode of the step flow is beneficial to the formation of the homoepitaxial layer, and it induces the propagation of the substrate crystalline structure to the epitaxial layer. The lateral growth mode is thought to form a 2D island nucleation, which leads to the increase in surface defects. In the step flow growth domination, the BPDs in the substrate propagate into the epitaxial layer. On the contrary, the two sides of BPD etch pits will come closer and merge, and the BPDs are converted to TEDs in the epitaxial growth. The conversion process of BPD to TED during epitaxial growth is depicted in Fig. 8(b). In Fig. 8(b), the shell shape of BPD is observed using the molten KOH. By the analysis of BPD to TED conversion, it is believed that the conversion effectiveness of BPDs to TEDs can be enhanced by optimization of process parameter, such as in-situ etching, buffer process, interruption growth, and C/Si ratio in the drift layer.[38] The effect of the C/Si ratio and in-situ etching on conversion effectiveness of BPDs to TEDs during epitaxial growth was presented in our previous work.[39]

4. Summary

In this work, several defects in the 4H-SiC homoepitaxial layer are discussed, including the origin, mechanism, characterization, and negative impact on devices. Meanwhile, the controlling methods of different defects are studied in detail. It is suggested that the defects in the 4H-SiC epitaxial layer can be reduced by the following aspects: through the improvement of the 4H-SiC substrate quality, such as reduction of the dislocation density, and through the optimization of process parameters, such as growth temperature. Therefore, the lowest defect density of the 4H-SiC homoepitaxial layer can be prepared by accurately controlling the surface chemistry during the growth process. In addition, the development of 4H-SiC epitaxial layer with large diameter and fast growth rate for the epitaxial process is a research focus in the future.

Declaration of Competing Interest

The authors declare no conflict of interest.

Acknowledgments

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