Manuel Oliveira

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Professional Profile

Senior Digital Designer with over 8 years of experience in VLSI circuits. Problem solver, driven by improving the quality and robustness of the RTL. Member of the PCIe team for more than 7 years, acquired the capability to specify and implement RTL meeting systems requirements (PCIe Spec and/or customer additional requirements) following the best practices in writing code - coding style and linter analyses. As Tech Lead, was responsible to coordinate a small team and planning project tasks. Experienced supervision of youngest peers and students in internships and Master's thesis. Nowadays, as an SoC designer, he is working close to the BE team, and diving deeply into Formal Verification, being the person in touch for any Formal Verification initiative in the team.

Skills

- **HDL:** System Verilog, Verilog, and SVA
- Formal Verification
- Languages: Python, TCL, Perl
- ASIC and FPGA design flow
- PCIe
- Micro-architecture
- Linux, Mac, and Windows

Career Summary

2022/08 – Present **Axelera AI, SoC Senior Digital Designer**

- Owner of Formal Verification, responsible for implementation and helping designer to adopt it
- Developed system infrastructure to measure performance at the SoC level, using FW code
- Develop and document micro-architectures from high-level specifications.
- Block and system-level RTL coding, performing static checks to enhance the quality of the RTL
- Automate tasks using scripting for efficiency (Python)
- Working closely with the verification team to define test plan, run regressions, reproduce, and debug functional and performance bugs.
- Perform preliminary design synthesis to identify and fix timing issues for the Physical Design team

2015/09 – 2022/07 **Synopsys, ASIC Digital Designer**

- Hyper-DMA tech leader, responsible for the micro-architecture, defining and assigning design tasks to the team, defining test plan, planning new enhancements and gen6 adoption
- Specification, implementation, and maintenance of RTL to high-performance systems synthesized at high speeds in accordance with specifications and customer requirements.
- Responsible for supervising the code quality using a linter tool and assigning the issues to the correct person.
- Responsible for process automation and readability improvements using scripting languages like Python.
- Supervising youngest peers and students in internships and Master's thesis.

2014/09 – 2015/07 **Faculty of Engineering, University of Porto, Technical Assistant**

- Designer and manufacturer of PCBs.
- Fixing issues in existing circuits.
- Welding the components in the PCB (surface mount and through-hole).

2014/07-2014/09 **Synopsys, ASIC Digital Designer Intern**

- Exploration of SysML language for specification and documentation in the digital design flow of VLSI circuits.

2014/02–2014/05 **Faculty of Engineering, University of Porto, Teacher's Assistant**

- Supported classroom activities, including tutoring, grading homework and reviewing exams.

Education

2010/09-2015/07 **Master of Science: Electrical and Computer Engineering**
Telecommunications, Electronics and Computers

- Majored in Microelectronics and Embedded Systems.
- Thesis: A SysML-based Design Flow for Digital VLSI Circuits
- 16 values

Certifications

2018 **MindShare course: PCI Express Gen4**