



Engineering

University of Windsor

ELEC 4450: Power Electronics

Instructor: Dr. Caniggia Castro Diniz Viana

Switched-Mode Power Supply: Preliminary Design

Manveer Aujla 110072428

Alice Seo 110072503

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Question 1. In this question, you design the active power LPF.

- a) Briefly discuss the theoretical tools developed in other courses you are leveraging to guide the LPF design.

The design of the Low Pass Filter (LPF) requires an understanding of several theoretical concepts from Circuit Analysis, and Electronics I & II:

- Ideal operational amplifier (op amp) characteristics (e.g., infinite input impedance)
- Derivation of DC gain of the op amp circuit using Kirchhoff's Voltage and Current Laws
- The filter's frequency response and Bode plots, including the cutoff frequency, i.e., ω_{cut} where

$$|H(j\omega_{\text{cut}})| = \frac{1}{\sqrt{2}} |H(j0)|$$

- Basic filter design knowledge to select proper resistor and capacitor values

By applying these theoretical tools, we can design the LPF to meet the requirements. Specifically, we will design a first-order Butterworth filter because its frequency response indicates that low input frequencies will mainly be affected by the DC gain, while higher input frequencies (after the cutoff) will be heavily attenuated.

- b) Enumerate all missing information that must be gathered to produce an implementable design.

Hint: E.g., specific aspects of op amp and microcontroller specifications.

To fully implement the LPF, the following information must be gathered:

1. Ranges for differential input voltage and supply voltage that the op amp will be subjected to in our overall design.
2. The maximum input voltage of the ADC of the MCU.
3. Expressions for DC gain and cutoff frequency of the Butterworth filter in terms of circuit parameters.
4. The 0-dB crossover frequency of the controller, ω_c , since we need $\omega_{\text{cut}} \geq 25\omega_c$.
5. Available components such as resistors, capacitors, and op amps on Digikey that meet our design constraints (e.g., nominal values, power and voltage ratings) and specifications. Specifically, we want the DC gain to adhere to the ADC maximum input voltage and the cutoff frequency to be 25 times greater than the controller's crossover frequency.

- c) Complete your design and provide a schematic snapshot and a brief description of the suitability of each passive and active component used.

A first-order Butterworth LPF is shown below in Figure 1.1, obtained from Lecture 11 [1].

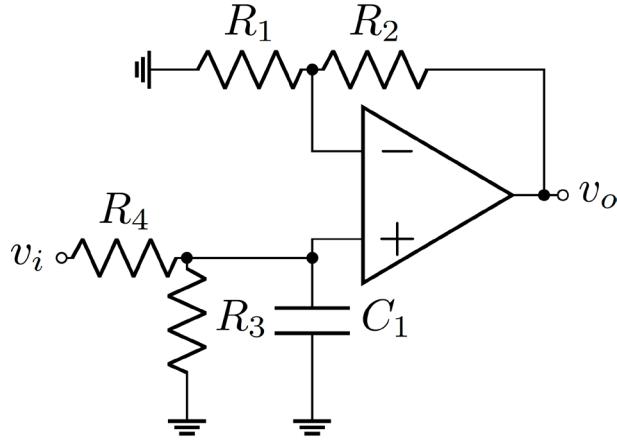


Figure 1.1: First-order Butterworth LPF [1].

The DC gain of the LPF is given as

$$\frac{V_o}{V_i}(j0) = \left(1 + \frac{R_2}{R_1}\right) \left(\frac{R_3}{R_3 + R_4}\right)$$

We need to normalize the buck voltage to values that the MCU can safely take. A DC gain of 0.05 will work for our application. The buck should at maximum produce 50 V, and $0.05(50\text{ V}) = 2.5\text{ V}$ is still acceptable for the MCU. Let us take $R_1 = R_4$ and $R_2 = R_3$:

$$\begin{aligned} \frac{V_o}{V_i}(j0) &= 0.05 = \left(1 + \frac{R_2}{R_1}\right) \left(\frac{R_2}{R_1 + R_2}\right) = \frac{1}{R_1}(R_1 + R_2) \left(\frac{R_2}{R_1 + R_2}\right) = \frac{R_2}{R_1} \\ R_1 &= 20R_2 \end{aligned}$$

In the market, 1 kΩ and 20 kΩ resistors are inexpensive and easily obtainable. Thus, we will choose

$$R_1 = R_4 = 20 \text{ k}\Omega \quad R_2 = R_3 = 1 \text{ k}\Omega$$

We will use the [RMCF0805FT1K00](#) 1 kΩ resistor and the [RC0805FR-0720KL](#) 20 kΩ resistor. These both have a power rating of 0.125 W; this is sufficient because the maximum instantaneous power of each resistor is lower than 0.125 W. Suppose the output could spike up to 50 V. Then,

$$P_{R1} = \frac{V_{R1}^2}{R_1} = \frac{1}{1000} (50 \cdot \frac{1000}{1000 + 20000})^2 = \frac{1}{1000} (2.38)^2 = 5.67 \text{ mW}$$

$$P_{R2} = \frac{V_{R2}^2}{R_2} = \frac{1}{20000} (50 \cdot \frac{20000}{1000 + 20000})^2 = 0.113 \text{ W}$$

Next, the capacitance for the LPF based on its cutoff frequency and resistances is given by

$$C = \frac{1}{(R_3 \parallel R_4)\omega_{\text{cut}}}$$

We need $\omega_{\text{cut}} \geq 25\omega_c$ where ω_c is the controlled open-loop system's 0-dB crossover frequency. In Q3, a controller was designed such that $\omega_c = 20 \text{ rad/s}$. So,

$$C = \frac{1}{\left(\frac{R_3 R_4}{R_3 + R_4}\right) 25\omega_c} = \frac{1}{\left(\frac{(1)(20)}{1+20} \times 10^3\right) 25(20)} = 2.1 \mu\text{F}$$

So, we must have $C \leq 2.1 \mu\text{F}$ to achieve $\omega_{\text{cut}} \geq 500 \text{ rad/s}$. The [CGA4J3X7R1H155K125AB](#) 1.5 μF ceramic capacitor is suitable, as it is cheap and easily available, has a voltage rating of 50 V which is more than enough for our application, and its 10% tolerance is not a big deal. Using the nominal capacitance, the cutoff frequency will be

$$f_{\text{cut}} = \frac{1}{(R_3 \parallel R_4) 2\pi C} = \frac{1}{\left(\frac{(1)(20)}{1+20} \times 10^3\right) 2\pi(1.5 \times 10^{-6})} = 111.4 \text{ Hz}$$

Finally, regarding the op amp for the filter, the [LM358DGKR](#) IC is a good choice since it can be fed with 3.3 V and ground to ensure that the MCU does not receive voltages outside of its acceptable range. It can tolerate a differential input voltage between $-0.3 \text{ V} < v_d < 32 \text{ V}$ which is within spec for our application. Furthermore, the 3.3 V can be supplied directly by the MCU board.

A schematic snapshot of the active LPF is shown in Figure 1.2. A summary of the components is shown below in Table 1.1.

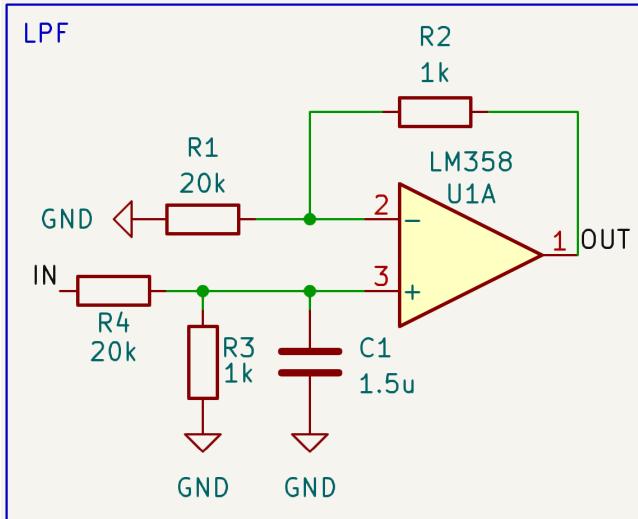


Figure 1.2: Schematic snapshot of active LPF.

Table 1.1: Summary of components chosen for active LPF.

Parameter	$R_1 = R_4$	$R_2 = R_3$	C	Op Amp
Part Number	RC0805FR-0720KL	RMCF0805FT1K00	CGA4J3X7R1H155K125AB	LM358DGKR
Nominal Value	$20 \text{ k}\Omega \pm 1\%$	$1 \text{ k}\Omega \pm 1\%$	$1.5 \mu\text{F} \pm 10\%$	---
Rating	0.125 W	0.125 W	50 V	$v_d \in (-0.3, 32)$
Cost Per Unit	\$0.16	\$0.16	\$0.52	\$0.37
Quantity	2	2	1	1

Question 2. In this question, you design the LC voltage LPF.

- a) Briefly discuss the theoretical tools developed in this course you are leveraging to guide the power filter design.

In this course, RLC and steady-state analysis are covered in Lectures 2 and 3, respectively. We will use the following theoretical tools developed in this course to guide the power filter design:

- Assuming periodic steady-state and analyzing one semi-cycle at a time, i.e., Q on/off, \bar{Q} off/on.
- Capacitor Charge Balance (CCB): The capacitor accumulates zero net charge over T_{sw} , i.e.,

$$\langle i_C \rangle = \frac{1}{T_{sw}} \int_{T_{sw}} i_C dt = 0$$

- Volt-Second Balance (VSB): The inductor accumulates zero net charge over T_{sw} , i.e.,

$$\langle v_L \rangle = \frac{1}{T_{sw}} \int_{T_{sw}} v_L dt = 0$$

- Low Ripple Assumption (LRA): All capacitor voltages in DC/DC converters are constant.
- Deriving current ripple Δi_L and voltage ripple Δv_C from the plots of v_L , i_L , i_C , and v_C .
- Analyze the expressions for ripple and determine the worst-case operating scenarios by observing how each expression will be maximized as the parameters (i.e., V_i & R_o) change.
- Intuition on low pass filters: inductors “hold” current and capacitors “hold” voltage. Also, the cutoff frequency of the LC filter should be lower than the switching frequency.

- b) Enumerate all missing information that must be gathered to produce an implementable design.
 Enumerate all intermediate steps to get to the solution.

To determine the implementable design, the following missing information should be gathered:

- 1) Expressions for the average capacitor voltage V_C and inductor current I_L
- 2) Expressions for the output voltage ripple Δv_C and inductor current ripple Δi_L
- 3) The worst-case scenario operating points for Δv_C and Δi_L
- 4) Minimum C and L values to meet ripple requirements
- 5) Existing capacitors and inductors on Digikey that satisfy the design requirements including voltage and current ratings, prices, and packages

We can take the following steps to find the listed missing information:

- 1) First, we can analyze the buck converter circuit over the switching period to find equations for the state variable derivatives, i.e., derivatives of capacitor voltage and inductor current.
 - 2) We assume that the circuit is operating at periodic steady-state. Applying VSB and CCB, we set the state variable derivatives equal to zero and solve for V_C and I_L .
 - 3) Then, we can plot v_L , i_L , i_C , and v_C using the capacitor/inductor voltage and current relationships and accumulate the rates of change to obtain the expressions for ripple.
 - 4) The minimum capacitance and inductance can be calculated by isolating for C and L from Δv_C and Δi_L , setting the operating points such that C and L are maximized, and solving for these values. These will be the minimum C and L needed to meet the ripple requirements.
 - 5) Search for suitable inductors and capacitors on Digikey, ensuring we select components that are rated for the requirements listed previously.
- c) Analytically derive an expression for the buck current and voltage ripple as a function of all appropriate parameters. Determine the minimum value of L and C .

The buck converter circuit is shown below in Figure 2.1. It was obtained from Lecture 3 [2].

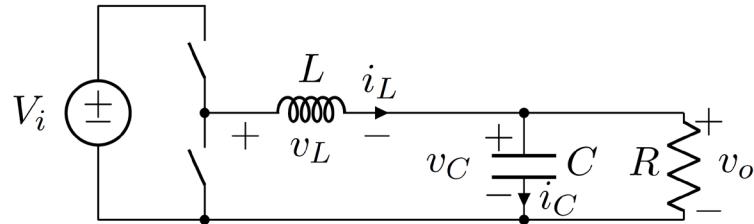


Figure 2.1: Buck converter [2].

First, we will do some analysis to help with plotting the waveforms. For each semi-cycle,

$$0 \leq t < DT_{sw}$$

$$DT_{sw} \leq t < T_{sw}$$

$$v_L = V_i - V_C$$

$$v_L = -V_C$$

$$i_C = i_L - \frac{V_C}{R_o}$$

$$i_C = i_L - \frac{V_C}{R_o}$$

Applying volt-second balance (VSB),

$$\langle v_L \rangle = D(V_i - V_C) - (1 - D)V_C = 0$$

$$V_C = DV_i$$

Applying capacitor charge balance (CCB),

$$\langle i_C \rangle = D \left(I_L - \frac{V_C}{R_o} \right) + (1 - D) \left(I_L - \frac{V_C}{R_o} \right) = 0$$

$$I_L = \frac{V_C}{R_o} = \frac{DV_i}{R_o}$$

Now we know that I_L is positive and V_C is positive for a positive input voltage V_i . Plots of v_L, i_L, i_C , and v_C are shown in Figure 2.2. These plots were obtained from the Lecture 3 slides [2].

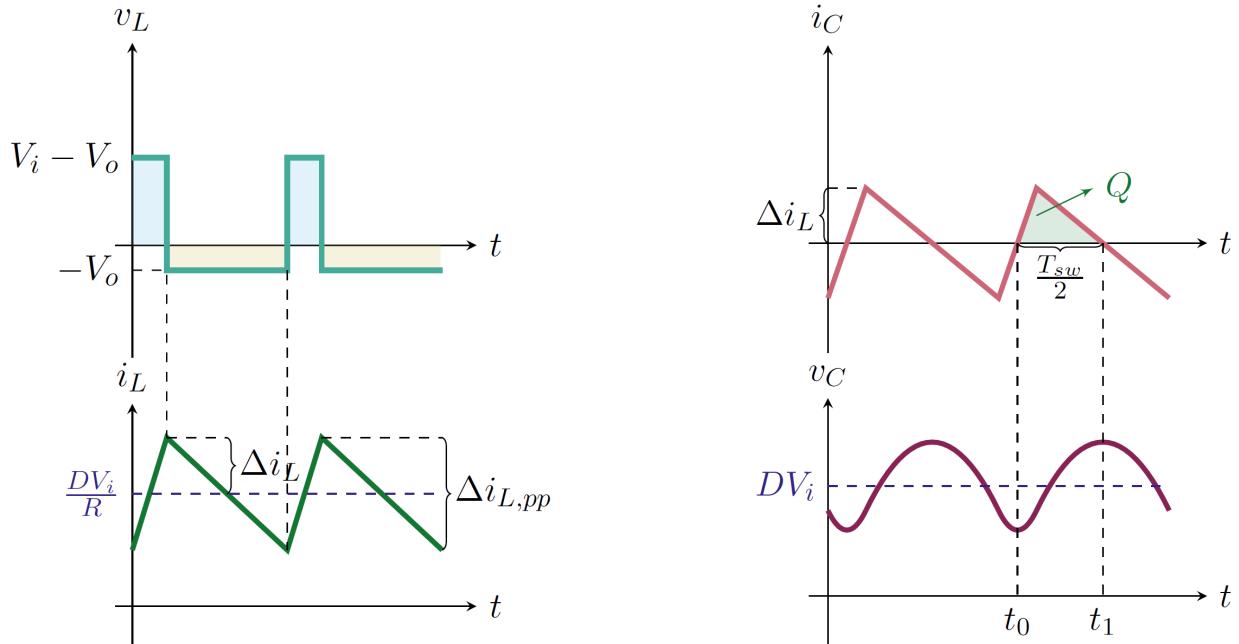


Figure 2.2: Plots of v_L, i_L, i_C , and v_C [2].

The inductor current i_L is equal to the area under the inductor voltage plot divided by the inductance L . The mathematical expression for the inductor current is:

$$i_L = \frac{1}{L} \int v_L dt$$

Using the above equation to derive the inductor current ripple equation:

$$\Delta i_{L,pp} = \frac{1}{L} \int_0^{DT_{sw}} v_L dt$$

$$\Delta i_{L,pp} = \frac{V_i(1 - D)D}{f_{sw}L}$$

Note that the inductor ripple is the change in i_L over the switching period T_{sw} divided by 2.

$$\Delta i_L = \frac{1}{2} \Delta i_{L,pp} = \frac{V_i(1-D)D}{2f_{sw}L}$$

Then, from the capacitor current plot, the capacitor voltage ripple equation is derived:

$$v_C = \frac{1}{C} \int i_C dt$$

$$\Delta v_{C,pp} = \frac{1}{C} \int_{t_0}^{t_1} i_C dt$$

Knowing that the integral is being taken over the half of one period as t_0 and t_1 are taking half of each semi-cycle, the voltage ripple is found as shown below.

$$\Delta v_{C,pp} = \frac{1}{C} \frac{\left(\frac{T_{sw}}{2}\right)(\Delta i_L)}{2} = \frac{V_i(1-D)D}{8f_{sw}^2 LC}$$

$$\Delta v_C = \frac{1}{2} \Delta v_{C,pp} = \frac{V_i(1-D)D}{16f_{sw}^2 LC}$$

The design requirements are $\Delta i_L \leq 30\% I_L$ and $\Delta v_o \leq 0.5\% V_o$. First, we solve for the minimum L to meet the current ripple requirement. We know $D = V_o/V_i$ and $I_L = DV_i/R$. Let δ_i be an arbitrary current ripple tolerance. So,

$$\Delta i_L \leq \delta_i I_L$$

$$\frac{D(1-D)V_i}{2f_{sw}L} \leq \delta_i \frac{DV_i}{R_o}$$

$$\frac{\left(1 - \frac{V_o}{V_i}\right)}{2f_{sw}L} \leq \frac{\delta_i}{R_o}$$

$$\frac{2f_{sw}L}{\left(1 - \frac{V_o}{V_i}\right)} \geq \frac{R_o}{\delta_i}$$

$$L \geq \frac{R_o \left(1 - \frac{V_o}{V_i}\right)}{2f_{sw}\delta_i}$$

L is maximized when V_i and R_o are maximized. So, $V_i = 50$ V, $R_o = 300$ Ω , and $\delta_i = 0.3$:

$$L \geq \frac{300 \left(1 - \frac{30}{50}\right)}{2(10000)(0.3)} = 20 \text{ mH}$$

Next, we solve for the minimum C to meet the voltage ripple requirement.

$$\Delta v_o \leq \delta_v V_o$$

$$\frac{D(1-D)V_i}{16f_{sw}^2LC} \leq \delta_v V_o$$

$$\frac{16f_{sw}^2LC}{V_o \left(1 - \frac{V_o}{V_i}\right) V_i} \geq \frac{1}{\delta_v V_o}$$

$$C \geq \frac{1 - \frac{V_o}{V_i}}{16f_{sw}^2 L \delta_v}$$

C is maximized when V_i is maximized. So, $V_i = 50$ V, $L = 20$ mH, and $\delta_v = 0.005$:

$$C \geq \frac{1 - \frac{30}{50}}{16(10000)^2(0.02)(0.005)} = 2.5 \text{ } \mu\text{F}$$

Hence, to meet the ripple requirements, the minimum inductance is $L = 20$ mH and the minimum capacitance is $C = 2.5 \mu\text{F}$.

- d) Describe the relevant constraints for the selection of an inductor and capacitor. Discuss how selecting an inductor is different from determining a value of L . Provide component part numbers for the inductor and capacitor along with a brief description of their suitability.
- Hint: Show how they meet all constraints listed in 2b.*

The relevant constraints for the selection of the inductor and capacitor include the following:

- Inductance and capacitance to meet the ripple requirements
- Current rating of the inductor needs to be greater than the maximum i_L
- Voltage rating of the capacitor needs to be greater than the maximum v_C
- Cost and availability of each component on online vendors (in our case, Digikey)
- ESR of each component must be reasonable for our application, i.e., power conversion
- Size of each component must be small enough to fit on the PCB

Expanding on the selection of the inductor, the minimum inductance is $L = 20$ mH. Therefore, we need our LC filter in the power stage to have an equivalent inductance of $L \geq 20$ mH. We do not need a single inductor with an inductance of 20 mH or more. Instead, we can select a smaller, cheaper, more easily available inductor and place multiple in series to achieve the minimum L . At steady-state, the maximum inductor current is shown below and is maximized when $R_o = 57 \Omega$ and $V_i = 50$ V:

$$i_{L,\max} = I_L + \Delta i_L = \frac{V_o}{R_o} + \frac{\frac{V_o}{V_i} \left(1 - \frac{V_o}{V_i}\right) V_i}{2f_{sw}L} = \frac{V_o}{R_o} + \frac{V_o \left(1 - \frac{V_o}{V_i}\right)}{2f_{sw}L}$$

$$i_{L,\max} = \frac{30}{57} + \frac{30 \left(1 - \frac{30}{50}\right)}{2(10000)(0.02)} = 0.556 \text{ A} = 556 \text{ mA}$$

We need to choose an inductor that satisfies this current rating. We will choose the [1468507C](#) fixed inductor with an inductance of 6.8 mH and a current rating of 700 mA by Murata Power Solutions. We will use three of these inductors in series to achieve an inductance of $L = 3(6.8) = 20.4$ mH. This component has an ESR of 2.3Ω which is rather low compared to some of the other options that were available. It is also cheap at only \$4.24 for each unit with a small enough size for three to fit on the PCB. The 700 mA current rating should be enough to avoid thermal issues.

A very important piece of information to note: this inductor has a tolerance of $\pm 10\%$, meaning that technically the inductance could be as low as $L = 0.9(20.4) = 18.36$ mH. This would lead to a ripple $\Delta i_L > 30\% I_L$ in the worst-case scenario operating point. However, our application is not critical for industry and the likelihood that all three inductors have their tolerance such that we go below the minimum inductance is not very high. Keeping this in mind, it is important to consider the tolerance of the inductor for future designs. We will henceforth consider only the nominal values of the inductor for analysis and control design.

Next is the capacitor selection. This is far easier to choose than the inductor, as there are many cheap and easily available capacitors on the market. The minimum capacitance is $C = 2.5 \mu F$. To be on the safe side, we want to have our output capacitor be rated for at least $V_i = 50$ V due to load transients. We will choose the [GRM31CC72A475KE11L](#) ceramic capacitor with a capacitance of $4.7 \mu F$ and a voltage rating of 100 V by Murata. The extra capacitance gives a good margin for keeping the ripple low and the output voltage relatively constant, even if it will negatively affect the transient performance. This capacitor is more expensive than usual at \$1.02 per unit, but the voltage rating is worth it.

A summary of the components is shown below in Table 2.1.

Table 2.1: Summary of the selected inductor and capacitor.

Parameter	Inductor	Capacitor
Part Number	1468507C	GRM31CC72A475KE11L
Nominal Value	$6.8 \text{ mH} \pm 10\%$	$4.7 \mu F \pm 10\%$
Rating	700 mA	100 V
Cost Per Unit	\$4.24	\$1.02
ESR	2.3Ω	---
Quantity	3	1

- e) Produce a steady-state simulation in Simulink showing how the system, with the selected parameters meets the specifications laid out on the project instructions.

The Simulink model of the buck converter is shown in Figure 2.3. As mentioned in Q2c, the maximum voltage and current ripple occur when $R_o = 300 \Omega$ and $V_i = 50 V$. We will also test when R_o and V_i are minimum to be rigorous. The duty cycle of the pulse generator is set to $D = \frac{V_o}{V_i}$.

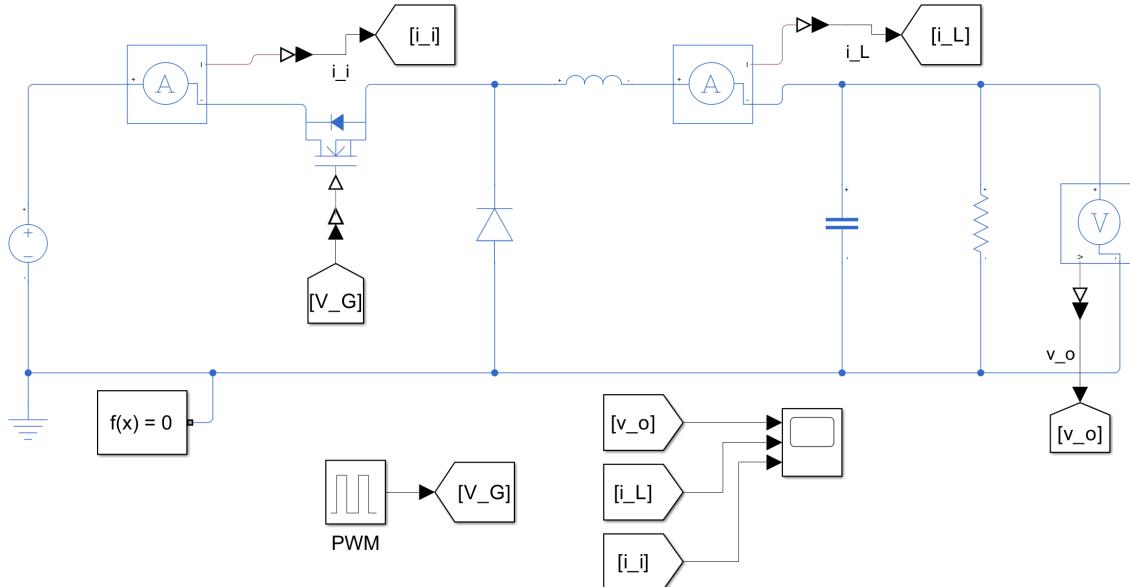


Figure 2.3: Buck converter simulation model.

Plots when the operating point is $V_i = 50 V$ and $R_o = 300 \Omega$ are shown in Figure 2.4. Steady-state behaviour is shown in Figure 2.5.

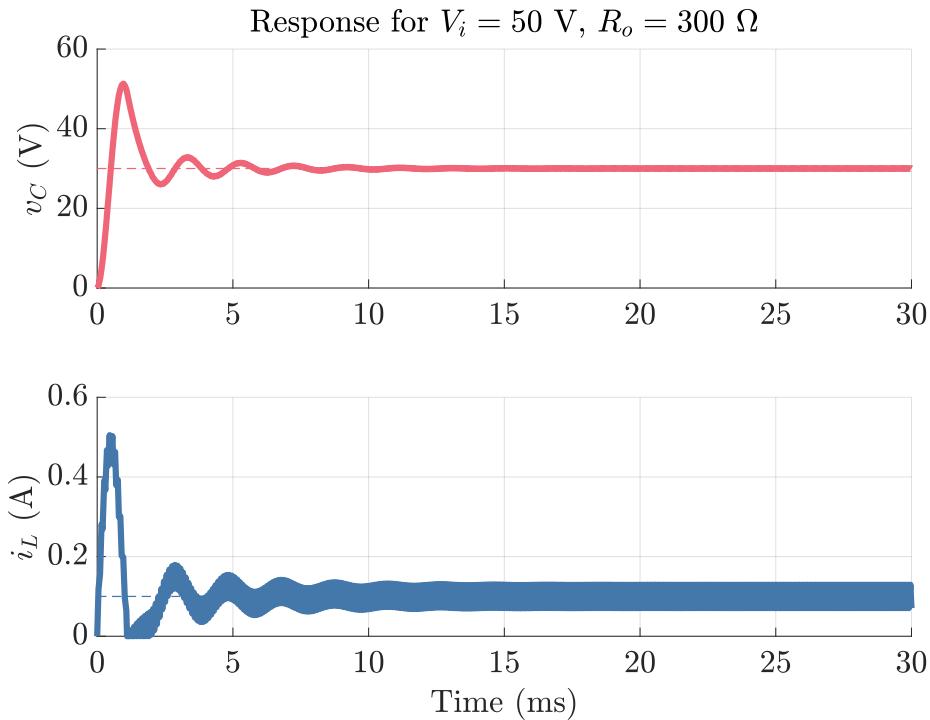


Figure 2.4: Response of buck converter when $V_i = 50 V$ and $R_o = 300 \Omega$.

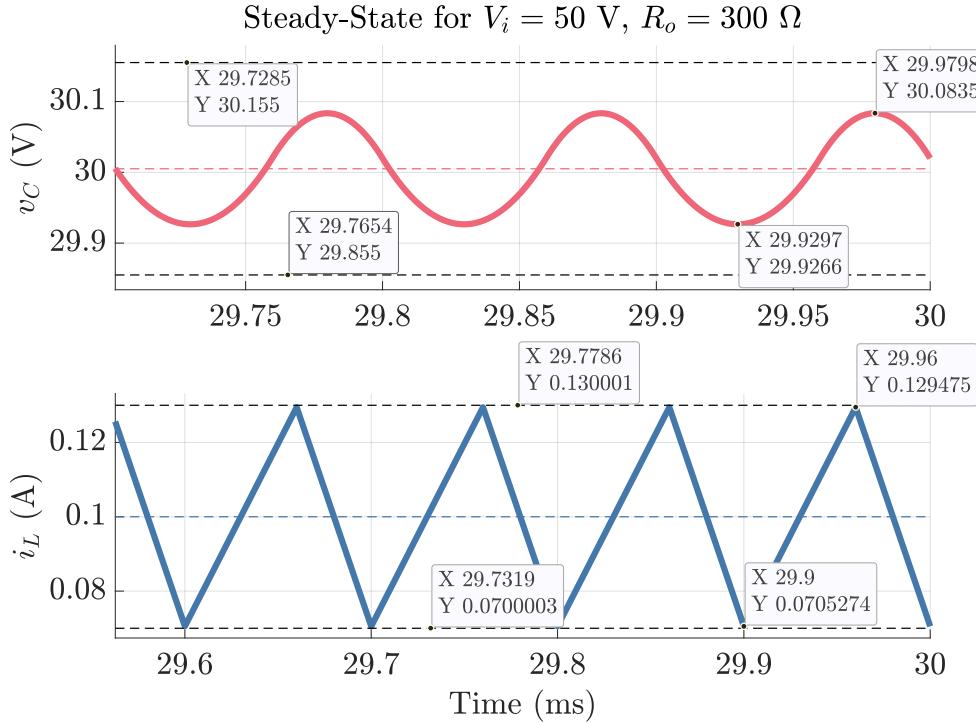


Figure 2.5: Steady-state when $V_i = 50$ V and $R_o = 300 \Omega$.

The horizontal dashed lines in Figure 2.5 indicate the values $V_o \pm 0.5\%V_o$ and $I_L \pm 30\%I_L$. Evidently, the design meets the Δv_o and Δi_L requirements. Plots at the operating point $V_i = 36$ V and $R_o = 57 \Omega$ are shown below in Figure 2.6. The design meets the ripple requirement here, too.

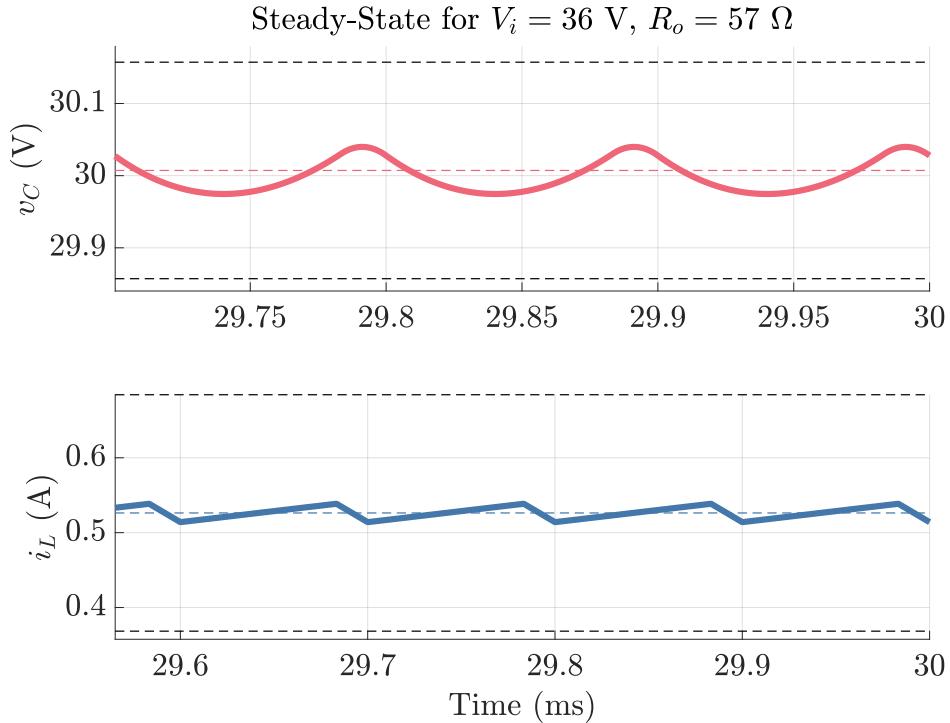


Figure 2.6: Steady-state when $V_i = 36$ V and $R_o = 57 \Omega$.

Question 3. In this question, you design the feedback control system.

a) Find the averaged model of the converter and, if applicable, linearize it.

Consider the average inductor voltage and capacitor current:

$$\begin{aligned}\langle v_L \rangle &= L \frac{d}{dt} \langle i_L \rangle = d \langle v_i \rangle - \langle v_C \rangle \\ \langle i_C \rangle &= C \frac{d}{dt} \langle v_C \rangle = \langle i_L \rangle - \frac{\langle v_C \rangle}{R_o}\end{aligned}$$

We will assume that our input voltage has no variation, i.e., $\langle v_i \rangle = V_i$. We have

$$d = D + \tilde{d} \quad \langle i_L \rangle = I_L + \tilde{i}_L \quad \langle v_C \rangle = V_C + \tilde{v}_C$$

Then,

$$\begin{aligned}L \frac{d}{dt} (I_L + \tilde{i}_L) &= (D + \tilde{d})(V_i) - (V_C + \tilde{v}_C) \Rightarrow L \frac{d}{dt} I_L + L \frac{d}{dt} \tilde{i}_L = DV_i + \tilde{d}V_i - V_C - \tilde{v}_C \\ 0 + L \frac{d}{dt} \tilde{i}_L &= DV_i - V_C + \tilde{d}V_i - \tilde{v}_C\end{aligned}$$

$0 = DV_i - V_C$ Indicates the DC (steady-state) terms.

$L \frac{d}{dt} \tilde{i}_L = \tilde{d}V_i - \tilde{v}_C$ Indicates the first-order (linear) AC terms.

Next,

$$\begin{aligned}C \frac{d}{dt} (V_C + \tilde{v}_C) &= (I_L + \tilde{i}_L) - \frac{V_C + \tilde{v}_C}{R_o} \Rightarrow C \frac{d}{dt} V_C + C \frac{d}{dt} \tilde{v}_C = I_L + \tilde{i}_L - \frac{V_C}{R_o} - \frac{\tilde{v}_C}{R_o} \\ 0 + C \frac{d}{dt} \tilde{v}_C &= I_L - \frac{V_C}{R_o} + \tilde{i}_L - \frac{\tilde{v}_C}{R_o}\end{aligned}$$

There are no nonlinear (second-order or greater) AC terms in either equation; hence, the system is already linear. For control of the buck converter, we must find how a small change in d creates a small change in v_C . That is, we want to find the transfer function $G(s) = \frac{\tilde{v}_C(s)}{\tilde{d}(s)}$.

$$C \frac{d}{dt} \tilde{v}_C = \tilde{i}_L - \frac{\tilde{v}_C}{R_o}$$

Taking the Laplace transform, noting that initial conditions are zero for the transfer function,

$$sC \tilde{v}_C(s) = \tilde{i}_L(s) - \frac{\tilde{v}_C(s)}{R_o} \Rightarrow \left(sC + \frac{1}{R_o} \right) \tilde{v}_C(s) = \tilde{i}_L(s)$$

Finding $\tilde{i}_L(s)$,

$$L \frac{d}{dt} \tilde{i}_L = \tilde{d}V_i - \tilde{v}_C \Rightarrow sL \tilde{i}_L = V_i \tilde{d}(s) - \tilde{v}_C(s) \Rightarrow \tilde{i}_L = \frac{1}{sL} \left(V_i \tilde{d}(s) - \tilde{v}_C(s) \right)$$

So,

$$\left(sC + \frac{1}{R_o} \right) \tilde{v}_C(s) = \frac{1}{sL} \left(V_i \tilde{d}(s) - \tilde{v}_C(s) \right)$$

$$\left(sC + \frac{1}{R_o} + \frac{1}{sL} \right) \tilde{v}_C(s) = \frac{V_i \tilde{d}(s)}{sL}$$

$$\frac{\tilde{v}_C(s)}{\tilde{d}(s)} = \frac{V_i}{sL \left(sC + \frac{1}{R_o} + \frac{1}{sL} \right)}$$

$$G(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{V_i}{s^2 LC + s \frac{L}{R_o} + 1}$$

Therefore, the averaged model is given by

$$L \frac{d}{dt} \langle i_L \rangle = d \langle v_i \rangle - \langle v_o \rangle \implies L \frac{d}{dt} \tilde{i}_L = \tilde{d} V_i - \tilde{v}_C$$

$$C \frac{d}{dt} \langle v_o \rangle = \langle i_L \rangle - \frac{\langle v_o \rangle}{R_o} \implies C \frac{d}{dt} \tilde{v}_C = \tilde{i}_L - \frac{\tilde{v}_C}{R_o}$$

The transfer function relating \tilde{v}_o and \tilde{d} is

$$G(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{V_i}{s^2 LC + s \frac{L}{R_o} + 1}$$

- b) Design a PI controller with crossover frequency $\omega_c \geq 10$ rad/s and $PM \geq 60^\circ$. Document your control design and show the compensated loop bode-plot, highlighting the phase-margin and crossover frequency.

The plant transfer function can be manipulated as follows:

$$G(s) = K \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \Rightarrow V_i \frac{\frac{1}{LC}}{s^2 + s \frac{1}{R_o C} + \frac{1}{LC}}$$

$$K = V_i \quad \omega_n = \sqrt{\frac{1}{LC}} \quad \zeta = \frac{\sqrt{L}}{2R_o \sqrt{C}}$$

As V_i increases, so does the open-loop system gain K and hence the 0-dB crossover frequency increases. With the 0-dB crossover frequency further to the right, the phase margin will drop and so the system becomes less stable. As R_o increases, the damping ratio ζ decreases and hence the overshoot and oscillations increase making the system less stable. Hence, the most unstable case is when V_i is maximum and R_o is maximum. We will design the compensator using these values to ensure stability and then check to ensure all operating points have met the performance specifications.

The Bode plot of $G(s)$ is shown below. Since $PM > 0^\circ$ and $GM > 0$ dB, the closed-loop system $\frac{G(s)}{1+G(s)}$ is already stable.

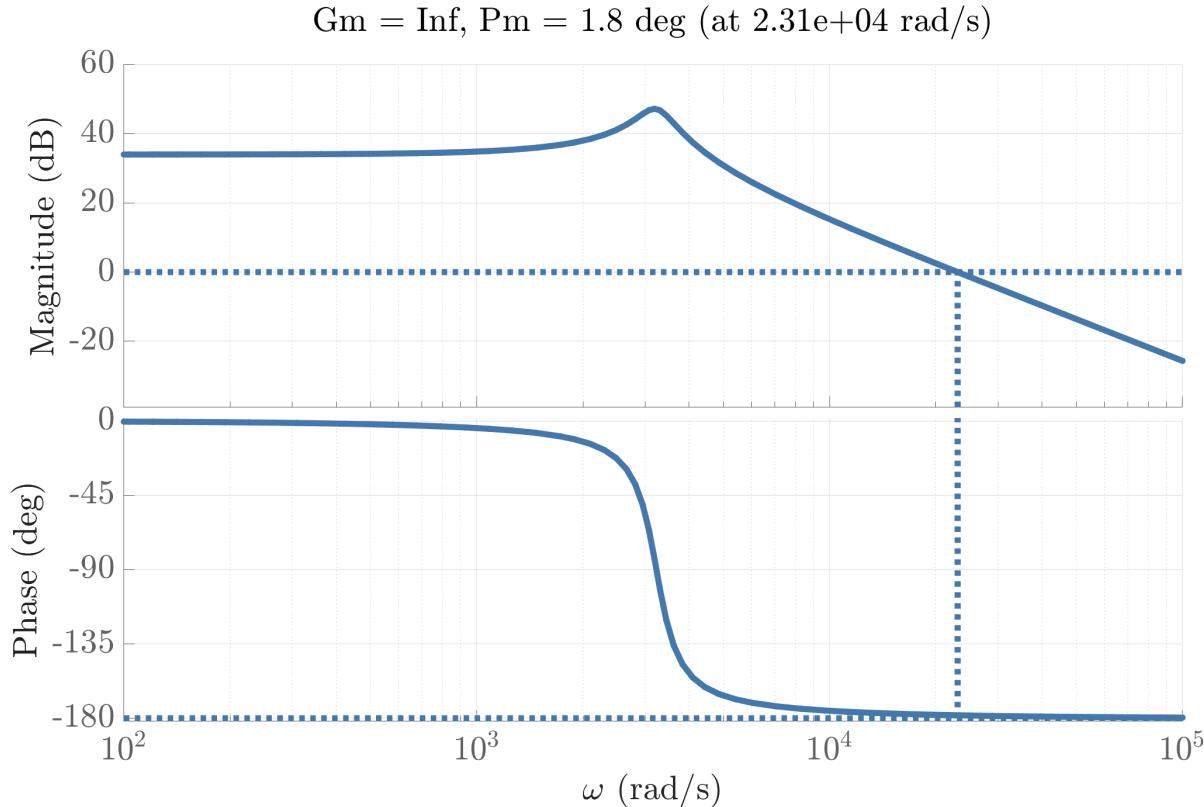


Figure 3.1: Bode plot of the plant $G(s)$ when $V_i = 50$ V and $R_o = 300 \Omega$.

Using sisotool for design, the resulting loop transfer function $C(s)G(s)$ plots are shown in Figure 3.2.

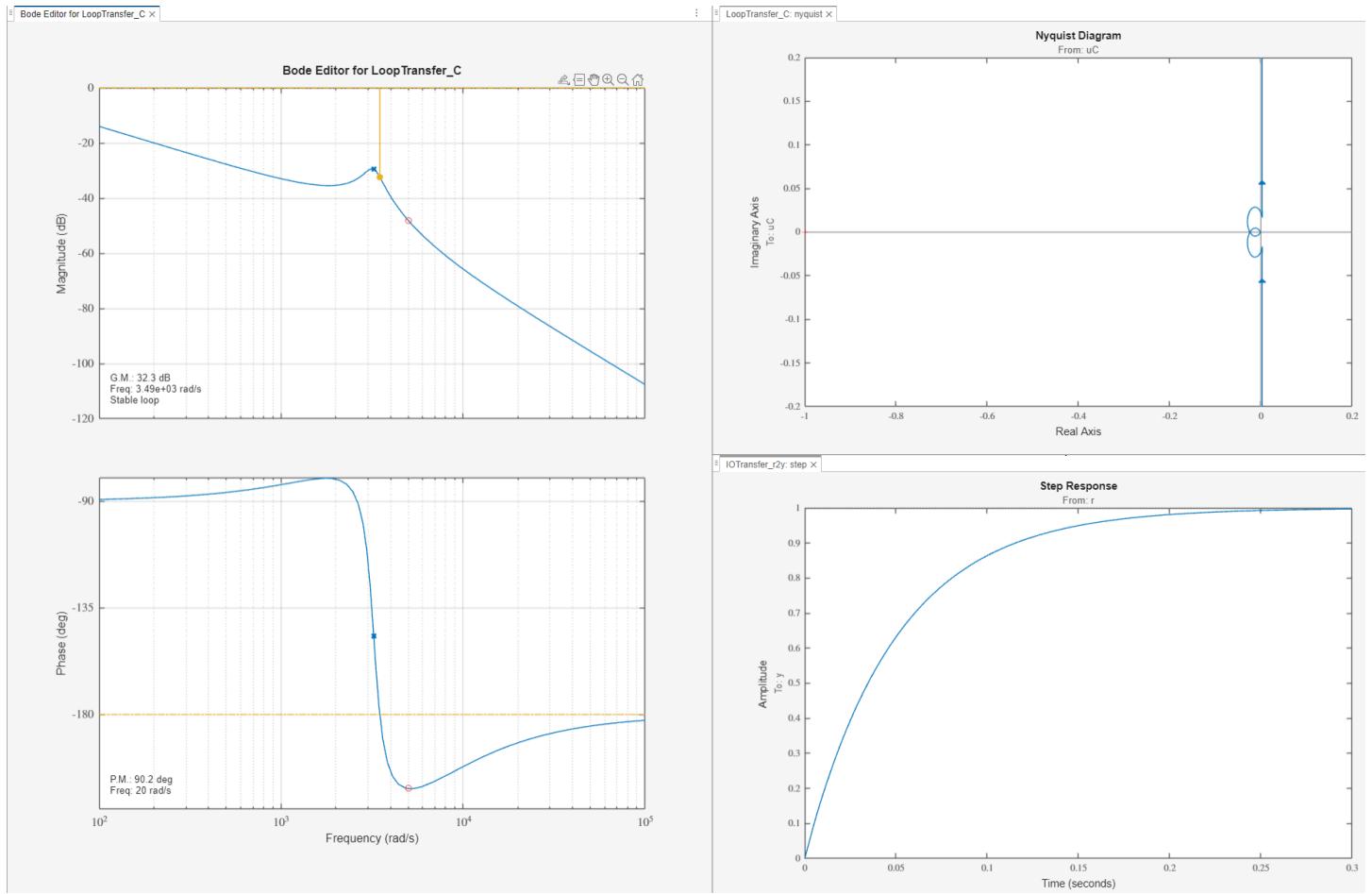


Figure 3.2: Loop transfer function $C(s)G(s)$ in sisotool.

The designed PI compensator is

$$C(s) = 0.4 \left(\frac{s/5000 + 1}{s} \right)$$

The Bode plots of $C(s)G(s)$ when $V_i = 50$ V, $R_o = 300$ Ω and $V_i = 36$ V, $R_o = 57$ Ω are shown in Figures 3.3 and 3.4, respectively.

- For $V_i = 50$ V, $R_o = 300$ Ω : $PM = 90.2^\circ > 60^\circ$ and $\omega_c = 20$ rad/s > 10 rad/s
- For $V_i = 36$ V, $R_o = 57$ Ω : $PM = 89.9^\circ > 60^\circ$ and $\omega_c = 14.4$ rad/s > 10 rad/s.

Hence, the compensated system meets the performance specifications.

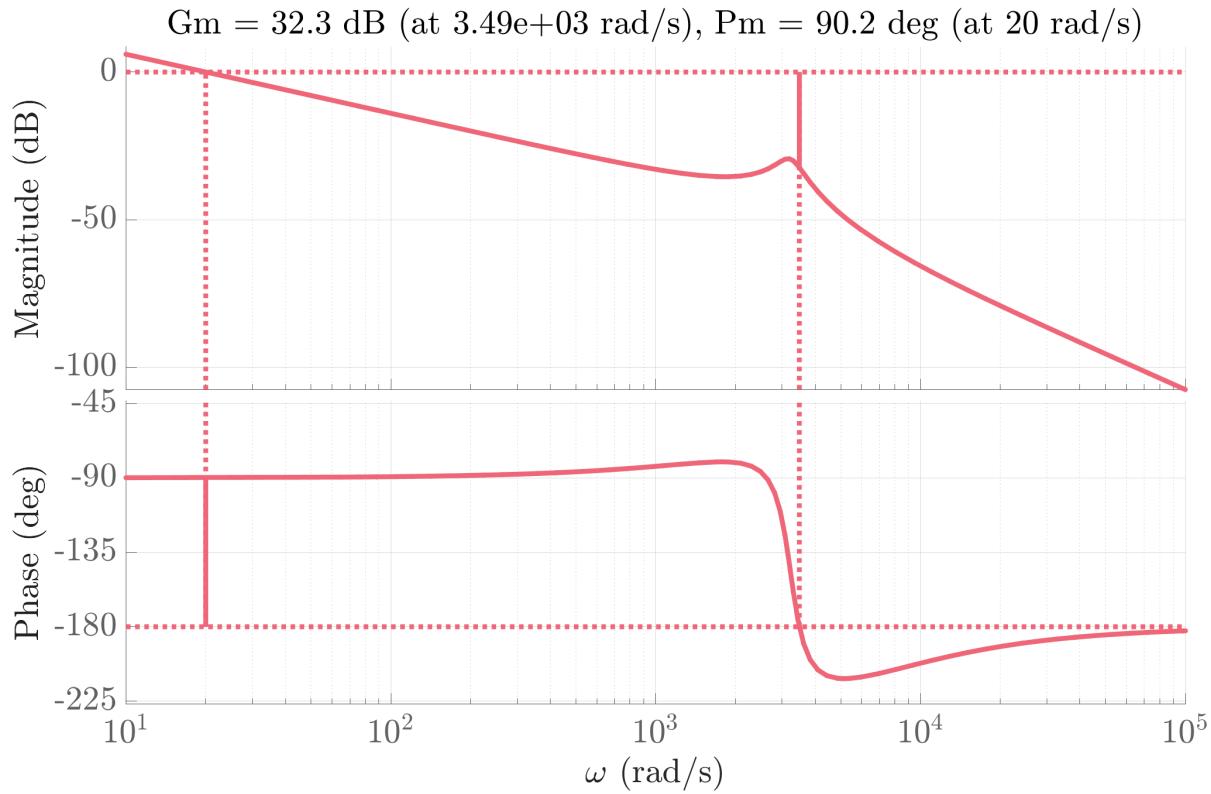


Figure 3.3: Bode plot of the loop transfer function $C(s)G(s)$ when $V_i = 50 \text{ V}$ and $R_o = 300 \Omega$.

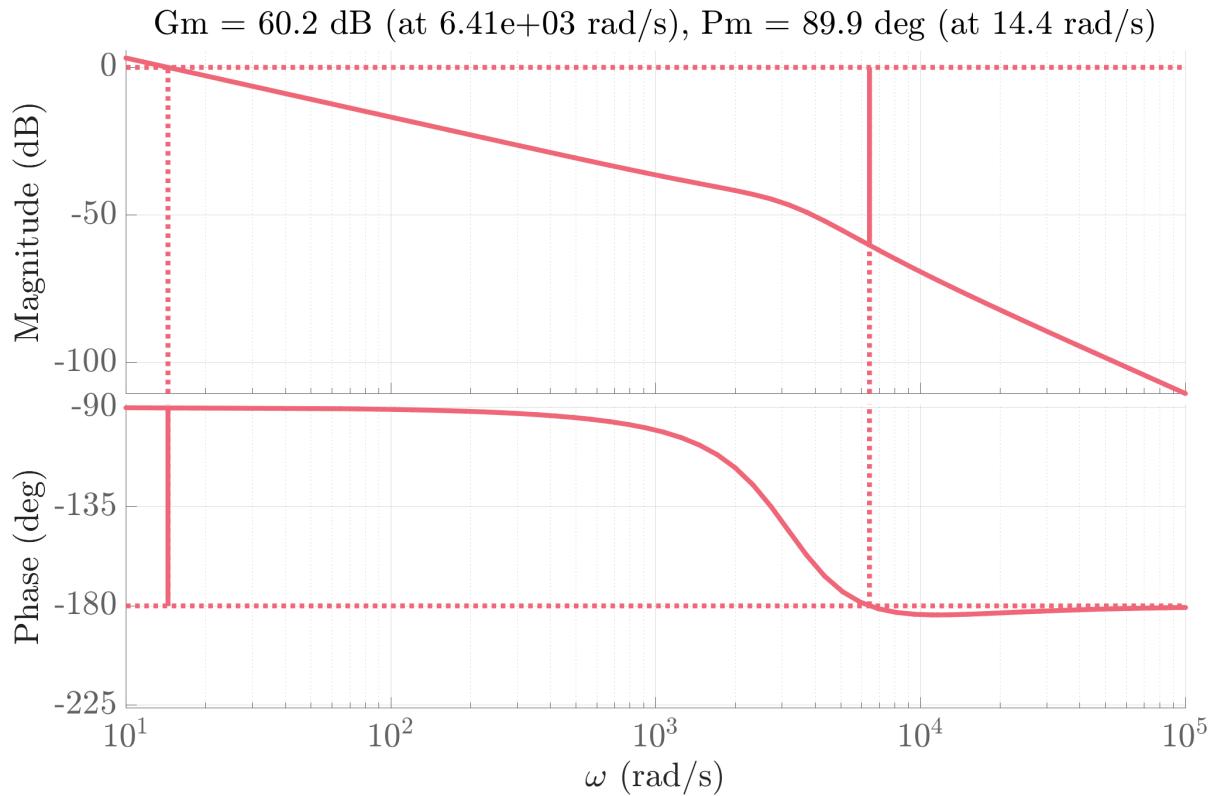


Figure 3.4: Bode plot of the loop transfer function $C(s)G(s)$ when $V_i = 36 \text{ V}$ and $R_o = 57 \Omega$.

- c) Simulate your system under load transients from $R_o = 57 \Omega$ to $R_o = 100 \Omega$. In the simulation, include non-idealities such as inductor and capacitor ESR, diode forward voltage drop, and transistor R_{on} . Present your results and discuss the observed performance. You must also model the LPF from **Question 1** in the feedback signal.

The Simulink model is shown in Figure 3.5.

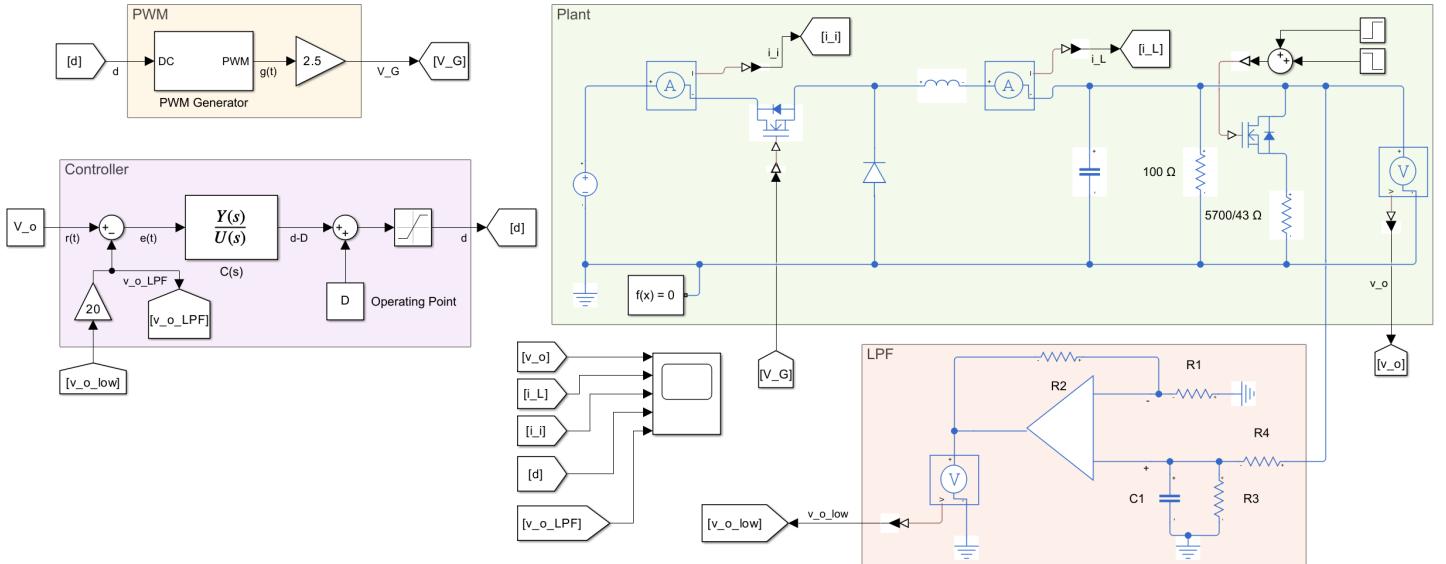


Figure 3.5: Simulink model of controlled switched buck converter with active LPF feedback.

A few notes about the design:

- The load transient is simulated using a parallel resistor network with a switch. When the switch is closed, the resistance is $R_o = 100 \parallel (5700/43) = 57 \Omega$. When the switch is open, $R_o = 100 \Omega$.
- The system is already linear so it will converge to the operating point naturally, i.e., there is no need to have D added to $d - D$. It will, however, improve the initial transient performance.
- The reference is 30 V. The active LPF has a DC gain of 1/20 and hence the controller amplifies this feedback signal by 20 to compare it to the reference.

The losses modelled are shown in Table 3.1. The values for R_L , R_{on} , and V_f were taken from each component's datasheet, with the exception of R_{on} being rounded up from 44 mΩ. A value for R_C could not be found in the datasheet, so a conservative estimate of 0.1 Ω was used based on typically quoted values [3].

Table 3.1: Nonidealities modelled in the simulation.

Nonideal Parameter	Value
Inductor ESR R_L	6.9 Ω
Capacitor ESR (LC and LPF) R_C	0.1 Ω
MOSFET R_{on}	50 mΩ
Diode Forward Voltage V_f	0.85 V

At $t = 0.3$ s, the load changes from $R_o = 57 \Omega$ to $R_o = 100 \Omega$; at $t = 0.7$ s, the load changes back to $R_o = 57 \Omega$. Plots of the simulation results when $V_i = 50$ V are shown in Figures 3.6 to 3.8.

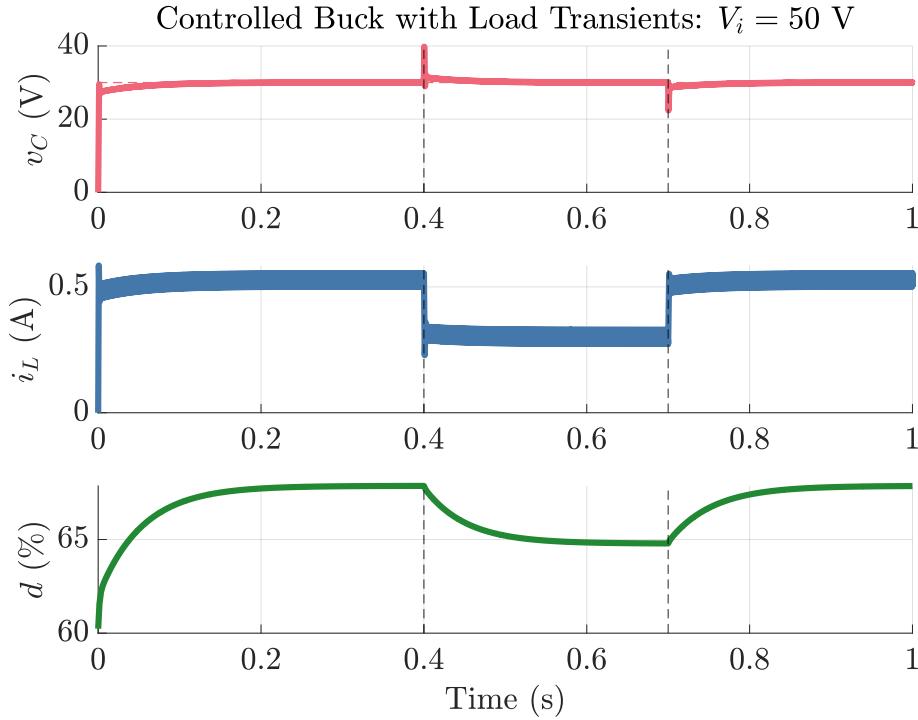


Figure 3.6: Controlled buck response to load transients, $V_i = 50$ V.

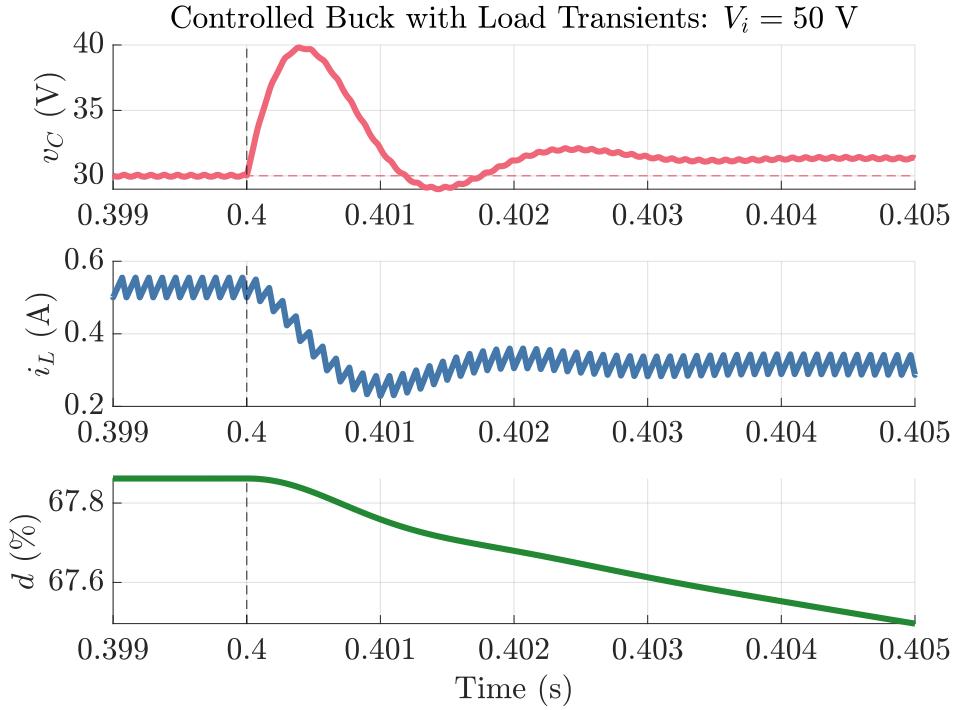


Figure 3.7: Transient response when load changes from $R_o = 57 \Omega$ to $R_o = 100 \Omega$, $V_i = 50$ V.

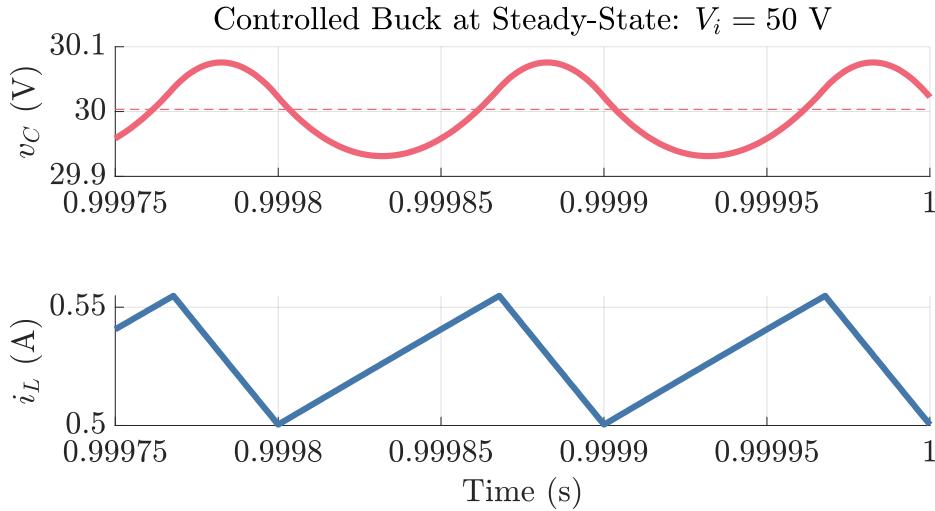


Figure 3.8: Controlled buck steady-state reference tracking, $V_i = 50$ V.

The controlled system responds decently well to load transients. From Figure 3.7, the output voltage overshoots to nearly 40 V and takes some time to return to the reference. The compensator we designed was not particularly fast as the crossover frequency was not much over spec, so this performance is expected. Figure 3.8 demonstrates that the controlled system tracks the 30 V reference despite the nonidealities that were modelled in the simulation.

Next, the simulation results when $V_i = 36$ V are shown in Figures 3.9 to 3.11.

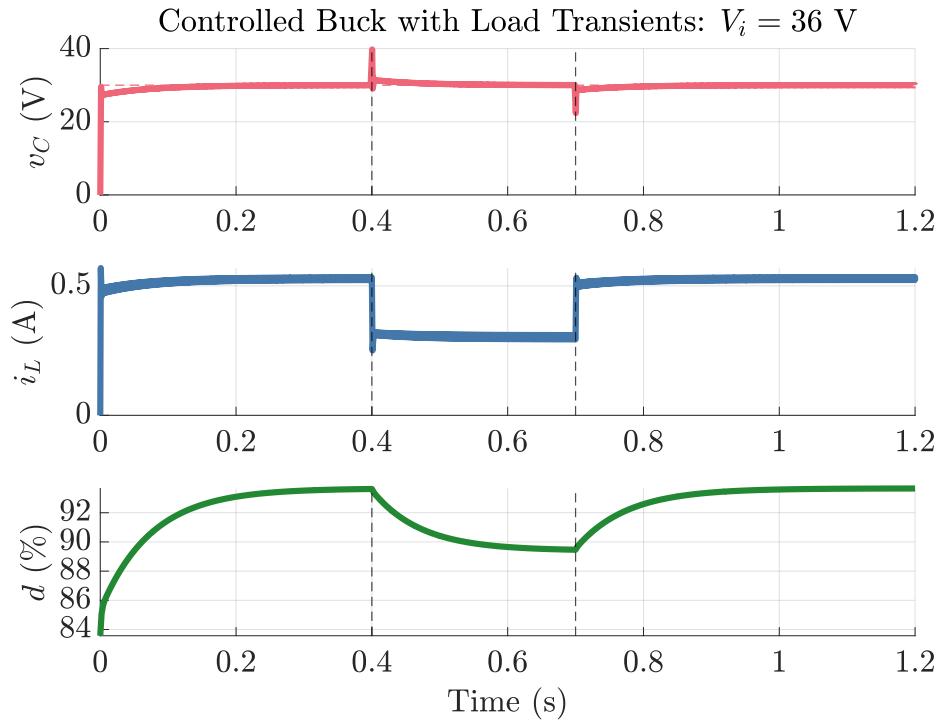


Figure 3.9: Controlled buck response to load transients, $V_i = 36$ V.

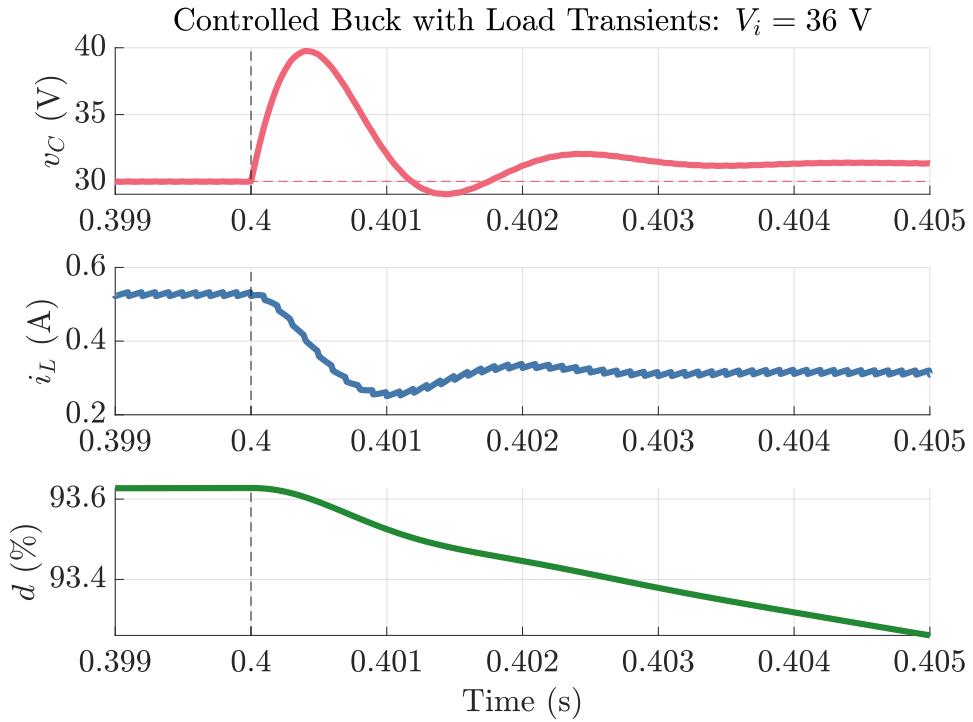


Figure 3.10: Transient response when load changes from $R_o = 57 \Omega$ to $R_o = 100 \Omega$, $V_i = 36$ V.

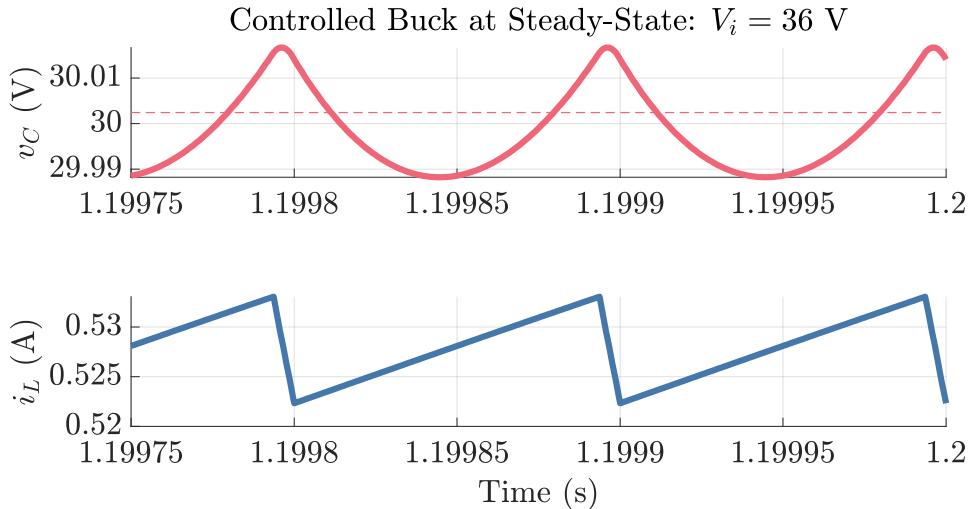


Figure 3.11: Controlled buck steady-state reference tracking, $V_i = 36$ V.

The compensated system performs as expected even with a different input voltage to the buck. To observe the effect of the active LPF, see Figure 3.12.

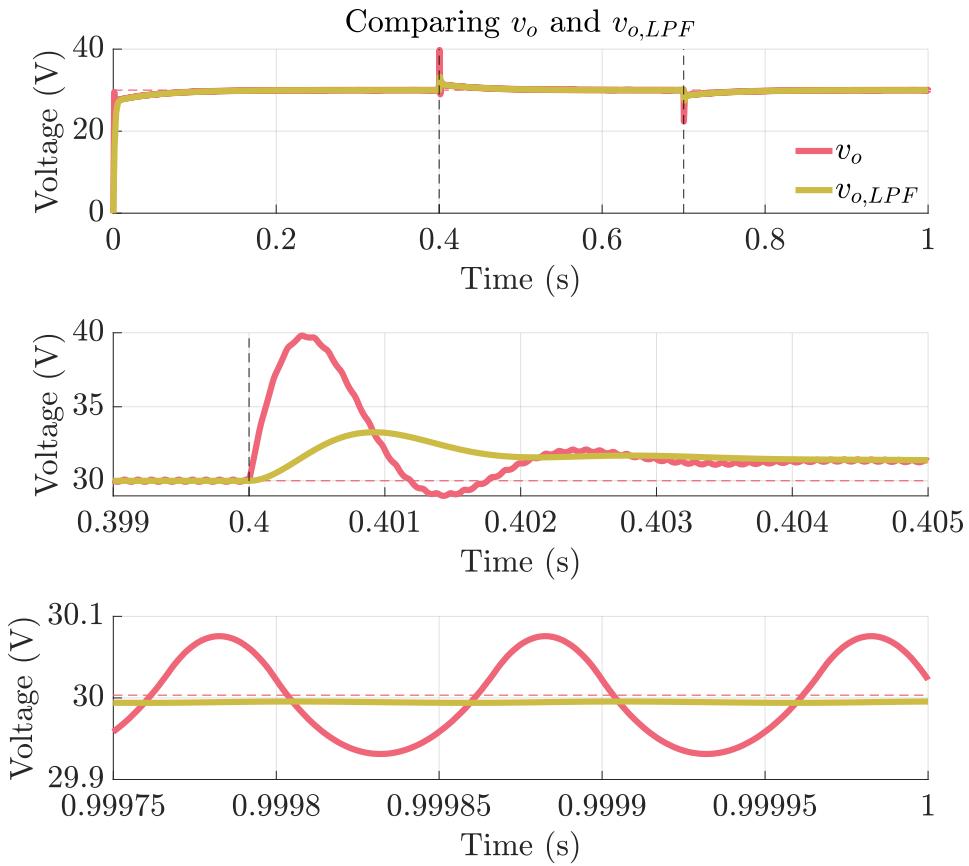


Figure 3.12: Comparison of the output voltage and active LPF output used by the controller.

Evidently, the LPF has heavily attenuated the higher frequency components of the output. This allows the controller to use a value closer to the average output voltage V_o and produce an appropriate d .

Question 4. Produce a PCB schematic, layout, and bill-of-materials (BOM).

- a) Show a high-level schematic detailing the connections. In particular, show what MCU pin is used for PWM and ADC. Show the PCB layout.

The high-level schematic is shown in Figure 4.1.

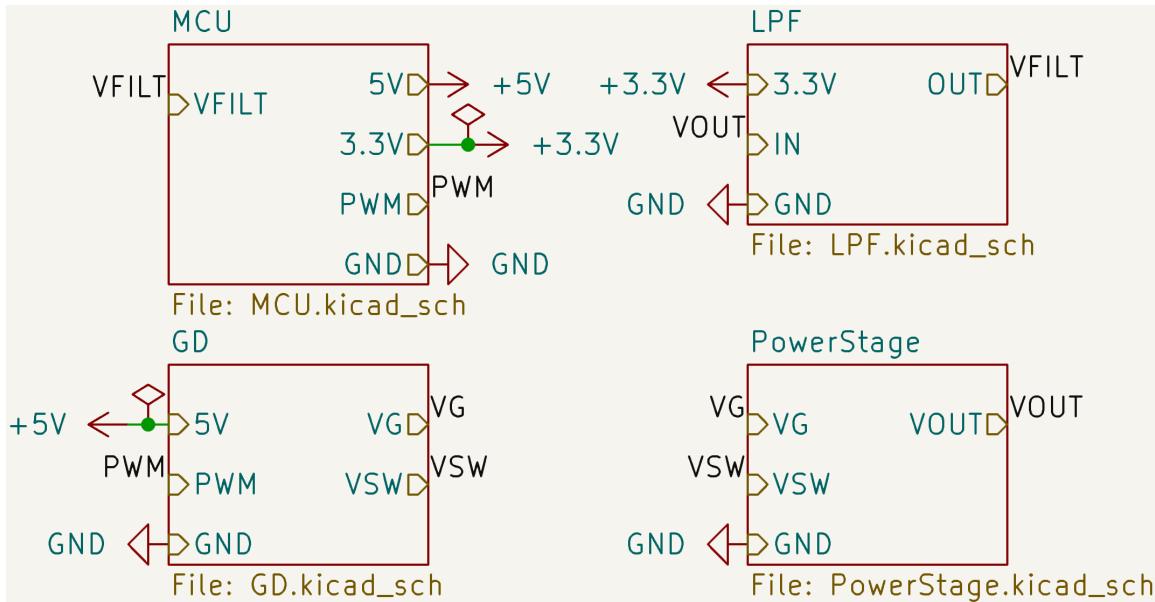


Figure 4.1: High-level schematic.

From the [LAUNCHXL-F28379D](#) board, the **J3_3** pin is used for the ADC and the **J8_5** pin is used for the PWM. These connections are shown in Figure 4.2.

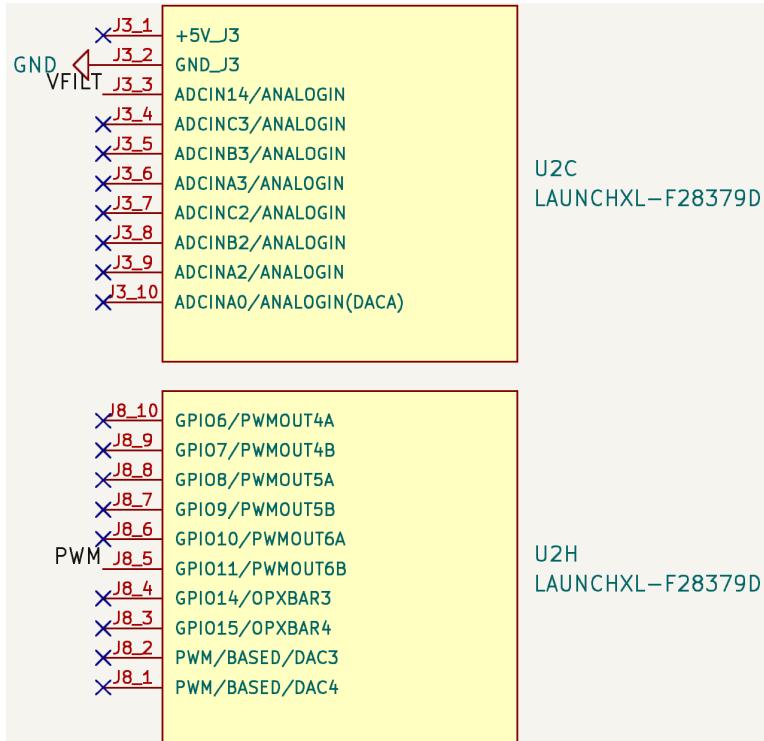
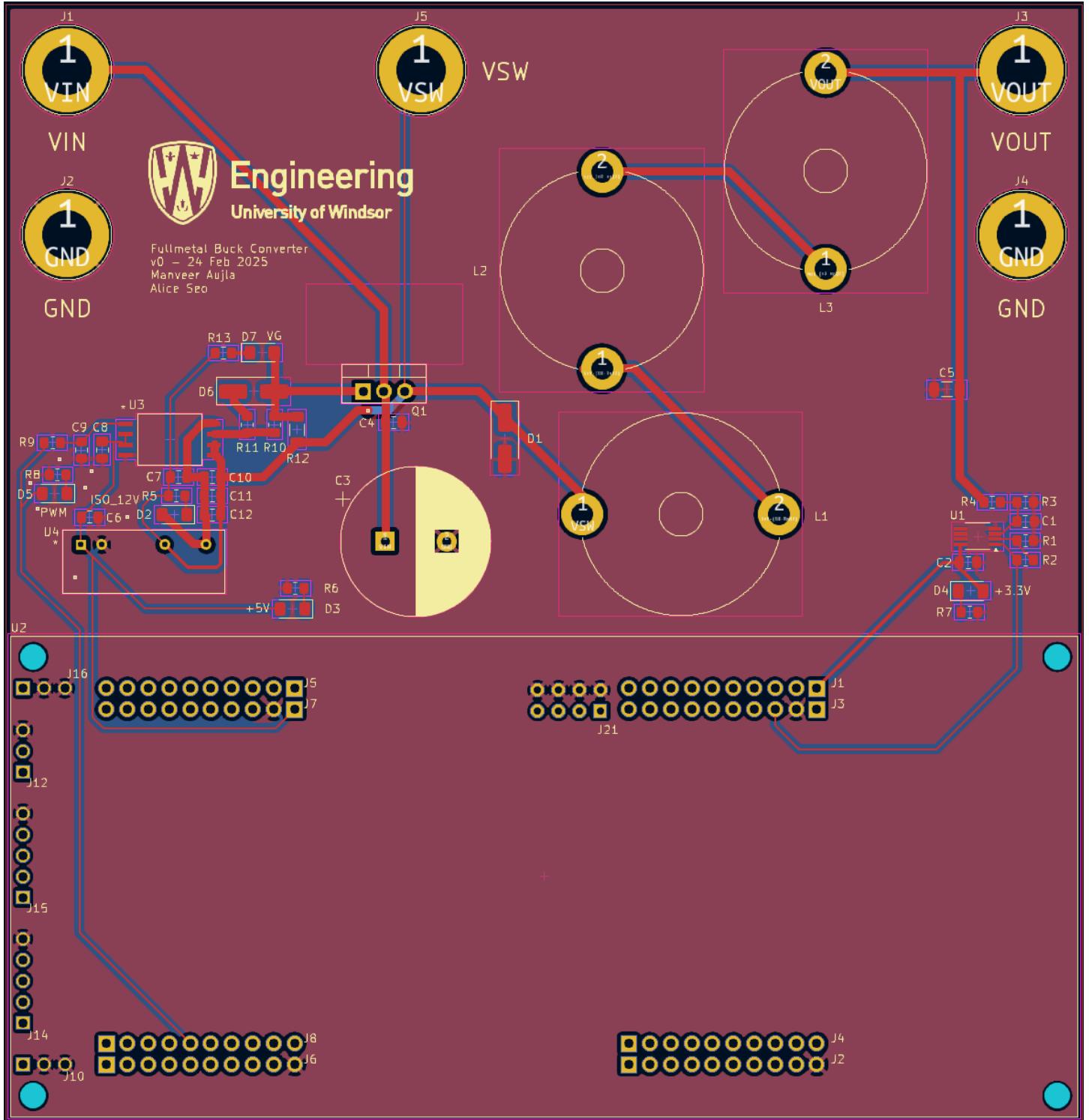


Figure 4.2: Pins used for ADC (**J3_3**) and PWM (**J8_5**).

The PCB layout is shown in Figure 4.3. The 3D view is shown in Figure 4.4.



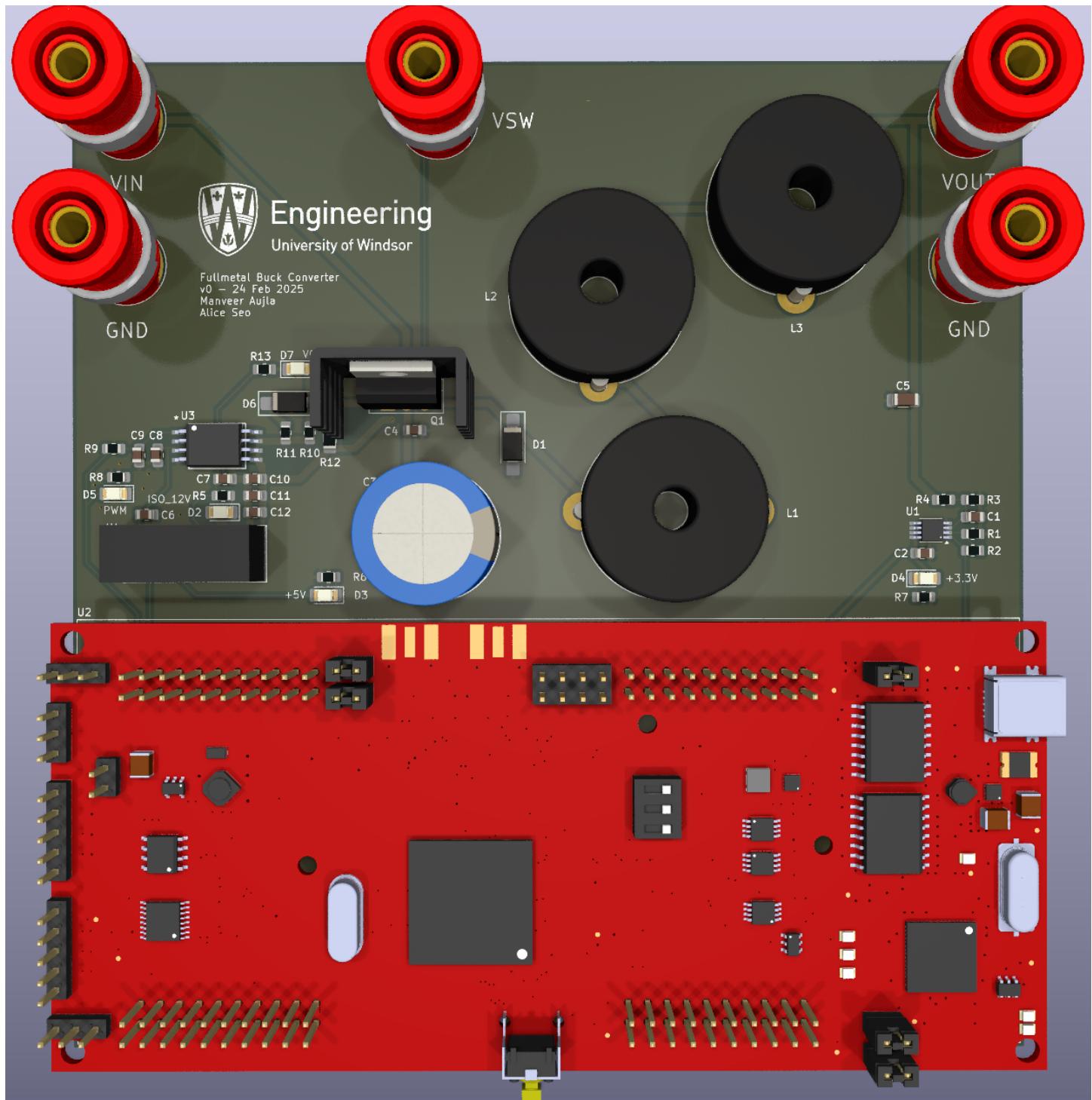


Figure 4.4: PCB 3D view.

- b) Show the LPF schematic (it should be its own hierarchical sheet) and zoomed in images of the PCB layout. Discuss your implementation including calculations such as cutoff frequencies, voltage limits, etc.

The LPF schematic is shown in Figure 4.5. The LPF in the PCB layout is shown in Figure 4.6.

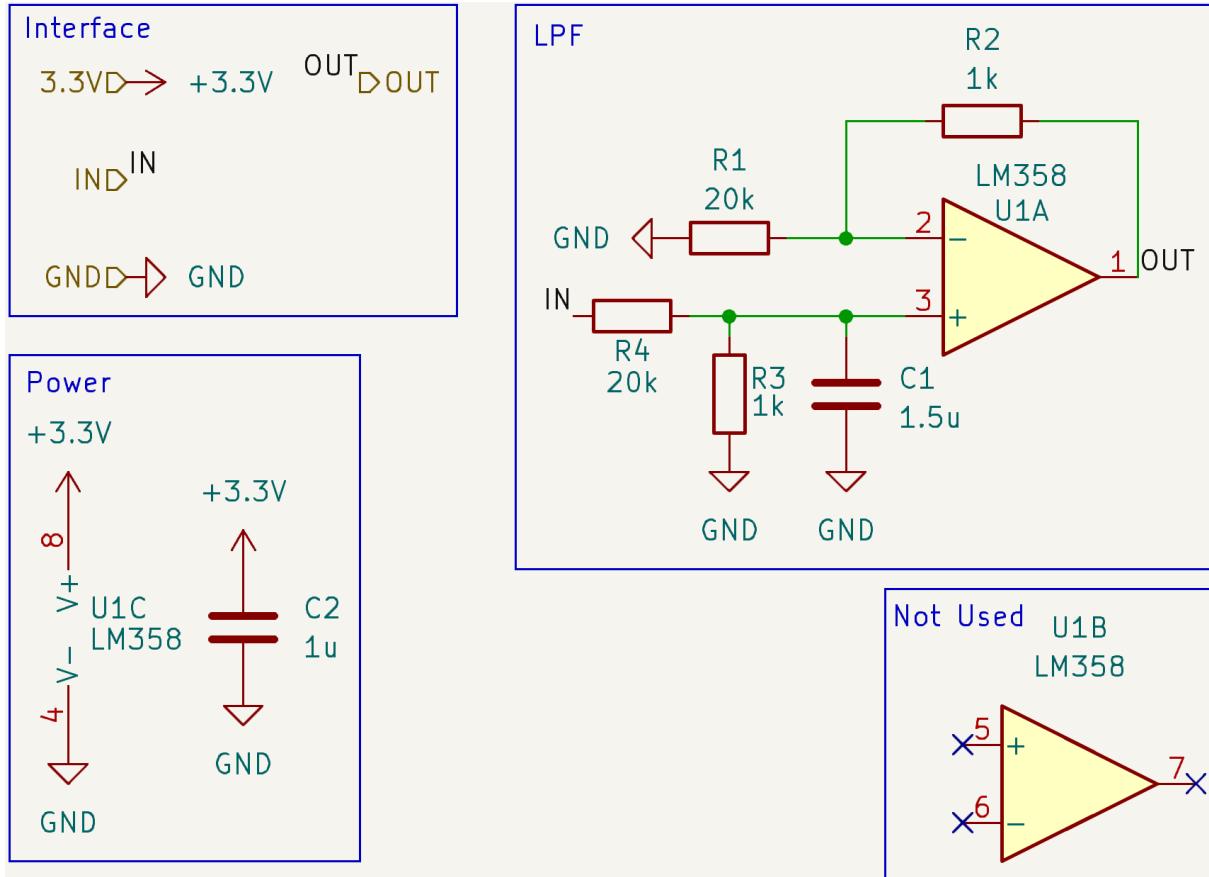


Figure 4.5: LPF schematic.

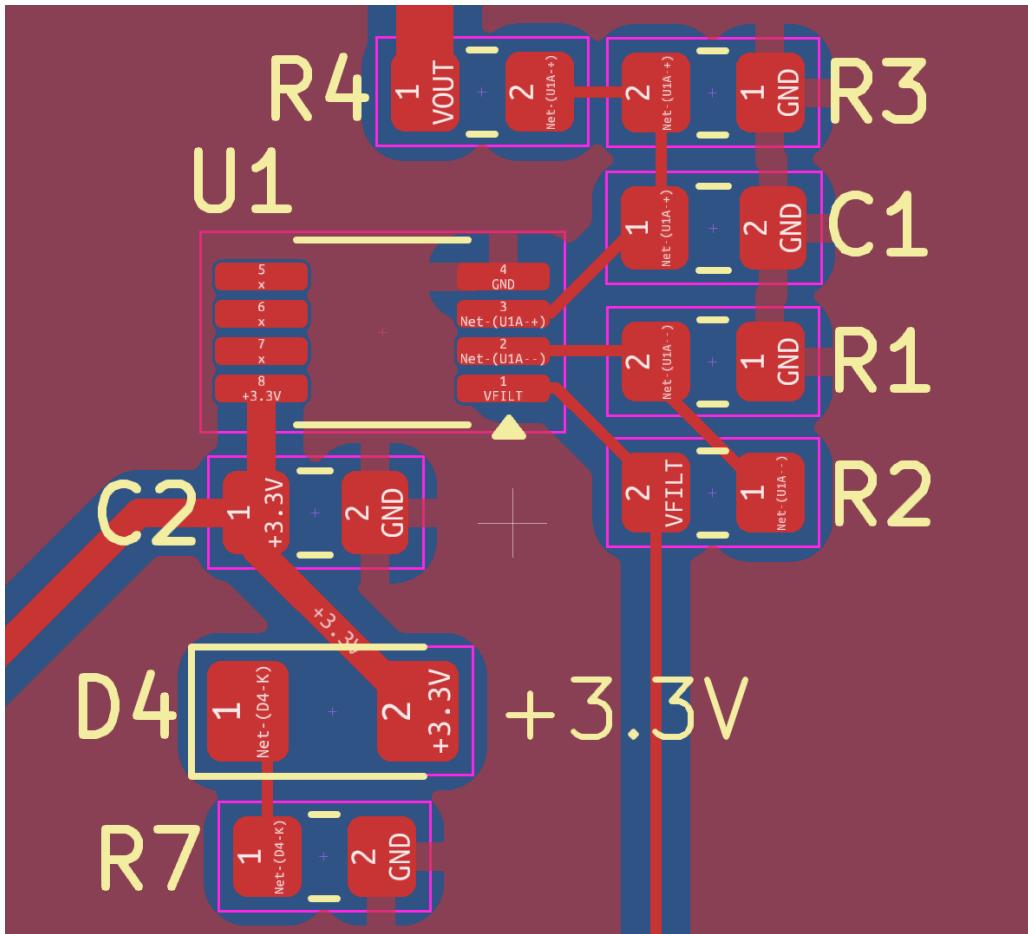


Figure 4.6: LPF in PCB layout.

In Question 1, we decided to implement a first-order Butterworth filter with the following parameters:

$$R_1 = R_4 = 20 \text{ k}\Omega$$

$$R_2 = R_3 = 1 \text{ k}\Omega$$

$$C = 1.5 \mu\text{F}$$

The specific resistors, the capacitor, and the op amp that were chosen are outlined in Table 1.1. The DC gain is 0.05 and the cutoff frequency is $f_{\text{cut}} = 111.4$ Hz. These calculations are shown in Question 1c). The only source used for designing the active LPF was Lecture 11 [1].

- c) Show the GD schematic (it should be its own hierarchical sheet) and zoomed in images of the PCB layout. Discuss your implementation including calculations such as power drawn, power supply voltages, etc.

For each subsystem, such as gate driver and sensor Op Amp filter, present a separate schematic representation and include links to sources you used to make your designs, such as reference design and datasheets.

Upload your KiCAD project, including library files, to github. Include a link to your project in the deliverable PDF.

The GD schematic is shown in Figure 4.7. The GD in the PCB layout is shown in Figure 4.8.

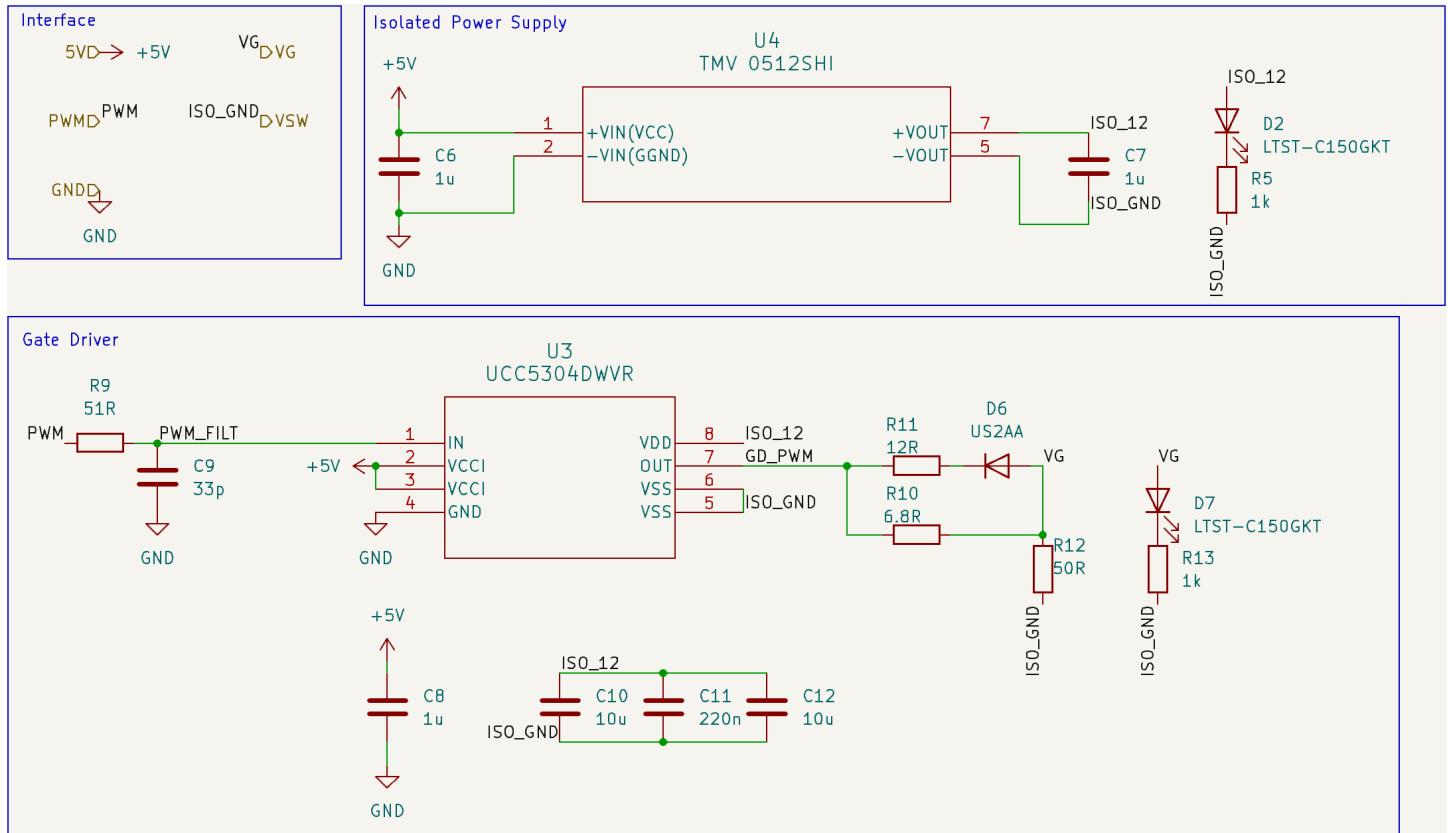


Figure 4.7: GD schematic.

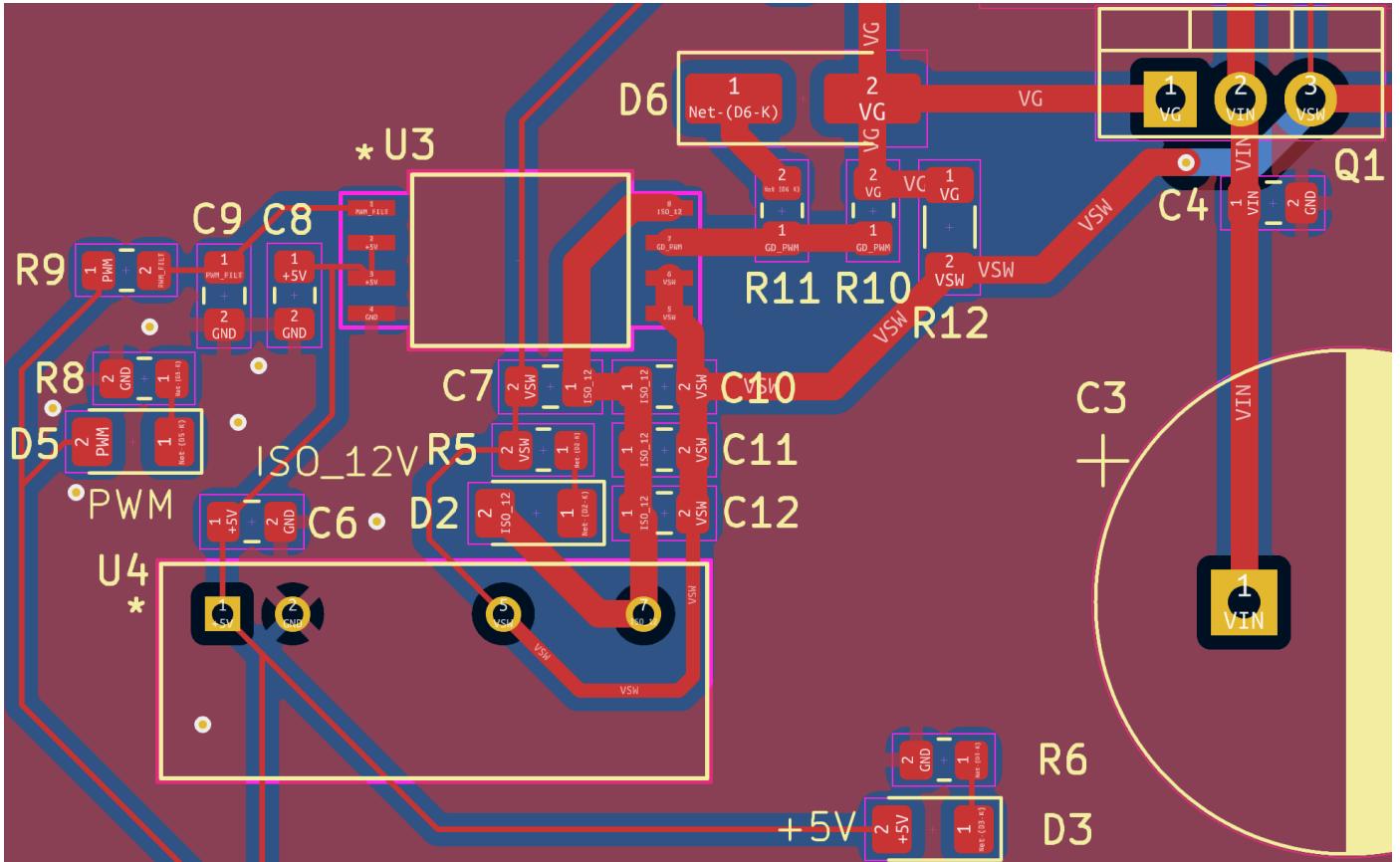


Figure 4.8: GD in PCB layout.

Some notes about the GD implementation:

- The [UCC5304DWVR](#) GD and [TMV 0512SHI](#) isolated power supply were selected by default for this project, as together they worked to meet the required gate voltage of the [IRF540NPBF](#) MOSFET.
- The power supply uses $1 \mu\text{F}$ tantalum capacitors at the input and output for decoupling.
- The PWM RC filter at the input of the GD (U3) comprised of the 51Ω resistor (R9) and 33 pF capacitor (C9) was made based on the “Typical Application” (9.2.2.1) of the [GD datasheet](#).
- The resistor and diode network at the output of the GD (R10, R11, R12, & D6) was made based on the “Typical Application” (9.2) of the [GD datasheet](#). Resistors were chosen to have at least a 0.5 W power rating since the GD_PWM signal can be 12 V causing 0.125 W to be insufficient.
- The [GD datasheet](#) gives recommendations for selecting a VCCI capacitor (9.2.2.3.1) and a VDD capacitor (9.2.2.3.2); hence, the capacitors C8, C10, C11, and C12 were selected based on this advice.

To ensure that all resistors had a sufficient power rating, some calculations were necessary. The indicator LED used has a forward voltage of $V_f = 2.1 \text{ V}$ and is sufficiently bright with 10 mA . So, each indicator LED needs to have a series resistor such that the current is roughly 10 mA . This calculation was performed for each indicator LED to determine the required resistance, and a sample calculation for the LED to indicate the ISO_12V signal is as follows:

$$R = \frac{12 - 2.1 \text{ V}}{10 \text{ mA}} = 990 \Omega \approx 1 \text{ k}\Omega$$

So, applying 12 V to the LED and $1 \text{ k}\Omega$ resistor in series will cause a diode current of roughly 10 mA .

The MCU schematic is shown in Figure 4.9.

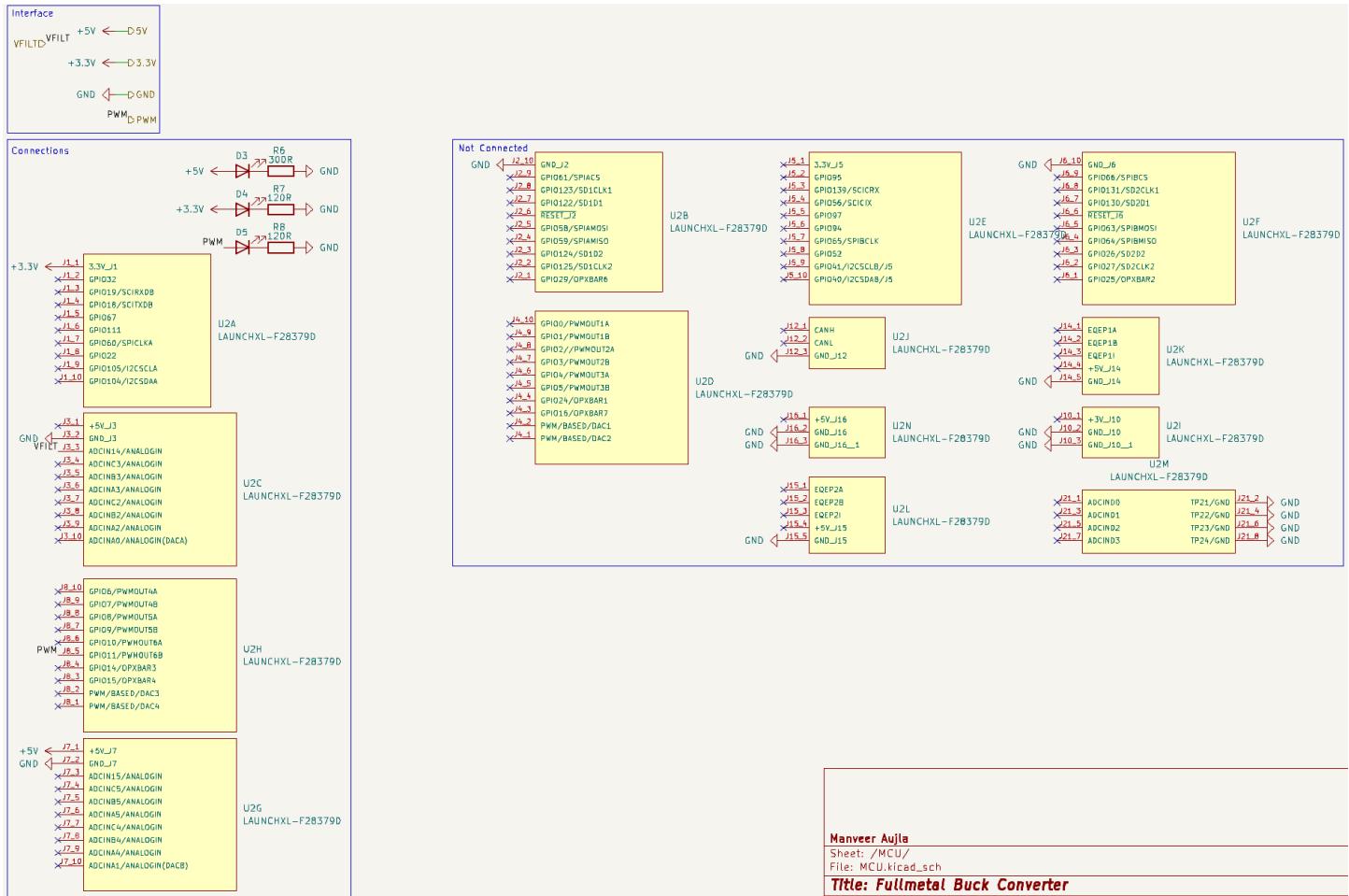


Figure 4.9: MCU schematic.

From the MCU, we use the 3.3 V, 5 V, GND, ADCIN, and GPIO/PWMOUT pins for our application. The other pins are not connected.

The power stage (buck converter) schematic is shown in Figure 4.10.

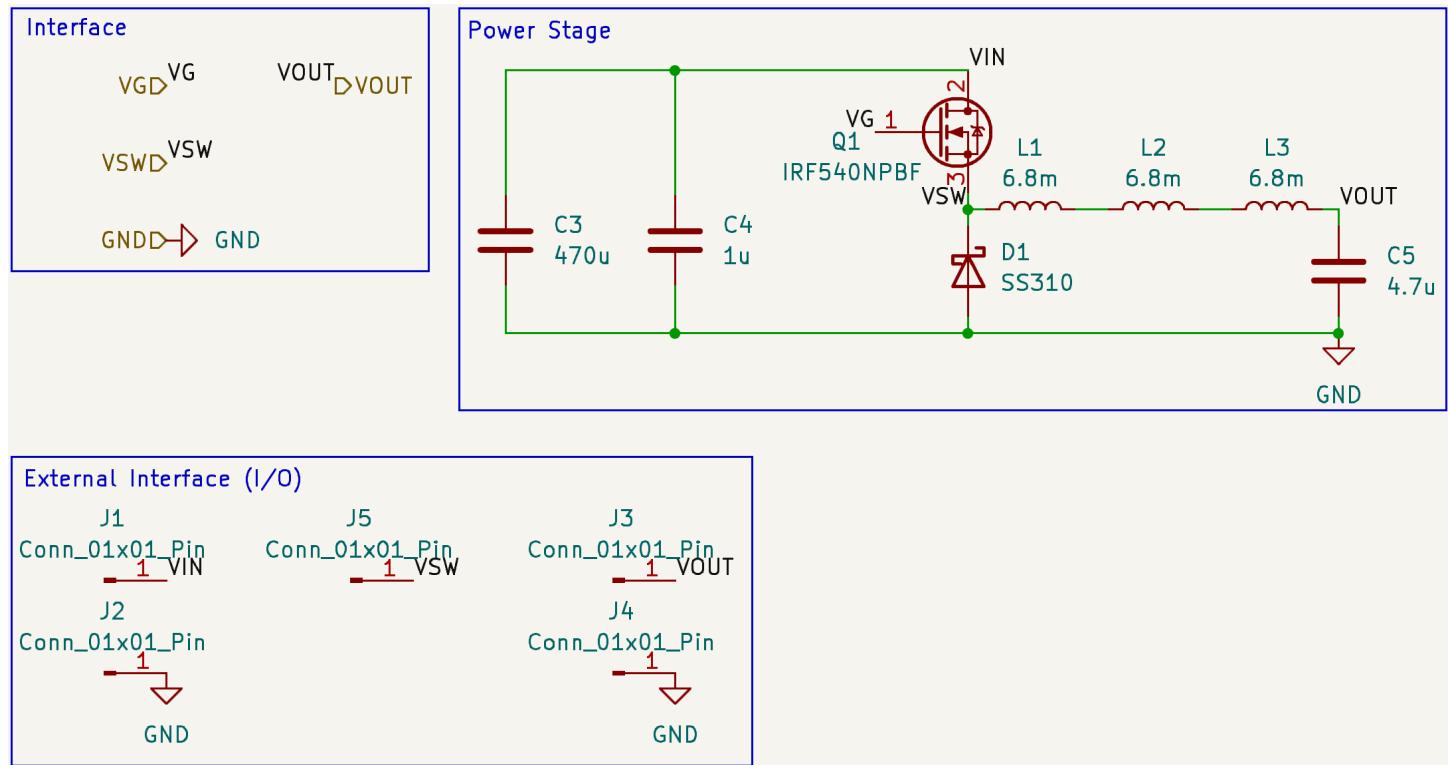


Figure 4.10: Power stage schematic.

The decision to choose the inductor and capacitor has been discussed at length in Question 2. The specific components chosen are outlined in Table 2.1. The IRF540NPBF MOSFET has been selected as the active switch with the 507302B00000G heatsink. The SS310 diode will be used as the second switch.

All of the project files can be found at the [GitHub repository here](#). The BOM (also included on GitHub) is shown below in Table 4.1. Uploading the BOM onto Digikey, as of Feb 23, the subtotal is \$155.22.

Table 4.1: Bill of materials.

Reference	Part Number	Description	Value	Qty
C1	CGA4J3X7R1H155K125AB	LPF Cap	1.5u	1
C2,C6,C7,C8	TMCP1D105MTRF	Tantalum Cap	1u	4
C3	100ZLH470MEFC16X31.5	Electrolytic Cap	470u	1
C4	GRM21BC72A105KE01L	Ceramic Cap	1u	1
C5	GRM31CC72A475KE11L	Output Cap LC	4.7u	1
C9	C0805C330K5GACTU	GD Input Filter	33p	1
C10	F951C106MPAAQ2	ISO_12 C _{VDD}	10u	1
C11	C0805C224K5RACTU	ISO_12 C _{VDD}	220n	1
C12	GRM21BR61E106KA73L	ISO_12 C _{VDD}	10u	1
D1	SS310	Buck Diode	---	1
D2,D3,D4,D5,D7	LTST-C150GKT	Indicator LEDs	---	5
D6	US2AA	GD Output	---	1
J1,J2,J3,J4,J5	BU-P72930-2	Banana Jacks	---	5
L1,L2,L3	1468507C	Inductor LC	6.8m	3
Q1	IRF540NPBF	Buck MOSFET	---	1
Q1 Heatsink	507302B00000G	Heatsink for Q1	---	1
Q1 Heatsink Kit	4880G	Mounting Kit	---	1
R1,R4	RC0805FR-0720KL	LPF	20k	2
R2,R3,R5,R13	RMCF0805FT1K00	LPF, 12 V LED	1k	4
R6	RMCF0805JT300R	5 V LED	300R	1
R7,R8	RMCF0805FT120R	3.3 V LED	120R	2
R9	RC0805FR-0751RL	GD Input Filter	51R	1
R10	RCS08056R80FKEA	GD_PWM R	6.8R	1
R11	ERJ-P06J120V	GD_PWM R	12R	1
R12	RCP1206W50R0GEB	GD_PWM R	50R	1
U1	LM358DGKR	LPF Op Amp	---	1
U2	LAUNCHXL-F28379D	MCU	---	1
U2 Pin Header	TSW-110-07-F-D	MCU Header	---	4
U3	UCC5304DWVR	Gate Driver	---	1
U4	TMV 0512SHI	Isolated PS	---	1

Question 5. Discuss the risks to persons and equipment incurred during testing this project, especially before the design has been experimentally validated.

Provide an itemized bring-up plan for your board and, for each item, discuss what the objective and theoretical motivation for the test or inspection.

The major risks to both persons and equipment include:

- **Overheating**

Operating the converter for a long time can cause thermal issues. To mitigate this, we have used a heat sink for the MOSFET. We plan to test the circuit in a well-ventilated environment, and in the case of overheating, the input power will be removed to mitigate damage.

- **Circuit component damage due to overcurrent and overvoltage**

Components can be damaged if the circuit is operating over the current and voltage limitations. For example, the MCU and ICs have relatively low voltage ratings, and the maximum inductor current is 556 mA. When testing, we will apply an input voltage to the buck that is within the rated range (36 – 50 V) and use a current-limited source.

- **Electrical shock hazards**

Electrical shock hazards must be also considered especially when testing with significant voltage (in our case, 50 V). To minimize the risk of shock, we will ensure proper grounding of the buck, remove any jewellery that could conduct electricity, and prepare to turn off the input source in case of an emergency.

- **Soldering risks**

When soldering the PCB, we will use the appropriate Personal Protective Equipment (PPE). Soldering will be done with adequate ventilation (e.g., a fume hood) to avoid inhalation of fumes. Also, proper soldering techniques will be employed to avoid component/PCB damage.

The bring-up plan for our board is as follows:

1. **Out-of-box visual inspection:** Physically examine and check for major manufacturing defects. We want to ensure that the board is undamaged before doing any work. For example, check for
 - a. damage to the solder mask, such as dents and scratches;
 - b. missing or damaged components/traces; and
 - c. misaligned footprints/pads.
2. **Build & solder the board:** Ensure that all components have arrived from Digikey and are undamaged. Then, solder them onto the board, following all safety guidelines.
3. **Post-solder visual inspection:** Ensure soldering has not damaged any components or the board and confirm the absence of any short circuits from soldering. Verify that all components are securely mounted/soldered onto the board.
4. **Multimeter inspection:** Before powering the board, we should check that it is safe to do. With the board unpowered, use a multimeter to check continuity, resistance, and capacitance values for PWR/GND planes, traces, and components against our expectations. This includes measuring the ESR of components and checking continuity of all I/O.
5. **IC power & sanity test:** Before applying a significant voltage, we want to make sure the low voltage subsystems work. Supply power to the MCU using $V_{CC} = 5$ V. Then,
 - a. Check if GD, isolated power supply, and LPF receive sufficient voltage.
 - b. Confirm with indicator LEDs that 3.3 V, 5 V, and 12 V sources are on.
 - c. Ensure the isolated power supply has successfully converted from 5 to 12 V.
 - d. Confirm that the isolated power supply ISO_GND is isolated from GND.
 - e. Ensure that the GD is receiving $V_{DD} = 12$ V.
6. **Full power test:** Supply 36 V to the board input VIN from a reliable, current-limited source. Then,
 - a. Verify that the MCU is receiving less than 3.3 V from the active LPF. Ideally, it should be about $0.05(30) = 1.5$ V.
 - b. Verify that the output voltage is roughly 30 V.
 - c. Verify relevant waveforms using an oscilloscope to ensure the design specifications have been met, including steady-state ripple and load transient performance.

References

- [1] Caniggia Viana. *Lecture 11 – PCB Design*. 2025. University of Windsor.
- [2] Caniggia Viana. *Lecture 3 – Steady-State Analysis 1*. 2025. University of Windsor.
- [3] General Atomics. *Engineering Bulletins Capacitors*. URL: http://www.ieca-inc.com/images/Equivalent_Series_Resistance_ESR.pdf