

EC446

# SUBMICRON DEVICES

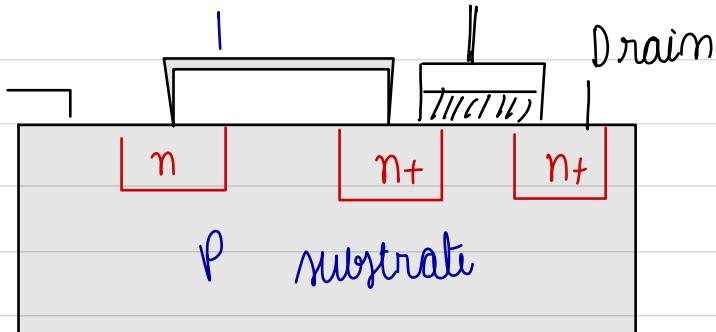
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211EC228

# SUB MICRON DEVICES

Integrated circuit technology:

- Single monolithic chips is used for integrated circuit.
- All components are realized in the chip by means of junctions diffusion region etc.

metal contacts



Materials:

Si, SiGe, GaN,  $\text{Ga}_2\text{O}_3 \rightarrow$  Semiconductor  
 $\text{SiO}_2$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{HfO}_2$ ,  $\text{Si}_2\text{N}_3 \rightarrow$  Insulator  
Poly Si, Ti, Al, Au, Ag, Ni, Cu  $\rightarrow$  Metal  
B, P, Ar, Si  $\rightarrow$  Dopant

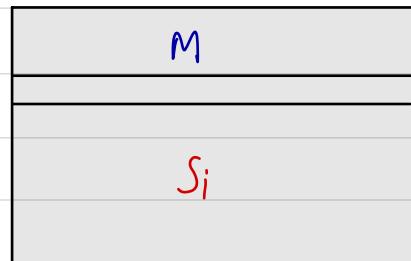
Si - Crystalline

Si - Amorphous

Poly Si - Polycrystal

Why Si?

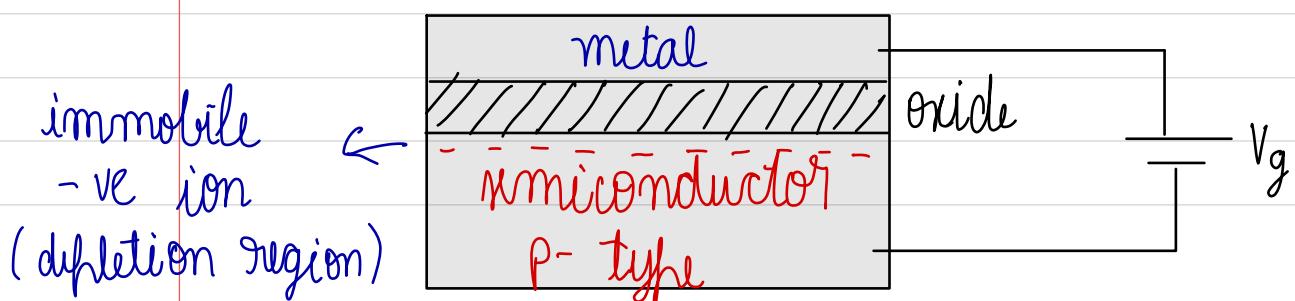
- Widely available as Sand extraction and fabrication
- Well established process
- Natural oxide of Si  $\rightarrow \text{SiO}_2$  can act as mask for self aligned processes
- Si -  $\text{SiO}_2$  interface is having less diff mobility.



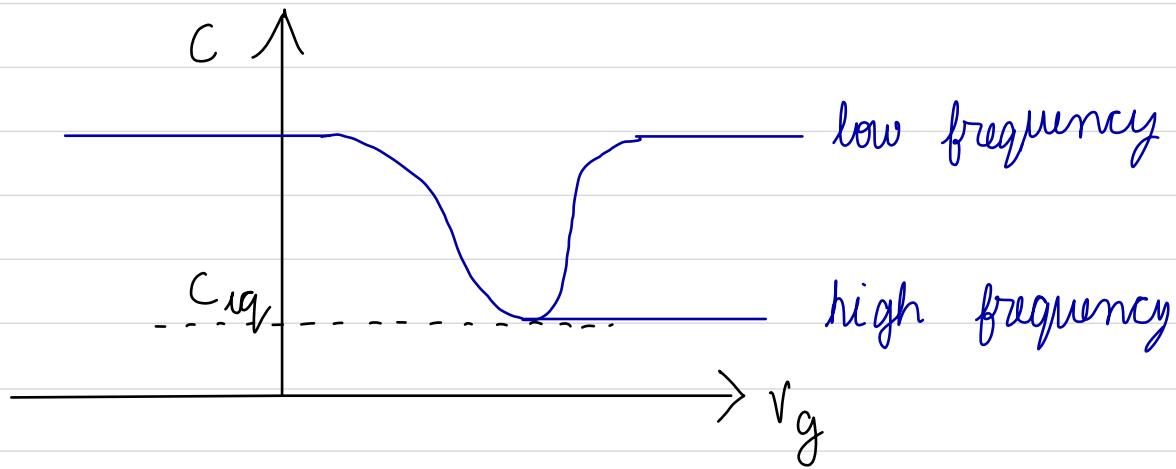
Differences in metal contact & Poly Si contact

Metal	Poly Si
→ Less melting point	→ Higher melting point
→ Depletion is not there	→ Gate Poly Si depletion is there
→ Used in FinFET as metal stack	→ Used in high voltage devices

MOSFET: Metal oxide semiconductor field effect transistors



If  $V_g$  increases, depletion region increases.



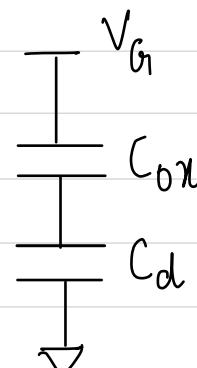
$C = p$  type MOS capacitor.

It has 3 regions: accumulation, depletion, -ve +ve

high +ve

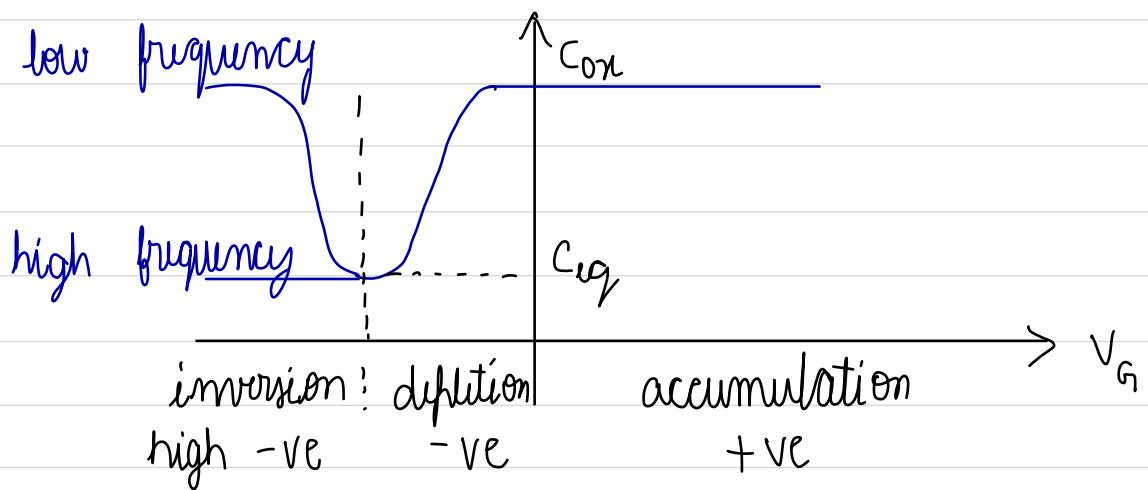
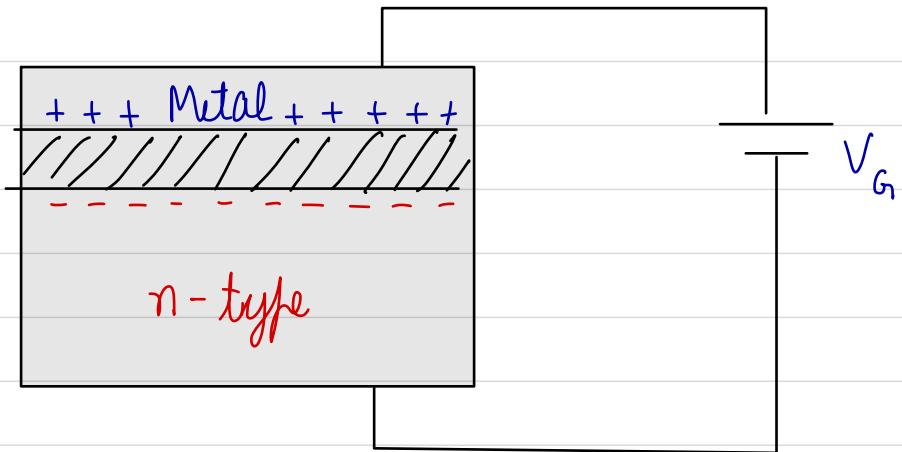
When high voltage is applied, it results in the formation of inversion layer due to electrons from battery getting deposited on substrate.

$$C_{ox} = \frac{\epsilon_{ox} \epsilon}{d}$$



$$C_{eq} = \frac{C_{ox} C_d}{C_{ox} + C_d}$$

$C = \frac{dQ}{dV}$  in lower frequency voltage change is less hence can capture charge resulting in higher capacitance.



Semiconductor : Intrinsic  
Extrinsic

Modulating conductivity :

- Doping : donors  $\rightarrow$  acceptor - p types (excess holes)  
 $\rightarrow$  donor - n type (excess electrons)
- Increasing temperature will increase free  $e^-$  and conduction increases.
- applying light

Intrinsic semiconductor: • without any impurity  
 • number of holes = number of electrons  
 • adding opposite impurity  $\rightarrow$  compensation

When Temperature increases (say 700 K) electron concentration changes from:  $10^{16}/\text{cm}^3$  to  $10^{18}/\text{cm}^3$ .

- For extrinsic semiconductor, increase temperature to make it intrinsic.
- Or add opposite element.

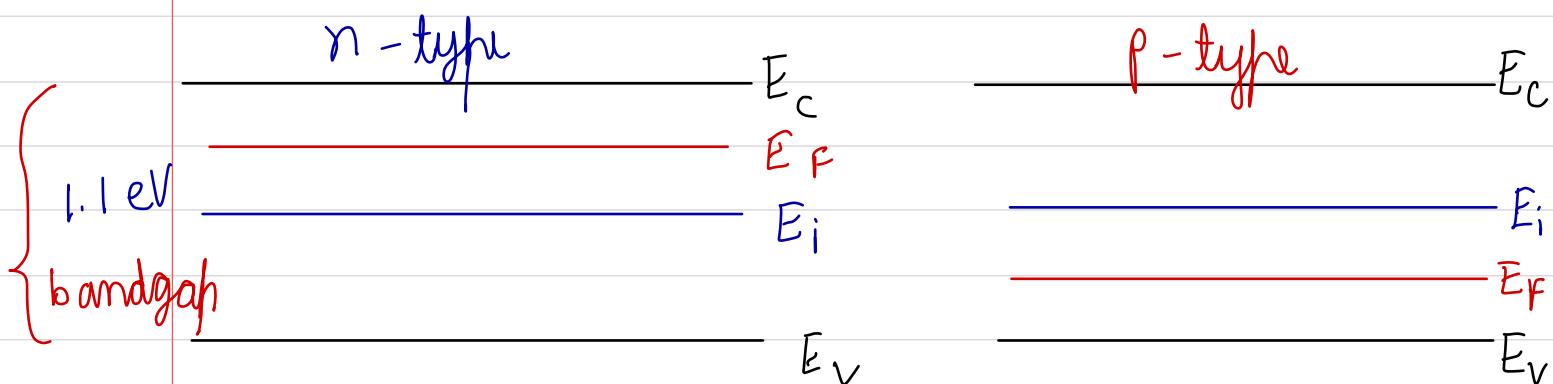
Fermi level:

Fermi - dirac distribution function: Probability that an available energy state at  $E$  will be occupied by an electron at absolute temperature  $T$

$$f(E) = \frac{1}{1 + e^{(E-E_F)/kT}}$$

$k$  = Boltzmann constant =  $8.62 \times 10^{-5} \text{ eV/K}$

$E_F$  = Fermi level



$E_V$  = valence band

$E_i$  = intrinsic level

$E_c$  = conduction band

$E_F$  = Fermi level

$$\begin{array}{l} \text{n type : } n_0 = n_i e^{(E_F - E_i)/kT} \\ \text{p type : } p_0 = n_i e^{(E_i - E_F)/kT} \end{array}$$

$$n_i = \text{intrinsic concentration} = 1.5 \times 10^{10}/\text{cm}^3$$

$$\text{For intrinsic : } E_i = E_F$$

Q> Find  $E_F - E_i$  if  $n_0 = 5 \times 10^{17}/\text{cm}^3$  at 300K  
 Ans  $n_0 = n_i e^{\chi/kT}$   $\chi = \frac{E_F - E_i}{kT}$

$$\chi = \frac{RT \ln \frac{n_0}{n_i}}{kT}$$

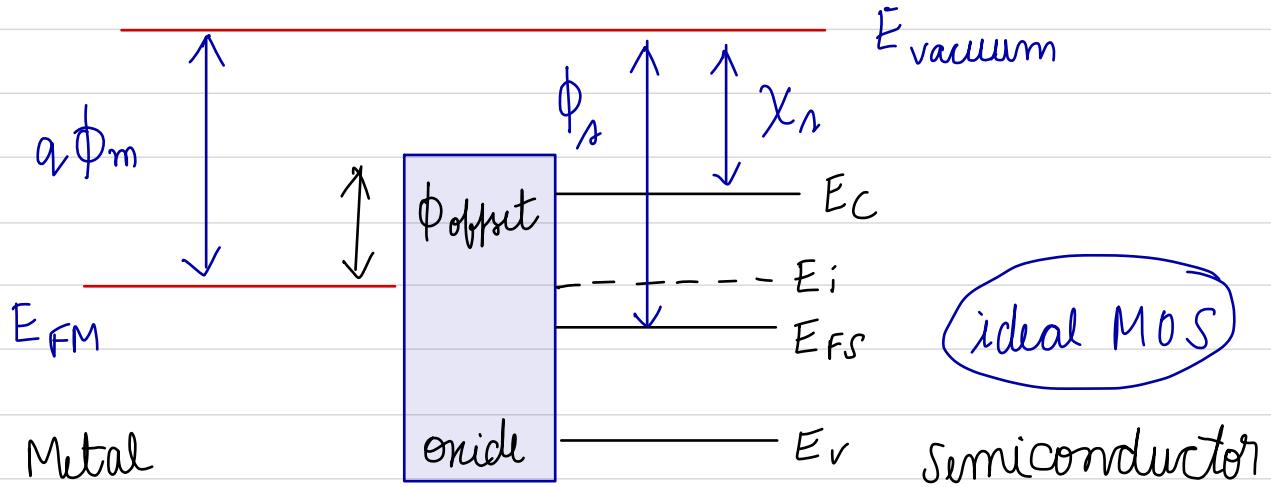
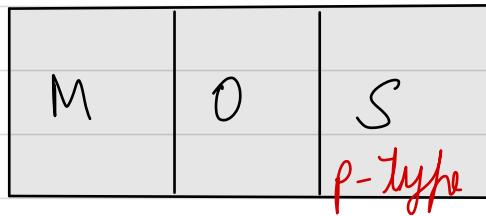
$$\chi = 8.62 \times 10^{-5} \times 300 \ln \frac{5 \times 10^{17}}{1.5 \times 10^{10}}$$

$$E_i - E_F = 0.447 \text{ eV}$$

$$\text{NOTE: } n_0 p_0 = n_i^2 \quad \text{at } 300 \text{ K}$$

Q> Find  $p_0$  if  $n_0 = 5 \times 10^{17}/\text{cm}^3$  at 300K  
 Ans  $n_0 p_0 = n_i^2$   
 $p_0 = \frac{(1.5 \times 10^{10})^2}{5 \times 10^{17}} = 0.45 \times 10^3$   
 $\therefore p_0 = 450/\text{cm}^3$

P - TYPE      bands :

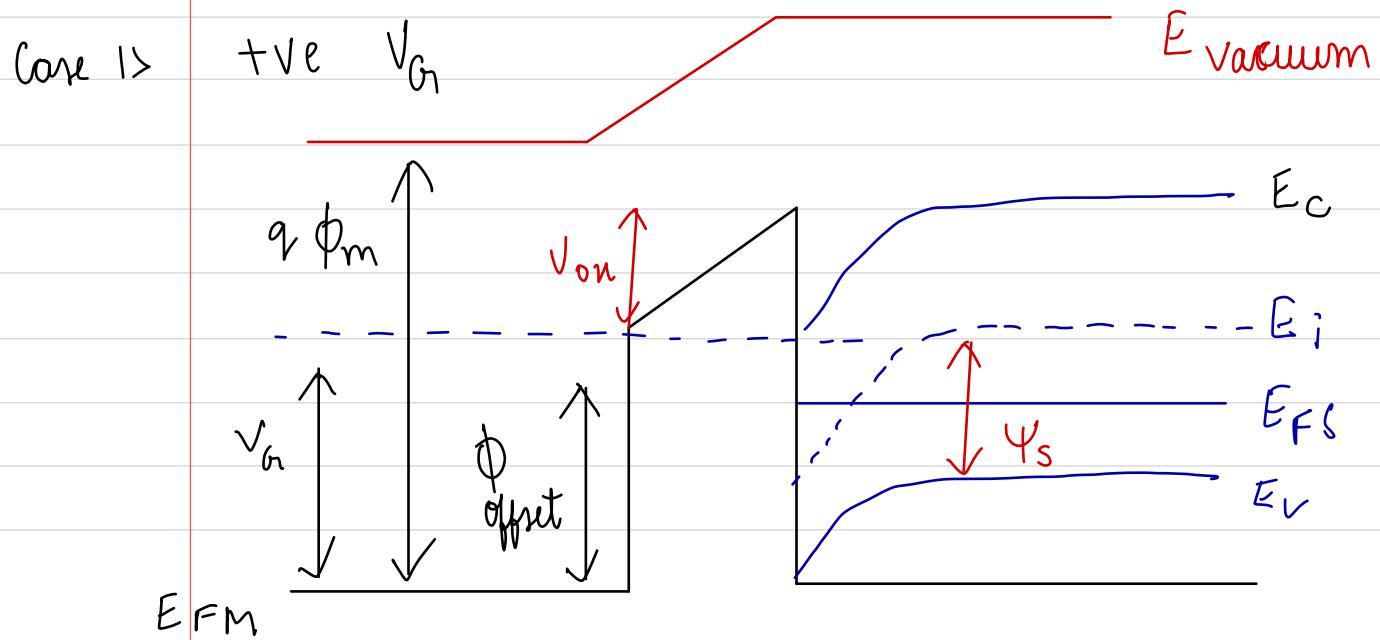


$$\phi_m = \phi_s \Rightarrow \phi_m - \phi_s = 0$$

$E_{FM}$  = metal fermi level

No interface charges  $Q_{it}$ ,  $Q_{ot}$ ,  $Q_f = 0$

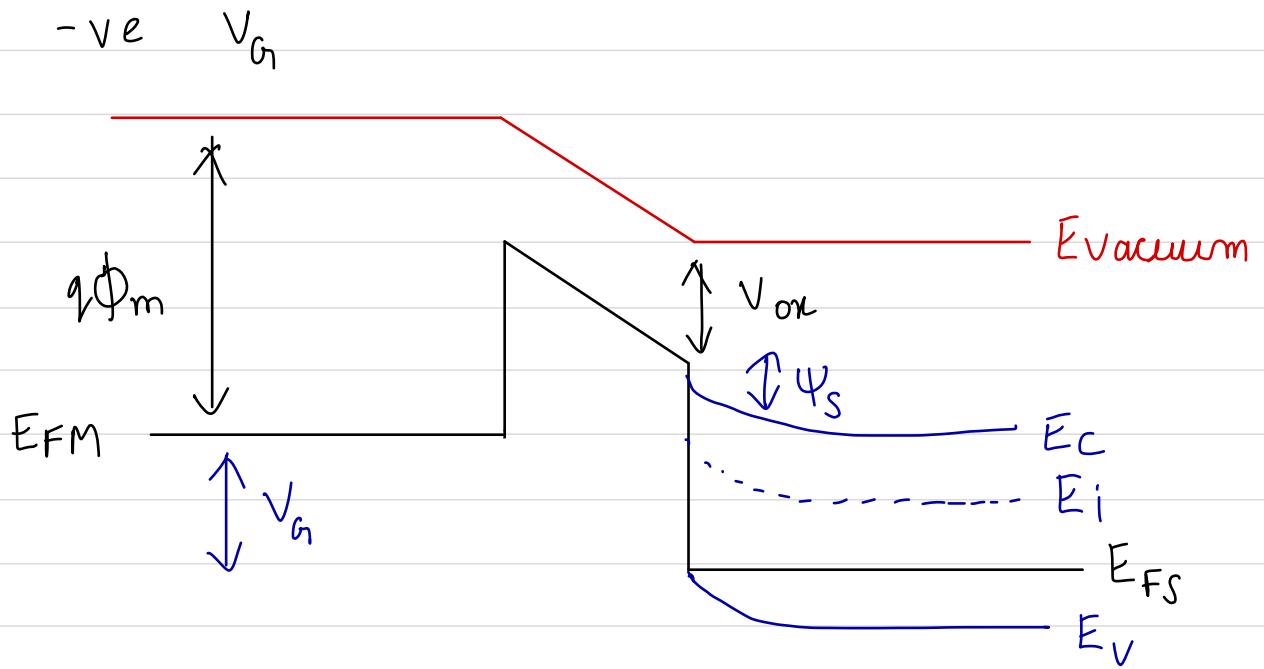
NOTE: Even if voltage applied between M, S, then  $\phi_{offset}$  remains unchanged.



$$V_G = V_{ox} + \Psi_s$$

$\Psi_s$  = surface potential

case 2 >

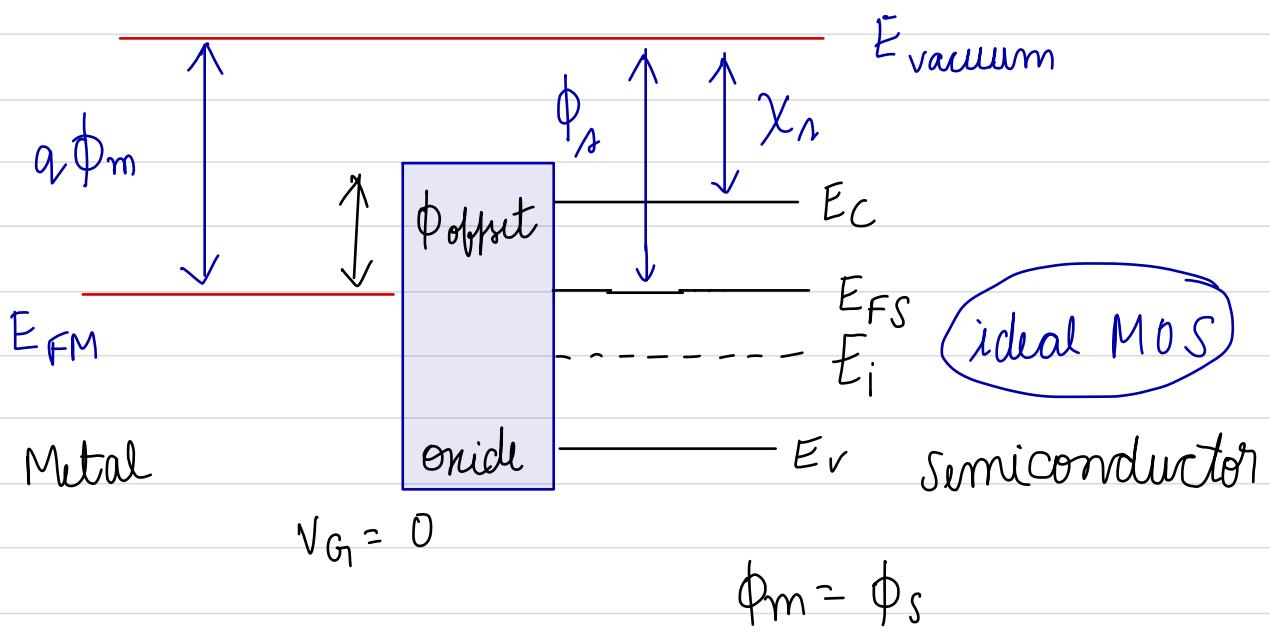
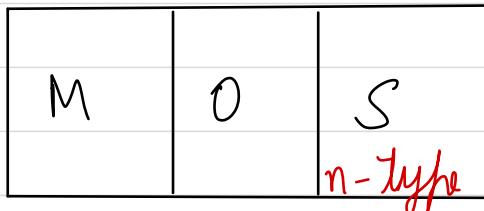


NOTE: When we apply +ve voltage bands will go down.

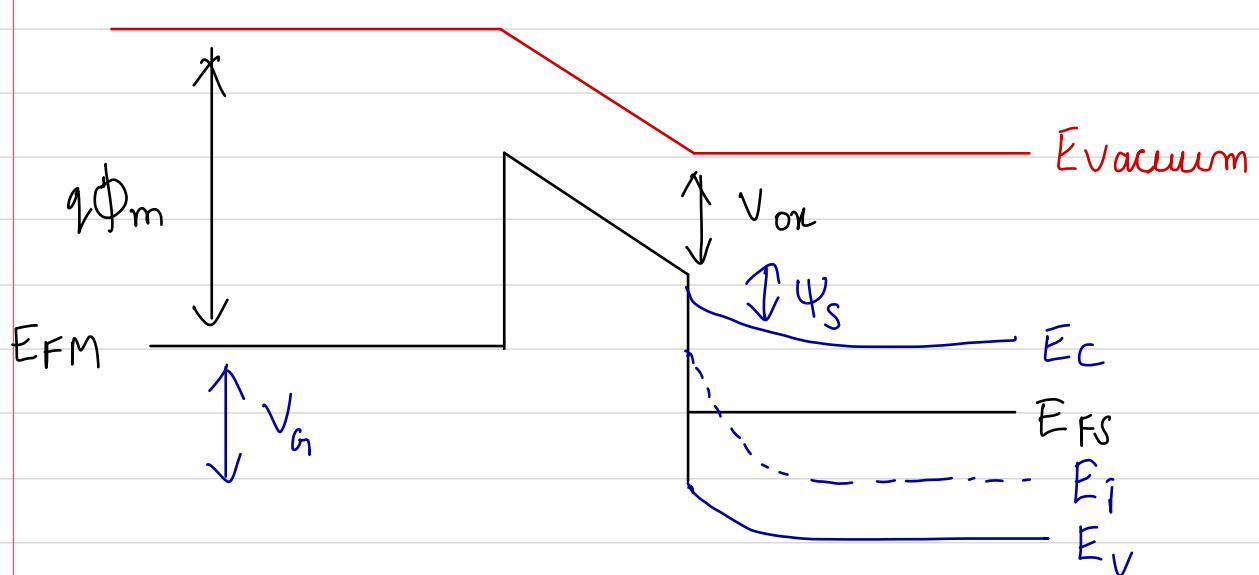
When we apply -ve voltage bands will go up.

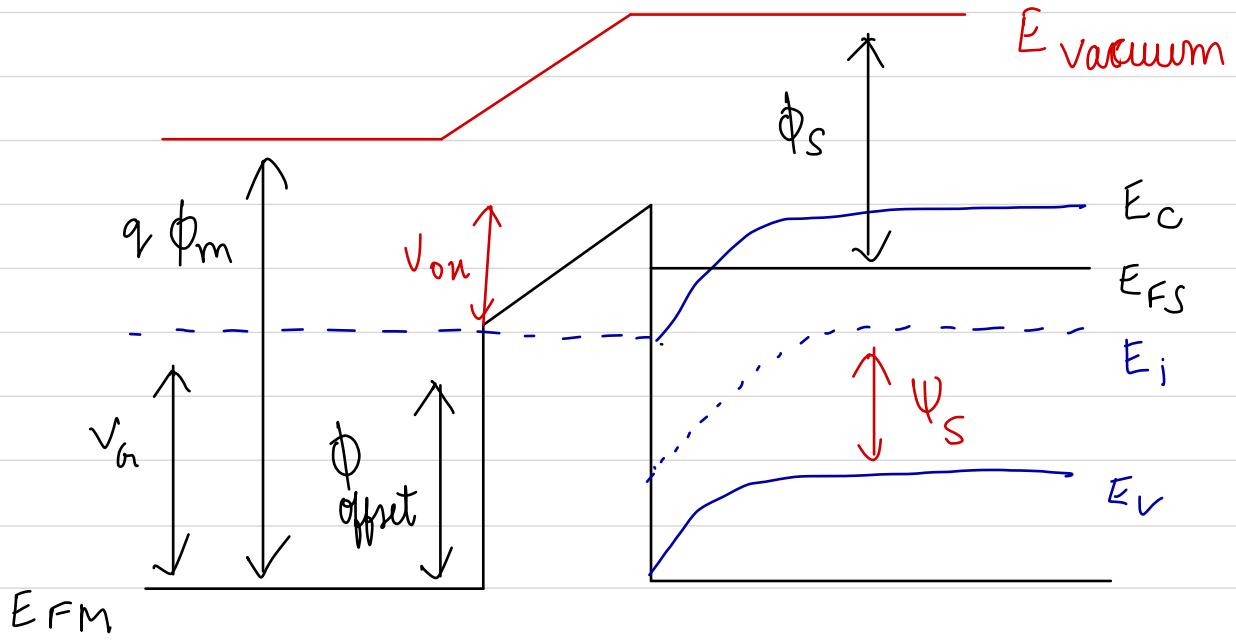
In this case Fermi level will come closer to  $E_V$ .

N Tyhe bands:



Case 1 : -ve  $V_G$

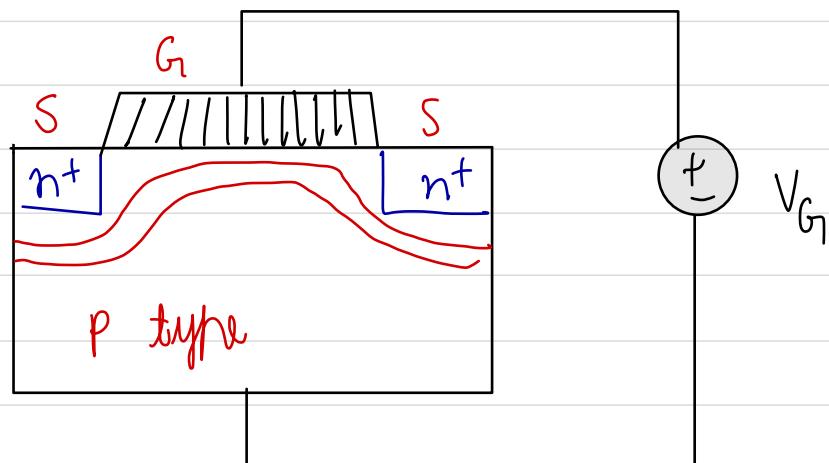




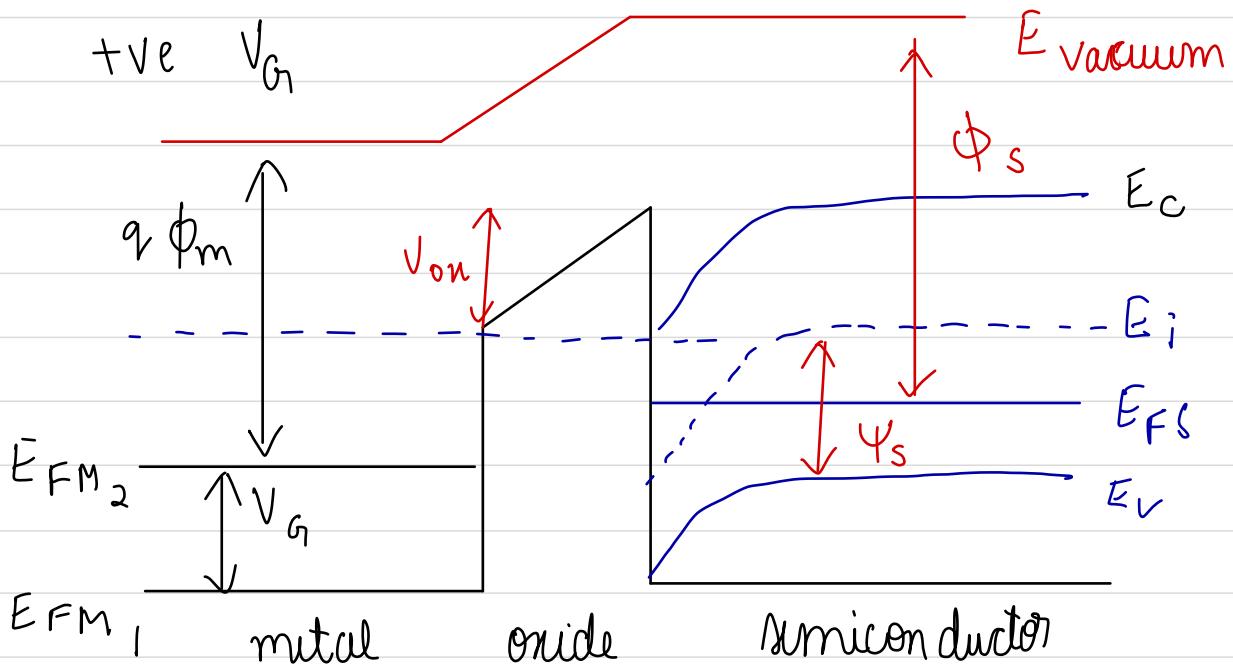
$$\Psi = 2\phi_F \quad \phi_F = \text{fermi potential}$$

MOS capacitor threshold

Threshold : Gate voltage at which the MOSFET turns on when the channel is formed between source & drain



Voltage at which inversion layer forms in a MOS capacitor:  $P - \mu_b = 10^{14} / \text{cm}^3$



Inversion occurs when  $\psi_s = 2\phi_F$

$$\phi_F = \frac{kT}{q} \ln \left( \frac{N_A}{n_i} \right)$$

$N_A$  = acceptor concentration or  $p_0$

Threshold voltage - ideal MOS capacitor

$$V_G = V_{ox} + \psi_s$$

$$C_{ox} V_{ox} = Q_d$$

$$V_{ox} = \frac{Q_d}{C_{ox}}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$Q_d = q N_A W$$

$$W = \sqrt{\frac{2 \epsilon_{si} \psi_s}{q N_A}}$$

$$Q_d = \left( \sqrt{q N_A} \right)^2 \sqrt{\frac{2 \epsilon_{si} 2 \phi_F}{q N_A}}$$

$$Q_d = 2 \sqrt{q N_A \phi_F \epsilon_{si}}$$

Q) p-type MOS capacitor is made with  
 $N_A = 5 \times 10^{15} / \text{cm}^3$ . Gate oxide thickness  
 $t_{ox} = 100 \text{ \AA}$ . Find  $C_{ox}$ ,  $C_{min}$ ,  $W_m$ ,  $V_{th}$   
 $n_i = 1.5 \times 10^{10} / \text{cm}^3$ ,  $\epsilon_0 = 8.854 \times 10^{-14} \text{ F/cm}$   
 $\epsilon_{n,i} = 11.8 \approx 12$ ,  $\epsilon_{n,ox} = 3.9 \approx 4$   
 Ans  $C_{ox} = \frac{\epsilon_{ox} \epsilon_0}{t_{ox}} = \frac{4 \times 8.854 \times 10^{-14}}{100 \times 10^{-8}}$   
 $= 0.35 \times 10^{-6}$   
 $= 0.35 \mu\text{F}/\text{cm}^2$

$$\begin{aligned}
 \phi_F &= \frac{kT}{q} \ln \left( \frac{N_A}{n_i} \right) \\
 &= 8.62 \times 10^{-5} \frac{eV}{K} \times \frac{300K}{e} \ln \left( \frac{5 \times 10^{15}}{1.5 \times 10^{10}} \right) \\
 &= 0.026 \ln (3.33 \times 10^5) \\
 &= 0.329 \text{ V}
 \end{aligned}$$

$$\begin{aligned}
 W_m &= 2 \sqrt{\frac{\epsilon_0 \epsilon_{s_i} \phi_F}{q N_A}} = 2 \sqrt{\frac{8.854 \times 11.8 \times 0.329 \times 10^{-14}}{5 \times 10^{15} \times 1.6 \times 10^{-19}}} \\
 &= 2 \sqrt{4.29} \times 10^{-5} \\
 &= 4.15 \times 10^{-5} \text{ cm}
 \end{aligned}$$

$$\begin{aligned}
 Q_d &= q N_A W_m \\
 &= 1.6 \times 10^{-19} \times 5 \times 10^{15} \times 4.15 \times 10^{-5} \\
 &= 3.32 \times 10^{-8} \text{ C/cm}^2
 \end{aligned}$$

$$V_{th} = \psi_A + \frac{Q_d}{C_{ox}} = 2\phi_F + \frac{Q_d}{C_{ox}}$$

$$V_{th} = 2 \times 0.329 + \frac{3.32 \times 10^{-8}}{3.45 \times 10^{-7}}$$

$$= 0.658 + 0.096 = 0.74 \text{ V}_f$$

$$C_d = \frac{\epsilon_0 \epsilon_s}{W_m}$$

$$= \frac{8.854 \times 10^{-14} \times 12}{4.15 \times 10^{-5}} = 2.517 \times 10^{-8} \text{ F/cm}^2$$

$$C_{min} = \frac{C_{ox} C_d}{C_{ox} + C_d} = \frac{3.45 \times 10^{-7} \times 2.51 \times 10^{-8}}{3.45 \times 10^{-7} + 2.51 \times 10^{-8}}$$

$$= \frac{8.66 \times 10^{-15}}{3.701 \times 10^{-7}}$$

$$= 2.34 \times 10^{-8} \text{ F/cm}^2,$$

Q) Find the variation in  $t_{ox}$  so that  $V_{th} = 10$  for previous question.

Ans

$$V_{th} = \Psi_h + \frac{Q_d}{C_{ox}} = 2\phi_F + \frac{Q_d}{C_{ox}}$$

$$10 = 2 \times 0.329 + \frac{3.32 \times 10^{-8}}{C_{ox}}$$

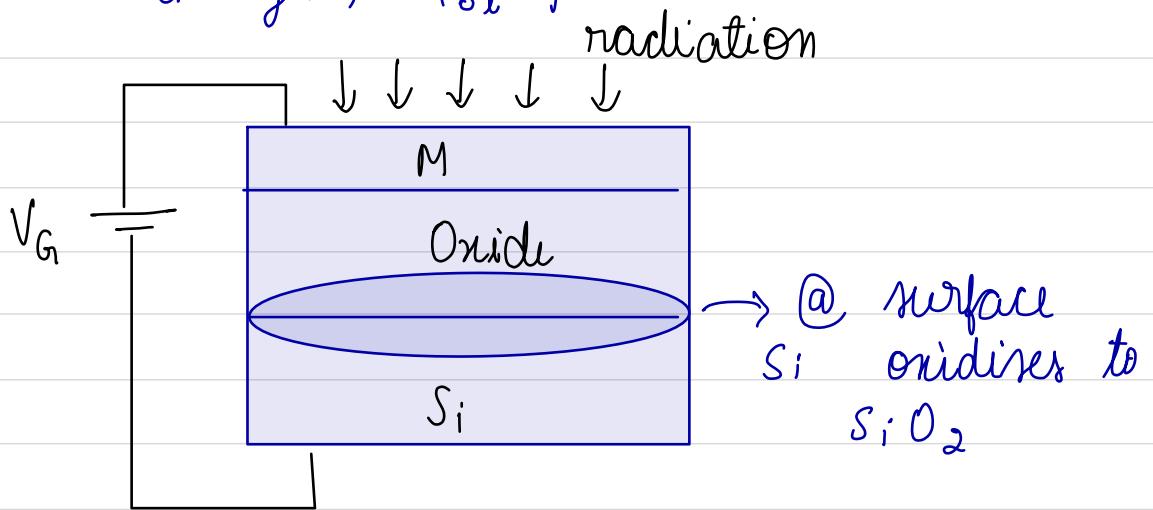
$$C_{ox} = 9.7 \times 10^{-8}$$

$$\frac{\epsilon_0 \epsilon_{ox}}{t_{ox}} = 9.7 \times 10^{-8}$$

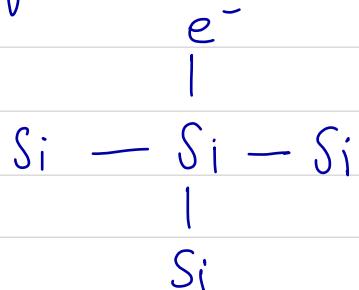
$$t_{ox} = \frac{8.854 \times 12 \times 10^{-14}}{9.7 \times 10^{-8}} = 3.65 \times 10^{-6} \text{ cm},$$

## Real MOS capacitor

- Work function difference between metal and semiconductor,  $\phi_m - \phi_s \neq 0$
- Interface charges,  $Q_{it} \neq 0$
- Fixed charges,  $Q_f \neq 0$
- Mobile charges in oxide,  $Q_m \neq 0$
- Oxide charges,  $Q_{ot} \neq 0$



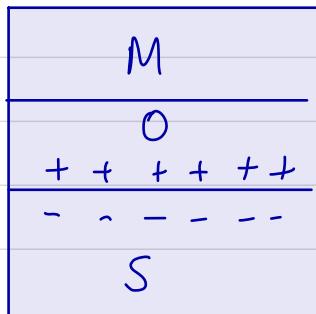
But there are few bonds in that layer  
not satisfied and has free electrons



$$\text{Ideally, } V_{th} = 2\phi_F + \frac{Q_d}{C_{ox}}$$

- Assume due to  $Q_{it}$ , there are few +ve charges @ surface of oxide
- When we apply  $+V_G$ , we have to apply lesser  $V_G$  for inversion to occur

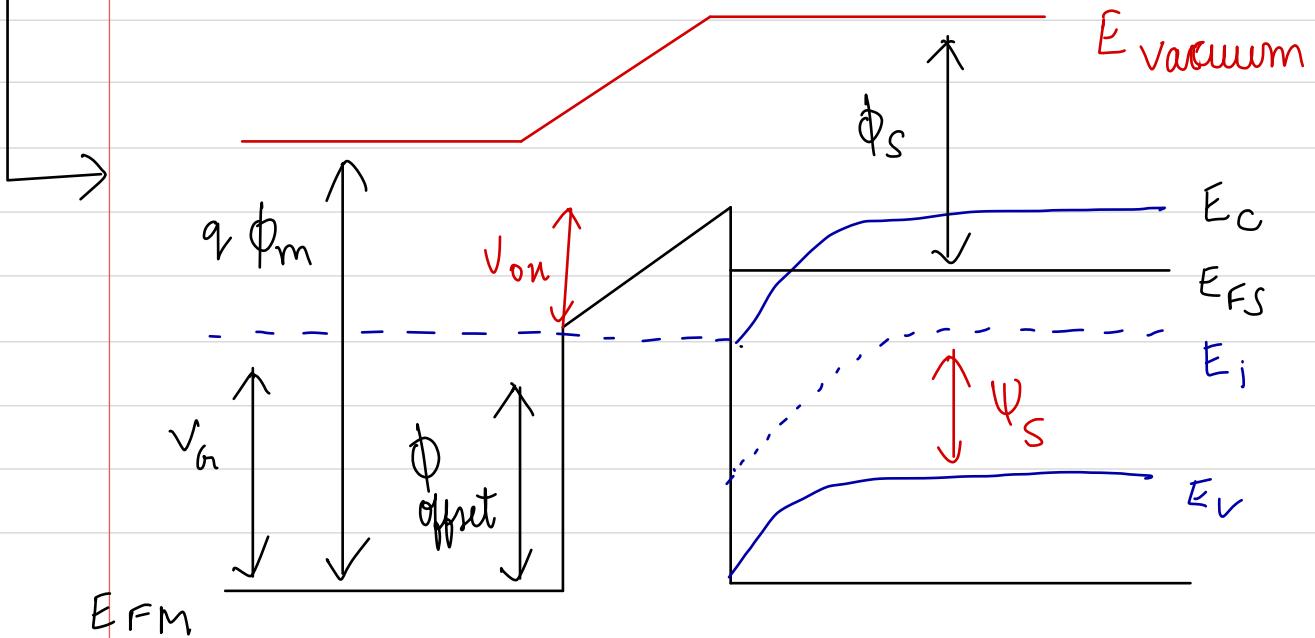
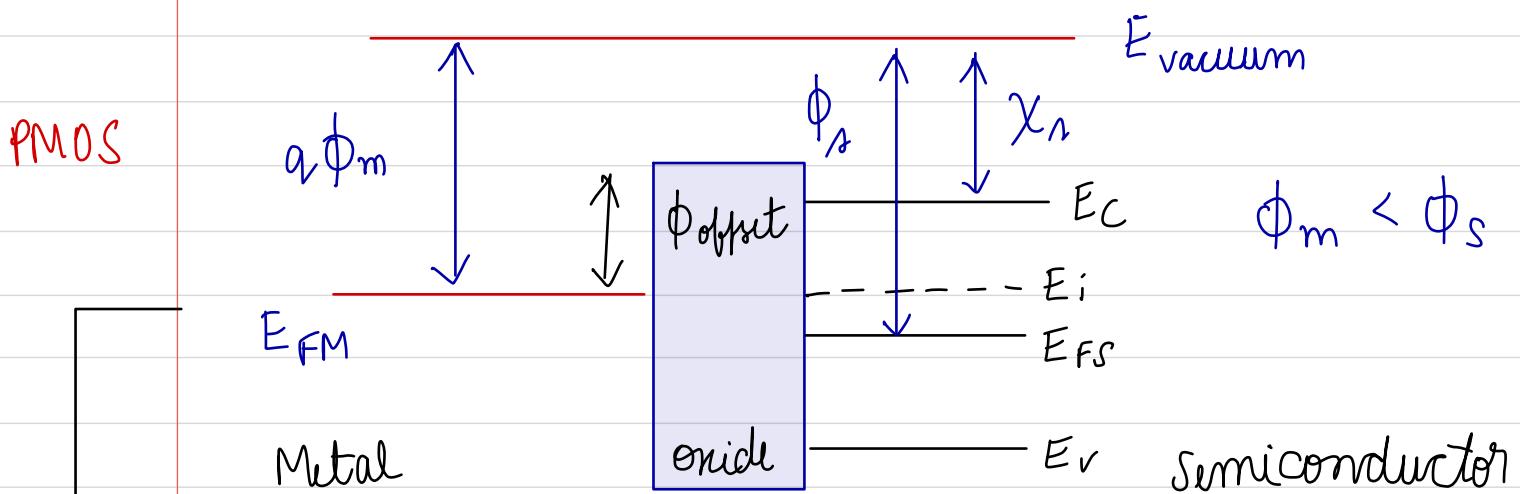
Because +ve charge at layer would have attracted -ve charge from Si already



with  $V_G = 0$ , -ve charges already present at Silicon.  
 $\therefore$  Apply lower  $V_G$  for inversion.

$$\text{here } V_{th} = \phi_F + \frac{Q_d}{C_{ox}} + \frac{Q_{it}}{C_{ox}}$$

work function



$$\phi_m - \phi_s = V_{FB}$$

$$\therefore V_{th} = 2\phi_f + \frac{Q_d}{C_{ox}} + V_{FB}$$

$V_{FB}$  = flat band voltage

$$V_{FB} = \phi_m - \phi_s + \frac{Q_{it}}{C_{ox}}$$

$$\therefore V_{th} = 2\phi_f + \frac{Q_d}{C_{ox}} + \frac{Q_{it}}{C_{ox}} + \phi_{ms}$$

where  $\phi_{ms} = \phi_m - \phi_s$

Q> A dual p-MOS capacitor with  $N_A = 10^{16}/\text{cm}^3$ ,  $t_{ox} = 20\text{ nm}$ ,  $Q_{it} = 4 \times 10^{10} \text{ gC/cm}^3$ . Find  $V_{th}$

$\phi_{ms} = -0.3\text{ V}$

$$V_{th} = 2\phi_f + \frac{Q_d + Q_{it}}{C_{ox}} + \phi_{ms}$$

$$\phi_f = \frac{kT}{q} \ln \left( \frac{N_A}{N_i} \right)$$

$$= 0.026 \ln \left( \frac{10^{16}/\text{cm}^3}{1.5 \times 10^{10}} \right)$$

$$= 0.026 \ln (6.66 \times 10^5) = 0.3486$$

$$W_m = 2 \sqrt{\frac{\epsilon_0 \epsilon_{si} \Phi}{q_i N_A}}$$

$$= 2 \sqrt{\frac{8.854 \times 10^{-14} \times 11.8 \times 0.3486}{1.6 \times 10^{-19} \times 10^{16}}}$$

$$= 3.014 \times 10^{-5} \text{ cm}$$

$$C_{ox} = \frac{\epsilon_0 \epsilon_{ox}}{t_{ox}} = \frac{8.854 \times 10^{-14} \times 3.9}{20 \times 10^{-7}}$$

$$= 1.72 \times 10^{-7} \text{ F/cm}^2 //$$

$$Q_d = q_i N_A W_m$$

$$= 1.6 \times 10^{-19} \times 10^{16} \times 3.014 \times 10^{-5}$$

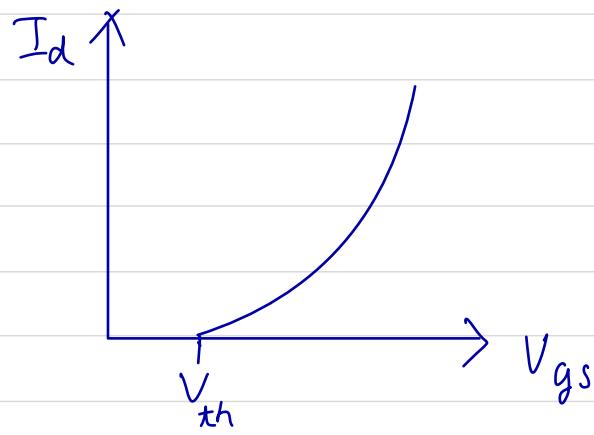
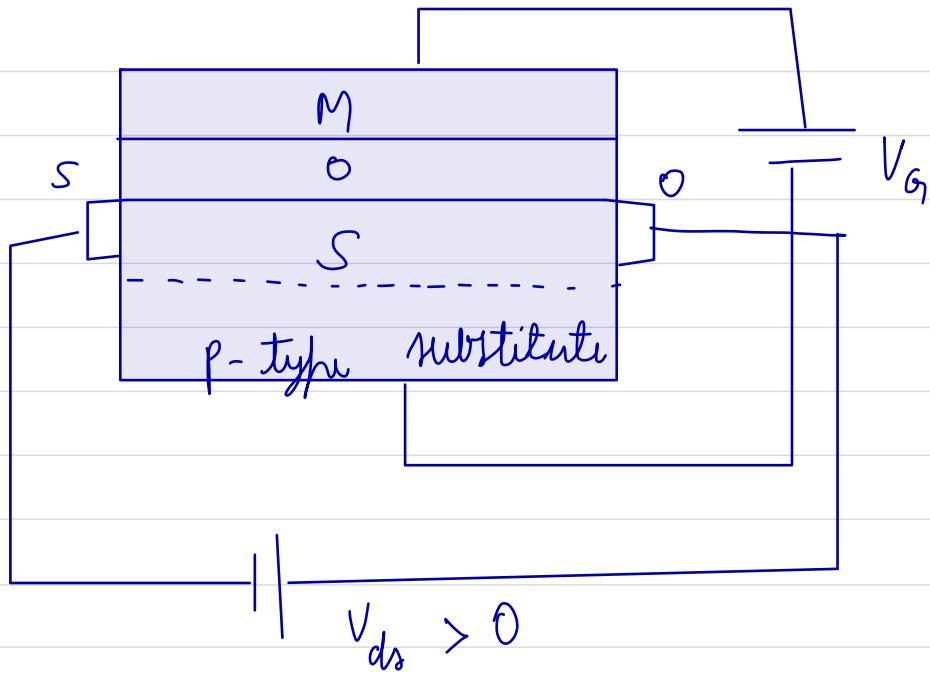
$$= 4.82 \times 10^{-8} \text{ C/m}^2$$

$$Q_{it} = 4 \times 10^{+10} \times 1.6 \times 10^{-19} = 6.4 \times 10^{-9}$$

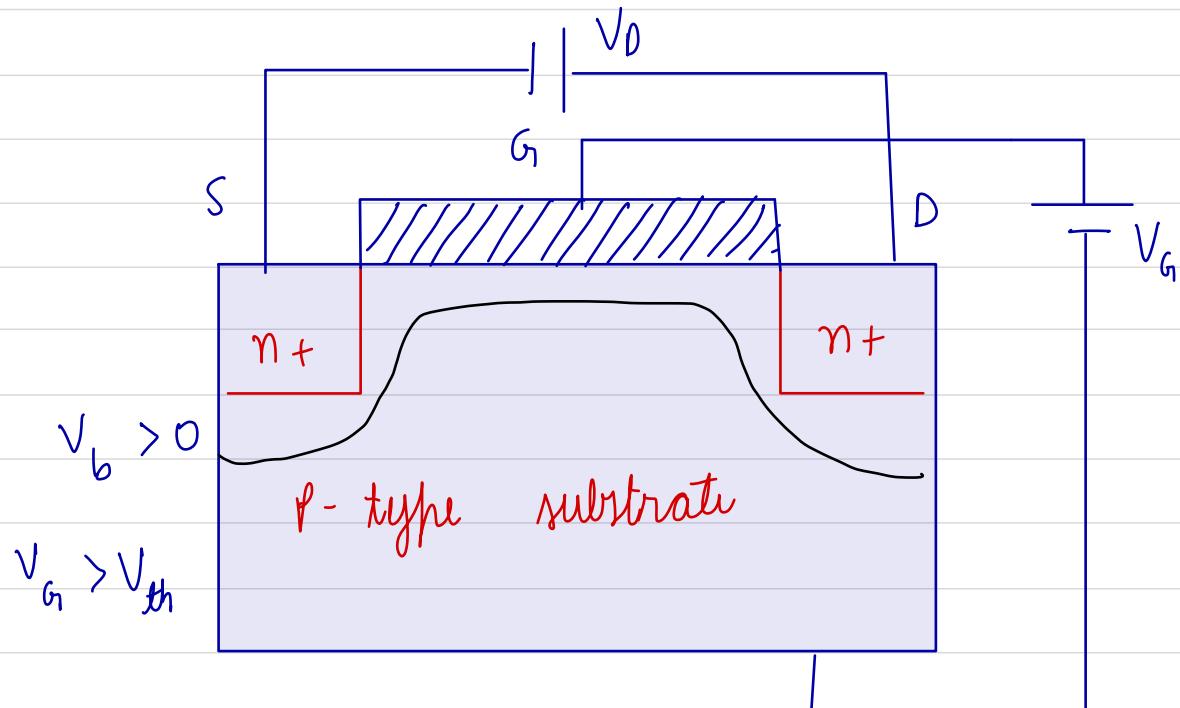
$$V_{th} = 2 \times 0.3486 + \frac{4.82 \times 10^{-8} + 6.4 \times 10^{-9}}{1.72 \times 10^{-7}} - 0.3$$

$$= 0.6972 - 0.3 + 0.317$$

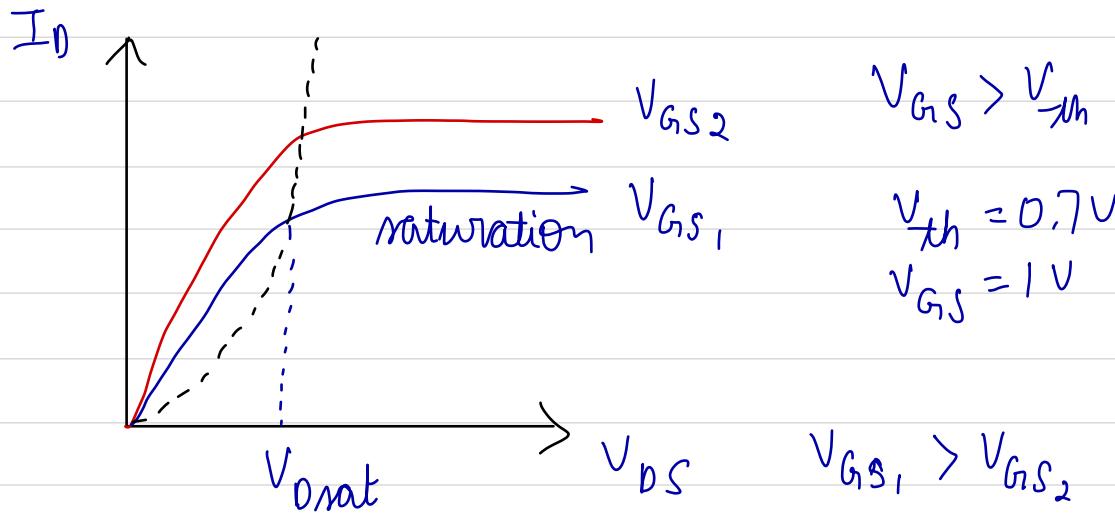
$$= 0.7142 //$$



threshold happens  
when MOS  
capacitor enters  
to inversion



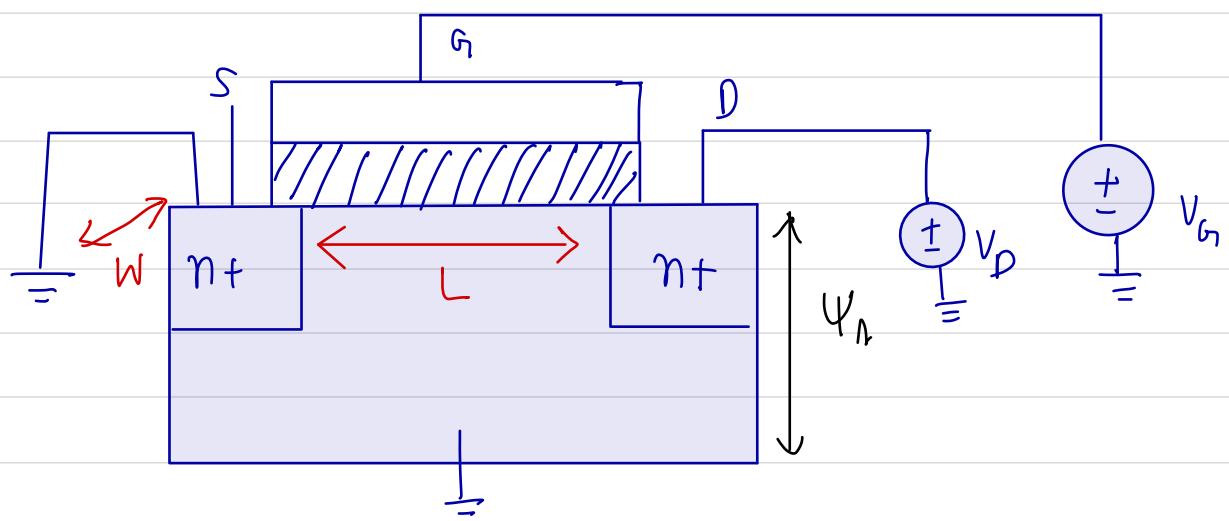
For MOSFET there should be a small overlap between drain/source with gate in channel that there is continuity between source / drain

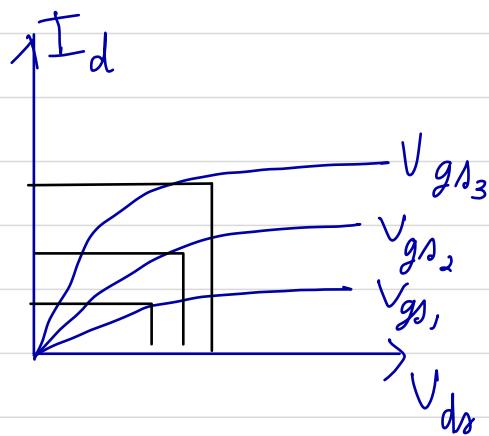
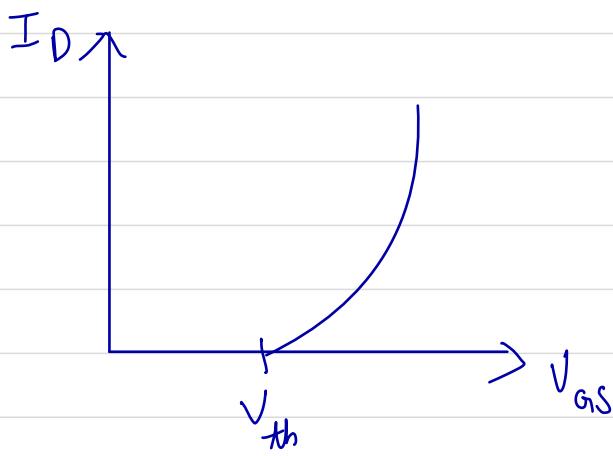


NOTE: After pinch off the charges drift

Mosfet drain current equation

$$I_{ds} = f(V_{ds}, V_{gs})$$





Spice model or compact model

- Optimized circuit simulator
- code written in verilog A
- Sifirati model for resistor, capacitor

- 1> Threshold voltage based model
- 2> Surface potential based model
- 3> Charge based model

Surface potential is potential between surface of gate oxide to bottom of p substrate "ψ".

Threshold based - less accurate  
other 2 - more accurate

1> Threshold voltage based :

$$\text{Linear: } I_d = \mu_n C_{ox} \frac{W}{L} \left[ (V_{gs} - V_{TH}) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

$$\text{Saturation: } I_d = \mu_n C_{ox} \frac{W}{L} \left[ \frac{(V_{gs} - V_{TH})^2}{2} \right]$$

$$\text{Cutoff : } I_d = 0$$

$$\text{Linear: } V_{gs} > V_{th} \quad V_{ds} < V_{gs} - V_{th}$$

$$\text{Saturation: } V_{gs} > V_{th} \quad V_{ds} > V_{gs} - V_{th}$$

$\mu$  = mobility of electrons

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

Q2 For an n-channel MOSFET with  $t_{ox} = 10 \text{ nm}$

$$V_{th} = 0.6 \text{ V} \quad W = 25 \mu\text{m}, \quad L = 1 \mu\text{m}.$$

Calculate the drain current at  $V_{gs} = 5 \text{ V}$

$$\text{Ans} \quad \frac{V}{\epsilon} \frac{V_{ds}}{ds} = 0.1 \text{ V} \quad \text{Assume } \mu_n = 200 \text{ cm}^2/\text{Vs}$$

$$V_{gs} - V_{th} = 5 - 0.6 = 4.4 \text{ V}$$

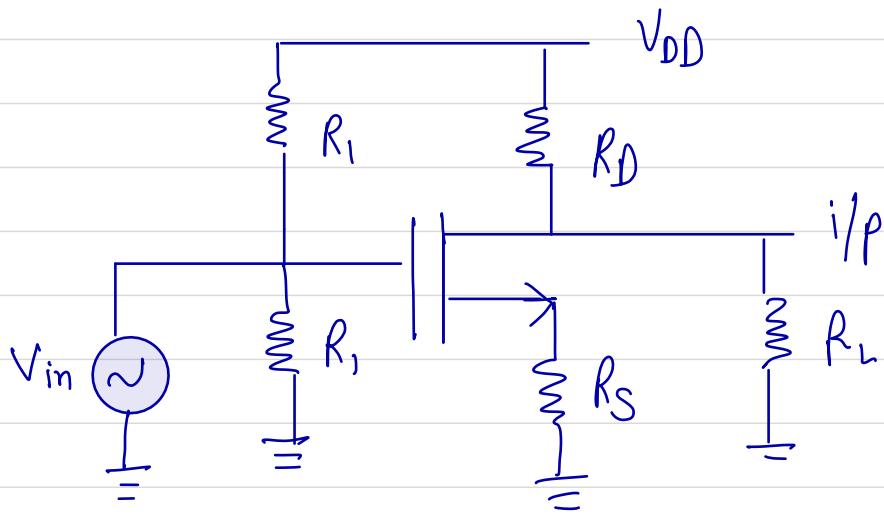
$$V_{ds} = 0.1 < V_{gs} - V_{th} \rightarrow \text{Linear}$$

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[ (V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

$$C_{ox} = \frac{\epsilon_{ox} \epsilon_{r,ox}}{t_{ox}}$$

$$= 200 \times 8.854 \times 10^{-14} \times 3.9 \times \frac{25}{1} \left[ 4.4 \times 0.1 - \frac{0.1^2}{2} \right]$$

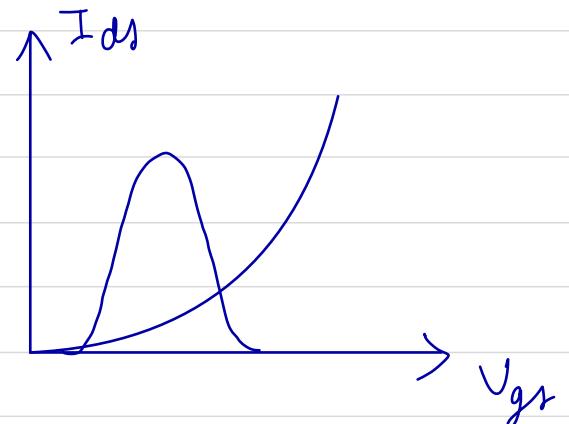
$$= 751 \mu\text{A}/$$



$$g_m = \frac{d I_{ds}}{d V_{gs}} = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})$$

$$g_m' = \frac{d^2 I_{ds}}{d V_{gs}^2}$$

$$g_m'' = \frac{d^3 I_{ds}}{d V_{gs}^3}$$



Q> Find the maximum value of  $R_D$  for which the MOSFET is in saturation.

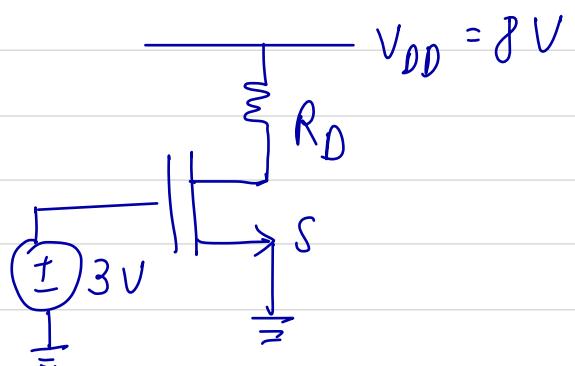
$$\mu_n = 350 \text{ cm}^2/\text{Vs}, \quad W = 10 \mu\text{m}, \quad L = 1 \mu\text{m}$$

$$V_{th} = 0.6 \text{ V} \quad t_{ox} = 5 \text{ nm}$$

Ans

$$V_{DS} > V_{GS} - V_{th}$$

$$V_{DS} > 3 - 0.6 = 2.4 \text{ V}$$



$$V_{DD} = V_{DS} + I_D R_D$$

$$8 = V_{DS} + \mu_n C_{ox} \frac{W}{L} \left( \frac{1}{2} \right) (V_{GS} - V_{th})^2$$

$$8 = 2.4 + R_D \times 350 \times \frac{8.854 \times 10^{-14} \times 3.9}{2 \times 5 \times 10^{-7}} \times (2.4)^2 \times 10$$

$$5.6 = 6.96 \times 10^{-3} R_D$$

$$R_D = 804 \Omega_{\parallel}$$

Q> A depletion type MOSFET with  $N_A = 10^{16}/\text{cm}^3$   
 $t_{ox} = 1\text{nm}$ ,  $\phi_m = -1.5\text{V}$ . Determine  
the doping concentration to convert it  
to enhancement type with  $V_{th} = 0.2\text{V}$

Ans

$$V_{th_1} = 2\phi_F + \frac{Q_d}{C_{ox}} + \phi_m$$

$$V_{th_1} = 0.2$$

$$\Delta V_{th} = V_{th_1} - V_{th_2}$$

$$\phi_F = \frac{kT}{q} \ln \left( \frac{N_A}{N_i} \right)$$

$$= 0.026 \ln \left( \frac{10^5}{1.5 \times 10^{10}} \right)$$

$$= 0.2887$$

$$W_m = 2 \sqrt{\frac{\epsilon_0 \epsilon_{si} \phi_F}{q N_A}}$$

$$= 2 \sqrt{\frac{8.854 \times 10^{-14} \times 0.2887 \times 11.8}{1.6 \times 10^{-19} \times 10^{15}}}$$

$$= 8.68 \times 10^{-5}$$

$$\begin{aligned} Q_d &= q N_A W_m \\ &= 1.6 \times 10^{-19} \times 10^{15} \times 8.68 \times 10^{-5} \\ &= 1.38 \times 10^{-8} \text{ C/cm}^2 \end{aligned}$$

$$C_{ox} = \frac{\epsilon_0 \epsilon_{n_{ox}}}{t_{ox}}$$

$$= 8.854 \times 10^{-14} \times 3.8$$

$$= 3.36 \times 10^{-6} \text{ F/cm}^2$$

$$V_{th_1} = 0.2887 \times 2 + \frac{1.38 \times 10^{-8}}{3.36 \times 10^{-6}} - 1.5$$

$$= -0.91 \text{ V}$$

$$\Delta V_{th} = V_{th_2} - V_{th_1}$$

$$= 0.2 - (-0.91)$$

$$= 1.1 \text{ V}$$

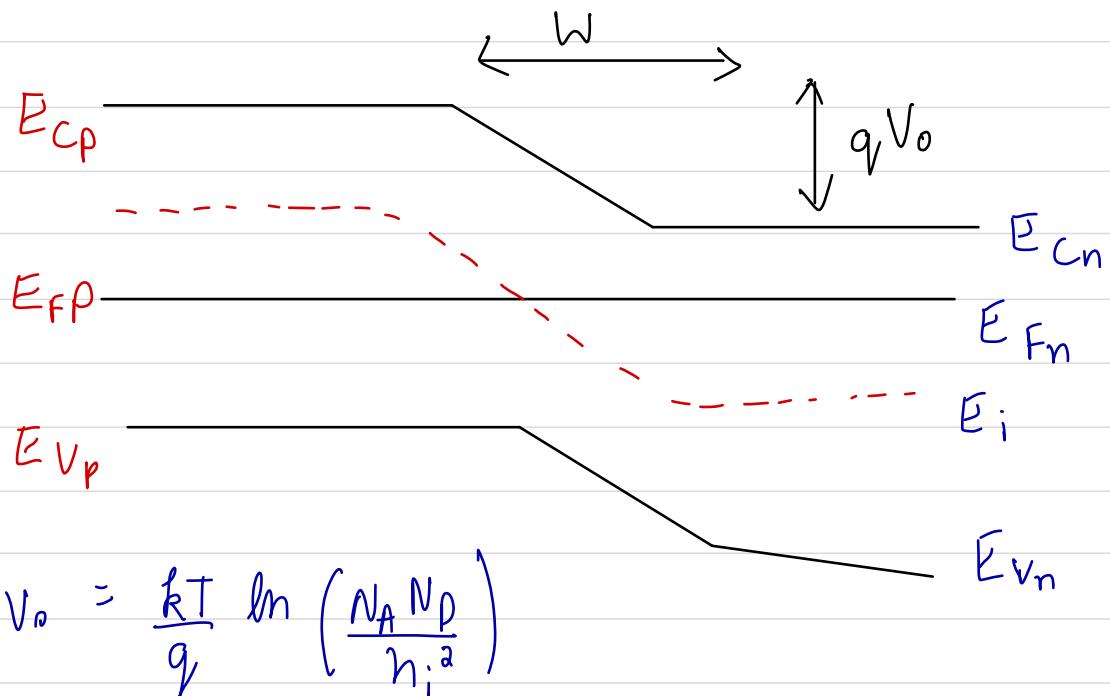
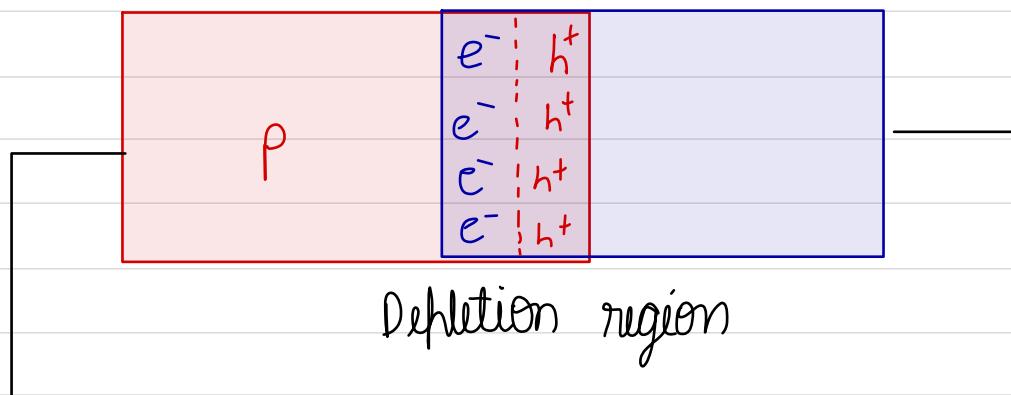
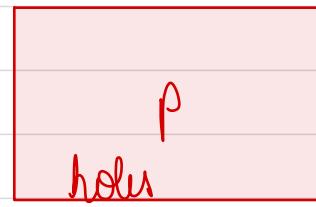
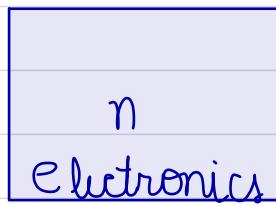
NOTE  $\phi_s = \chi_s + \frac{Eg}{2} + \phi_F \rightarrow ①$

$$\therefore \Delta \phi_m = \Delta \phi_s = \Delta \phi_F \rightarrow ②$$

$$1.1 \text{ V} = 2 \times 0.026 \ln \left( \frac{N_A}{N_i} \right) + \frac{q N_A W}{C_{ox}} + \Delta \phi_m \rightarrow ③$$

Input  $N_A$  values such that all ①, ②, ③ are satisfied.

## P-n junction



- 2 types of current:
- i> Diffusion current due to concentration gradient
- ii> Drift current due to electric field

$$J = J_n + J_p$$

$$J_n = J_{n\text{ diff}} + J_{n\text{ drift}}$$

$$J_p = J_{p\text{ diff}} + J_{p\text{ drift}}$$

At equilibrium

$$\Rightarrow J_p = J_n = 0$$

$$\Rightarrow J_{p\text{ diff}} + J_{p\text{ drift}} = 0$$

$$J_{n\text{ diff}} + J_{n\text{ drift}} = 0$$

Particle flow      Current

Hole diffusion  $\longrightarrow$   $\longrightarrow$

$$J_{p\text{ diff}}$$

Hole drift,  $\leftarrow$   $\leftarrow$

$$J_{p\text{ drift}}$$

Electron diffusion  $\leftarrow \dashrightarrow \dashrightarrow \rightarrow$

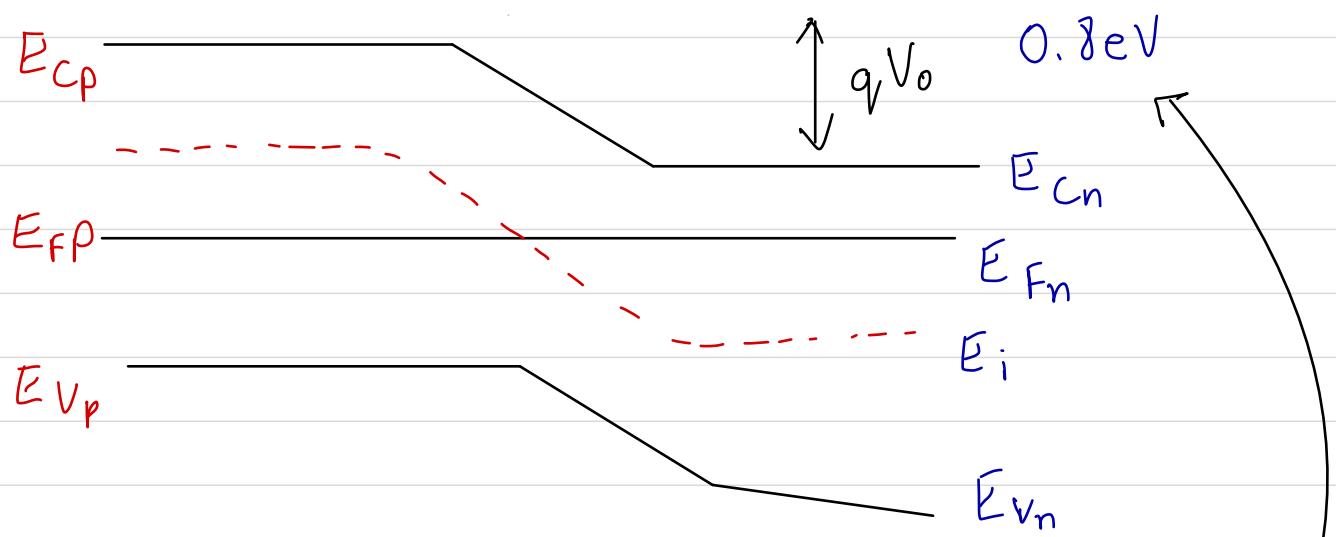
$$J_{n\text{ diff}}$$

Electron drift  $\dashrightarrow \leftarrow \dashrightarrow$

$$J_{n\text{ drift}}$$

$$J_p(x) = q \mu_p E(x) + q D_p \frac{dp(x)}{dx} = 0$$

Q> An abrupt Si pn junction has  $N_A = 10^{18}/\text{cm}^3$  and  $N_D = 5 \times 10^{15}/\text{cm}^3$ . Draw the band diagram and label the contact potential.



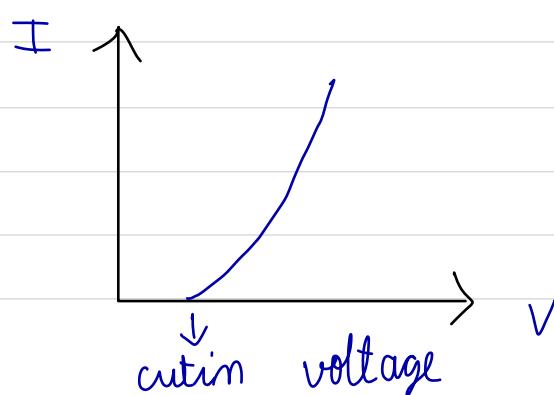
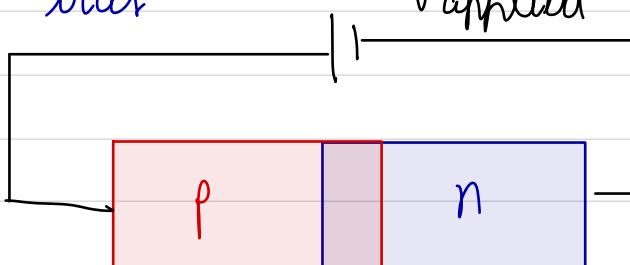
$$V_0 = \frac{kT}{q} \ln \left( \frac{N_A N_D}{n_i^2} \right)$$

$$V_0 = 0.026 \ln \left( \frac{10^{18} \times 5 \times 10^{15}}{(1.5)^2 \times 10^{26}} \right)$$

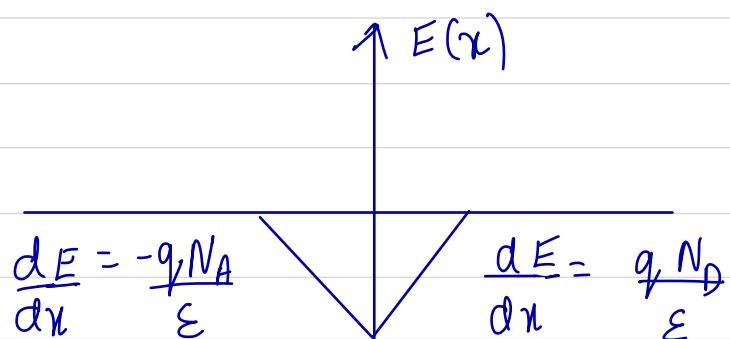
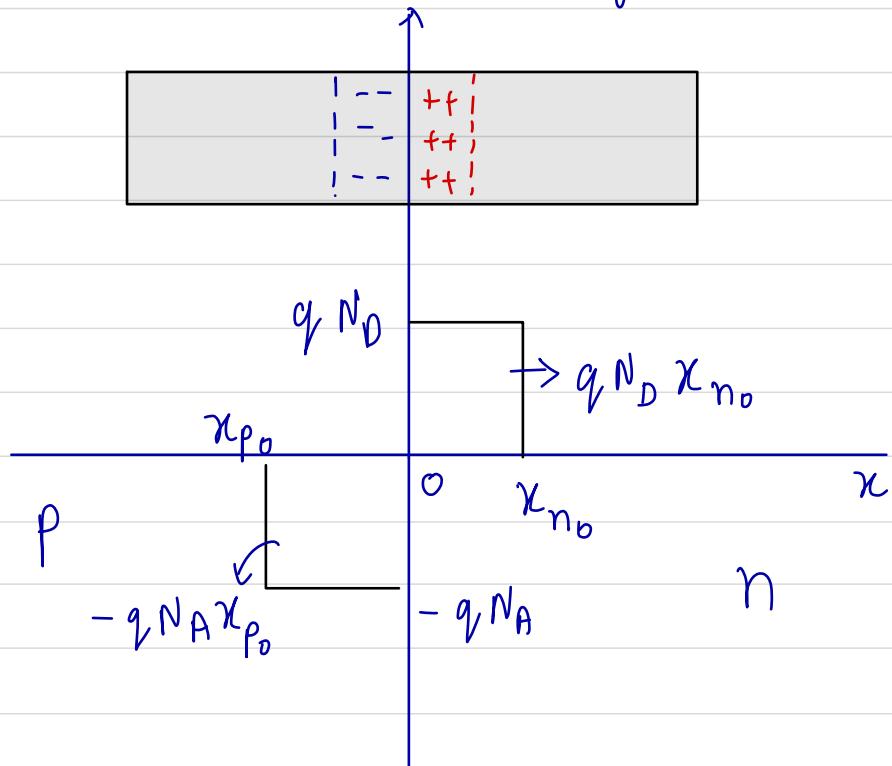
$$V_0 = 0.026 \ln (2.22 \times 10^{13}) = 0.8 \text{ V}$$

### Rectification

PN Junction allows current flow I only in forward bias



## Depletion region



At equilibrium, applied voltage = 0  
 $Q_- = Q_+$

$$-qN_A A x_{p_0} = q A N_D x_{n_0}$$

By Poisson equation  $\frac{dE(x)}{dx} = \frac{q}{\epsilon} [p - n + N_D - N_A]$

In p side of depletion region:

$$-x_{p_0} < x < 0, \quad \frac{dE(x)}{dx} = -\frac{qN_A}{\epsilon}$$

In n side of depletion region:

$$0 < x < x_{n_0}, \quad \frac{dE(x)}{dx} = \frac{qN_D}{\epsilon}$$

$$1) \int_{E_0}^0 E(x) dx = \frac{q}{\epsilon_0} N_D \int_0^{x_{n_0}} dx$$

$$2) \int_0^{E_0} E(x) dx = -\frac{q}{\epsilon_0} N_A \int_{-x_{p_0}}^0 dx$$

$$\Rightarrow E_0 = \frac{q N_D}{\epsilon} x_{n_0} \quad \& \quad E_0 = -\frac{q N_A}{\epsilon} x_{p_0}$$

Also  $E_0$  &  $V_0$  are related

$$-V_0 = \int_{-x_{p_0}}^{x_{n_0}} E(x) dx$$

$$V_0 = \frac{1}{2} E_0 W = \frac{1}{2} E_0 (x_{n_0} + x_{p_0})$$

PN junction depletion width

$$V_0 = \frac{1}{2} E_0 W = \frac{1}{2} \frac{q}{\epsilon} N_D x_{n_0} W$$

By change balance,

$$Q_- = Q_+ \\ |-q A N_A x_{p_0}| = |q A N_D x_{n_0}|$$

$$N_A x_{p_0} = N_D x_{n_0}$$

$$W = x_{n_0} + x_{p_0} = x_0 + \frac{N_D x_{n_0}}{N_A}$$

$$W = x_{n_0} \left[ \frac{N_A + N_D}{N_A} \right]$$

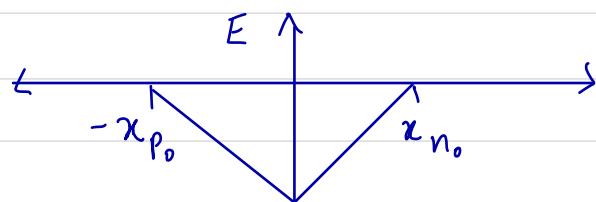
$$x_{n_0} = \frac{WN_A}{[N_A + N_D]}$$

$$x_{p_0} = \frac{WN_D}{[N_A + N_D]}$$

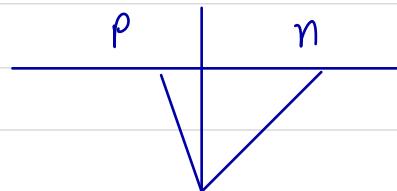
$$V_o = \frac{1}{2} \frac{q}{\epsilon} N_D \frac{W N_A}{[N_A + N_D]} = \frac{1}{2\epsilon} \frac{q N_A N_D W^2}{[N_A + N_D]}$$

$$W = \sqrt{\frac{2 V_o \epsilon}{q} \frac{[N_A + N_D]}{N_A N_D}} = \sqrt{\frac{2 \epsilon V_o}{q} \left[ \frac{1}{N_A} + \frac{1}{N_D} \right]}$$

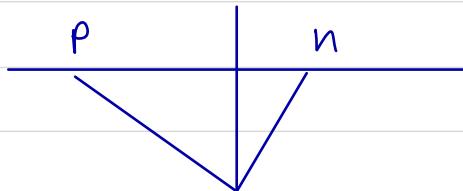
pn junction



p<sup>+</sup>n junction



pn<sup>+</sup> junction



Q) A pn junction has a circular cross-section with a diameter of 10 μm. Calculate  $x_{n_0}$ ,  $x_{p_0}$ ,  $Q_f$  and  $E_0$  for this junction at 300K. Plot  $E(x)$  and charge density to scale.  $N_A = 10^{18}/\text{cm}^3$  and  $N_D = 5 \times 10^{15}/\text{cm}^3$ .

$$V_o = \frac{kT}{q} \ln \left( \frac{N_D N_A}{n_i^2} \right)$$

$$= 0.026 \ln \left( \frac{5 \times 10^{15} \times 10^{18}}{(1.5)^2 \times 10^{20}} \right) = 0.795,$$

$$W = \sqrt{\frac{2 \epsilon V_o}{q} \left[ \frac{1}{N_A} + \frac{1}{N_D} \right]}$$

$$\begin{aligned}
 W &= \sqrt{\frac{2 \times 8.854 \times 10^{-14} \times 11.9 \times 0.795}{1.6 \times 10^{-19}} \left[ \frac{1}{10^{18}} + \frac{1}{5 \times 10^{15}} \right]} \\
 &= \sqrt{\frac{104.7 \times 10^5}{10^{15}}} \left[ \frac{1}{1000} + \frac{1}{5} \right] \\
 &= \sqrt{\frac{104.7 \times 10^{-10} \times 1005}{5000}} = 45 \times 10^{-6} \text{ cm} \\
 &= 0.457 \mu\text{m}
 \end{aligned}$$

$$x_{n_0} = \frac{WN_A}{N_A + N_D} = \frac{0.457 \times 10^{18}}{1005 \times 10^{15}} = 0.455 \mu\text{m}$$

$$x_{p_0} = \frac{WN_D}{N_A + N_D} = \frac{0.457 \times 10^{15} \times 5}{1005 \times 10^{15}} = 0.00228 \mu\text{m}$$

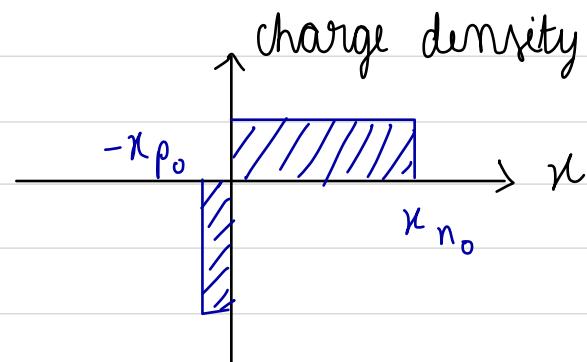
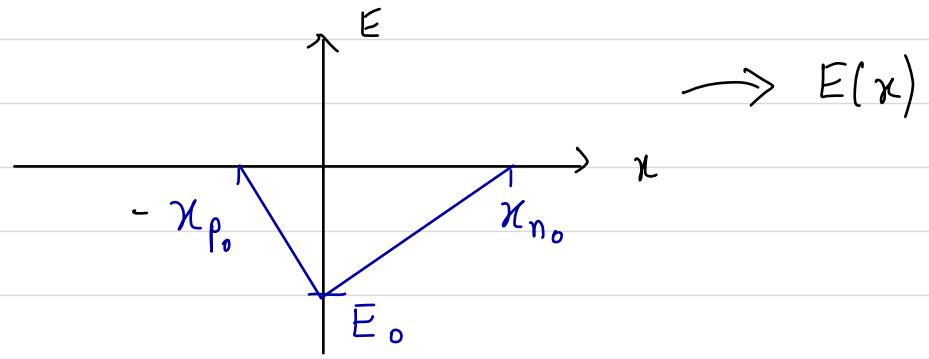
$$Q_+ = q x_{n_0} A N_D, \quad d = 10 \mu\text{m} \quad n = 5 \mu\text{m} \\ \therefore n = 5 \times 10^{-4} \text{ cm}$$

$$\begin{aligned}
 A &= \text{area} = \pi r^2 \\
 &= 3.14 \times 25 \times 10^{-8} \text{ cm}^2 \\
 &= 78.54 \times 10^{-8} \text{ m}^2
 \end{aligned}$$

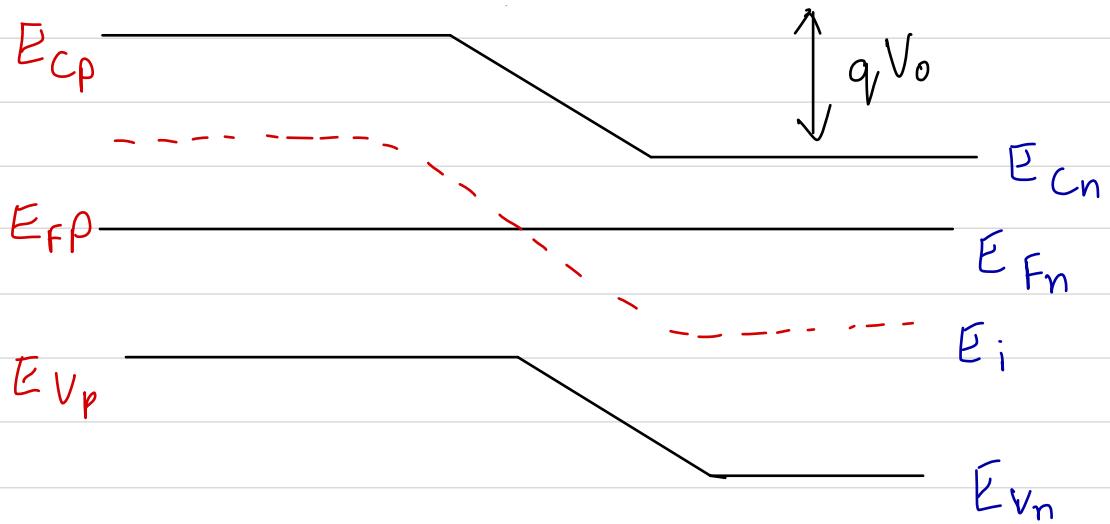
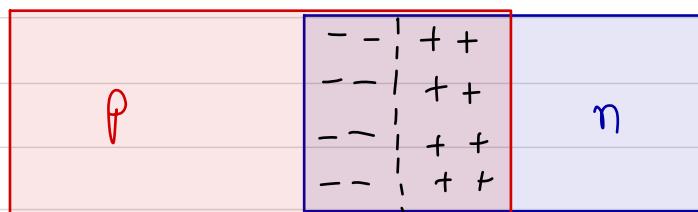
$$\begin{aligned}
 \therefore Q_+ &= 1.6 \times 10^{-19} \times 0.455 \times 10^{-4} \times 78.54 \times 10^{-8} \times 5 \times 10^{15} \\
 &= 2.85 \times 10^{-14} \text{ C}
 \end{aligned}$$

$$V_o = \frac{E_o W}{2}$$

$$\begin{aligned}
 \therefore E_o &= \frac{2V_o}{W} = \frac{2 \times 0.795}{0.457 \times 10^{-6}} = 3.479 \times 10^6 \text{ V/m} \\
 &= 3.479 \times 10^4 \text{ V/cm}
 \end{aligned}$$

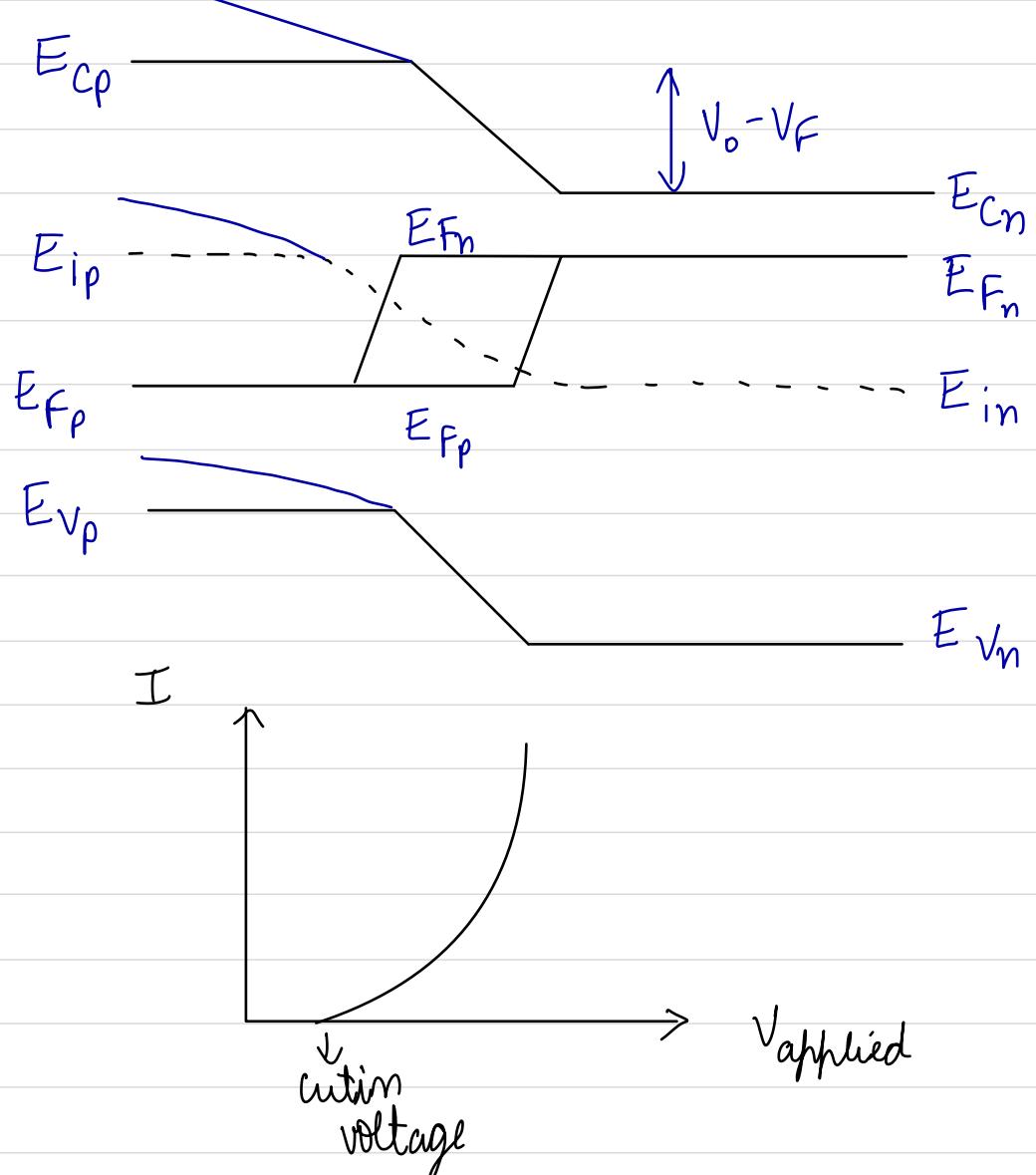
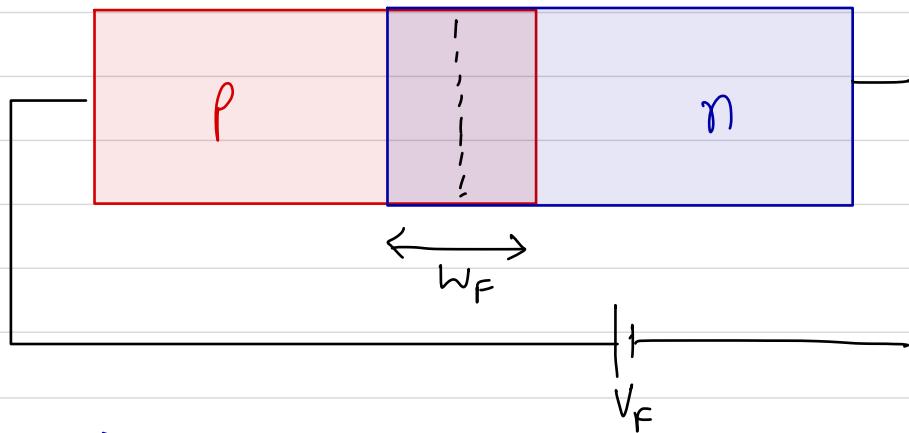


pn junction



Forward bias

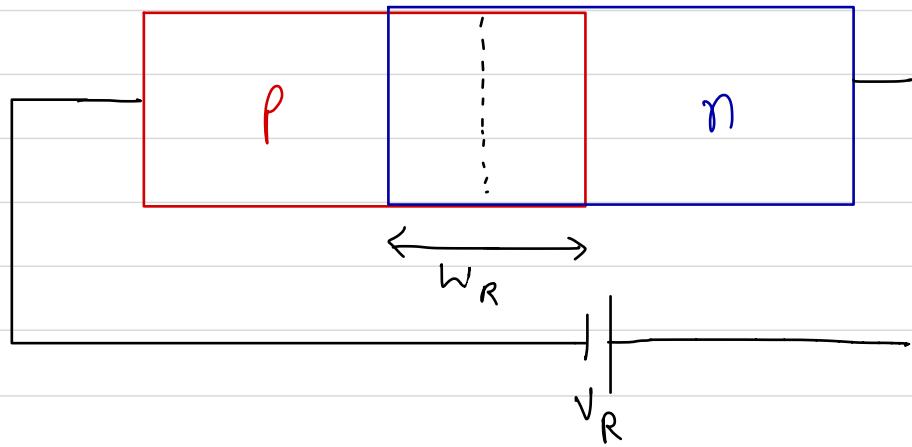
$$W_F < W$$



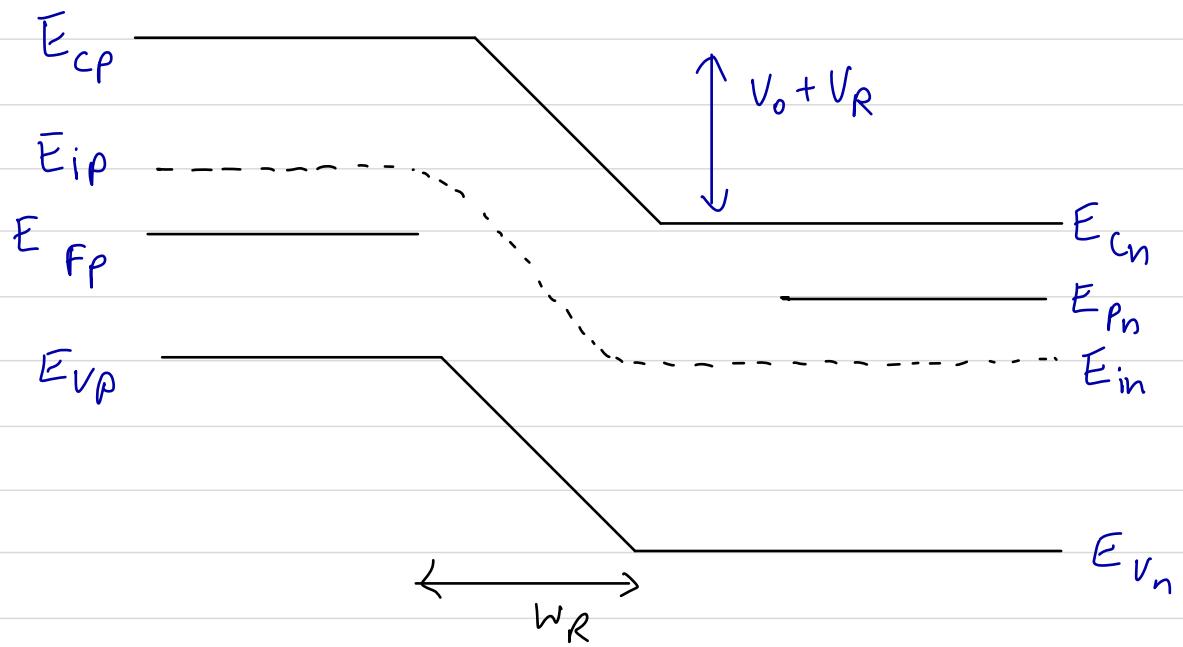
$$I = I_0 \left( \exp \left( \frac{q V_{\text{applied}}}{kT} \right) - 1 \right)$$

$I_0$  = reverse saturation current

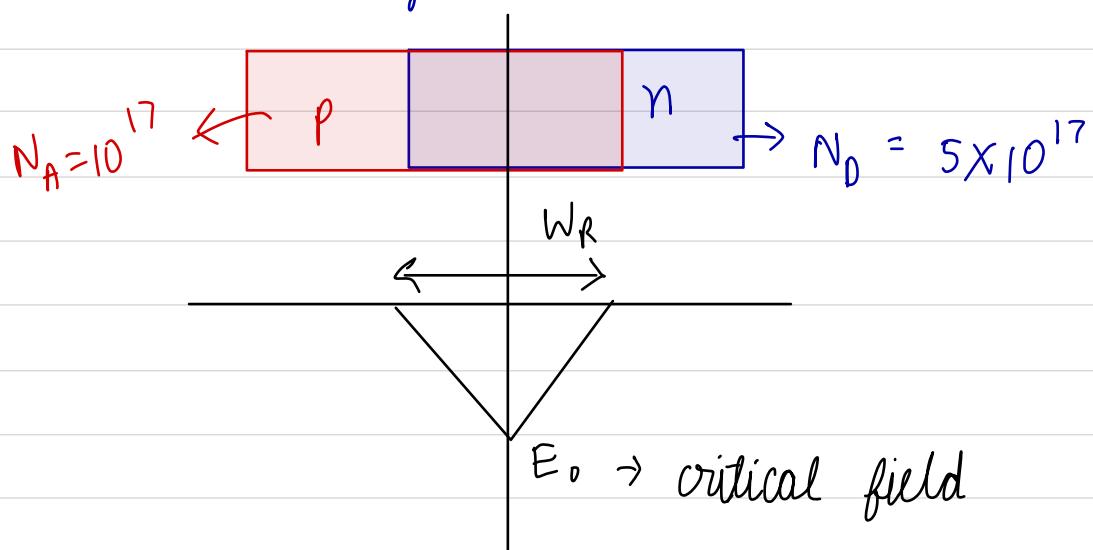
Reverse bias



$$w_R > w$$



Breakdown voltage:

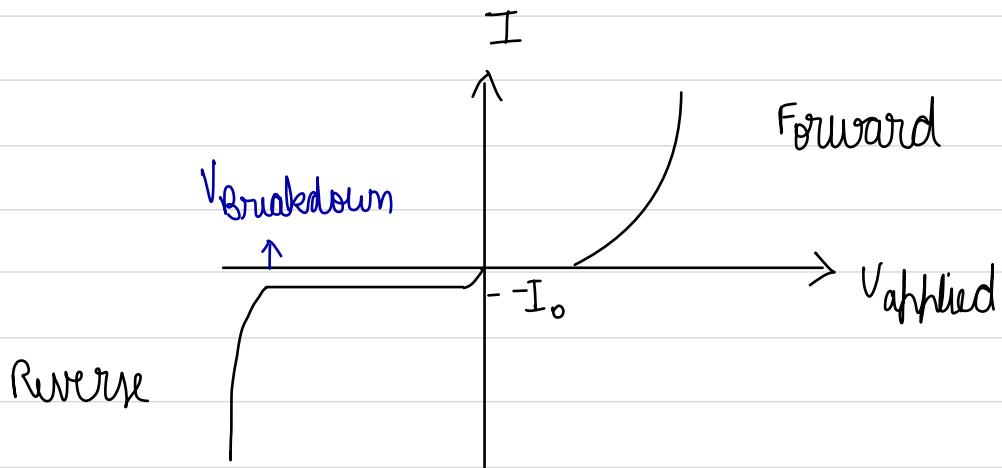


$$V_{BR} = \frac{1}{2} W_R E_{critical}$$

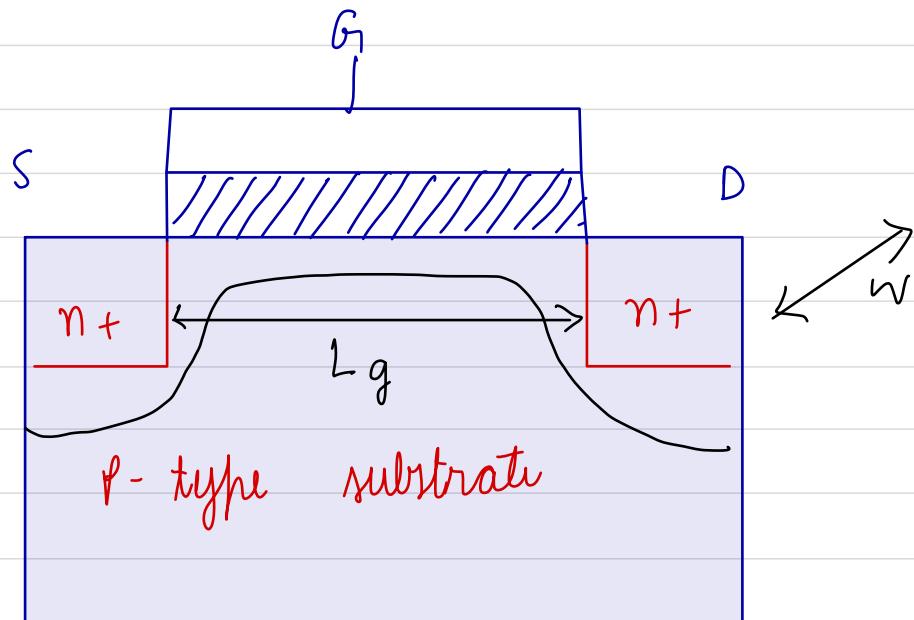
$$V_{BR} \propto W$$

Also  $W \propto \frac{1}{N_A} \quad \& \quad W \propto \frac{1}{N_D}$

$$\therefore V_{BR} \propto \frac{1}{N_A} \quad \& \quad V_{BR} \propto \frac{1}{N_D}$$



## MOSFET scaling



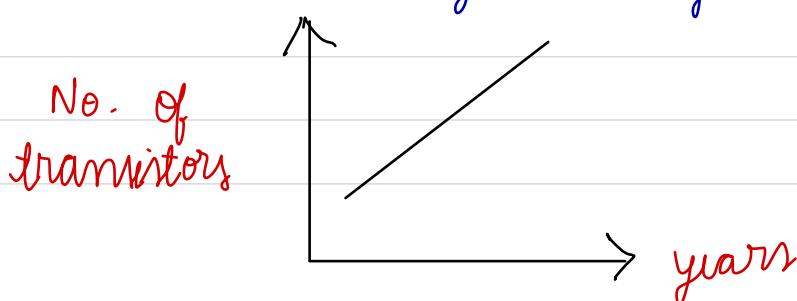
Advantages of scaling:

- 1) Transistor size can be reduced, more transistors per chip.
- 2) Increase in switching speed & frequency
- 3) Power dissipation can be reduced
- 4) Cost of electronic device reduces

Negative consequences of scaling  
→ causes short channel effects

Moore's law of scaling:

- 1) Gordon Moore - one of the founders of Intel
- 2) The number of transistors on a chip doubles in every 2 years



# Scaling rules for MOSFET

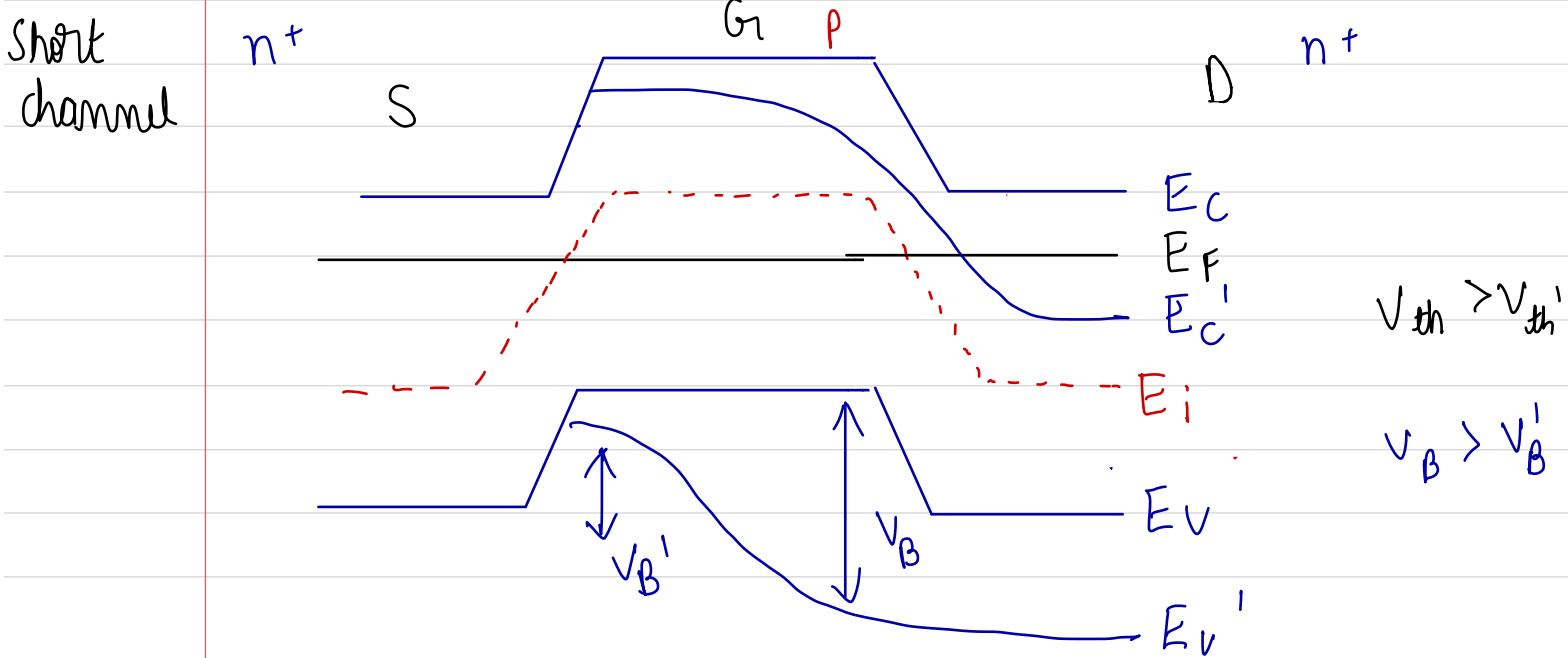
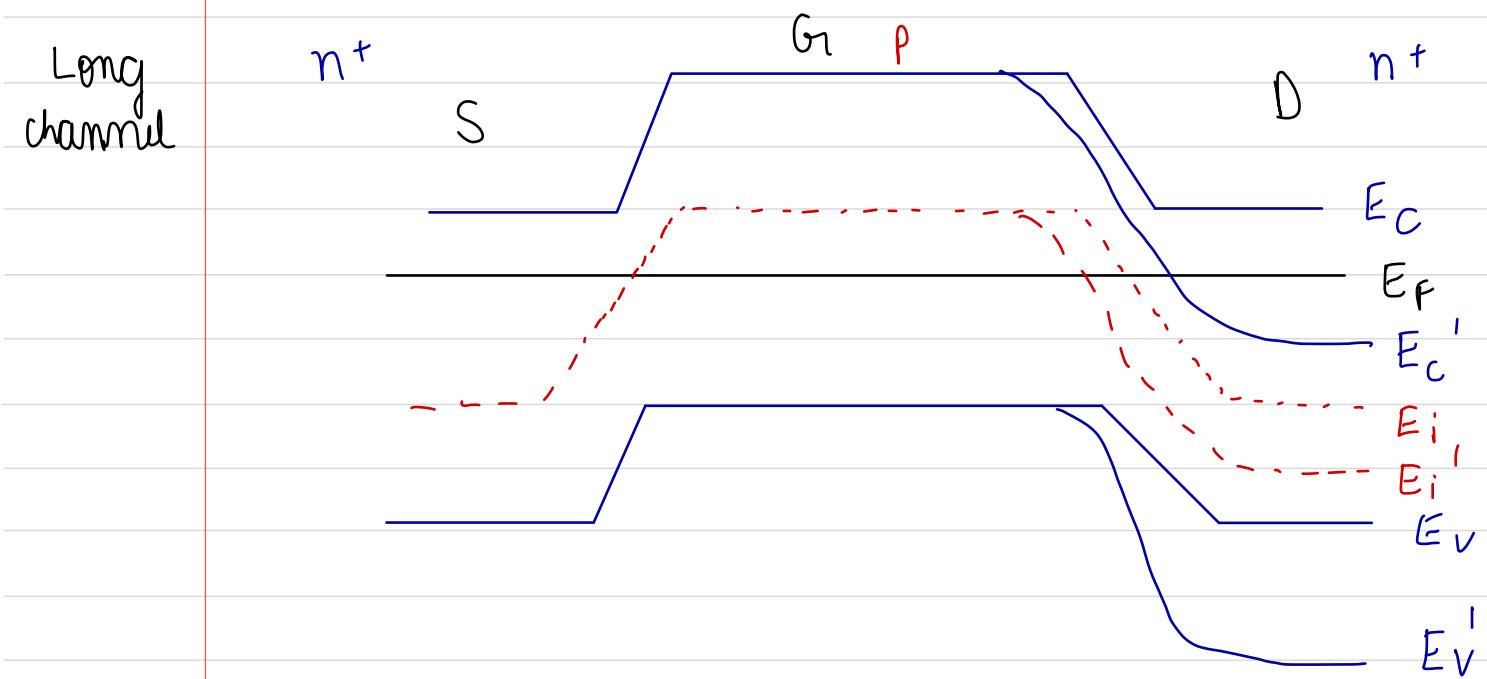
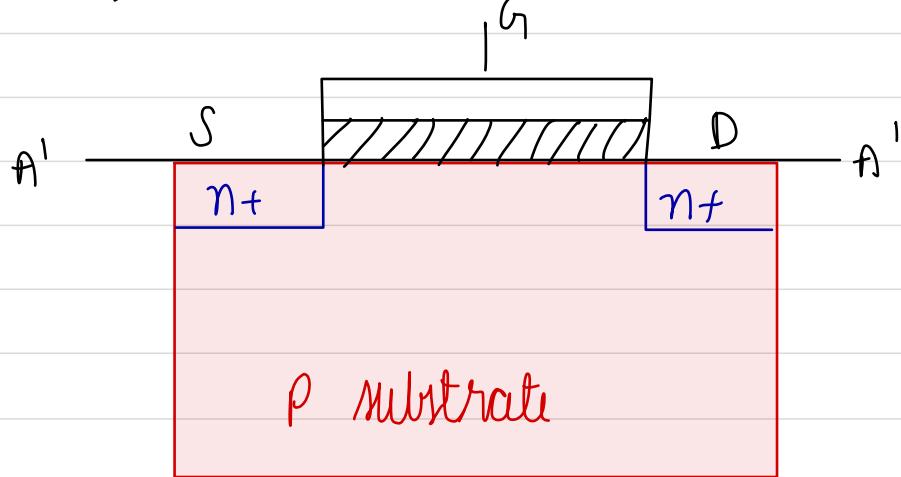
## Scaling factor

Surface dimensions ( $L, W$ )	$1/k$
Vertical dimensions ( $t_{ox}, x_j$ )	$1/k$
Impurity concentrations	$K$
Current, voltage	$1/K$
Current density	$K$
Transconductance	$1$
Capacitance for unit area	$K$
Circuit delay time	$1/K$
Power dissipation	$1/K^2$
Power density	$1$
Power delay product	$1/K^3$

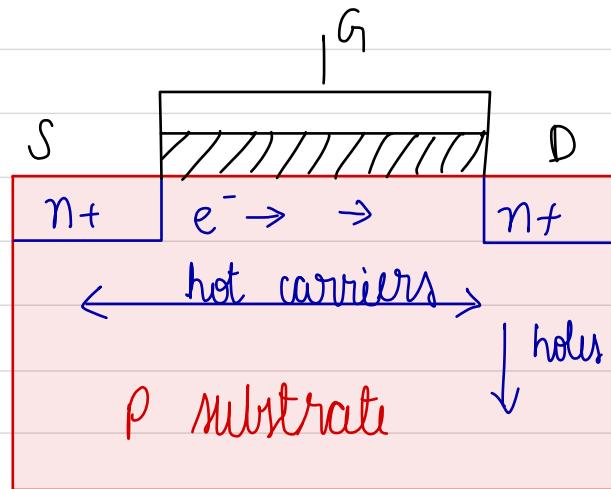
## Short channel effects:

- 1> Drain induced barrier lowering (DIBL)
- 2> Hot carrier generation
- 3> Velocity saturation
- 4> Gate induced drain leakage
- 5> Thin gate oxide breakdown
- 6> Reduction of threshold voltage
- 7> Punch through breakdown between source and drain.
- 8> Impact ionization

1) Drain induced Barrier lowering (DIBL)



## 2) Hot carrier generation

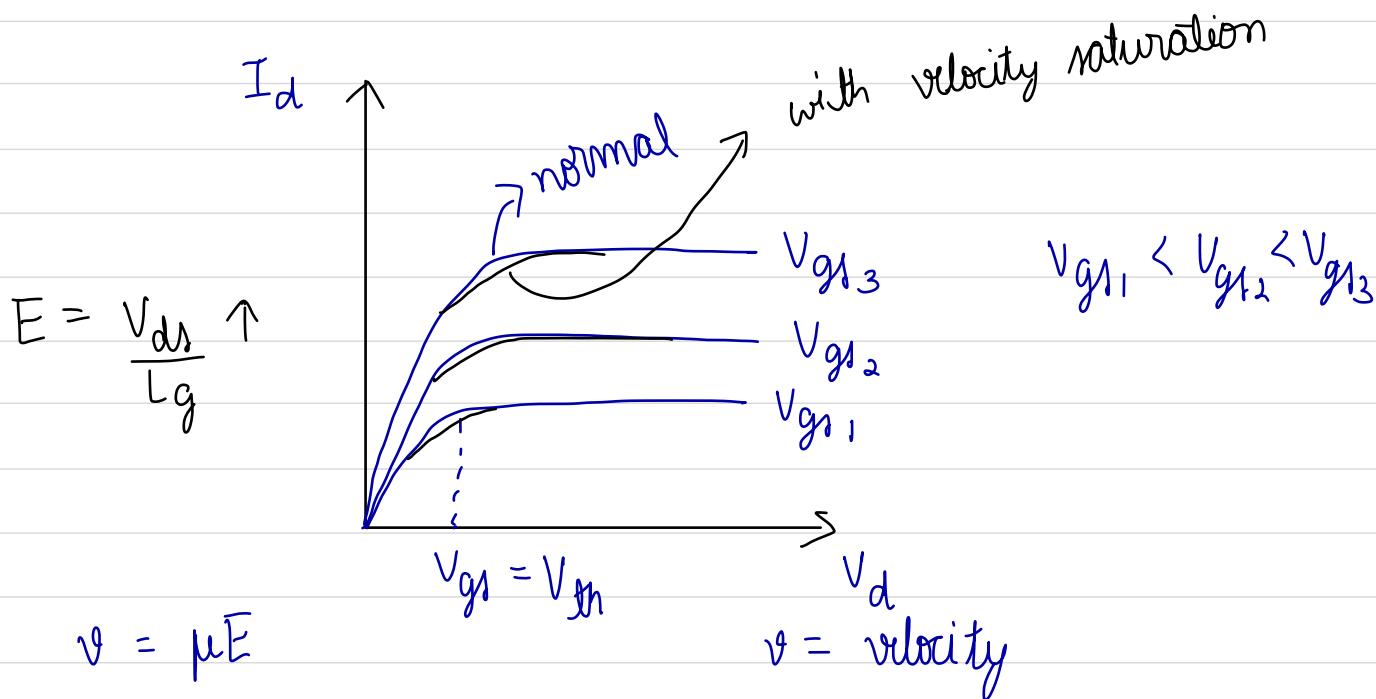


$$\uparrow E_{ds} = \frac{V_{ds}}{L_g}$$

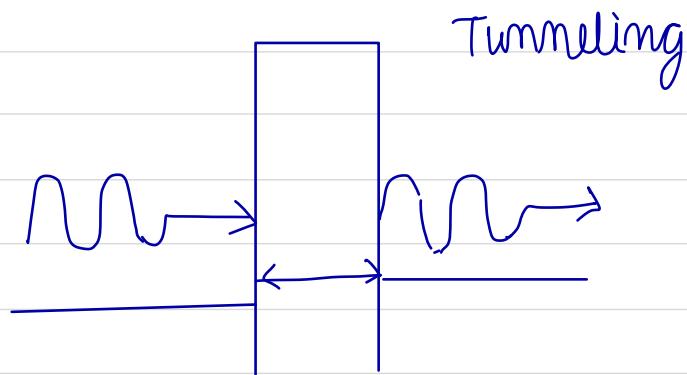
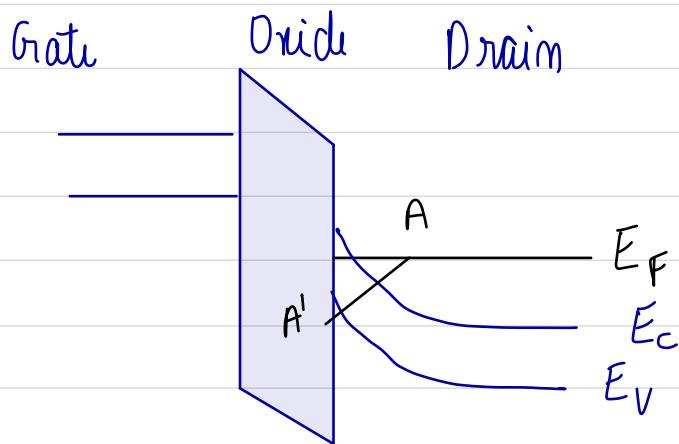
(short channel)

Breakdown  $\rightarrow$  uncontrolled increase in current leading to damage of transistors

## 3) Velocity saturation

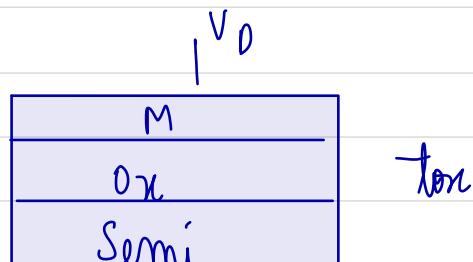


4) gate Induced Drain leakage (GIDL)



Around  $A'$  plane we have  $E_C < E_V$ .  
 $\therefore e^-$  from oxide goes on to conduction band by tunneling

5) Thin gate oxide breakdown



$E = \frac{V_{GS}}{t_{ox}}$  when  $E$  reaches  $E = 3 \times 10^5 \text{ V/cm}$  and have breakdown

Techniques to reduce short channel effects:

- 1> Use oxide with higher dielectric constant  $\kappa$ . For eg:  $\text{SiO}_2$  ( $\kappa = 4$ ),  $\text{HfO}_2$  ( $\kappa = 23$ )
- 2> Increase gate thickness

NOTE: EOT (Effective oxide thickness): The equivalent thickness to replace  $\text{SiO}_2$

- 3> Halo implants near junction
- 4> Silicon on insulation
- 5> Multigate transistors

Q> List 5 technology nodes & give examples for each

- Ans
- i> 7nm = Snapdragon 865
  - ii> 22nm = Intel Xeon E5, Intel Ivy-Bridge
  - iii> 65 nm = Intel Pentium 4
  - iv> 180 nm = Intel Pentium 3 Celeron
  - v> 5 nm = Snapdragon 8 Gen1, Apple M1
  - vi> 2 nm = Intel Arrow lake
  - vii> 3 nm = Apple M3

Advantages of high  $k$  dielectric:

- 1) Thick oxide can be used reducing leakage current
- 2) Reduced chances of leakage current
- 3) Reduces short channel effect
- 4) More drain current due to improved capacitance. Eg:  $\text{HfO}_2$ ,  $\text{Zr}_2\text{O}_3$ ,  $\text{Al}_2\text{O}_3$

Disadvantages of high  $k$  dielectric:

- 1) Interface between high  $k$  dielectric and Silicon is not as good as  $\text{Si-SiO}_2$ .
- 2) Interface charges increase
- 3) Parasitic capacitance increases
- 4) Process complexity increases as self-aligned process cannot be used.
- 5) Problems related to Fermi level pinning

Q) A MOSFET with  $t_{ox} = 5 \text{ nm}$  is scaled down such that  $C_{ox}$  is reduced to half. If the scaled MOSFET is using  $\text{HfO}_2$ . Find the new gate oxide thickness.

Ans

$$\epsilon_{\text{HfO}_2} = 24 \quad \epsilon_{\text{SiO}_2} = 4$$

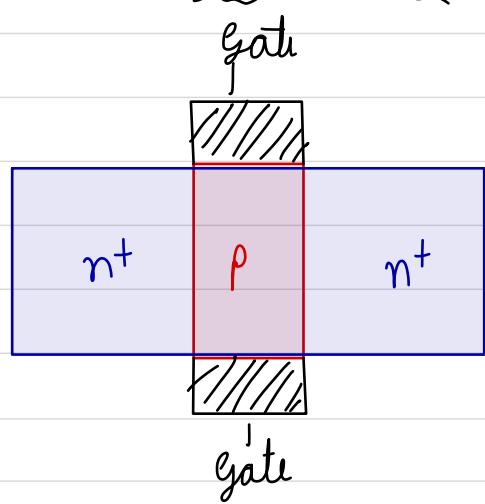
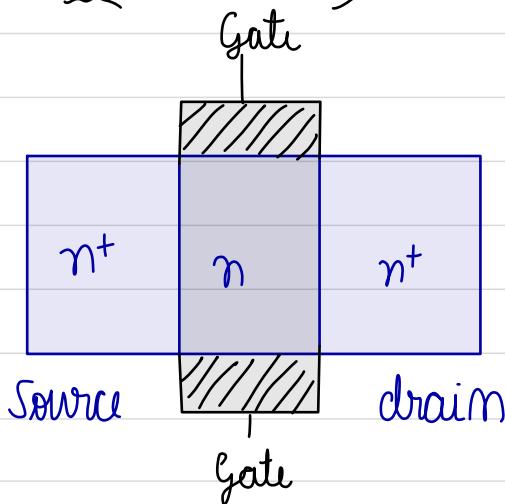
$$\frac{C_{ox_2}}{C_{ox_1}} = \frac{1}{2}$$

$$\frac{\epsilon_{ox_2}}{\epsilon_{ox_1}} \cdot \frac{t_{ox_1}}{t_{ox_2}} = \frac{1}{2}$$

$$\frac{24}{4} \cdot \frac{5}{x} = \frac{1}{2}$$

$$\therefore t_{ox} = 60 \text{ nm}$$

## Difference between junctionless FETs & FETs



Double gate junctionless  
field effect transistor

Double gate conventional  
FET with junction

### Junctionless FET

- 1) Normally ON
- 2) Channel region is doped with n type
- 3) No pn junctions are there
- 4) Less short channel effects
- 5) Less complex fabrication process & less number of Lithography steps

### Conventional FET

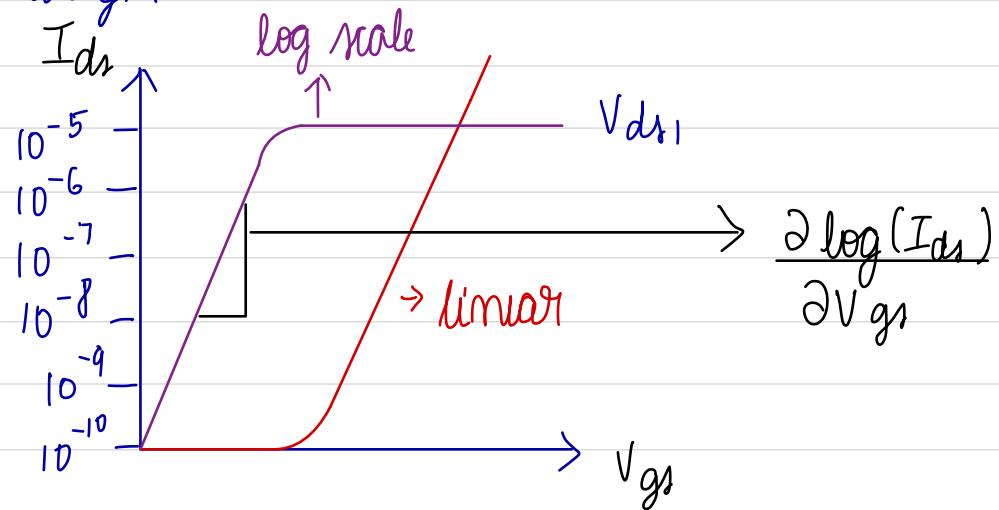
- 1) Normally OFF
- 2) Channel region is doped with p type.
- 3) pn junctions at source channel and drain channel
- 4) More short channel effects
- 5) More complex fabrication process & more number of Lithography steps

↳ Scaling is possible

↳ Scaling is difficult.

$$\frac{I_{on}}{I_{off}}$$
 ratio

- It is a performance metric for Low power VLSI design.



$I_{off}$  = Drain current at  $V_{gs} = 0$  or when the device is OFF. It is determined by the leakage current.

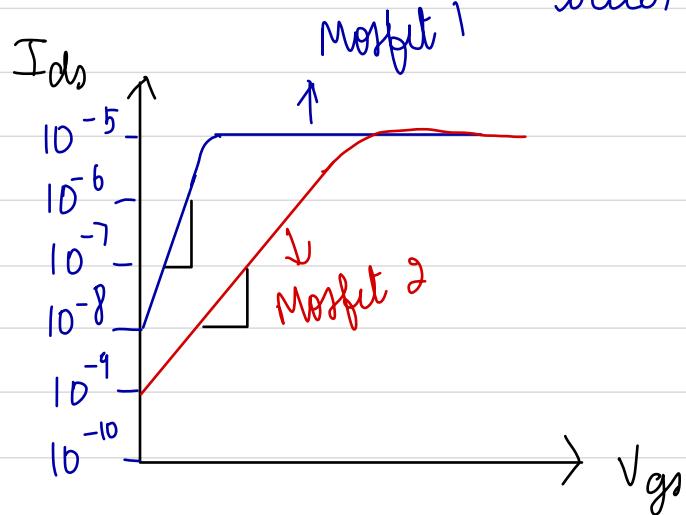
$I_{on}$  = saturated drain current when  $V_{gs}$  is higher.

For better device  $I_{on}/I_{off}$  should be as high as possible.

Subthreshold slope (SS)

$$\left[ \frac{\partial \log(I_{ds})}{\partial V_{gs}} \right]^{-1}$$

- SS should be less for better performance



For bulk MOSFETs or SOI MOSFET,

$$SS = 2.3 \frac{kT}{q} \left[ 1 + \frac{C_d + C_{it}}{C_{ox}} \right]$$

$k$  = Boltzmann constant

$T$  = temperature in K

$q$  = electron charge

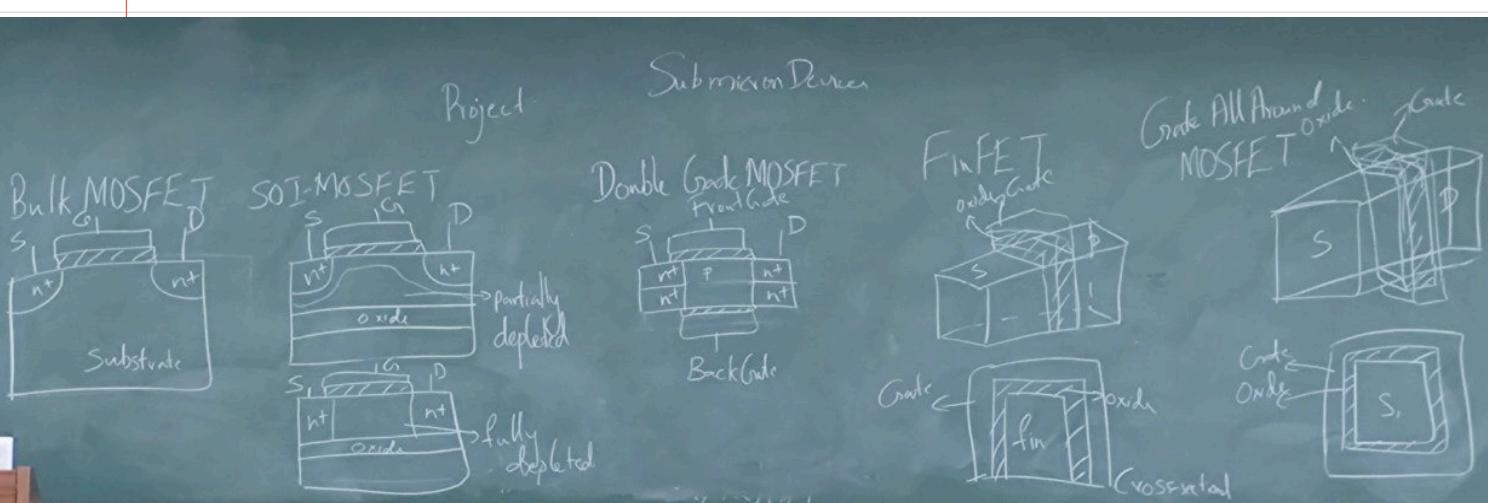
$C_d$  = depletion capacitance

$C_{it}$  = capacitance due to interface trap charge

$C_{ox}$  = gate oxide capacitance

Minimum SS =  $\frac{2.3 kT}{q} = 60 \text{ mV/V decade}$

Type of MOSFETs



## Strain engineering in MOSFETs

To scale down and maintain high speed, current to charge capacitance should be increased

$$I_{ds} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2$$

2 types of strain:

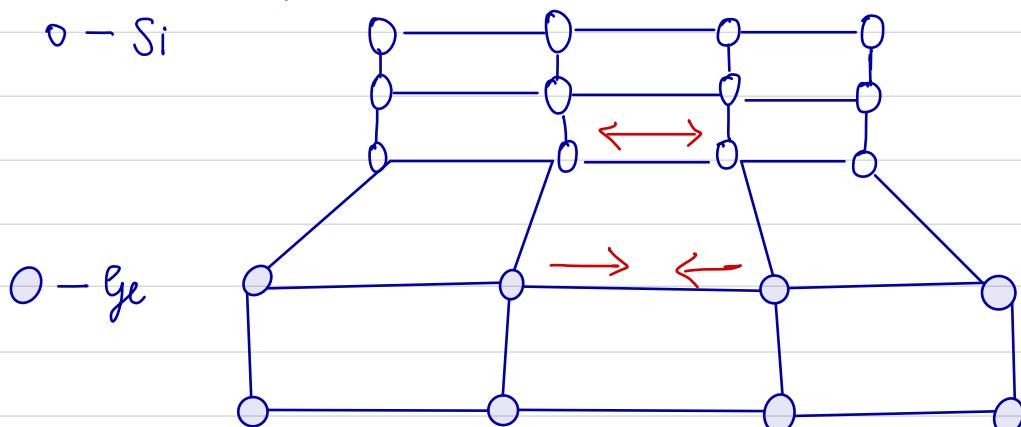
- 1> Tensile strain =
- 2> Compressive strain =

Another way of classification of strain is:

- 1> Global strain engineering
- 2> Local strain engineering

1> Global strain engineering: Put strain over entire wafer in orthogonal directions  
(Biaxial strain)

Developing strain globally:



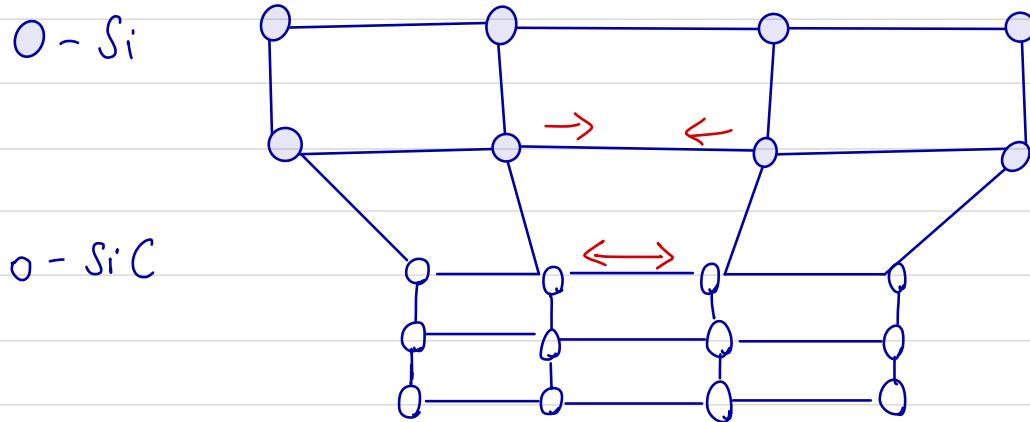
Size of  $Ge >$  size of  $Si$

- So distance between atoms in lattice of  $Ge > Si$

- The above formation is called epitaxial Si deposition.

∴ At boundary of Si, Ge, there is a strain created due to position.

→ Similarly Si - SiC has lesser strain than Si - Ge

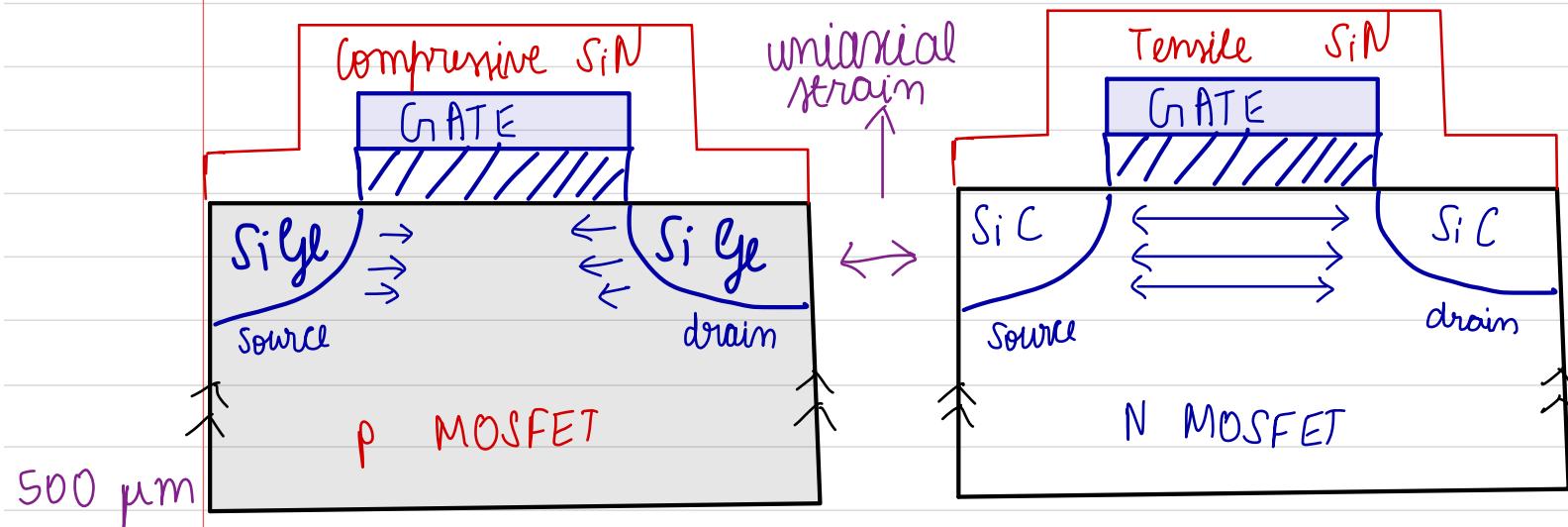


- Global strain is generated by epitaxy of a thin strained Si layer on a thick relaxed SiGe virtual substrate.

Drawbacks:

- 1> Fabrication process should be compatible to the thermal budget to prevent Ge migration at high temperature.
- 2> Expensive substrate
- 3> causes defects in epitaxial Si
- 4> It can provide only one type of strain while holes and electrons act differently.

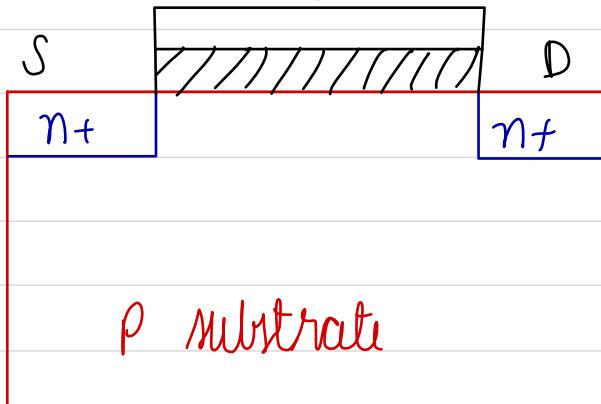
## 2) Local strain engineering;



### Advantages:

- 1) Strain can be independently tailored to optimize performance enhancement for both n & p mosfets.
- 2) Threshold voltage shift is smaller in uniaxially stressed mosfets.
- 3) Process is cheaper and compatible with standard CMOS fabrication process-flow.

## Equivalent circuit model



TCAD & SPICE simulators are used.

### TCAD modeling:

- 3 equation:
  - 1> current continuity method equation
  - 2> Poisson equation
  - 3> Temperature equation

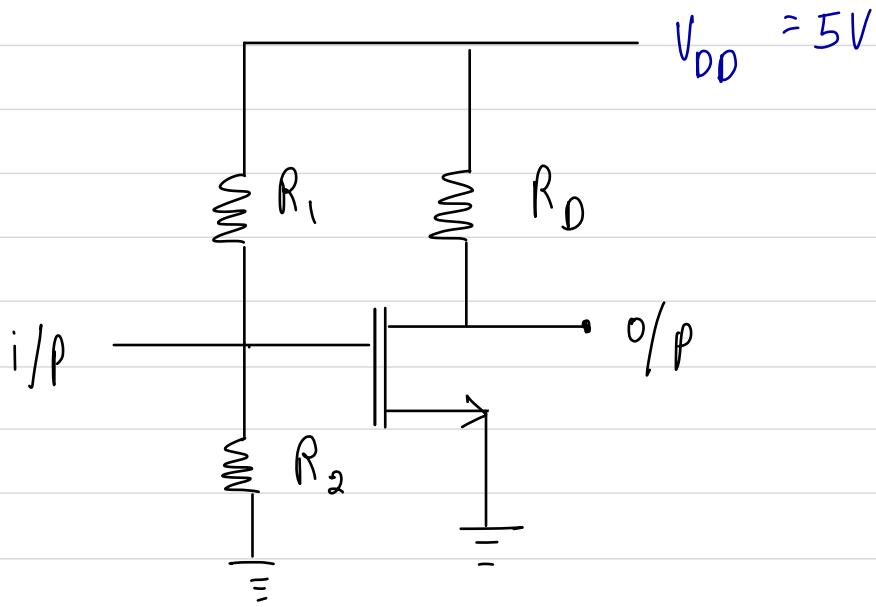
These equations can be solved using:

- 1> finite element method
- 2> finite difference method.

### SPICE modeling:

- 1> circuit simulation and design
- 2> combination of circuit components like resistor, inductor, current source, voltage source
- 3> solving simpler KCL, KVL equations of form  
 $I = f(V)$

large signal model      v/s      small signal model



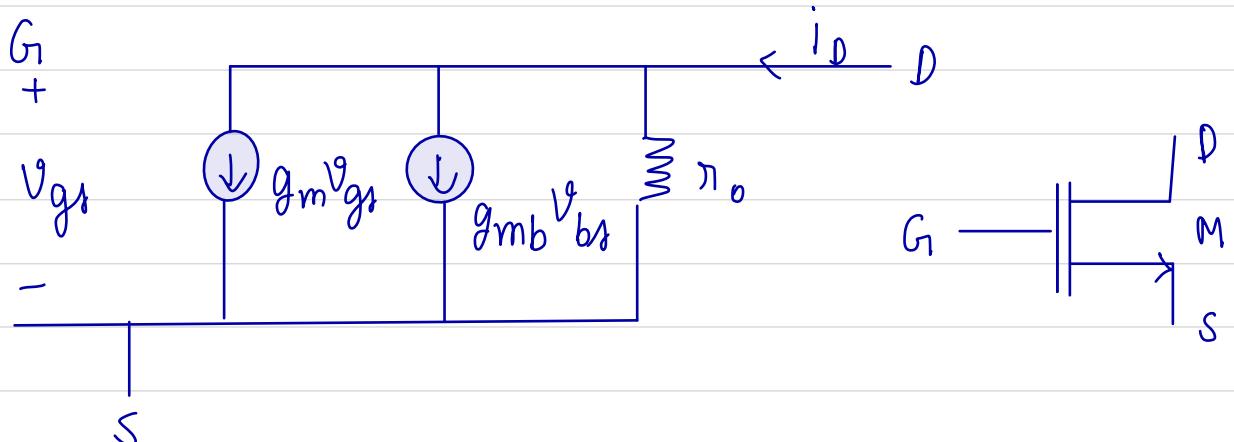
Small signal modelling:  $i = f(v)$   
 $C = f(v)$

Large signal modelling:  $I = f(V)$   
 $Q = f(V)$

$$I_D = g_m V_{GS} + g_{mb} V_{BS} + \frac{V_{DS}}{r_o}$$

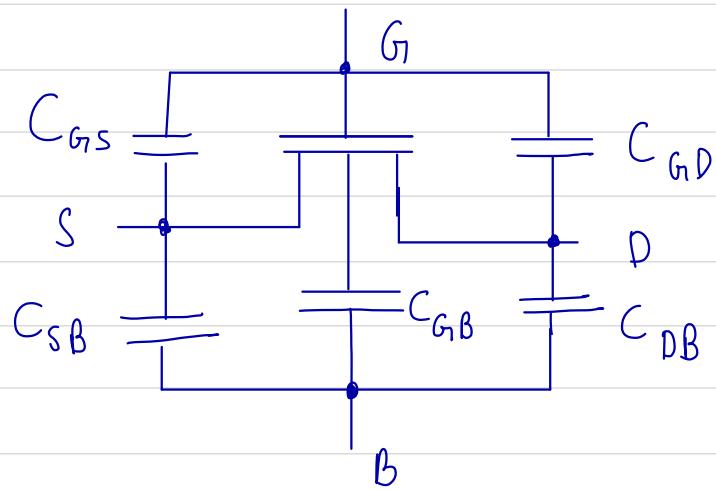
→ The circuit elements are linear:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad g_o = \frac{1}{r_o} = \frac{\partial I_D}{\partial V_{DS}} \quad g_{mb} = \frac{\partial I_D}{\partial V_{BS}}$$

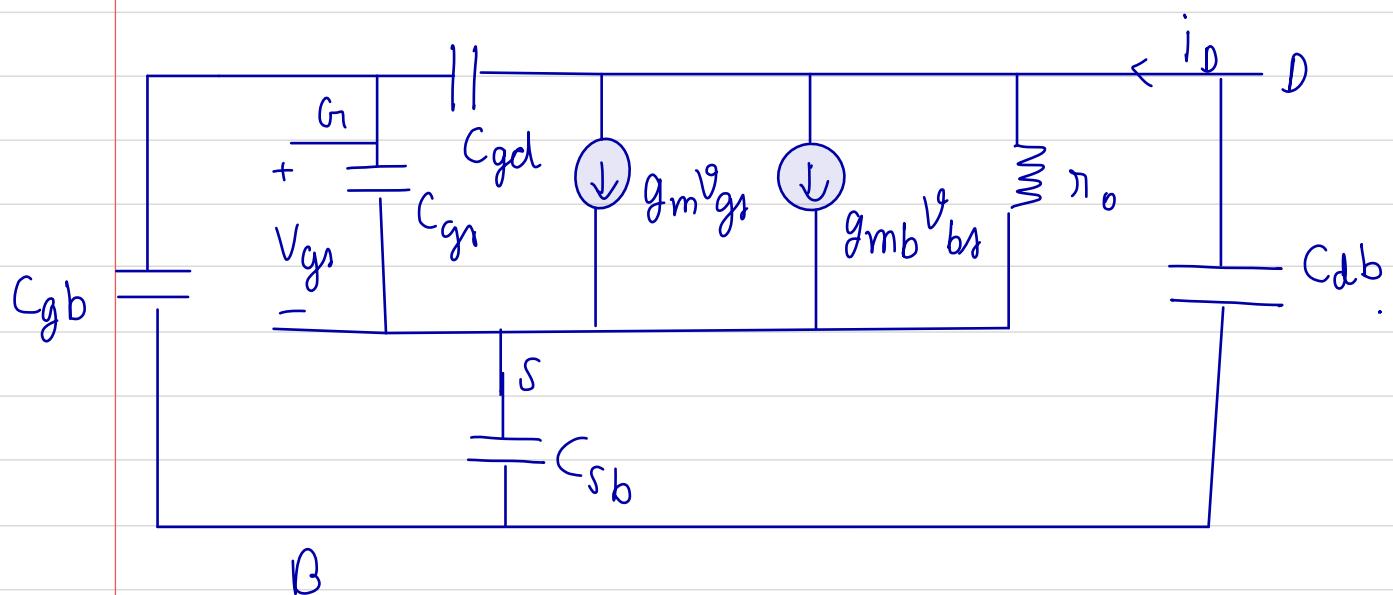


Steps for small signal equivalent circuit modeling:

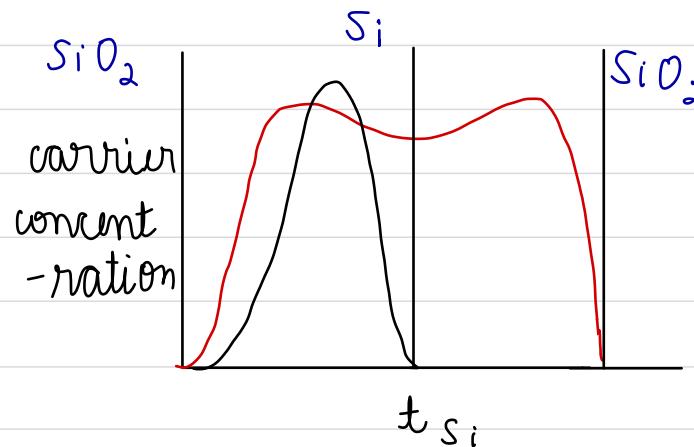
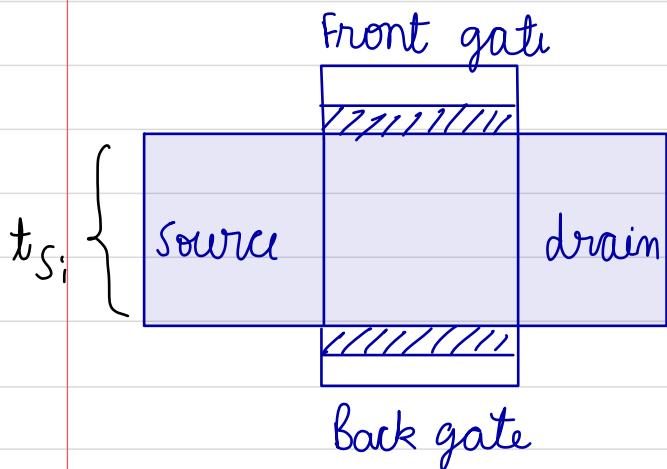
- 1> Replace transistor with it's small signal equivalent
- 2> DC voltage sources are short circuited.
- 3> DC current sources are open circuited.



High frequency small signal modelling including capacitor:



## Double gate MOSFET modelling



Advantages :

- 1> Reduced short channel effect occurring due to scaling
- 2> Improved switching speed due to reduced capacitance
- 3> Current increases by volume inversion.
- 4> Reduced static and dynamic power dissipation.

Disadvantages :

- 1> Fabrication process is complex and expensive
- 2> Device variability is more.
- 3> SPICE modelling is complex .
- 4> Parameter extraction is difficult due to more model parameters .

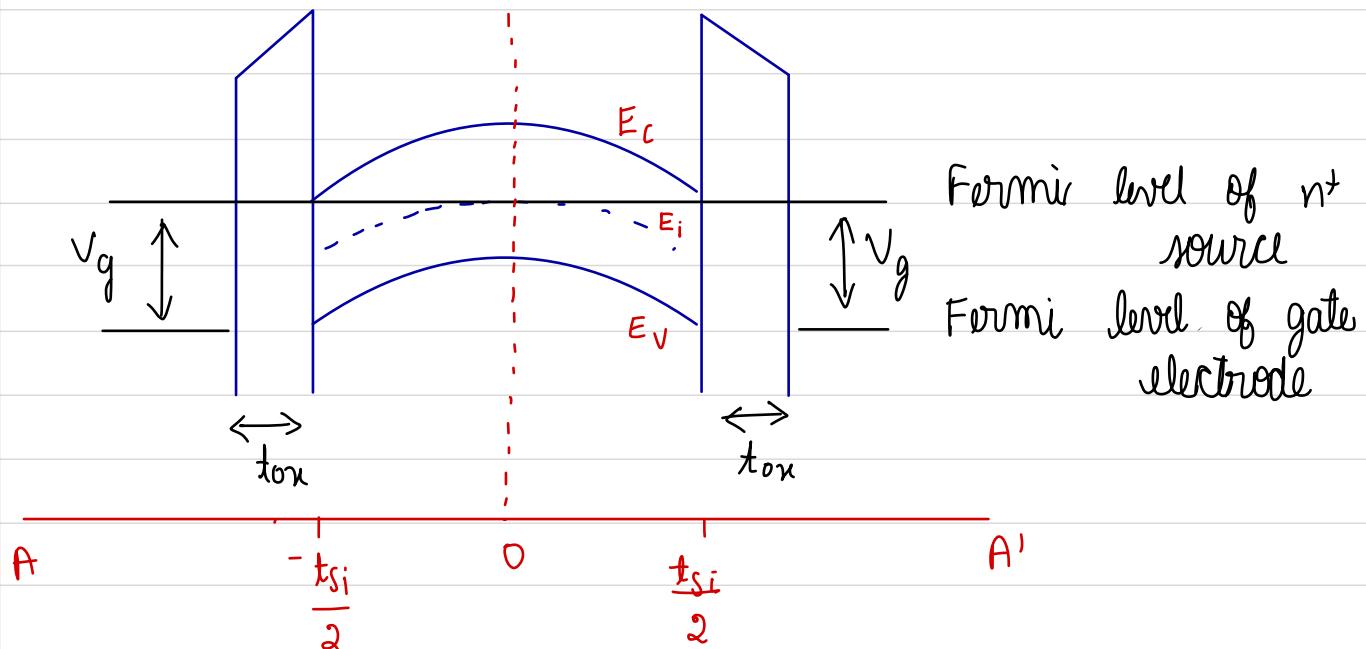
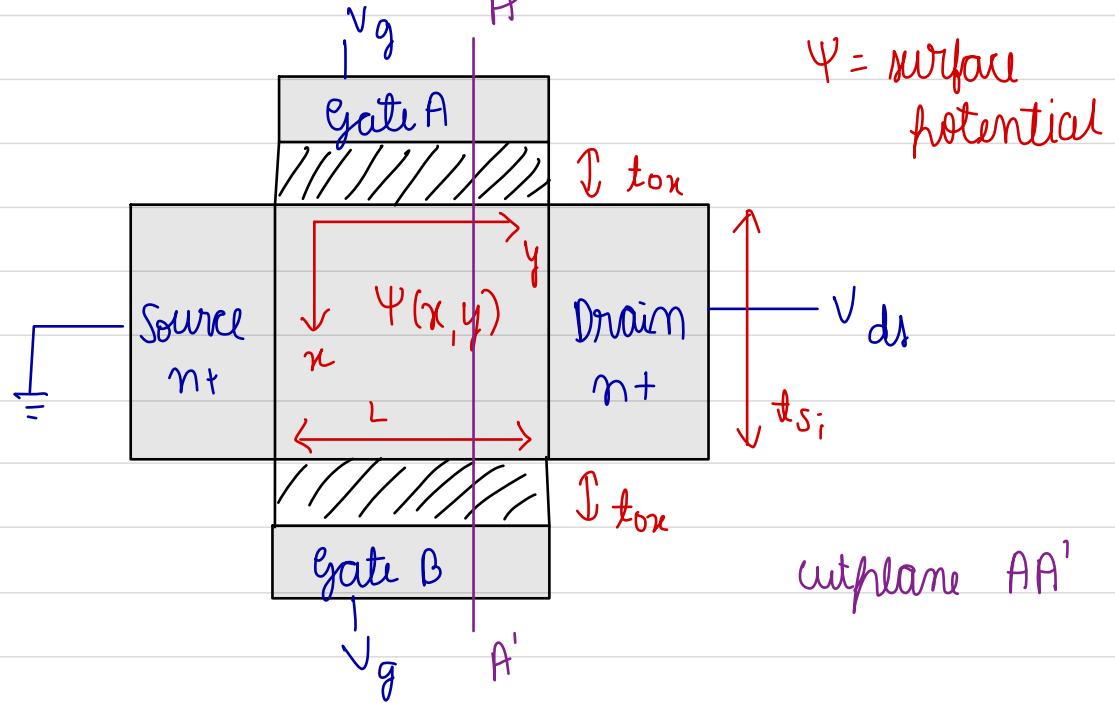
Pao-Sah integral model for MOSFET

$$I_{ds} = \mu \frac{W}{L} \int_{V_{ds}}^{V_{ds}} Q_i(V) dV$$

$$= \mu \frac{W}{L} \int_{\beta_0}^{\beta_d} Q_i(\beta) \frac{dV}{d\beta} d\beta$$

where  $\beta_0$ ,  $\beta_d$  are parameters at  $V=0$  and  
 $V = V_{ds}$  and  $Q_i$  is inversion charge.

Drain-current model for double gate MOSFET



Poisson's equation along vertical cut perpendicular to Si film

$$\frac{d^2\psi}{dx^2} = \frac{q}{\epsilon_{Si}} e^{\left(\frac{\psi - V}{kT}\right)}$$

$$\therefore \psi(x) = V - \frac{2kT}{q} \ln \left[ \frac{t_{Si}}{\beta} \left( \sqrt{\frac{q^3 n_i}{2 \epsilon_{Si} kT}} \right) \cos \left( \frac{2\beta x}{t_{Si}} \right) \right]$$

$\beta$  = constant &  $V$  = voltage in Si between source & drain

Using Par-Sah integral & above equation:  
For linear region:

$$I_{ds} = 2\mu C_{ox} \frac{W}{L} \left( V_g - V_{th} - \frac{V_{ds}}{2} \right) V_{ds}$$

$$= 2\mu C_{ox} \frac{W}{L} \left[ (V_g - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

For saturation region:

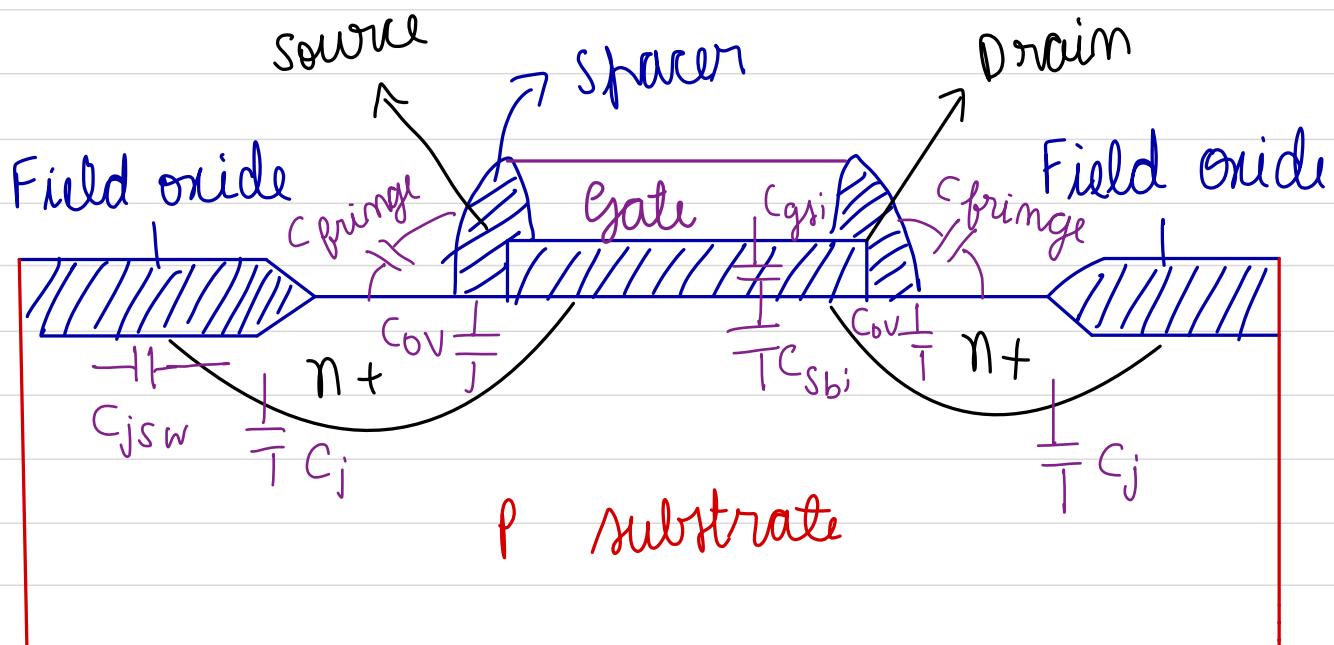
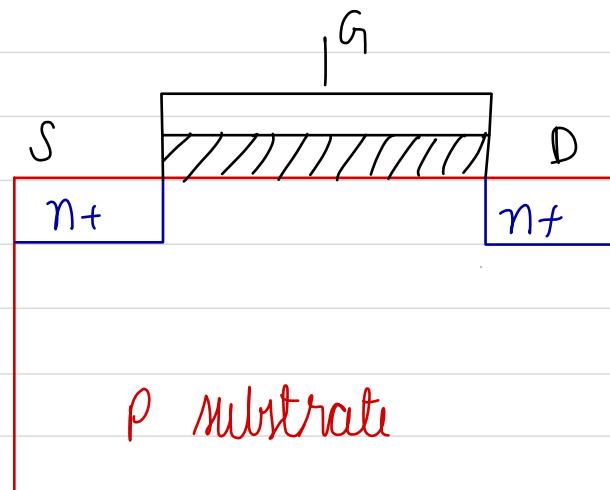
$$I_{ds} = \mu C_{ox} \frac{W}{L} \left[ (V_{gs} - V_{th})^2 - \frac{8\gamma^2 k^2 T^3}{q^2} e^{q \left( \frac{V_g - V_o - V_{ds}}{kT} \right)} \right]$$

$$\text{where } \gamma = \frac{\epsilon_{Si} t_{ox}}{\epsilon_{ox} t_{Si}} = \frac{C_{Si}}{C_{ox}}$$

$$V_o = \Delta\phi + \frac{2kT}{q} \ln \left[ \frac{2}{t_{Si}} \sqrt{\frac{2\epsilon_{Si} kT}{q^2 n_i}} \right]$$

↓  
constant

Capacitances in high frequency case for MOSFET



$\Rightarrow C_{gs} \equiv$  intrinsic gate capacitance + overlap capacitance + fringe capacitance

$$\Rightarrow C_{gs} = C_{gss} + C_{ov} + C_{fringe}$$

$\Rightarrow C_{gd} \equiv$  overlap capacitance + fringe capacitance

$$\Rightarrow C_{gd} = C_{ov} + C_{fringe}$$

3>  $C_{gb} \equiv$  Parasitic capacitance

↳  $C_{Sb} \equiv$  source junction capacitance + side wall  
+ channel substrate capacitance

$$\Rightarrow C_{Sb} = C_j + C_{jsw} + C_{sbi}$$

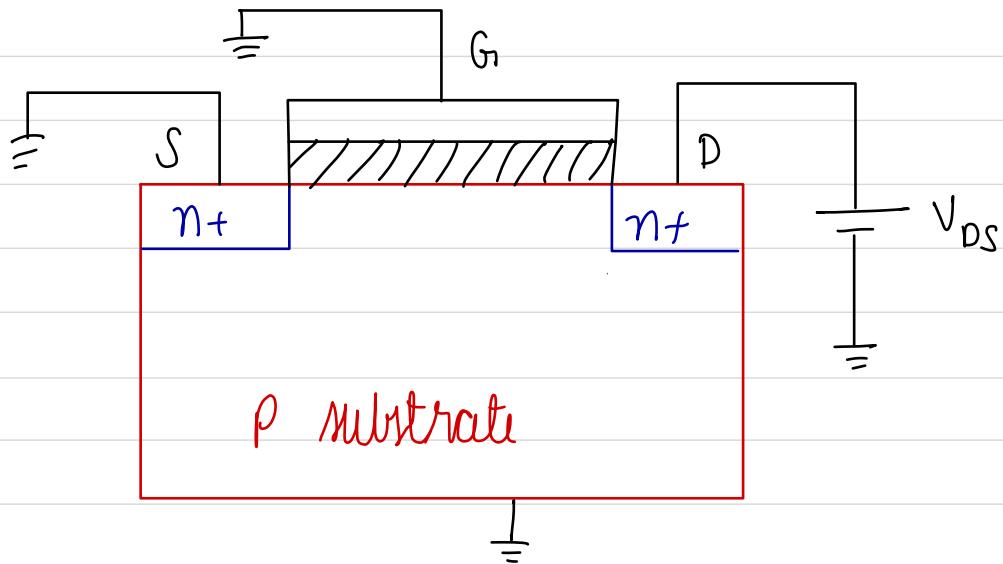
5>  $C_{db} \equiv$  drain junction capacitance + side wall

$$\Rightarrow C_{db} = C_j + C_{jsw}$$

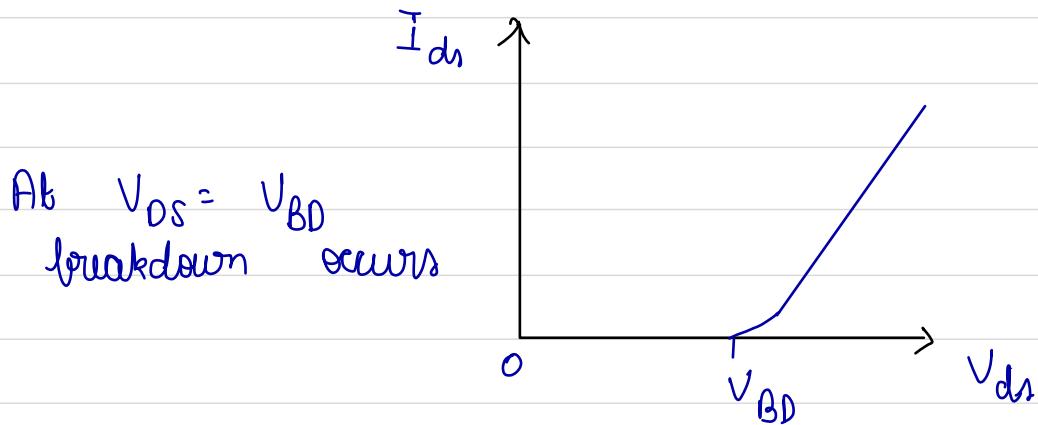
Equivalent formula :

$$1> C_{gs} \equiv \frac{2}{3} WL C_{ox} + WC_{ov} + C_{fringe}$$

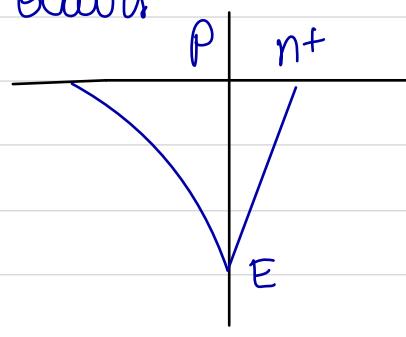
## Drain extended devices



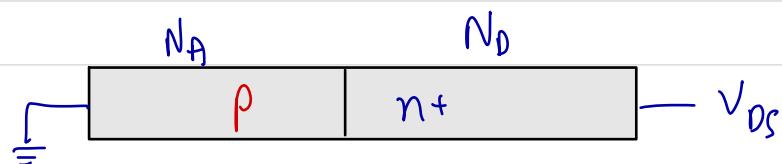
Electric vehicle applications:  
→ high breakdown voltage MOSFETs.

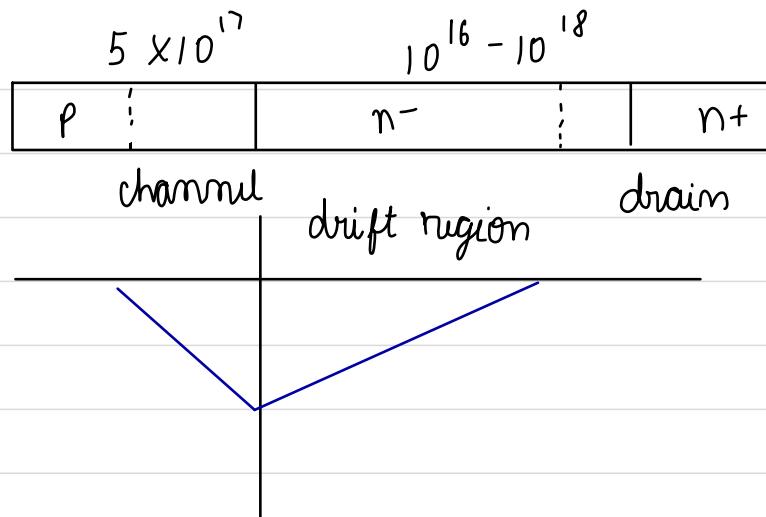


Weak electric field at junction of  $p n^+$  ⇒ breakdown occurs



We want to increase  $V_{BD}$





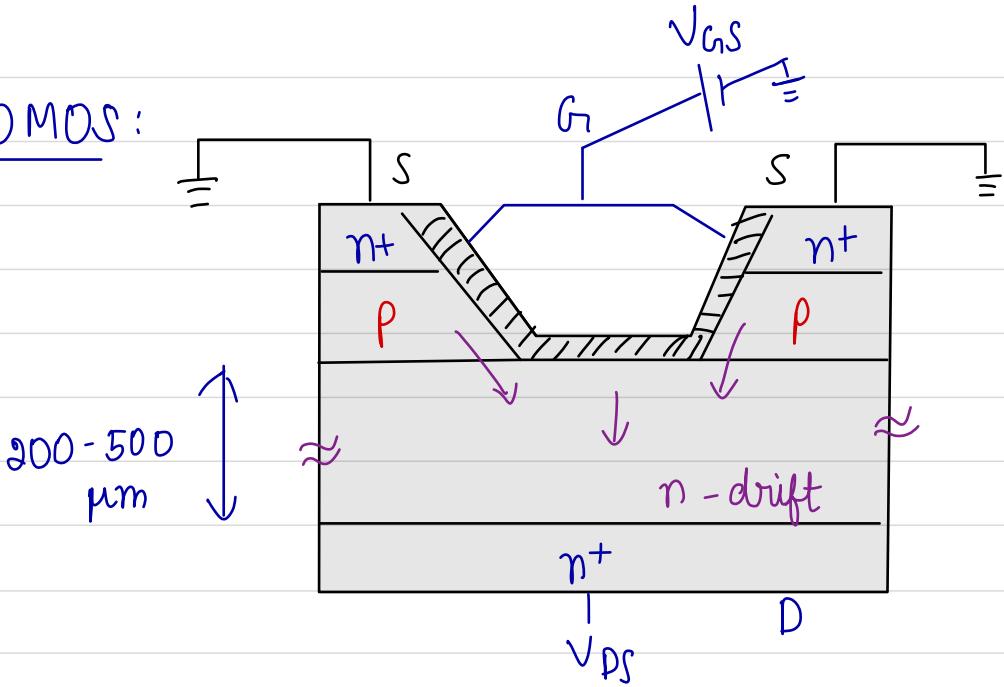
There are 2 types of DMOS (drain extended MOS) :

- 1> Vertical DMOS (VDMOS)
- 2> Lateral DMOS (LDMOS)

Differences between lateral & vertical DMOS:

Vertical	Lateral
1> Current flow in vertical direction	1> Current flow in lateral direction.
2> Integrated circuit is not possible	2> Integrated circuit is possible.
3> Very high power device is possible	3> Very high power device is not possible
4> Used in high power application	4> Power IC applications
5> Large size devices	5> comparatively smaller

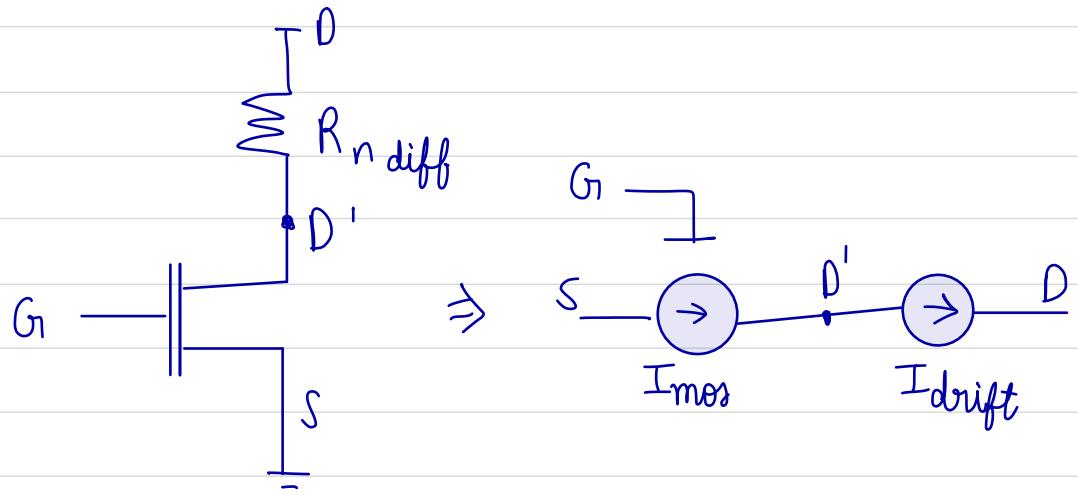
VDMOS:



$$V_{BD} \propto t_{drift}$$

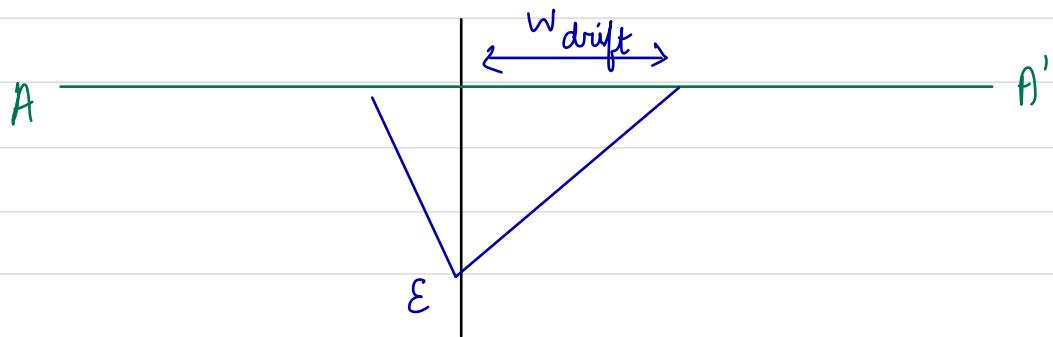
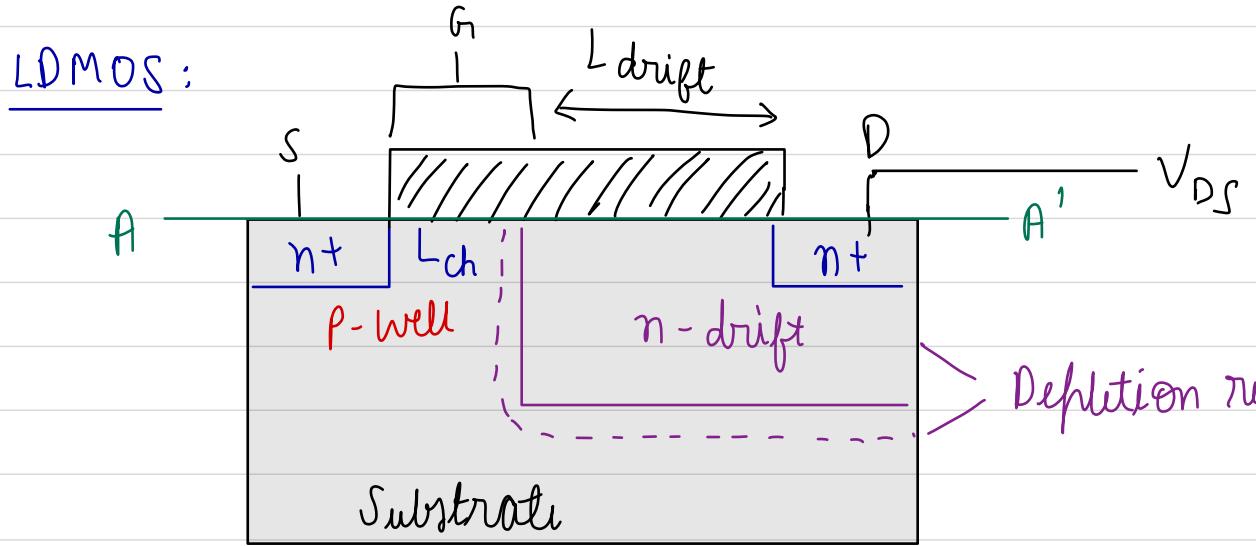
$$R_{on} \propto t_{n\text{ drift}}$$

Modul : MOSFET model  
Resistor model



$$I_{mos} = f(V_{D's}, V_{GS})$$

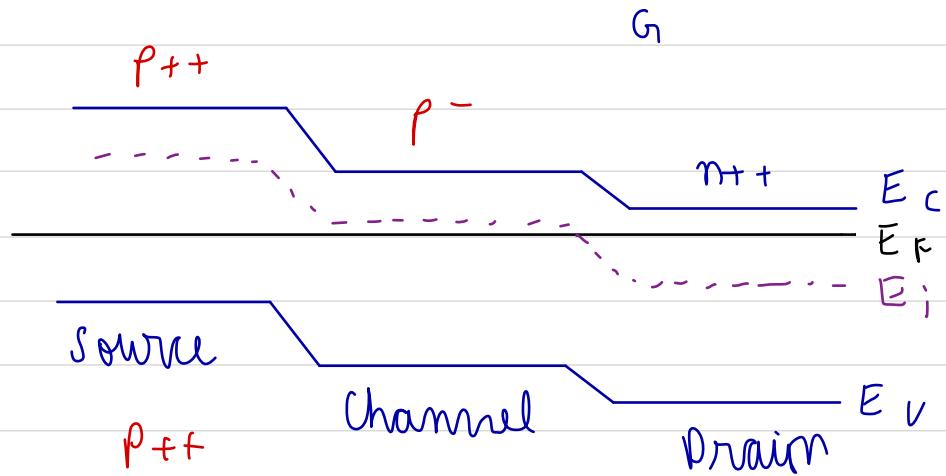
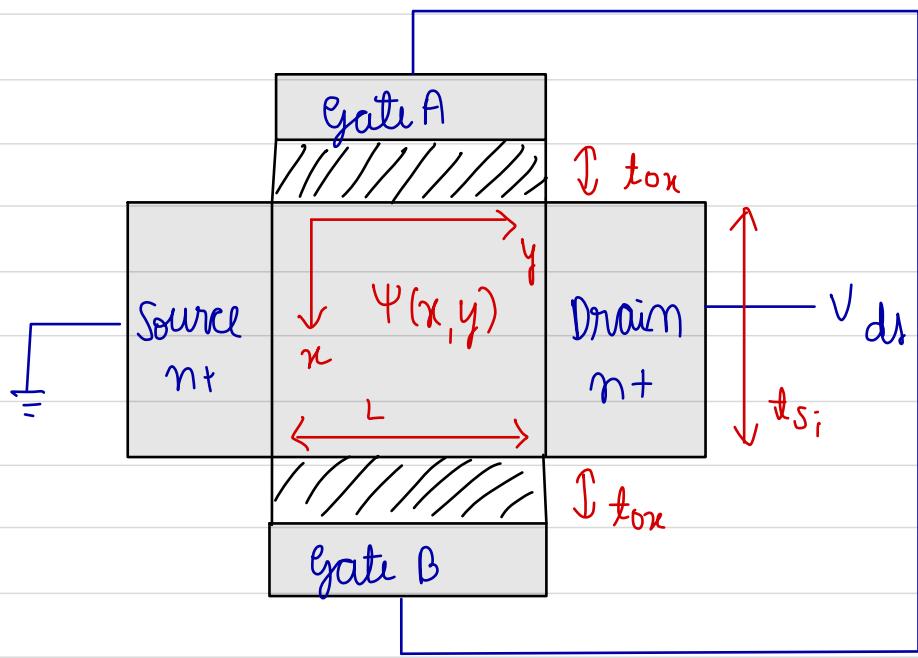
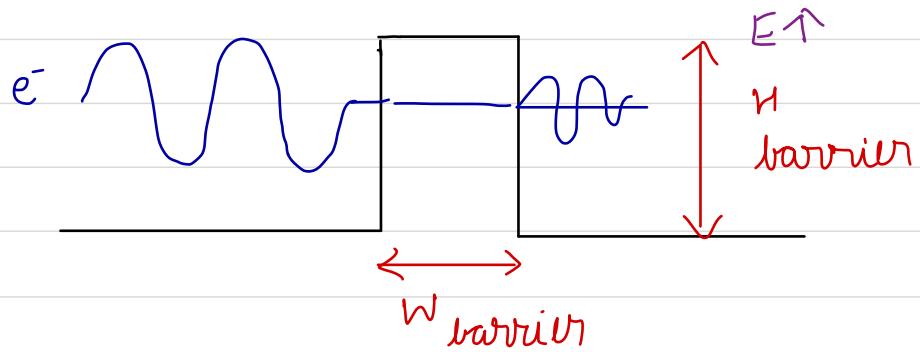
$$I_{drift} = f(V_{DD'})$$



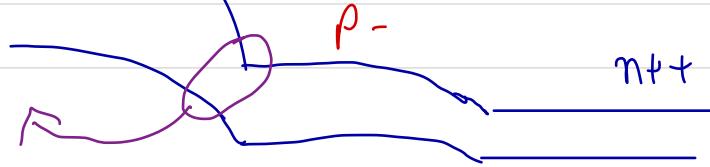
Techniques to improve  $V_{BD}$  in latent DMOS

- 1> RESURF or reduced surface electric field
- 2> Trench gate type
- 3> Field plated DMOS
- 4> Super junction type.

# Tunnel FET



tunnelling length



But here  $I_{ds} \propto I_{\text{tunnelling}}$

Here gate due to tunnelling controls  $I_{\text{channel}}$ . But same gate controls  $I_{ds}$  here.  
 $\therefore I_{on}$  is too low

Disadvantage:  $I_{on}$  current is too small to drive other circuit component.

Tunnelling: The tunnelling efficiency at source channel junction can be calculated using WKB approximation

$$I_{ds} \approx T_{WKB} \approx \exp \left[ -\frac{4\sqrt{2m^*}}{3q\hbar} \frac{E_g^{3/2}}{E} \right]$$

$T_{WKB} \rightarrow$  tunnelling probability

$m^* \rightarrow$  effective mass

$E_g \rightarrow$  Band gap

$E \rightarrow$  Electric field at the source channel tunnel junction

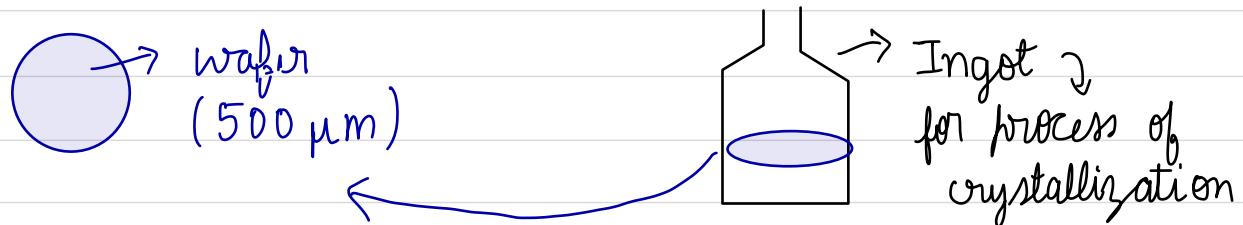
$\hbar = \frac{h}{2\pi} \rightarrow$  Planck's constant

$q \rightarrow$  electric charge

## CMOS Process flow

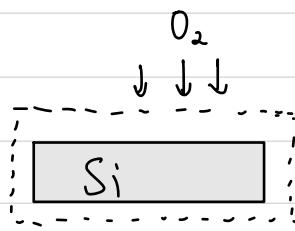
- 1> Wafer preparation
- 2> Oxidation
- 3> Diffusion
- 4> Ion - Implantation
- 5> Etching
- 6> Lithography
- 7> Metallization
- 8> Epitaxial deposition

### 1) Wafer preparation:



### 2) Oxidation:

- a) wet oxidation
- b) dry oxidation



#### a) wet oxidation:

- Uses H<sub>2</sub>O
- faster process
- less quality SiO<sub>2</sub>
- Field oxide

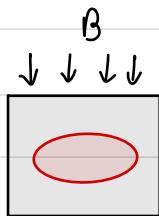
#### b) Dry oxidation

- Uses O<sub>2</sub>
- Slower process
- High quality SiO<sub>2</sub>
- gate oxide

3) Diffusion: Diffusing the impurity into the Si wafer through thermal annealing



4) Ton implantation:

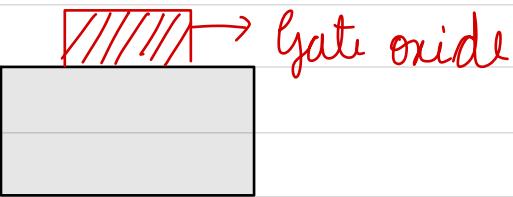


Dose  $\rightarrow$  impurities /  $\text{cm}^2$

Energy  $\rightarrow$  eV

Angle  $\rightarrow$  not exactly  $90^\circ$  in real

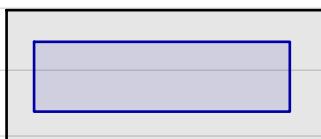
5) Etching:



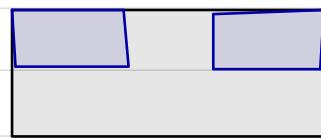
Etching involves removal of material

a) Chemical etching;  $\rightarrow$  using chemical  
 $\rightarrow$  Isotropic in nature

b) Plasma etching.  $\rightarrow$  using high energy plasma  
 $\rightarrow$  anisotropic

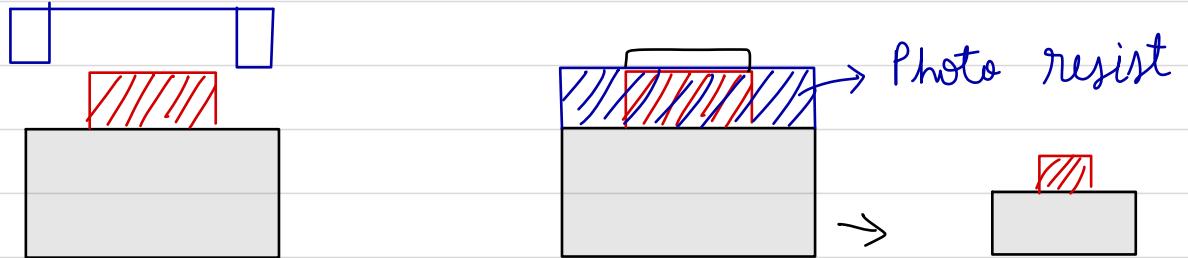


isotropic

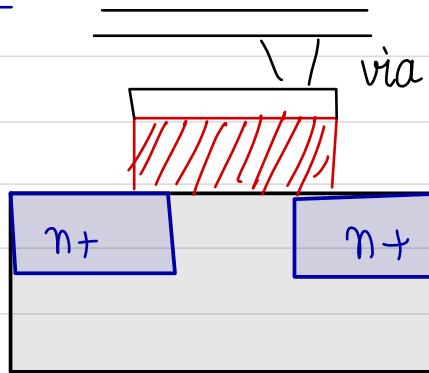


anisotropic

6) Lithography:  $\rightarrow$  most expensive  
 $\rightarrow$  Transforming the pattern on the mask to the wafer surface

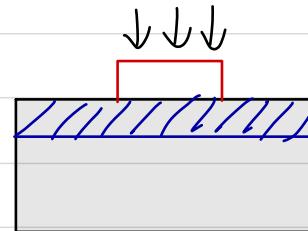


7) Metallization:



Deposition of metals for contacts

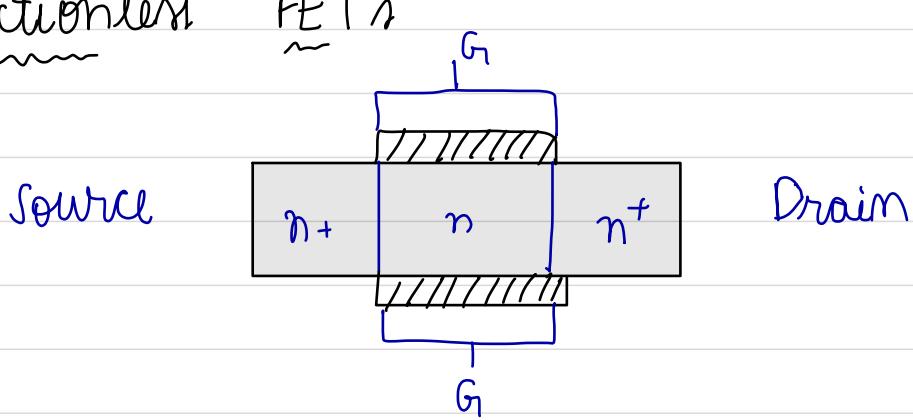
8) Epitaxial deposition:



→ This is the last stage of CMOS process flow.

Junctionless

FETs



$V_{th}$  is the voltage at which the channel is fully depleted

$$V_{th} = V_{FB} - \frac{q N_D \chi^2_{deh}}{2 \epsilon_{Si}} - \frac{q N_D \chi_{deh}}{C_{ox}}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

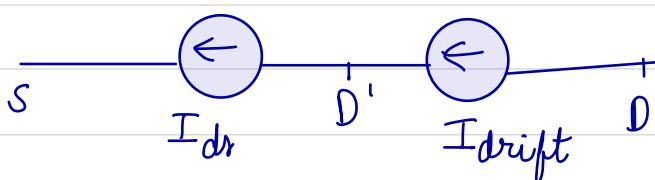
$$\frac{Q_d}{2 C_{deh}}$$

$$\frac{Q_d}{C_{ov}}$$

Drain current:

$$I_d = \frac{2q N_D \mu_n W}{L_g} \left[ \left( \frac{t_{Si}}{2} + \frac{C_{eq}}{q N_D} (V_{gs} - V_{FB}) \right) V_{DS} - \frac{C_{eq} V_{DS}^2}{2 q N_D} \right]$$

$$C_{eq} = \frac{C_{deh} C_{ox}}{C_{deh} + C_{ox}}$$



## Topics for Endsem:

- Basics of ICs
- Basics of MOS capacitor, MOSFET, band diagram,  $V_{TH}$ , regions of operation,  $I_{ds} - V_{ds}$ ,  $I_{ds} - V_{gs}$  characteristics
- pn junction, breakdown voltage, IV current equation, short channel effects
- Techniques to reduce short channel effects
- Junctionless FET, Subthreshold slope,  $I_{ON}/I_{OFF}$  ratio, high k-dielectric, strain engineering
- Equivalent circuit model - Razavi textbook
- Double gate MOSFET modelling
- Volume Inversion
- Drain extended devices
- Tunnel FET
- CMOS process flow
- Fin FET