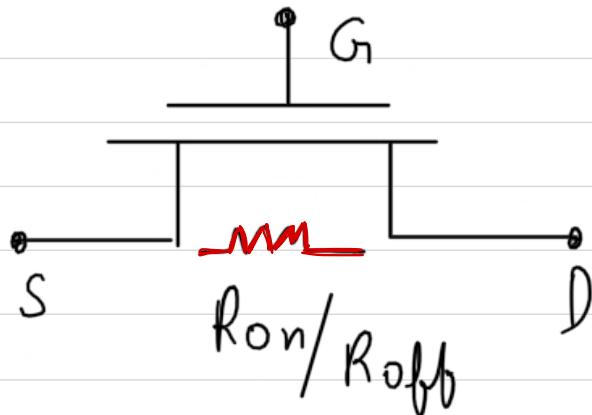


MANVITH PRABHU,
211EC228

EC300 - VLSI

VLSI

MOSFET



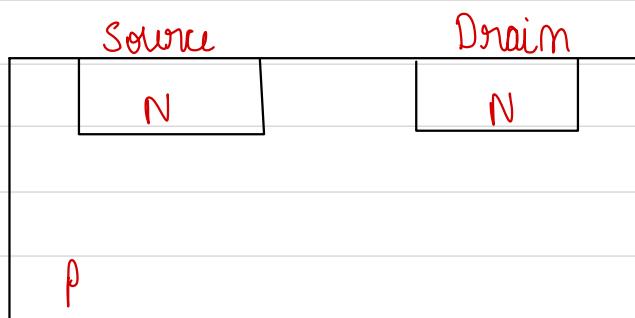
enhancement mode: By default the mosfet is off / no channel

Depletion mode : MOSFET is on / channel is present.

Type: PMOS , NMOS

MOSFETs are created on substrate made of insulators doped lightly.

NMOS :

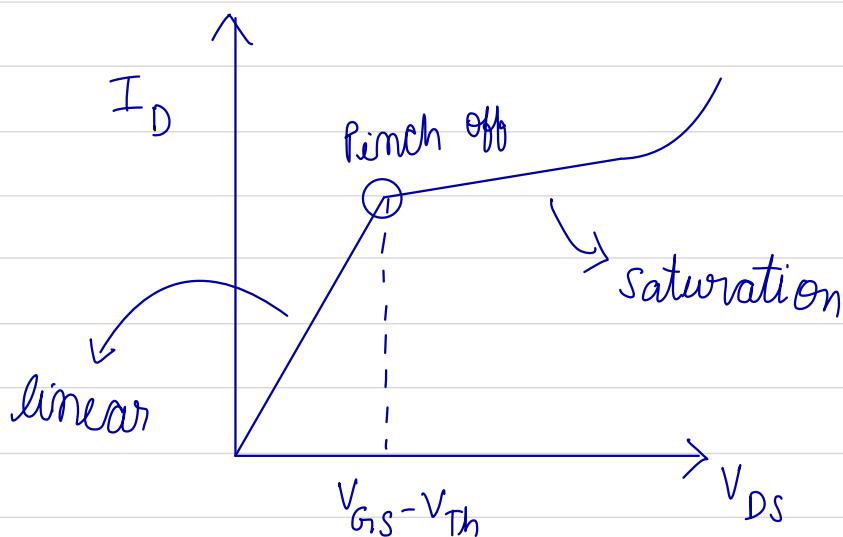


If source = gate = drain = 0V , then current will flow.

If only drain is connected to +ve voltage

then subthreshold current flows.

- The amount of +ve gate voltage required to make concentration of electrons near gate equal to concentration of holes in other part of substrate is threshold voltage (V_{Th})
- Charge carrier density $\propto V_{Overdrive} = (V_{GS} - V_{Th})$



$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \rightarrow \text{linear}$$

$$I_D = \mu_n C_{ox} \frac{W}{L} \frac{(V_{GS} - V_{Th})^2}{2} \rightarrow \text{saturation.}$$

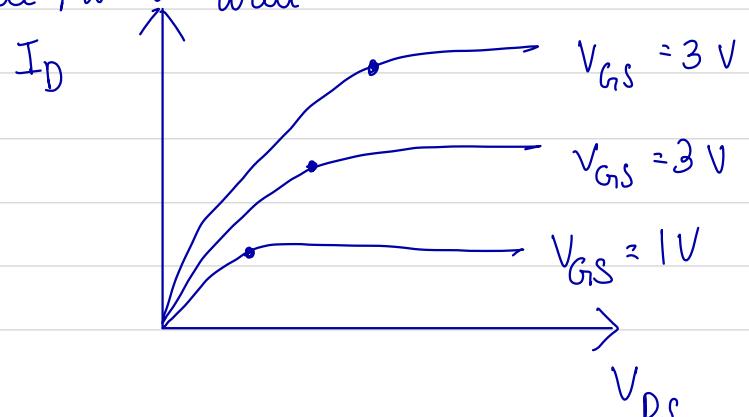
μ_n = Process parameter (mobility)

C_{ox} = Capacitance of oxide / unit area

W = Width

L = Length

V_{Th} = Threshold voltage



$$C_j = \frac{C_{j0}}{\left(1 - \frac{V_D}{\phi_0}\right)^m}$$

C_j = Junction capacitance
 C_{j0} = Junction capacitance with zero bias

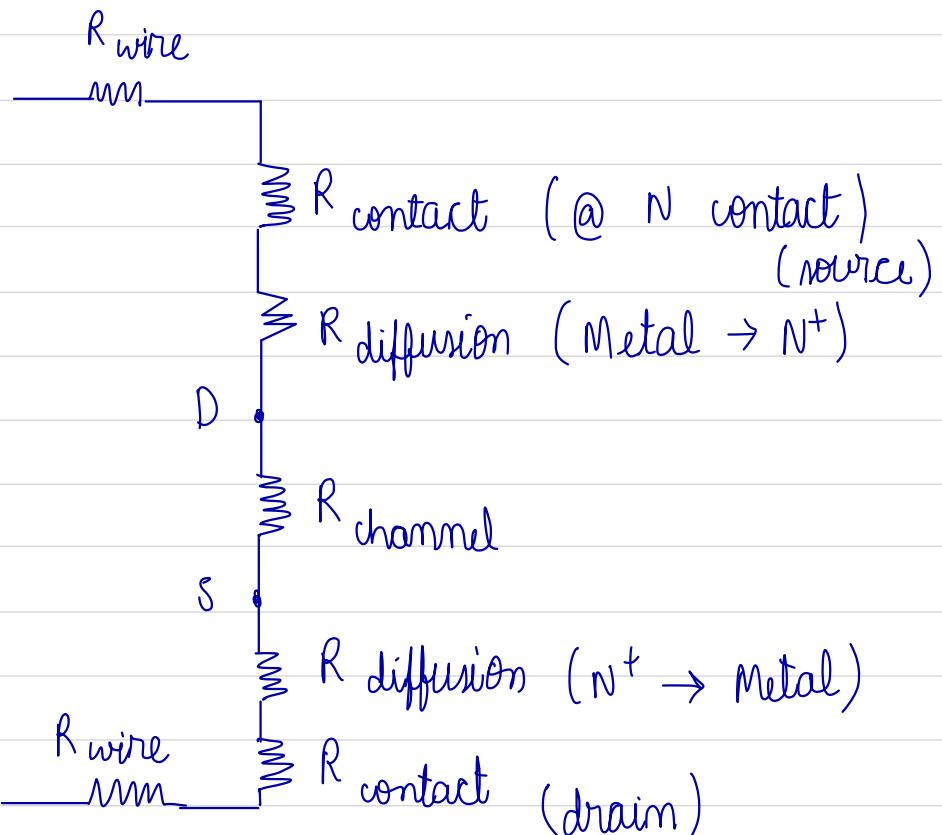
- If $V_{GS} \geq V_T$ MOSFET is in linear region.

NOTE:

- Gate \rightarrow metal (Polysilicon)
- Between gate & substrate \rightarrow Thin oxide

• Source / drain \rightarrow N^+ doped & metal attached to it is taken out as a wire.
 At this junction we get a layer called "N contact", similar to junction potential.

we get :



$$R_{channel} = \frac{V_{DS}}{I_{DS}} = \frac{V_{DS}}{\mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right]}$$

• generally metals used are : Al / Cu
 Al is used in memory
 Cu is used in other circuits .

Depletion mode: channel is present at no bias .

Enhancement mode: channel is not present at no bias .

• By increasing bulk potential a MOSFET can be made to sleep -

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \epsilon_{ox}}{t_{ox}} \rightarrow \text{Process Transconductance Parameter}$$

unit of k'_n is Siemens / Volts = S/V

Long channel device:

$$I_D = k'_n \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \epsilon_{ox}}{t_{ox}}$$

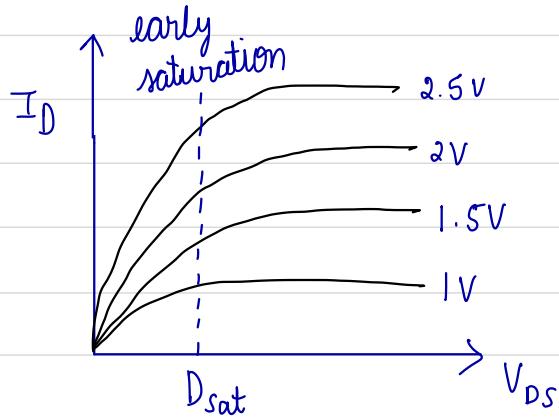
Saturation mode: $V_{DS} \geq V_{GS} - V_T$, channel length in modulator

$$I_D = k'_n \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) (1 + \lambda V_{DS})$$

Long channel: for $V_{GS} < V_{DS} - V_T$, curve almost quadratic

Short channel : for $V_{GS} < V_{DS} - V_T$, linear curve
 For submicron devices

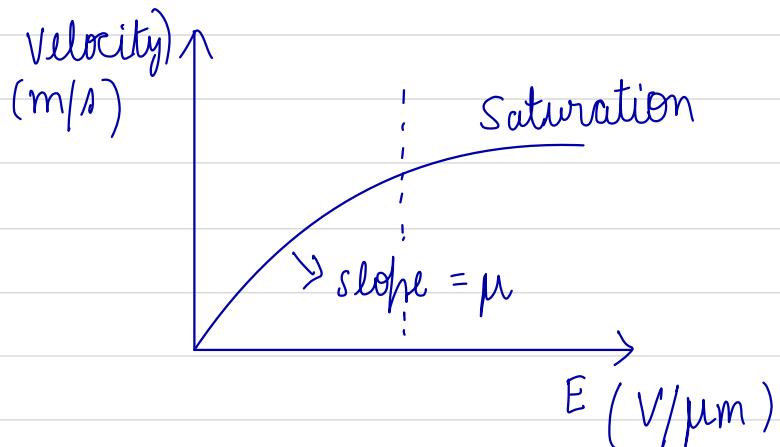
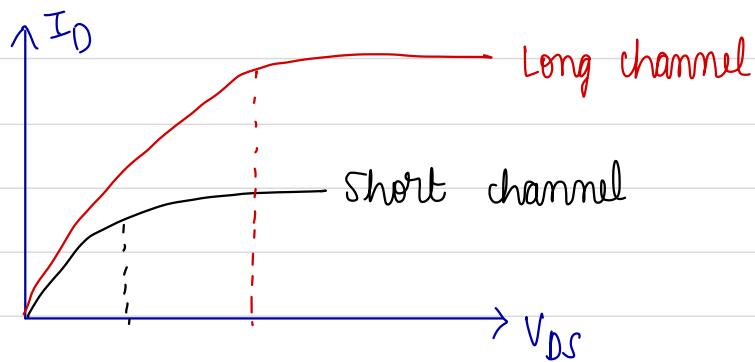
$$D_{SAT} \ll V_{GS} - V_T$$



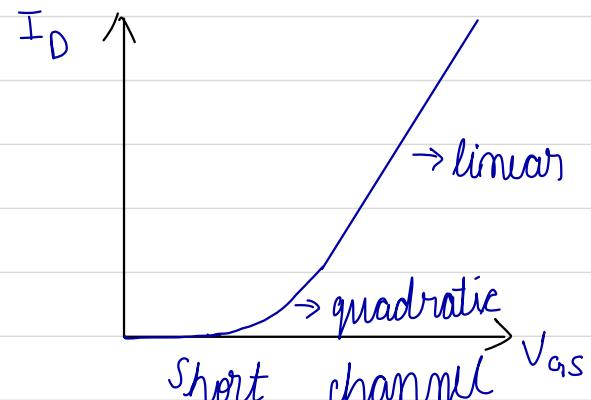
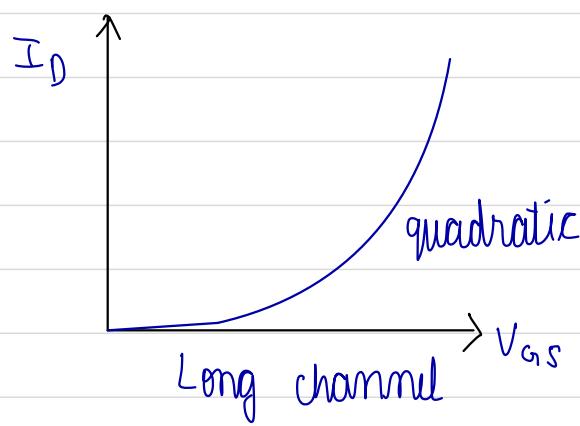
For same operating point :

Long channel : quadratic (difference between saturation level of I_D increases quadratically as gate voltage increases)

short channel : Linear because we have early saturation.



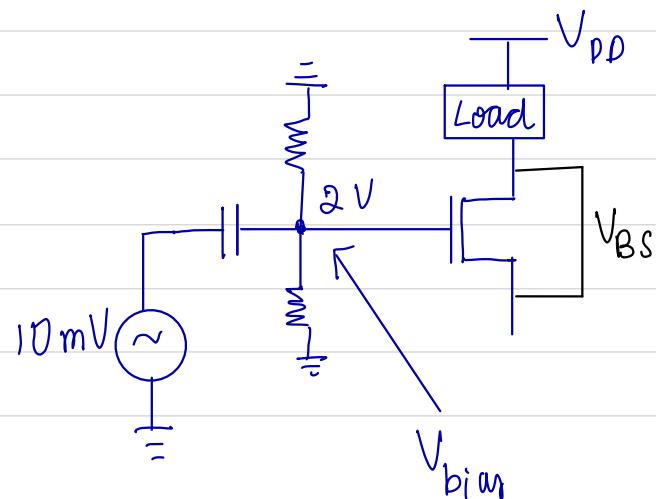
I_D vs V_{GS}



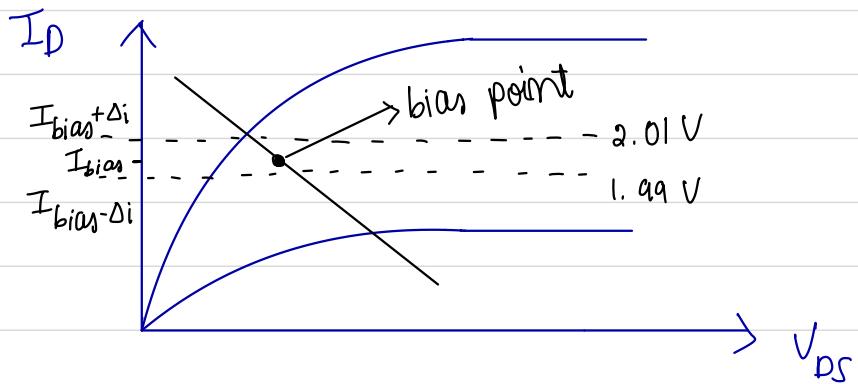
- As we decrease size of transistor, $t_0 \downarrow$, channel length \downarrow , capacitance/unit area \uparrow , Power $\propto C \Rightarrow$ Power \uparrow
- Ratio of current in NMOS to PMOS for same dimension of MOSFET and name operating point will be around 2 to 2.5
- \because All dimensions & operating voltage being same but mobility μ_n is different of e^- , holes

$$\frac{I_{NMOS}}{I_{PMOS}} = \frac{\mu_n}{\mu_p}$$

Switch resistance



Switch resistance:



Small signal resistance:

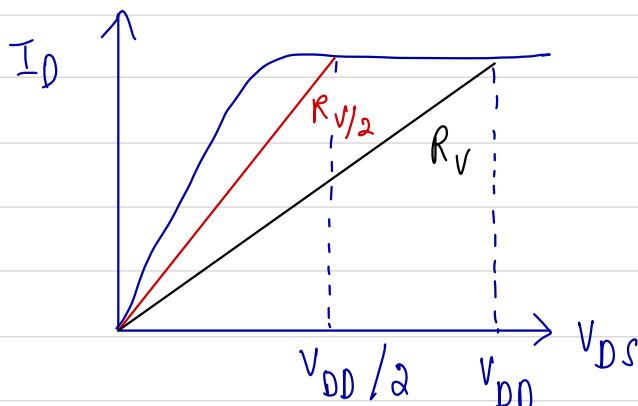
$$r_{\text{small signal}} = \frac{\Delta V_{DS}}{\Delta I_D} \approx 0$$

$\therefore r_{\text{small signal}} \rightarrow \infty$

Large signal resistance

$$R_{\text{large signal}} = \frac{V_{DS}}{I_D} \quad I_D = \text{Bias current}$$

Irrespective of i/p signal (present or not) we have I_{bias} & V_{bias} , so we have power dissipation always.



$$R_{eq} = \frac{R_V/2 + R_V}{2}$$

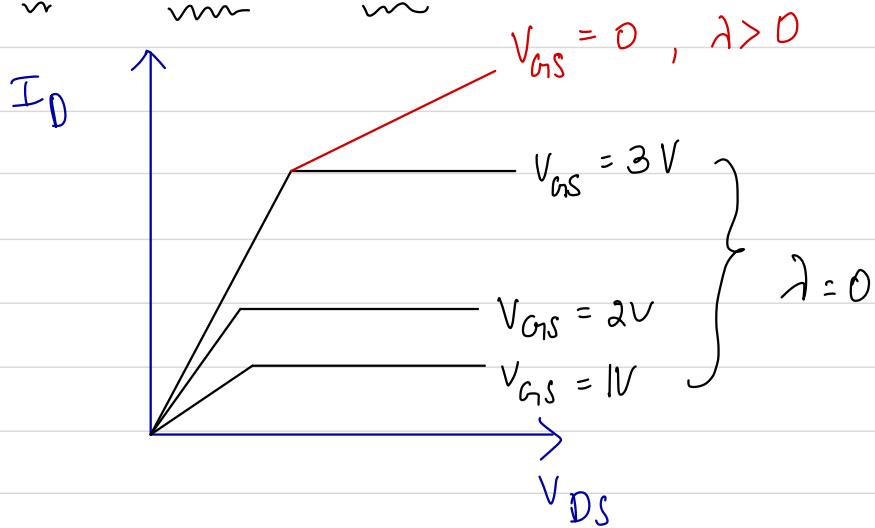
$$R_{eq} = \frac{1}{2} \left[\frac{V_{DD}}{I_{DDnat}(1+\lambda V_{DD})} + \frac{V_{DD}}{2I_{DDnat}(1+\lambda \frac{V_{DD}}{2})} \right]$$

NOTE

- λ = Slope of saturation region.
- $\lambda = 0$ for long channel.
- λ is large for short channel.
- Longer channel should be used for current source.
- Analog transistor (MOSFET) is usually based on 10 μm technology
- Mixed signal design eg. Analog to digital converters larger analog transistors are used.

MOSFET

as current source



Note:

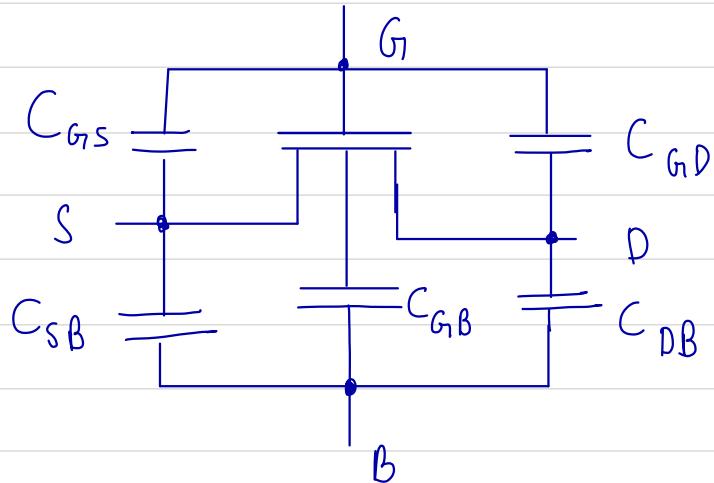
• Aspect ratio = $\frac{W}{L}$

• For same aspect ratio, current is same at same V_{DS}

• BJT has positive thermal coefficient i.e. $I \propto T$

- Below threshold V_T , MOSFET has positive thermal coefficient but above threshold MOSFET has negative thermal coefficient.

Dynamic Behavior of MOSFET

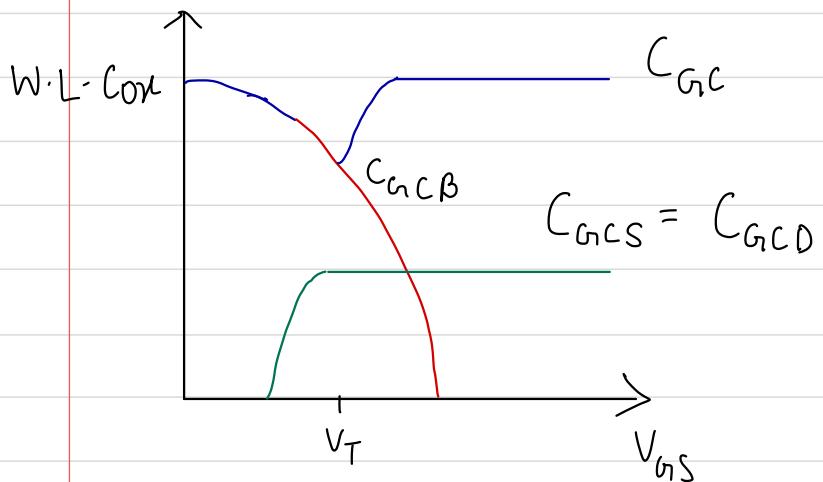


Region of operations	C_{GCB}	C_{GCS}	C_{GCD}	C_{GIC}	C_G
1 > Cutoff	$C_{ox} \cdot W \cdot L$	0	0	$C_{ox} \cdot W \cdot L$	$C_{ox} \cdot W \cdot L + 2 \cdot C_o \cdot h$
2 > Linear	0	$\frac{C_{ox} \cdot W \cdot L}{2}$	$\frac{C_{ox} \cdot W \cdot L}{2}$	$C_{ox} \cdot W \cdot L$	$C_{ox} \cdot W \cdot L + 2 \cdot C_o \cdot W$
3 > Saturation	0	$\frac{2}{3} (C_{ox} \cdot W \cdot L)$	0	$\frac{2 \cdot C_{ox} \cdot W \cdot L}{3}$	$(\frac{2}{3}) (C_{ox} \cdot W \cdot L) + 2 \cdot C_o \cdot W$

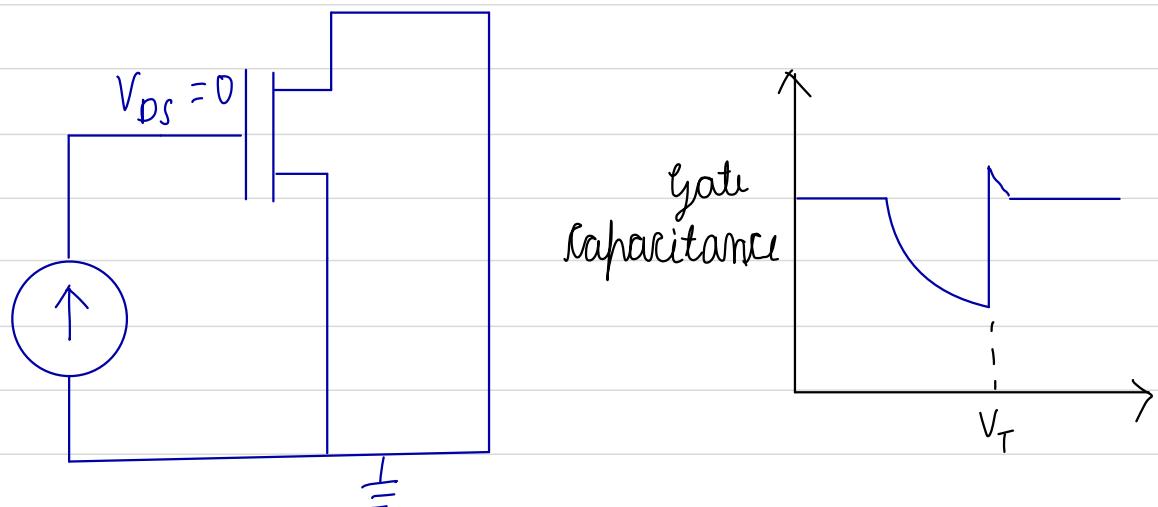
C_{ox} = Capacitance of oxide layer

C_o = Capacitance of overlap.

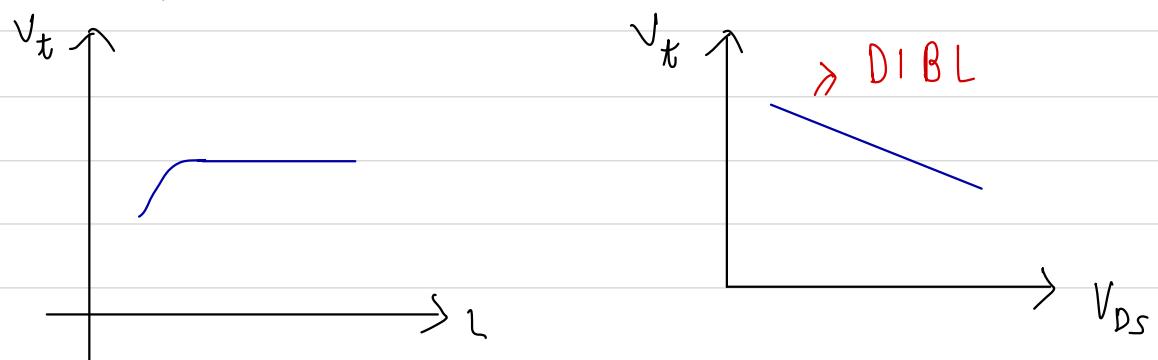
Variation of Gate capacitance



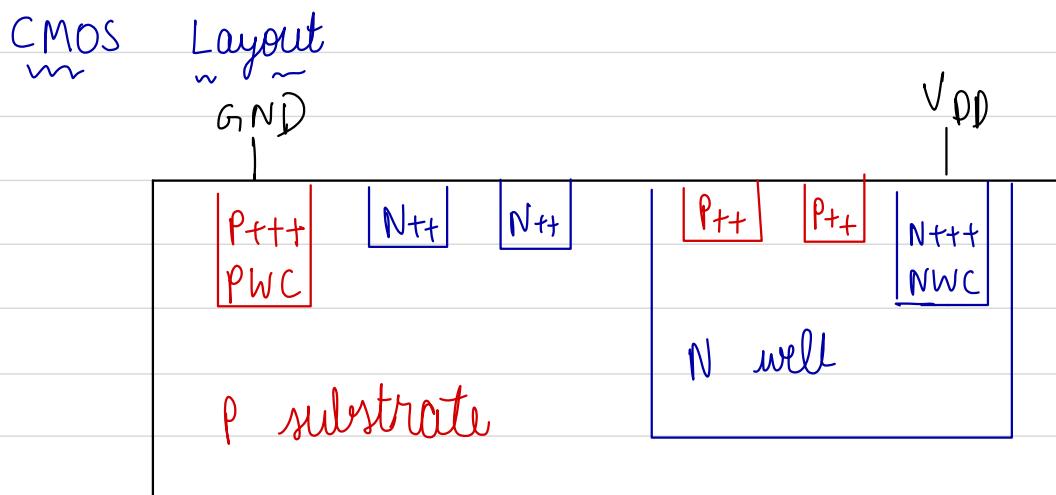
Measuring gate capacitance v/s V_{DS}



Threshold variation in deep sub micron (DSM) technology :



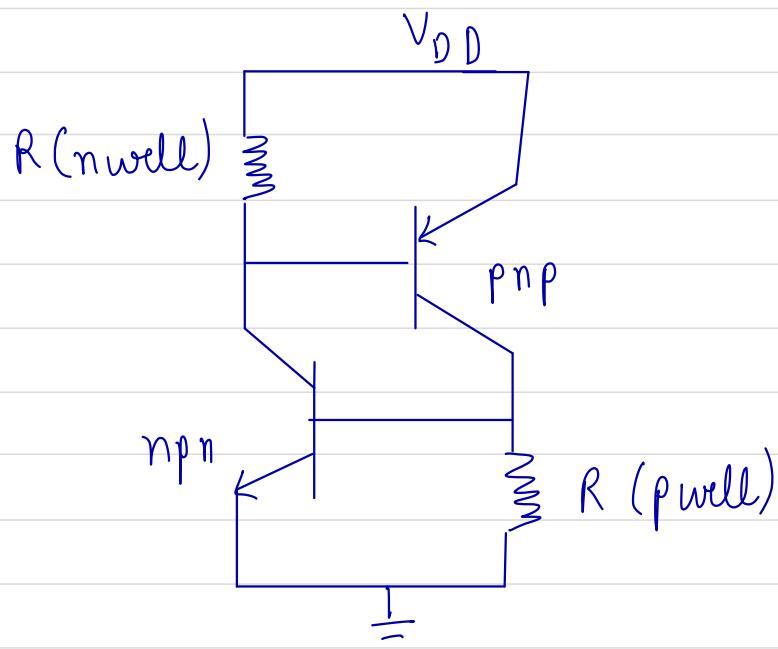
DIBL = Drain induced Barrier lowering



PWC = P well contact

NWC = N well contact

Silicon control Rectifier (SCR)

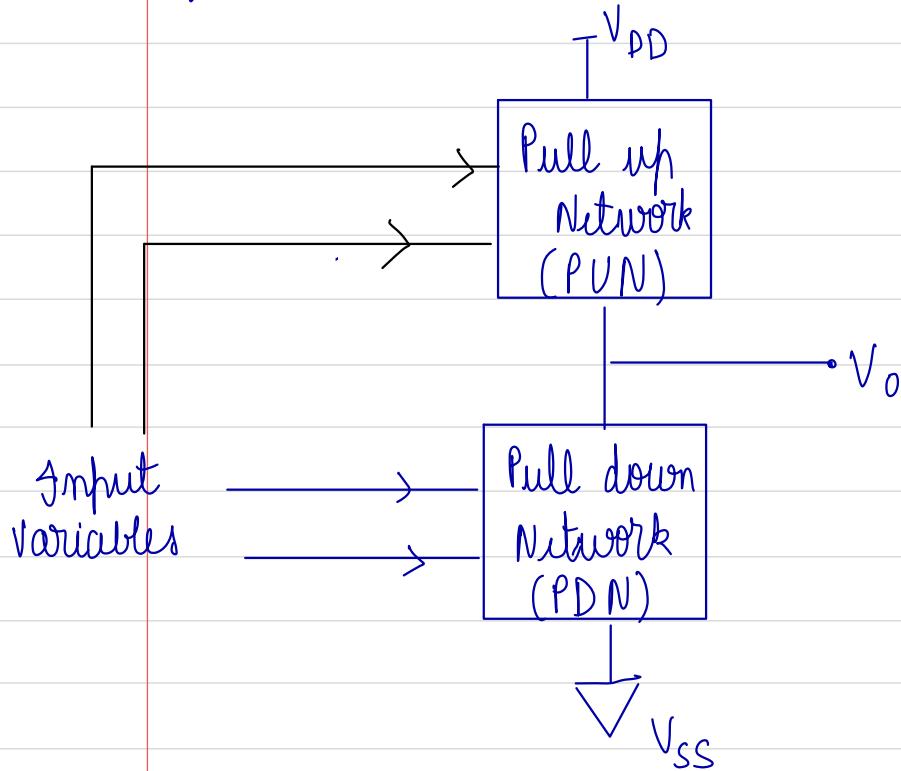


In this configuration current starts to flow from V_{DD} to ground and it increases. This is called Latch up.

Also in CMOS we connect PWC & bulk to ground to as to take out additional charges in bulk. Else charge accumulation happens and will increase the potential & hence leakage current in bulk.

Spiral

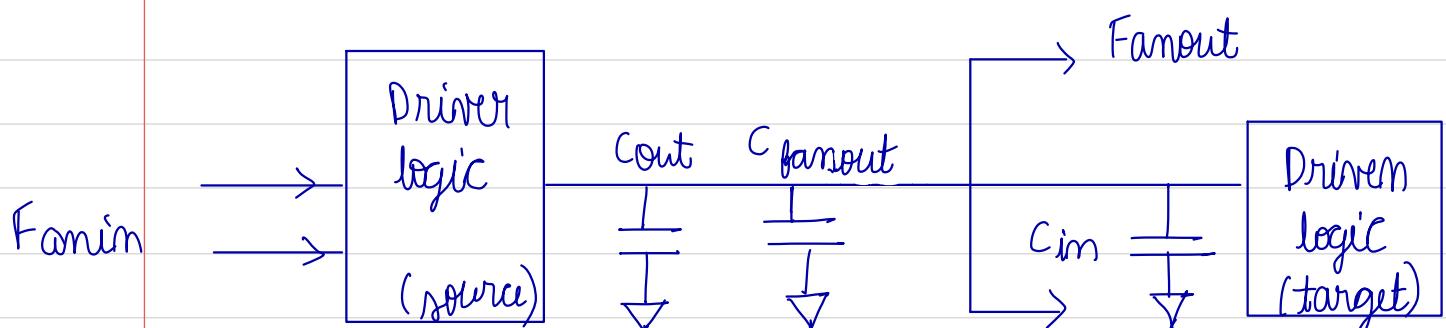
General structure of any static logic gate:



- In CMOS family: all inputs are connected to PUN.
- In other families: inputs are not connected to PUN.

F_{anim} : No. of inputs ≥ 1

F_{fanout} : No. of outputs = 1

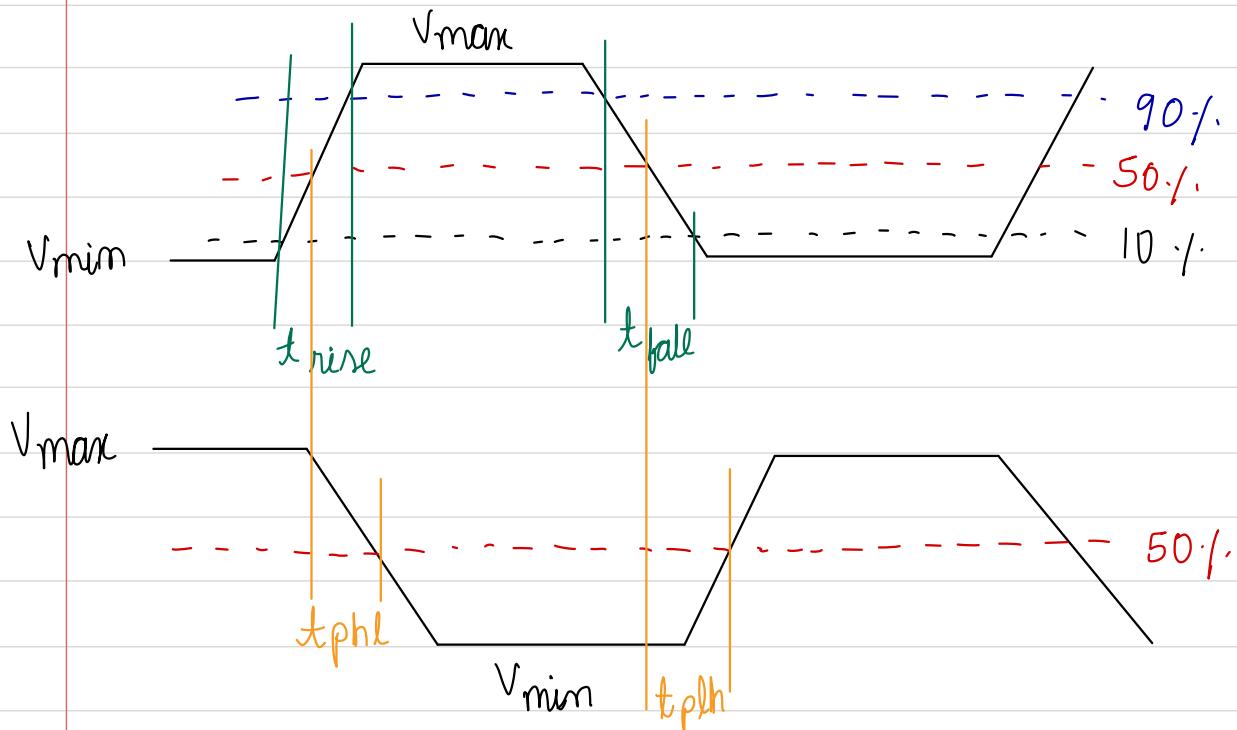


We must have driver charging / discharging all the capacitor, through its voltage.

- C_{out} = Output (drain) capacitance of MOSFETs connected to output of the logic gates.
- C_{in} = Input capacitance of all the fanout logic gates input. Sum of C_G of all the MOSFETs to which the signal is connected.
- $C\text{-fanout-wire}$ = Capacitance of interconnect used to connect the output to all of the fanout nodes.

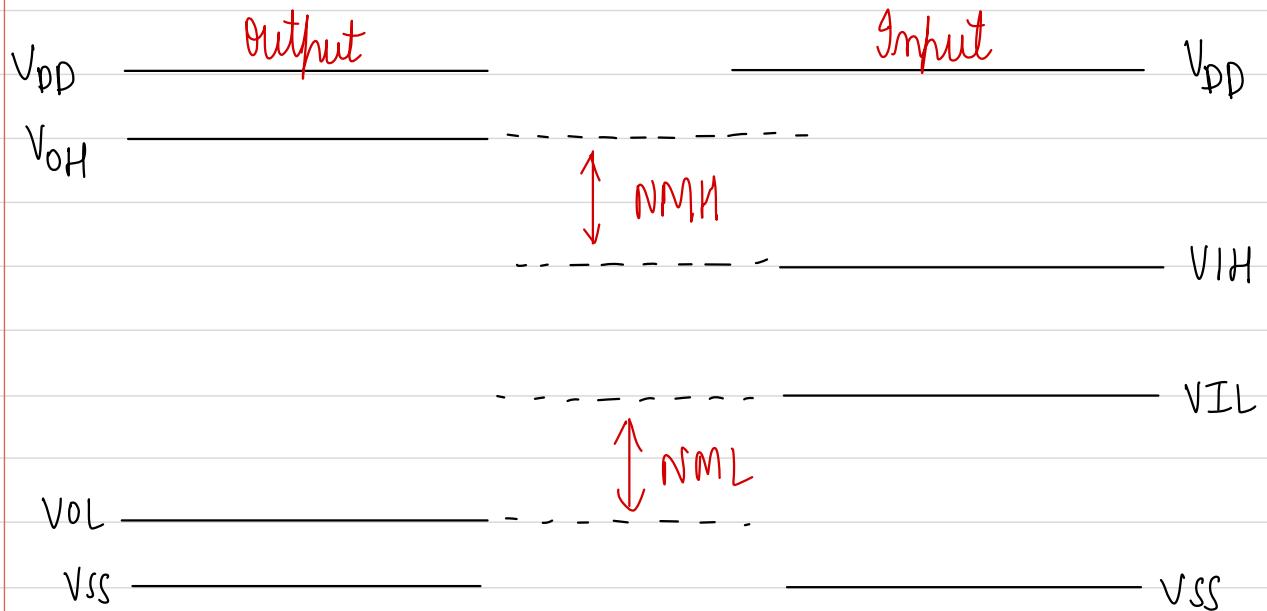
Load capacitance: $C_L = C_{out} + C_{fanout-wire} + C_{in}$ (of all fanout nodes)

Timings:



$$t_p = \text{Propagation delay} = \frac{1}{2} (t_{phl} + t_{plh})$$

Noise margin:

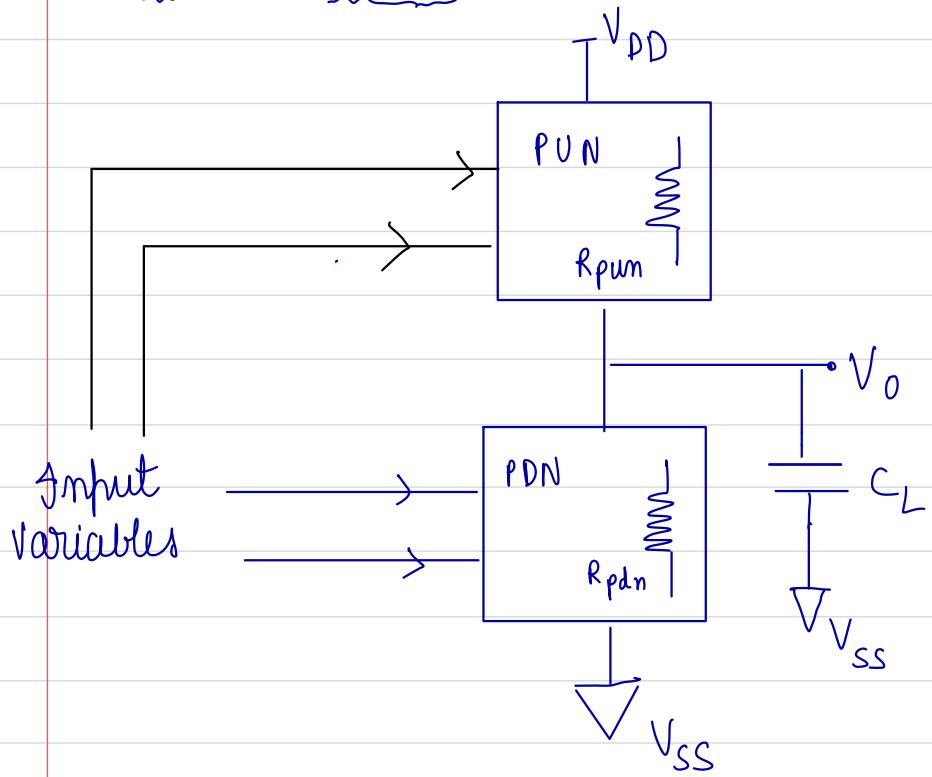


$NMH =$ Noise margin high
: Larger the better

$NML =$ Noise margin low
: Larger the better

Ideal situation: $NMH = NML = \frac{V_{DD}}{2}$

Generic structure:



$$V_O = \text{Logic_1}$$

- PUN is closed. Path from V_{DD} to V_O .
- C_L changes with R_{PUN}
- V_O rise can be approximated with time constant proportional to $R_{PUN} \cdot C_L$

$$V_O = \text{Logic_0}$$

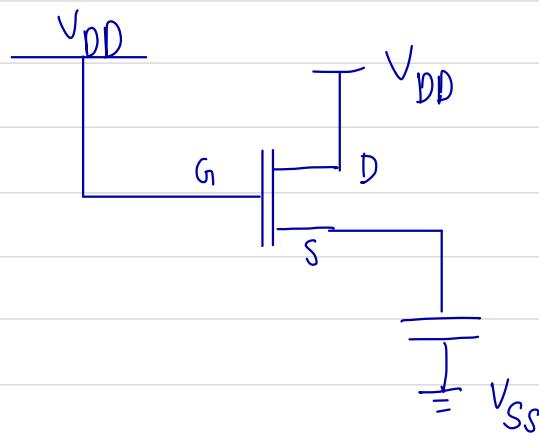
- PDN is closed. Path from V_O to V_{SS}
- C_L discharges through R_{PDN}
- V_O fall can be approximated with a time constant proportional to $R_{pdn} \cdot C_L$

$$V_O = R_{pdn} \cdot V_{DD} / (R_{pdn} + R_{pum})$$

- PDN with PUN acts like a potential divider.
- V_O is a function of R_{pdn} , R_{pum}

- Steady state value of V_o is decided by R_{pdn} & R_{pun}
- Transient value of V_o is decided by the values of R_{pdn} , R_{pun} , & C_L .

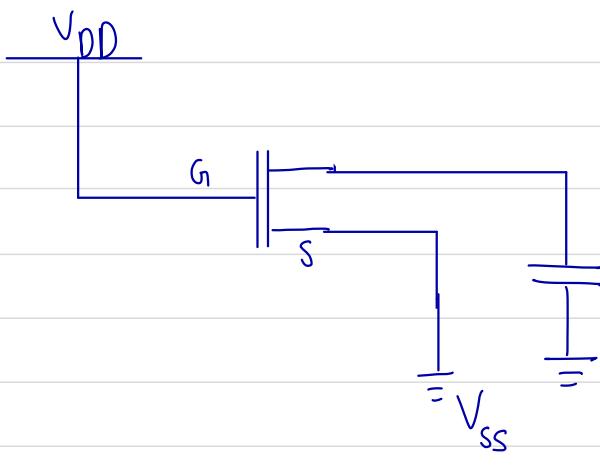
Suitability of MOSFETs in digital circuits



$$\text{Final value of } V_o = V_{DD} - V_t$$

$$V_o = V_{DD} - V_t$$

Poor conductor of logic '1'



Capacitor precharged To V_{DD}

Final value of $V_o = 0$
Good conductor of logic '0'

• NMOS is a good conductor of logic '0' for use in PDN.

good conductor of logic '1'.

• PMOS is a good conductor of logic '1' for use in PUN.

good conductor of logic '0'.

Therefore suitable

MOSFET based static logic families

- 1> Passive Resistive Load
- 2> Active (MOSFET) load.

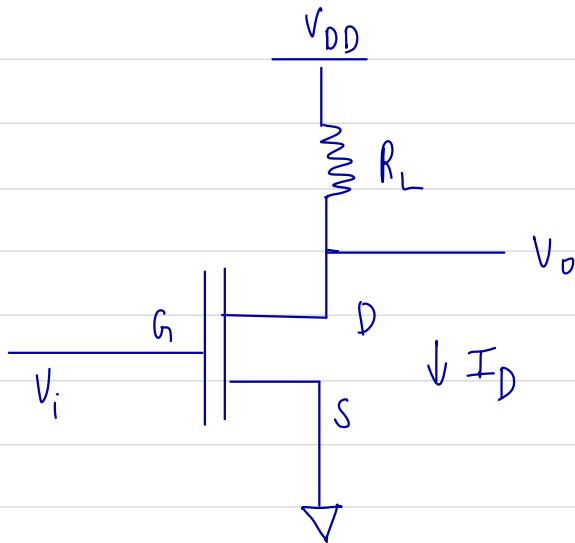
Passive	Active
1> Size is very large	1> Size is very small
2> Difficult to fabricate on a chip	2> Easy to fabricate on a chip
3> Externally connected to chip	3> Value can be controlled with a bias
4> Value is fixed	4> Large value of tolerance (poor precision eg. 20%)
5> Small value of tolerance (precision can be high eg 1%)	

Types of Active load:

- 1> Ratioed logic: Value of V_{OL} based on $R_{pdm} \& R_{pum}$ ratio of $R_{pdm}/(R_{pum} + R_{pdm})$
 - Enhancement mode NMOS Load
 - Depletion mode NMOS Load
 - Enhancement mode PMOS Load (Pseudo NMOS)
- 2> Non ratioed logic: $V_{OL} \& V_{OH}$ are independent

of R_{pdn} & R_{pum})
 Eg: Complementary MOS (CMOS)

NMOS with passive resistance:

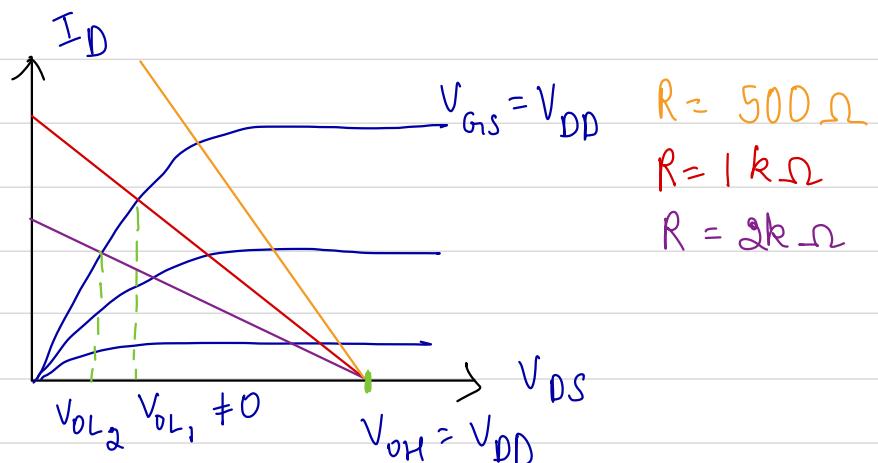


$$V_o = V_{DD} - I_D \cdot R_L$$

$$V_i = 0 : V_o = V_{OH} = V_{DD}$$

$$V_i = 1 : V_o = V_{OL}$$

- All MOSFETs in a digital circuit are of minimum length = feature size
 - Only aspect ratio changes (W/L) i.e. only W changes.



- Blue line represents VI characteristics of driver MOSFET
- Red line represents VI characteristics of Load Resistance.

To find Load line put $I = 0$ & $V_{DS} = 0$
 One at a time in
 $I = \mu_0 C_{Ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$ and join 2 points.

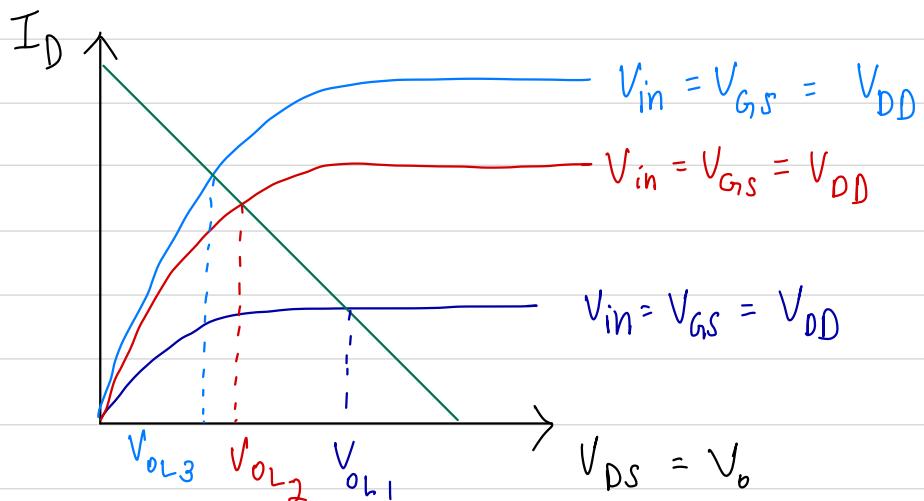
$$I_R = \frac{V_{DD} - V_{DS}}{R}$$

We can replace $V_{GS} = V_i$ & $V_{DS} = V_o$
 $\& I = I_R$ (serial connection)

$$I = \mu C_{Ox} \frac{W}{L} \left[(V_{in} - V_T) V_o - \frac{V_o^2}{2} \right]$$

- NOTE :
- Increasing Load resistance decreases V_{OL} , which is better.
 - But time constant will increase, so rise time will increase.

Impact of Aspect ratio on I_D



$$AR_3 > AR_2 > AR_1$$

$$AR = \text{Aspect Ratio}$$

Keep R fixed, vary $(\frac{W}{L}) \rightarrow$ aspect ratio

As $(\frac{W}{L}) \uparrow V_{OL} \downarrow$

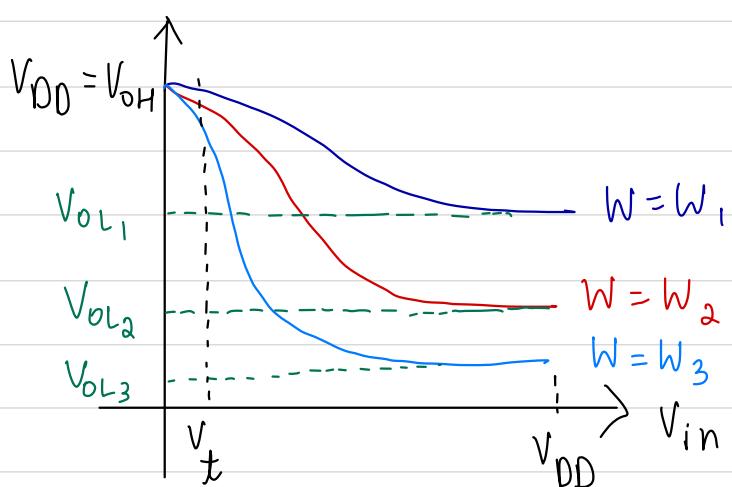
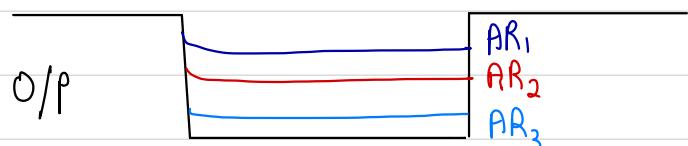
i.e. $W \uparrow R_{PDN} \downarrow V_{OL} \downarrow$
 $L \downarrow R_{PDN} \downarrow V_{OL} \downarrow$

As $V_{OL} = \frac{R_{PDN}}{R_{PDN} + R_{PUN}} \cdot V_{DD}$

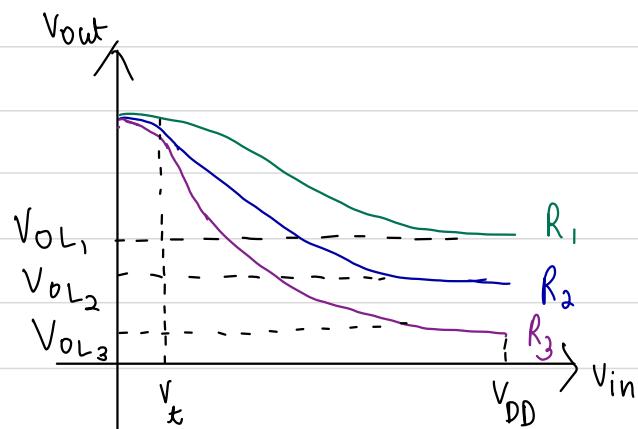
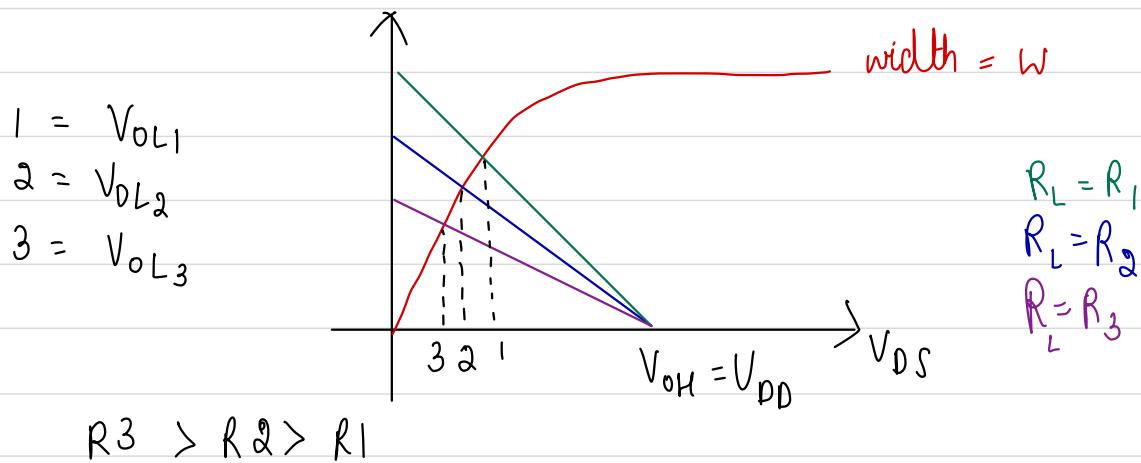
as $R_J, I \uparrow$
 $P = I^2 R$ so P dissipated increases -

Rise time remains the same as we have
 $R_{PUN} = \text{constant}$.

Fall time:

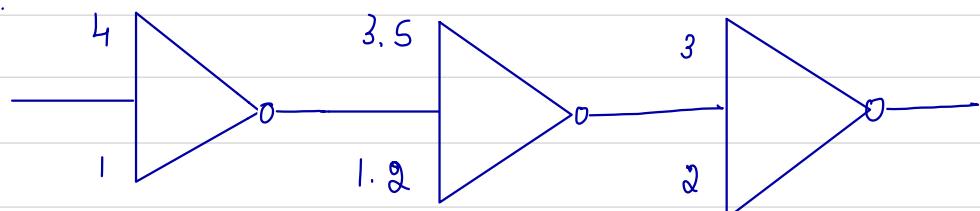


Varying R_L (load resistance):



NOTE: • Gain > 1 is required for a gate to work properly.

• Consider:

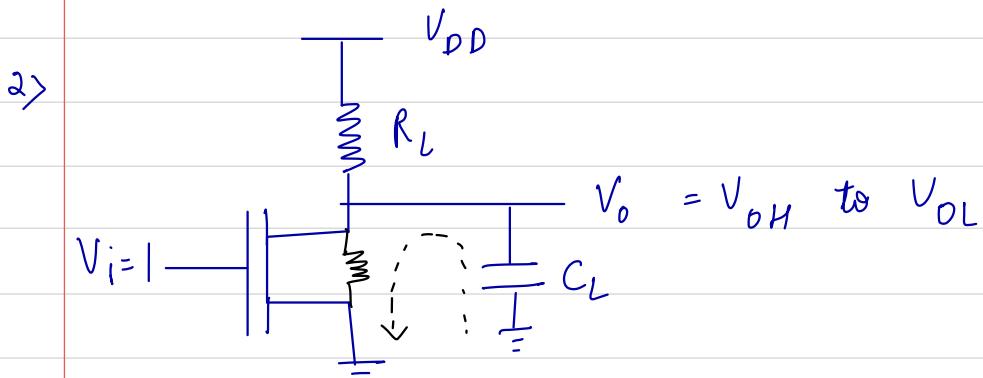
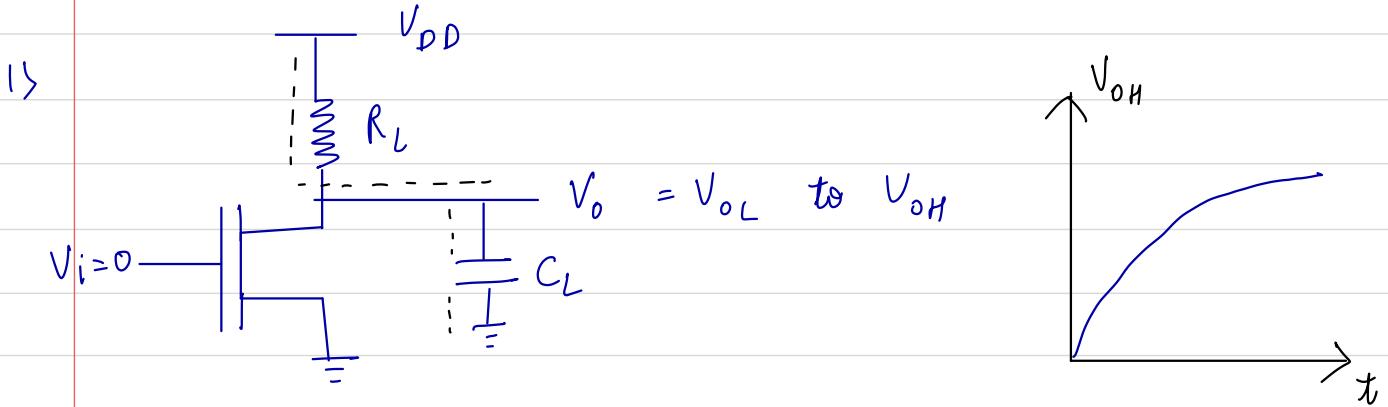


Then output will be constant value & gate won't work. So we need gain ≥ 1

Summary

- For given R_L , as (W/L) of driver \uparrow , we have,
 - 1> Driver switch resistance, $R_{\text{driver}} \downarrow$
 - 2> $V_{OL} \downarrow$ as $\frac{R_{\text{driver}}}{R_{\text{driver}} + R_{\text{load}}} \downarrow$
 - 3> Inverter gain \uparrow , VTC slope \uparrow
 - 4> VTC curve shifts to left
 - 5> I_D increases
 - 6> Power consumption \uparrow
 - 7> Fall time \downarrow

- For given W/L of NMOS, as $R_L \uparrow$



at $t=0$ $V_o = V_{PP}$ it discharges through R_{PPN} then as $V_{CL} \downarrow$ or also have a small current through $V_{DD} \rightarrow R_L$

Inverter operation:

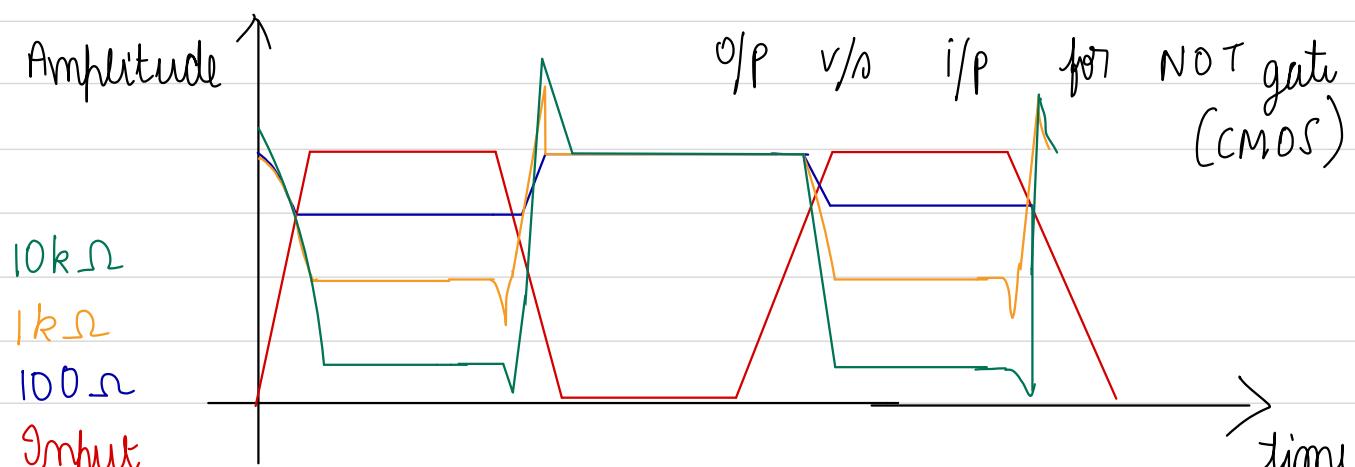
When $V_i = \text{Logic '0'}$:

- PDN path is open
- R_L connects V_{DD} to output node
- $V_o = V_{OH} = V_{DD}$, a perfect 1
- t_{rise} is given by $R_L * C_L$.

when $V_i = \text{Logic '1'}$

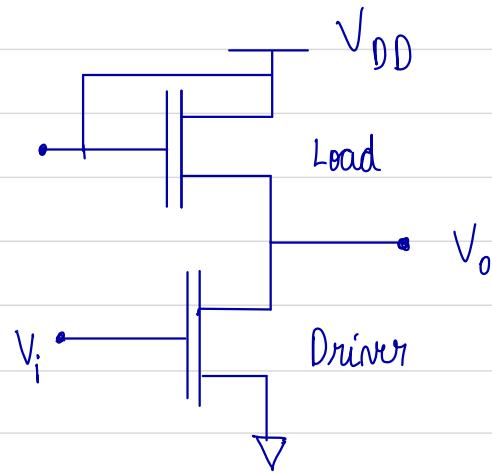
- $V_o = V_{OL}$, but not perfect 0.
- A path exists from V_{DD} to V_{SS} through R_L and PDN. A continuous current flows, leads to static power consumption.

NOTE: • Fall time is affected by resistance of MOSFET.
• Rise time is affected by external resistor.



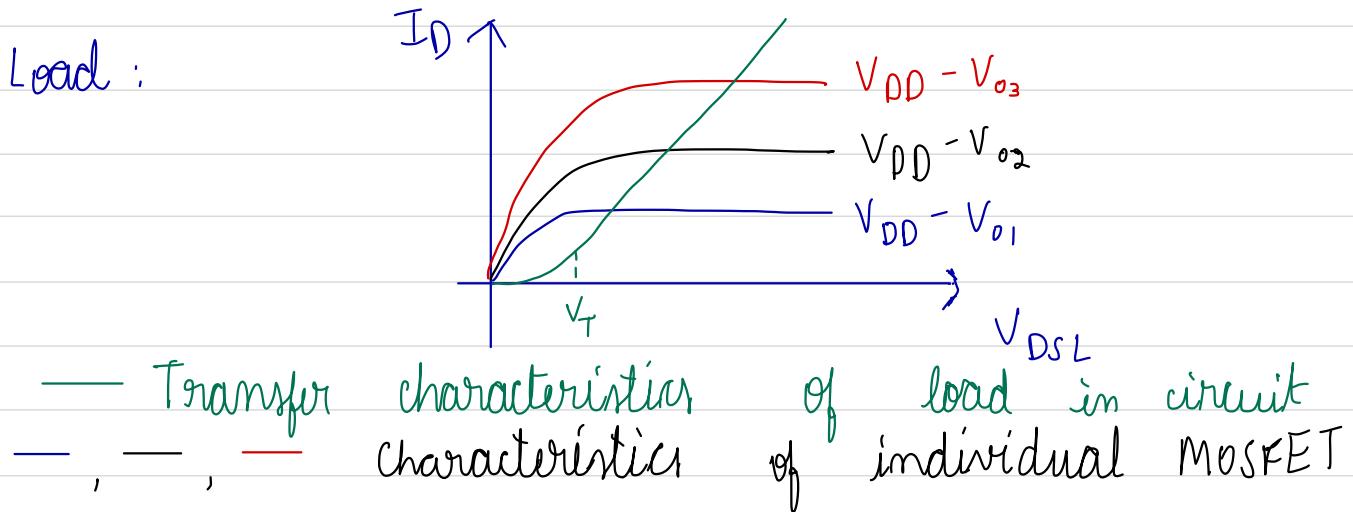
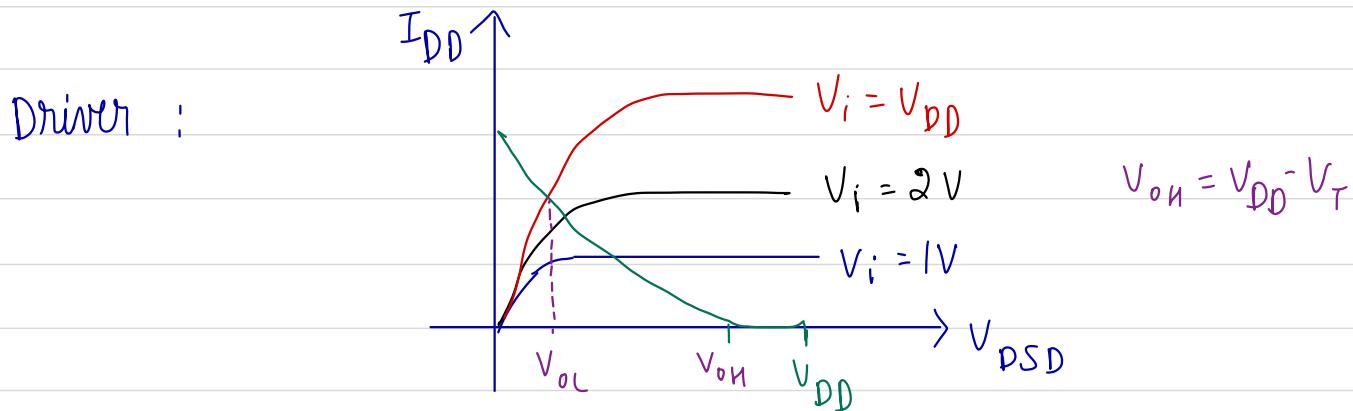
- overshoot is because of capacitor voltage + input voltage.

NMOS Inverter with Enhancement NMOS Load



Along when $V_i = 0$
 $V_o = V_{DD} - V_T$

$$V_{GSL} = V_{DSL} = V_{DD} - V_o$$



equation for Load:

$$I_{DL} = \mu_0 C_{ox} L \left(\frac{W}{L} \right)_L \left[(V_{GSL} - V_T) V_{DSL} - \frac{V_{DSL}^2}{2} \right]$$

equation for Driver:

$$I_{DD} = \mu_0 C_{ox} D \left(\frac{W}{L} \right)_D \left[(V_{GSD} - V_T) V_{DSD} - \frac{V_{DSD}^2}{2} \right]$$

But $I_{DL} = I_{DD}$

$$\Rightarrow \mu_0 C_{ox} L \left(\frac{W}{L} \right)_L \left[(V_{GSL} - V_T) V_{DSL} - \frac{V_{DSL}^2}{2} \right]$$

$$= \mu_0 C_{ox} D \left(\frac{W}{L} \right)_D \left[(V_{GSD} - V_T) V_{DSD} - \frac{V_{DSD}^2}{2} \right]$$

But Load is in saturation $\& V_{GSD} = V_i$

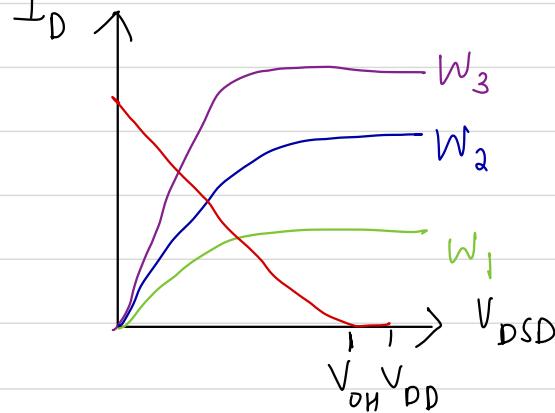
$$\& V_{DSD} = V_o$$

$$\Rightarrow \mu_0 L C_{ox} \left(\frac{W}{L} \right)_L \left[\left(\frac{V_{DD} - V_o - V_T}{2} \right)^2 \right] = \mu_0 D C_{ox} \left(\frac{W}{L} \right)_D$$

$$\left[(V_i - V_T) V_o - \frac{V_o^2}{2} \right]$$

changing aspect ratio of driver

— Load line



$$V_{DSD} = V_o \\ = V_{DD} - V_{DSL}$$

$$W_3 > W_2 > W_1$$

$$V_{oH} = V_{DD} - V_t$$

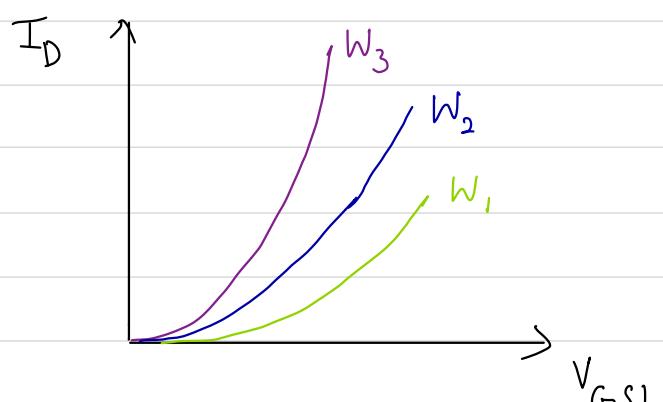
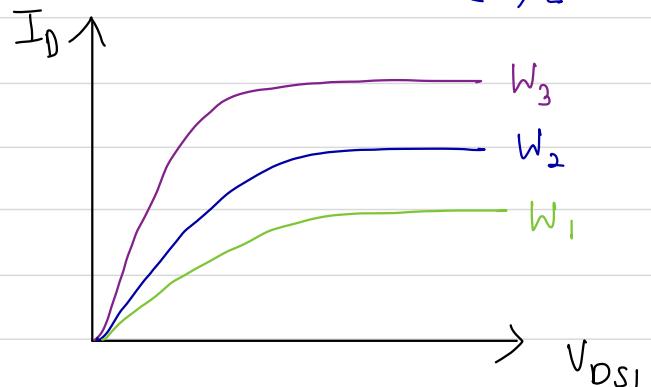
An $(\frac{W}{L})_D$ increases $R_{PD} \uparrow \Rightarrow V_{oL} \downarrow$ when $(\frac{W}{L})_L$ is constant.

- When $(\frac{W}{L})_D$ is constant & $(\frac{W}{L})_L$ is varied.

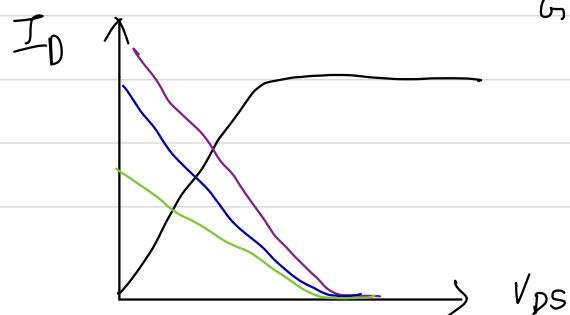
$$W_3 = 3x$$

$$W_2 = 2x$$

$$W_1 = x$$



\Rightarrow



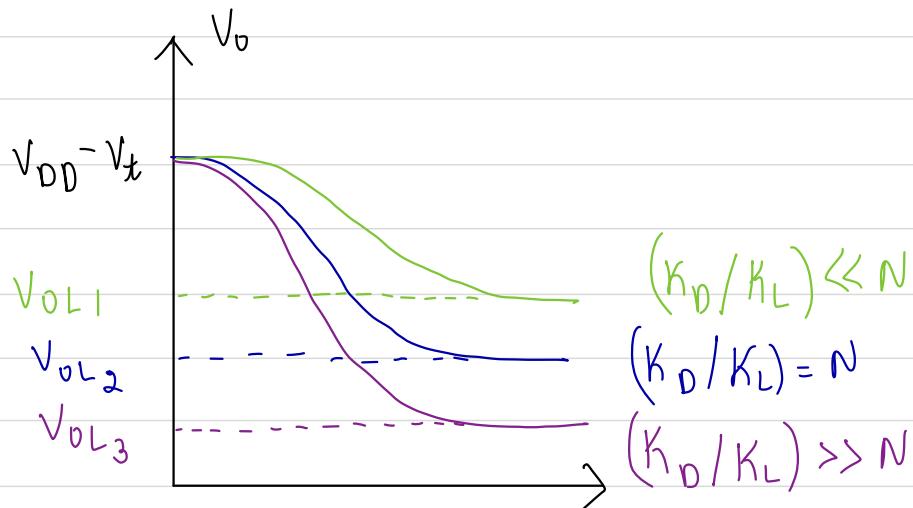
$$\text{Define } K = K_n' \left(\frac{W}{L} \right)$$

$$K_n' = \mu_n C_{ox}$$

$$K_D = \mu_n C_{ox} \left(\frac{W}{L} \right)_D \quad \& \quad K_L = \mu_n C_{ox} \left(\frac{W}{L} \right)_L$$

$$V_{OH} = V_{DD} - V_T \text{ (constant)}$$

$$V_{OL} = f \left(\frac{K_D}{K_L} \right) \quad \text{i.e. function of } \left(\frac{K_D}{K_L} \right)$$



For a given K_D : as K_L increases

$\rightarrow R_{\text{load}}$ decreases

$\rightarrow V_{OL}$ increases

$\rightarrow t_{ris}$ decreases

\rightarrow When $V_i = 1$ then static power consumption increases;

- Short circuit (continuous) current increases

\rightarrow VTC curve shifts to the right

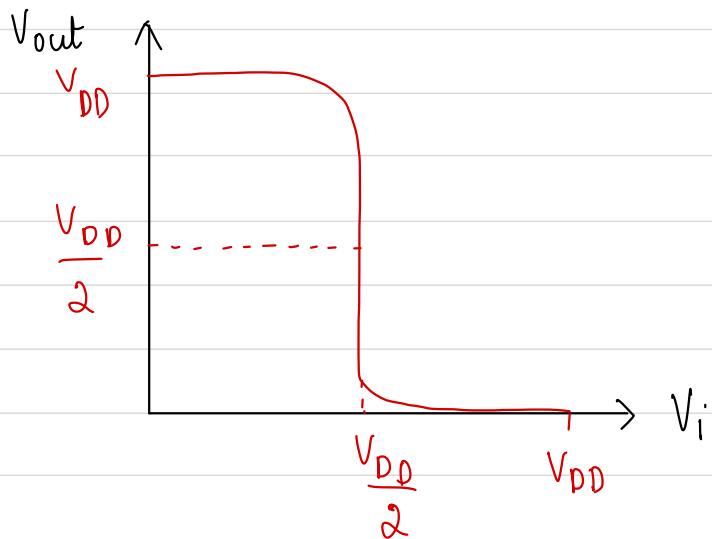
\rightarrow Inverter gain reduces.

VTC = voltage transfer characteristics.

For a given K_L as K_D increases:

- R_{PDN} decreases
 - V_{OL} decreases
 - t_{fall} decreases
 - When $V_i = 1$ then static power consumption increases:
 - Short circuit (continuous) current increases
 - VTC curve shifts to left
 - Inverter gain increases.
-
- V_{OL} is not perfect '0'.
 - V_{OH} is not perfect '1'. ($V_{OH} = V_{DD} - V_T$)

Ideal Transfer characteristics:



R_{Pun} depends on V_{OL} :

- If $V_o = V_{OL}$ then $V_{DSL} = V_{DD} - V_{OL}$ & is larger; R_{Pun} is smaller.
- If $V_o = V_{OH}$ then $V_{DSL} = V_{GSL} = V_T$ and is small; R_{Pun} is larger

- As V_o toggles between V_{OL} & V_{OH} , R_{PDN} dynamically changes - manually we can compute only R_{PDN} when V_o is either V_{OL} or V_{OH} but not during transition between V_{OL} & V_{OH} .

R_{PDN} does not depend on V_o . It depends on V_i :

- If $V_i = V_{OL} < V_t$ then R_{PDN} is very large (as no channel exists); but there will be subthreshold conduction leading to small leakage current flowing from V_{DD} to V_{SS} - leakage power.
- If $V_i = V_{OH}$ then R_{PDN} is small, leads to a path from V_{DD} to V_{SS} ; leads to considerable short circuit (static) current - static proportional to aspect ratios of PUN & PDN.

Inverter Operation

- When $V_i = \text{logic '0'}$
- PDN path is open
 - PUN path is closed
 - $V_o = V_{OH} = V_{DD} - V_t$, not a perfect '1'.

When $V_i = \text{Logic '1'}$

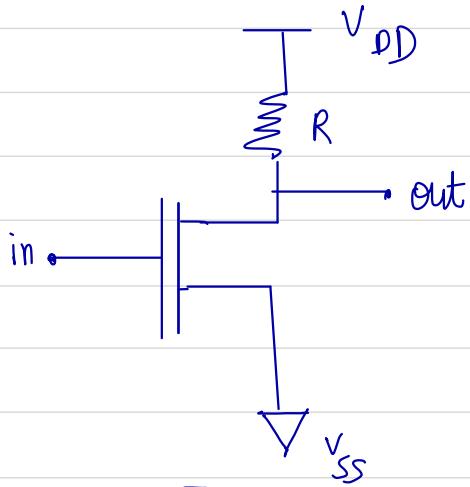
- Both PUN & PDN paths are closed.
- $V_o = V_{OL}$, but not perfect '0'

- A path exists from V_{DD} to V_{SS} through PUN & PDN - A continuous current flows, leads to static power consumption.
- If Load & W_{Load} & Driver) power consumption time rise & t_{fall} W_{driver} (aspect ratios of are large static increases. At the same time decreases.

Q) Given $V_{DD} = 5V$, $V_{SS} = 0V$, $V_T = 0.5V$
 $k_n = 50 \mu A/V^2$, Power = $5mV$, $V_{OL} = 1V$
 $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$. Design inverter.

Ans:

$$I_D = k_n \left(\frac{W}{L} \right) \left((V_{in} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$



$$I_D = 50 \times 10^{-6} \left[(V_{in} - 0.5) V_{out} - \frac{V_{out}^2}{2} \right] \left(\frac{W}{L} \right)$$

$$\text{Power} = \frac{V_{dd}}{5} I_d$$

$$5 \times 10^{-3} = 5 \times I_d$$

$$I_d = 1mA$$

$$\text{When } V_{IH} = 5V \quad V_{out} = V_{OL} = 1V$$

$$R = \frac{V_{DD} - V_{out}}{I_d}$$

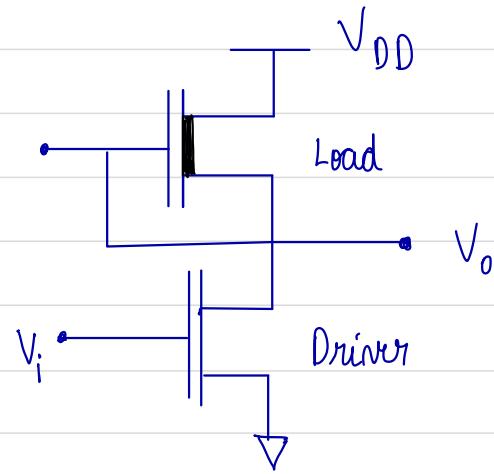
$$= \frac{5 - 1}{1mA} = 4 \times 10^3 = 4k\Omega$$

$$\text{So } I_d = 50 \times 10^{-6} \left(\frac{W}{L} \right) \left[(V_{in} - 0.5) V_{out} - \frac{V_{out}^2}{2} \right]$$

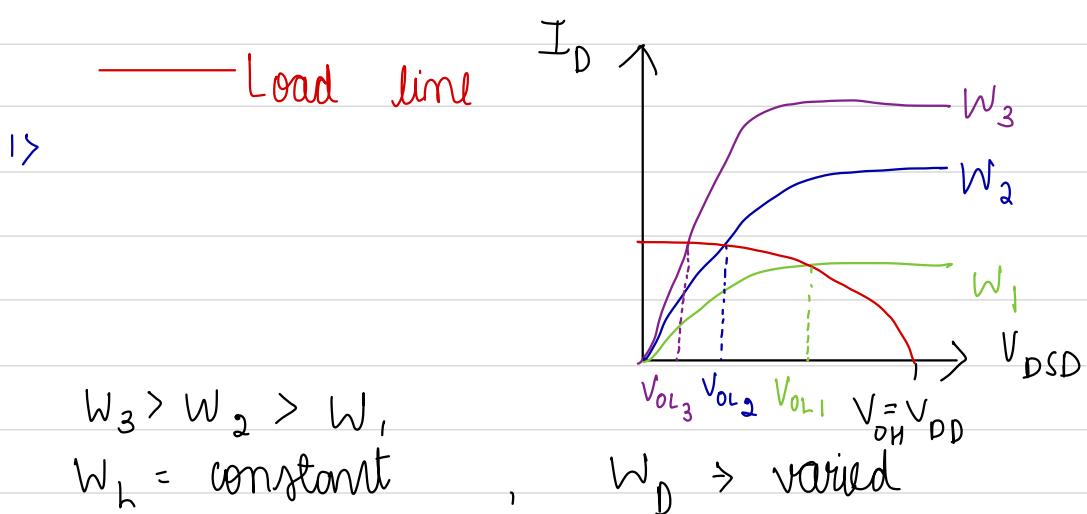
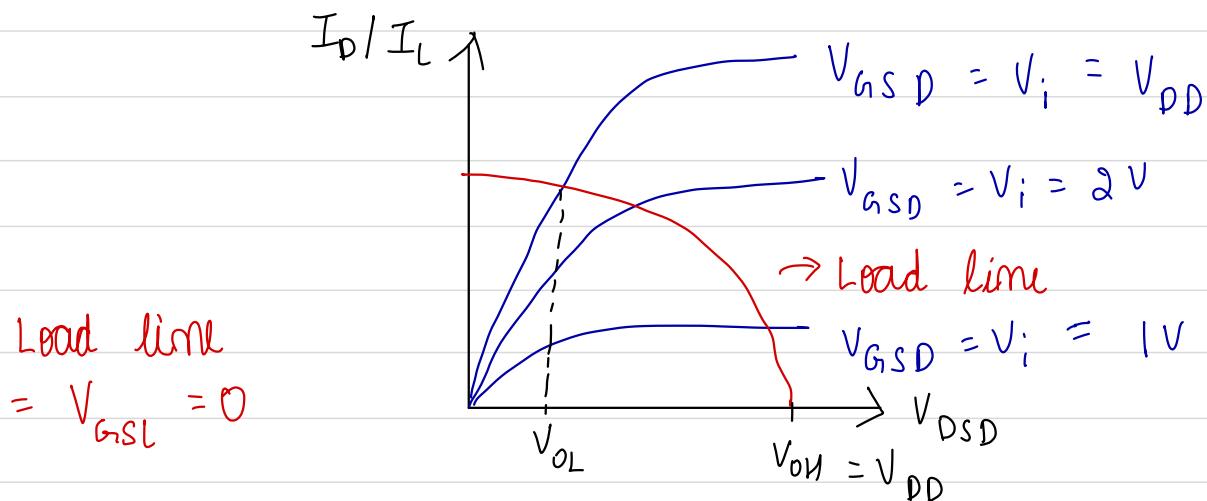
$$1mA = 5 \times 10^{-5} \left(\frac{W}{L} \right) \left[(5 - 0.5) 1 - \frac{1}{2} \right]$$

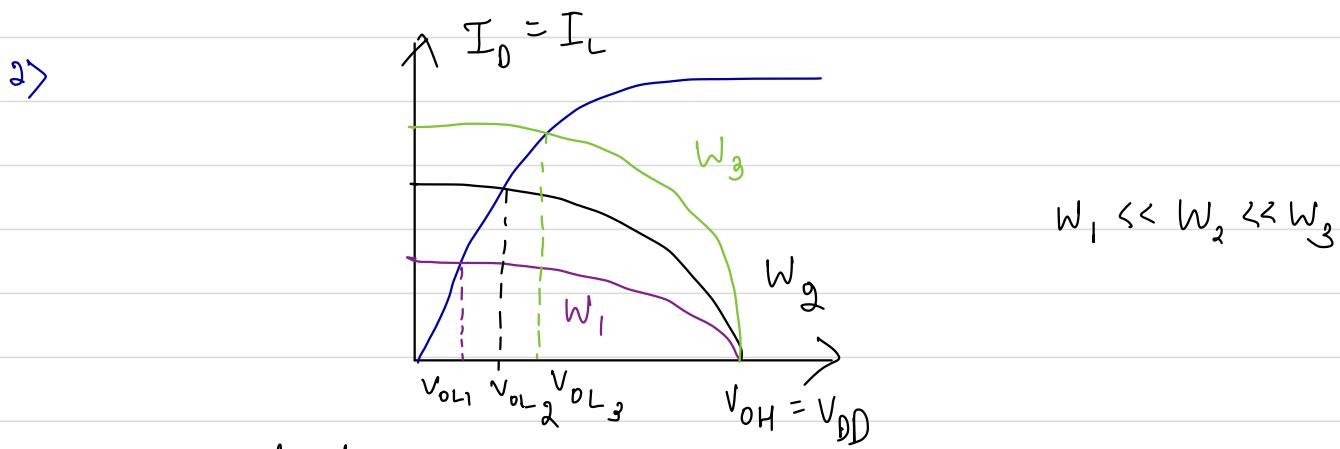
$$20 = \frac{W}{L} \times 4 \Rightarrow \frac{W}{L} = 5$$

NMOS Inverter with Depletion NMOS Load



- Even if $V_{GSL} = 0$, Load MOSFET is capable of conducting.





$W_D = \text{constant}$
 $W_L = \text{varied}$.

→ From 1st graph.

$(AR)_L = \text{constant}$ -

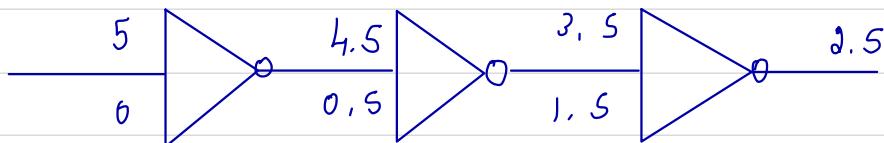
$(AR)_D \uparrow \Rightarrow R_{PD} \downarrow t_{fall} \downarrow V_{OL} \downarrow$ Gain \uparrow , $I_{\text{static}} \uparrow$, $P_{\text{static}} \uparrow$, VTC shifts left

→ From 2nd graph

$(AR)_D = \text{constant}$

$(AR)_L \uparrow \Rightarrow R_{PU} \downarrow t_{rise} \downarrow V_{OL} \uparrow$ Gain \downarrow , $I_{\text{static}} \uparrow$, VTC shifts right.

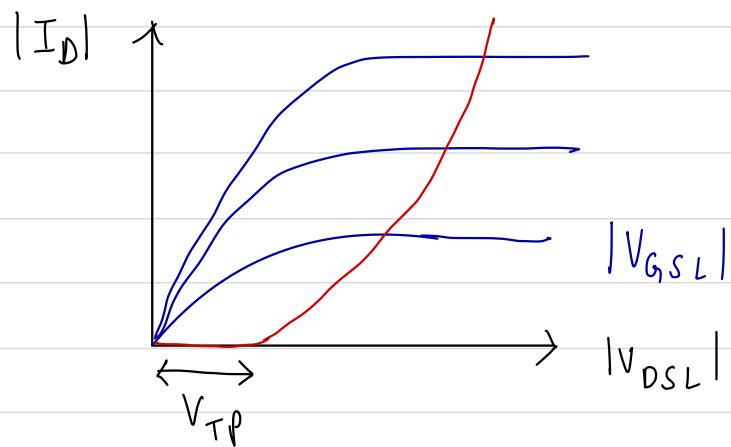
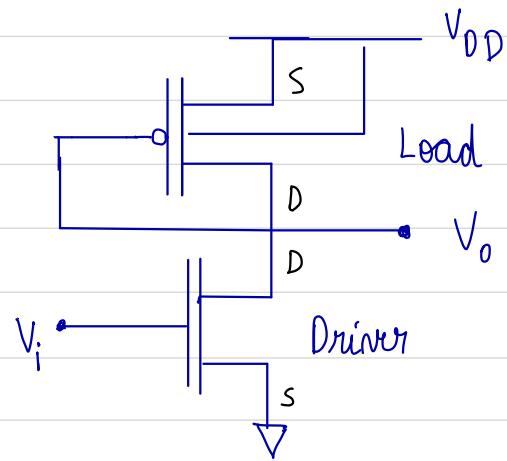
NOTE: gain decreases \Rightarrow



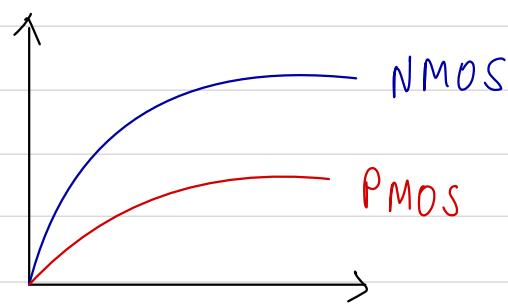
Comparison:

	Resistive	Enhancement	Depletion
V_{OL}	$\neq 0$	$\neq 0$	$\neq 0$
V_{OH}	Perfect V_{DD}	$V_{DD} - V_T$	Perfect V_{DD}

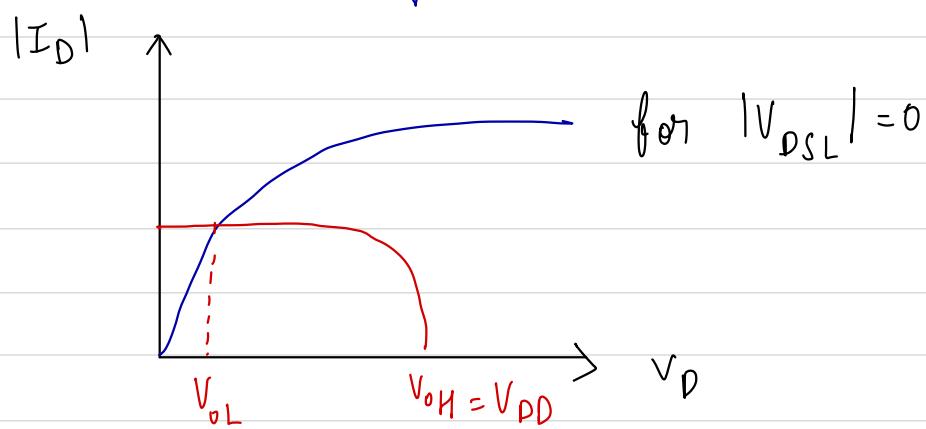
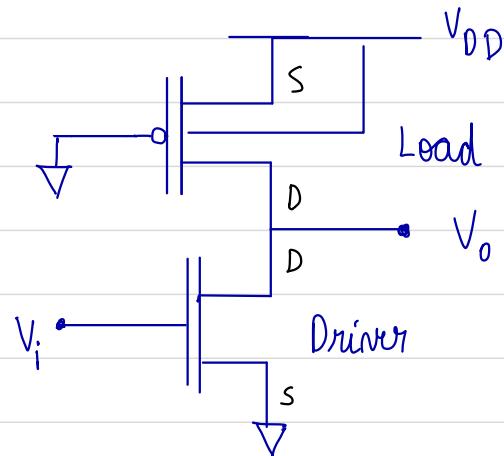
NMOS inverter with PMOS Load - Pseudo NMOS



NOTE: Difference between PMOS & NMOS for given $(\frac{W}{L})$



Because $\mu_p < \mu_n$ i.e. $\frac{\mu_n}{\mu_p} \geq 2, 5$



Varying $(AR)_L$ & $(AR)_D$ gives same result as in NMOS with depletion NMOS Load.

Drawbacks of Ratioed Logic

1> V_{oL} is not perfect '0'
cause: • Both full up & full down are closed simultaneously when input is logic high.
• If full up was open then, full up path resistance would have been huge (open)

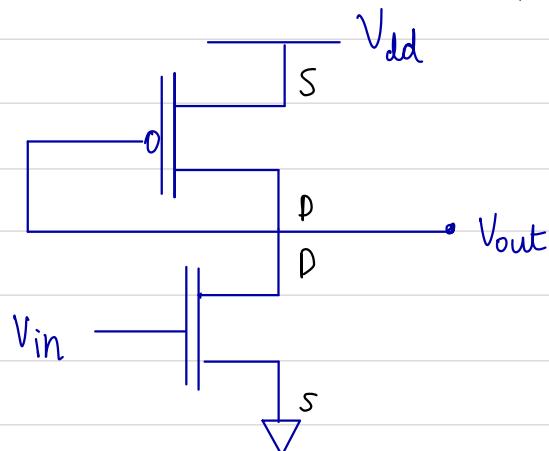
2> Continuous static power dissipation:
cause: • Both full up & full down are closed simultaneously when input is logic high
• If full up path was open then, there

would not be path from V_{DD} to GND when input is logic high.

solution: Both pull up & pull down paths should be conditionally open or closed i.e. connect to the pull up path.

Q) Given: $V_{DD} = 5V$, $V_{SS} = 0V$, $K_n' = 50 \mu A/V^2$
 $K_p' = 25 \mu A/V^2$, $V_{TN} = 0.5V$, $V_{TP} = 0.5V$.
 $K_D = 1$, $K_L = 2$. Pseudo NMOS is cascaded
with another identical inverter. L of mosfet
= 1 μm . Find V_{OH} , V_{OL} , t_{rise} , if $C = 10nF$

Ans



$$\begin{aligned} V_{OH} &= V_{DD} - V_{TP} \\ &= 5 - 0.5 \\ &= 4.5V \end{aligned}$$

When $V_{in} = 5V$

$$K_L \left[(V_{GSL} - V_{TP}) V_{DSL} - \frac{V_{DSL}^2}{2} \right] = K_D \left[(V_{GSD} - V_{TN}) V_{DSD} - \frac{V_{DSD}^2}{2} \right]$$

$$\begin{aligned} \text{For load: } V_{DS} &= V_{out} - V_{dd} \\ V_{GSS} - V_{TP} &= V_{out} - V_{dd} - V_{TP} < V_{DS} \end{aligned}$$

\Rightarrow saturation.

$$\therefore K_L \frac{(V_{GSL} - V_{TP})^2}{2} = K_D \left[(V_{GSD} - V_{TN}) V_{DSD} - \frac{V_{DSD}^2}{2} \right]$$

$$\text{at } V_{in} = 5, \quad V_{out} = V_{OL}$$

$$2 \times \frac{(V_{OL} - V_{dd} + V_{TP})^2}{2} = 1 \times \left[(5 - 0.5) V_{OL} - \frac{V_{OL}^2}{2} \right]$$

$$(V_{OL} - 4.5)^2 = 4.5 V_{OL} - \frac{V_{OL}^2}{2}$$

$$V_{OL}^2 + 20.25 - 9 V_{OL} = 1.5 V_{OL} - 0.5 V_{OL}^2$$

$$\Rightarrow 1.5 V_{OL}^2 - 13.5 V_{OL} + 20.25 = 0$$

$$\therefore V_{OL} = 1.9 V_0$$

$$\therefore I_{Dnat} = \frac{2 \times (1.9 - 1.5)^2}{2} = 6.76 \mu A$$

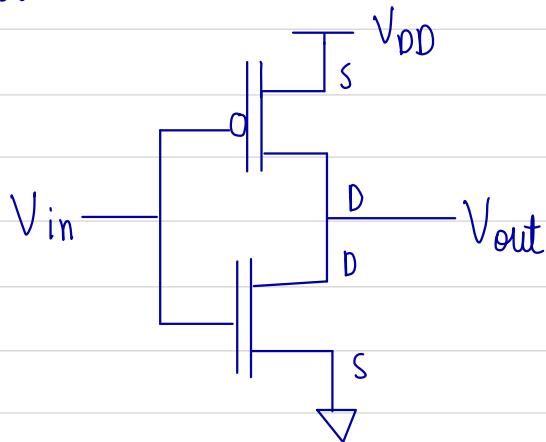
$$R_{eq} = \frac{3}{4} \frac{V_{DD}}{I_{Dnat}} = \frac{3}{4} \times \frac{5}{6.76 \times 10^{-6}} = 555 k$$

$$\begin{aligned} t_{rise} &= 2.2 R_{eq} C \\ &= 2.2 \times 555 \times 10^3 \times 10 \times 10^{-9} \\ &\approx 10 \text{ msec} \end{aligned}$$

Complementary Metal Oxide Semiconductor (CMOS)

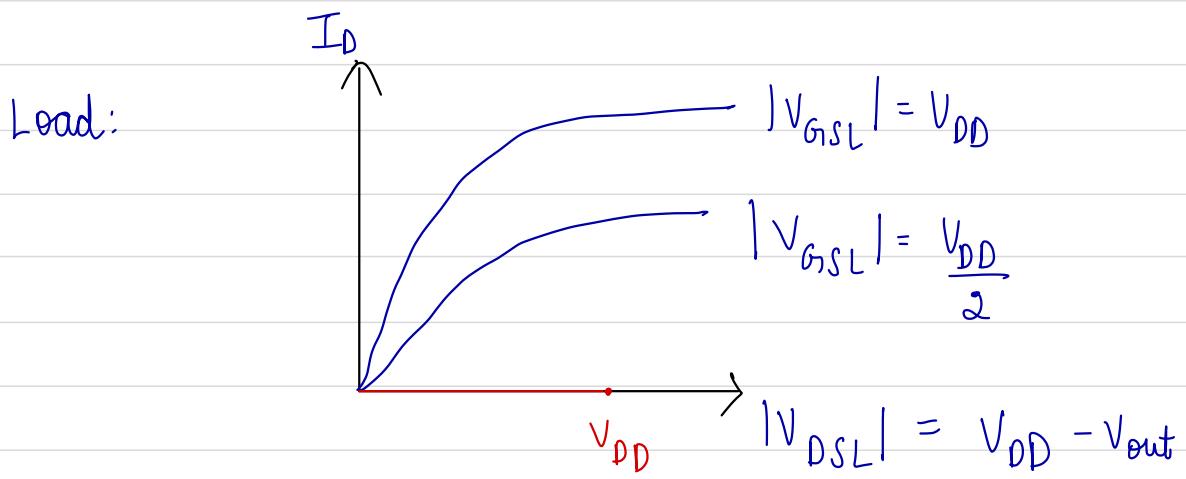
→ NMOS is a good conductor of '0'
 → PMOS is a good conductor of '1'.

Inverter with CMOS

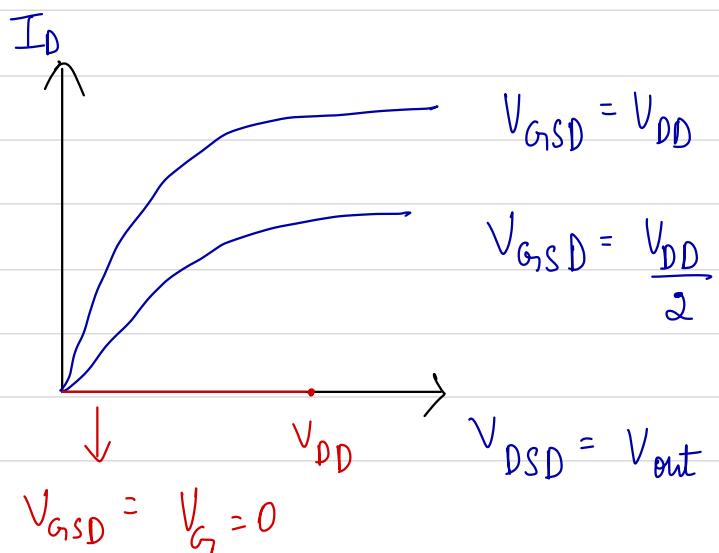


$$V_{GSL} = V_{DD} - V_{in}$$

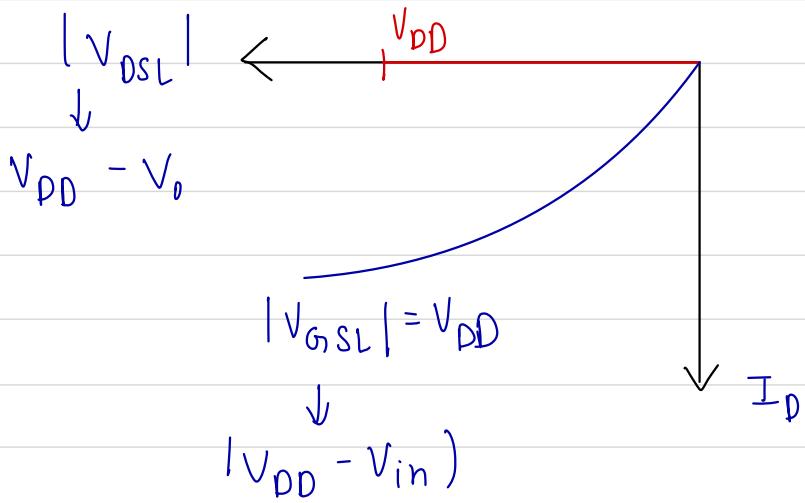
$$V_{GSD} = V_{in}$$



Driver:



PMOS characteristics :



Here $\frac{\mu_n}{\mu_p} = 2$.

$$\text{Usually } L_{NMOS} = L_{PMOS} = 1\mu m$$

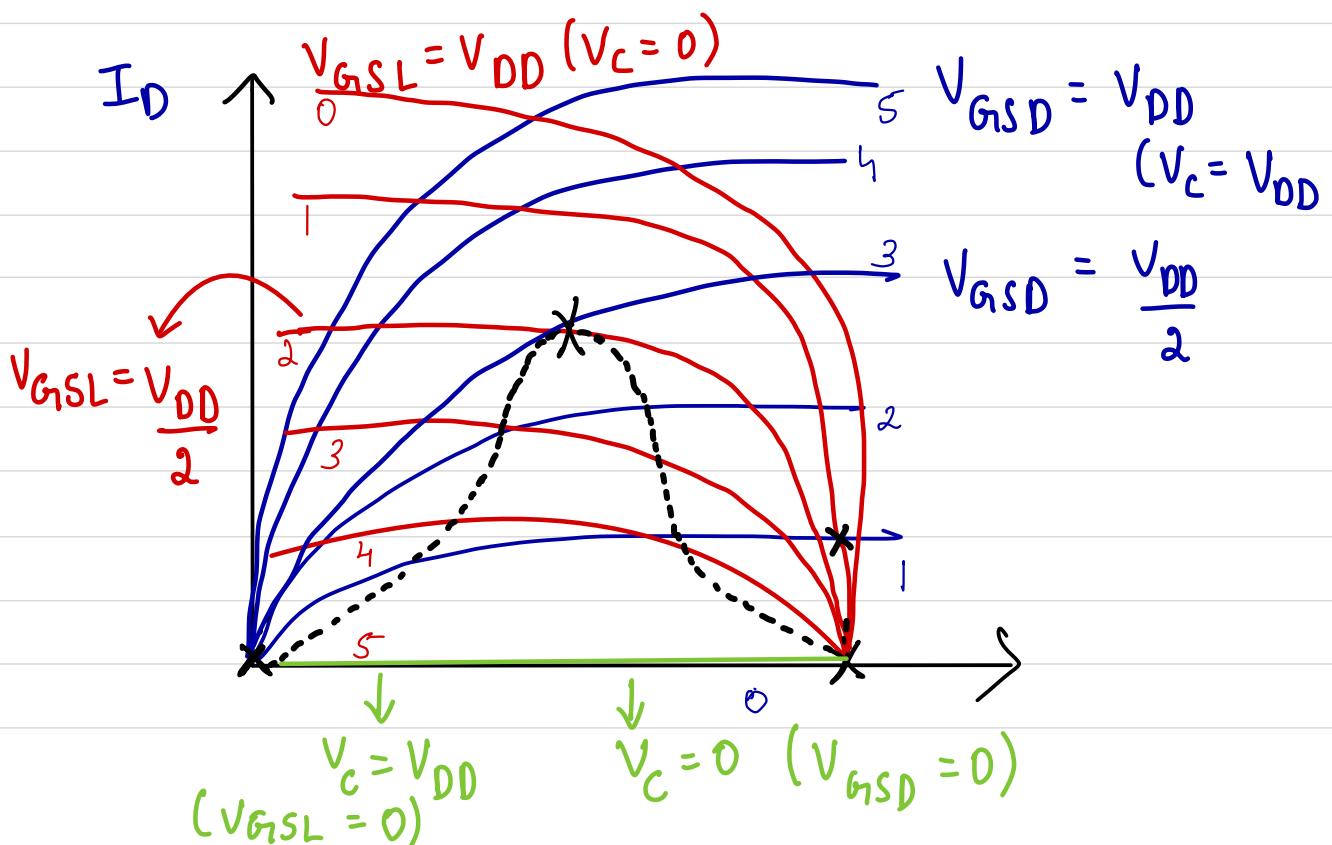
$$W_L = 2\mu$$

$$W_D = 1\mu m$$

$$\therefore K_L = 1$$

$$K_D$$

When $V_o = V_{DD}$ ($V_{DSD} = V_{DD}$)
from circuit $V_{DSL} = 0$ (in PMOS)

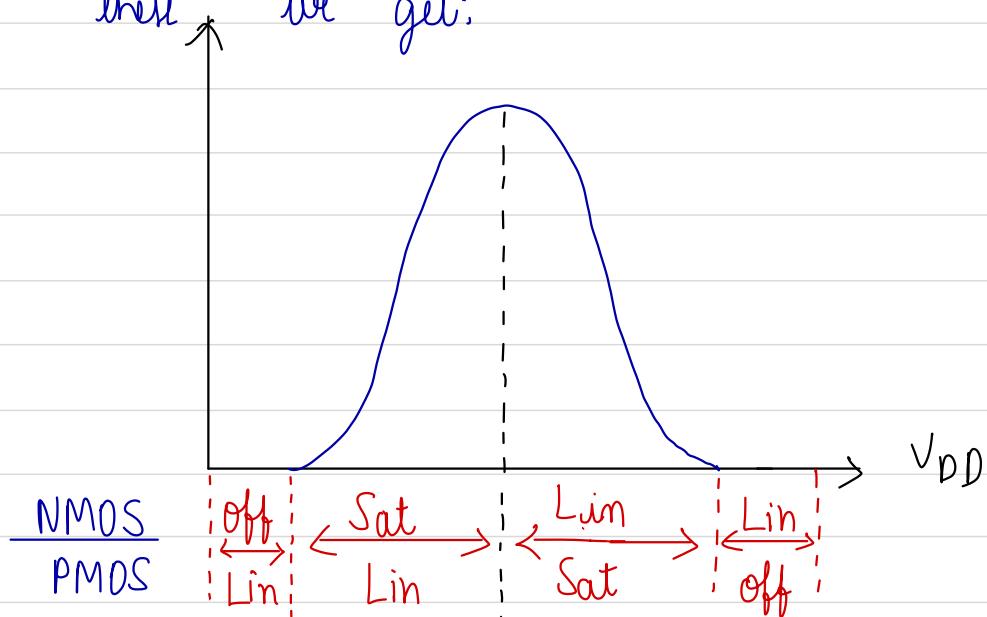


When $V_{in} = 0$: $V_{GSD} = 0$
 $V_{GSL} = V_{DD}$

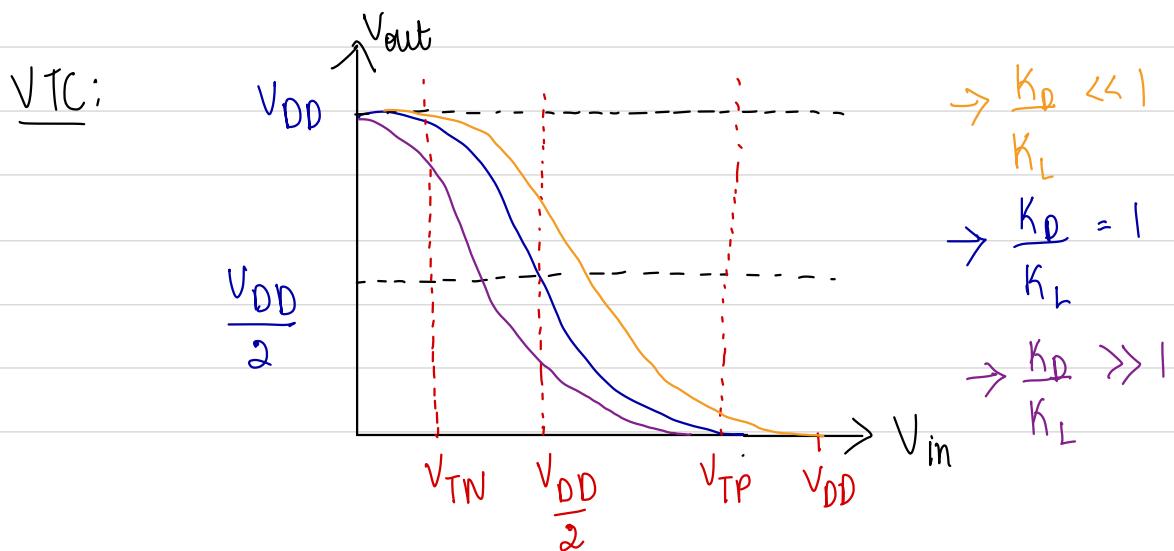
When $V_{in} = V_{DD}$: $V_{GSD} = V_{DD}$
 $V_{GSL} = 0$

When $V_{in} = \frac{V_{DD}}{2}$: $V_{GSD} = \frac{V_{DD}}{2}$
 $V_{GSL} = V_{DD} - \frac{V_{DD}}{2} = \frac{V_{DD}}{2}$

Joining them we get:



For rise time = fall time, we must have
 $R_{PUN} = R_{PDN} = R$. This happens if $\frac{K_D}{K_L} = 1$



For a given K_D ; K_L increase:

- 1> R_{pdn} decrease, $t_{rise} \downarrow$
- 2> can be used to manipulate t_{rise} of a buffer
- 3> V_{TC} curve shifts to the right

For a given K_L ; as K_D increases:

- 1> $R_{pdn} \downarrow$, $t_{fall} \downarrow$
- 2> can be used to manipulate t_{fall} of a buffer
- 3> V_{TC} curve shifts to the left.

$\rightarrow V_{OL}$ is perfect '0'
 $\rightarrow V_{OH}$ is perfect '1'

NOTE: CMOS do not have a limit for fanout.

When $K_D = K_L$

$$\rightarrow V_o = V_{DD}/2$$

$$\rightarrow t_{rise} = t_{fall}$$

\rightarrow By increasing K_D and K_L , maintaining $K_D/K_L = 1$ can manipulate drive strength i.e value of $t_{rise} = t_{fall}$.

\rightarrow Short circuit (continuous) and short current, power consumption increases with increase in K_D & K_L

Inverter operation

when $V_{in} = \text{Logic '0'}$:

→ PDN path is open

→ PUN path is closed

→ $V_o = V_{OH} = V_{DD}$, a perfect '1' (because full up device is a PMOS which is a good conductor of logic '1'; no V_t drop.)

when $V_{in} = \text{Logic '1'}$:

→ PDN path is closed

→ PUN path is open

→ $V_o = V_{OL} = 0V$, a perfect '0' (because full down device is a NMOS which is a good conductor of logic '0'; no V_t drop.)

when V_{in} is either V_{DD} or $0V$ (static case):

→ There is no short circuit path between V_{DD} & V_{SS} because either full up or the full down path is closed. No both simultaneously.

→ No static power consumption (except sub threshold conduction of the mosfets)

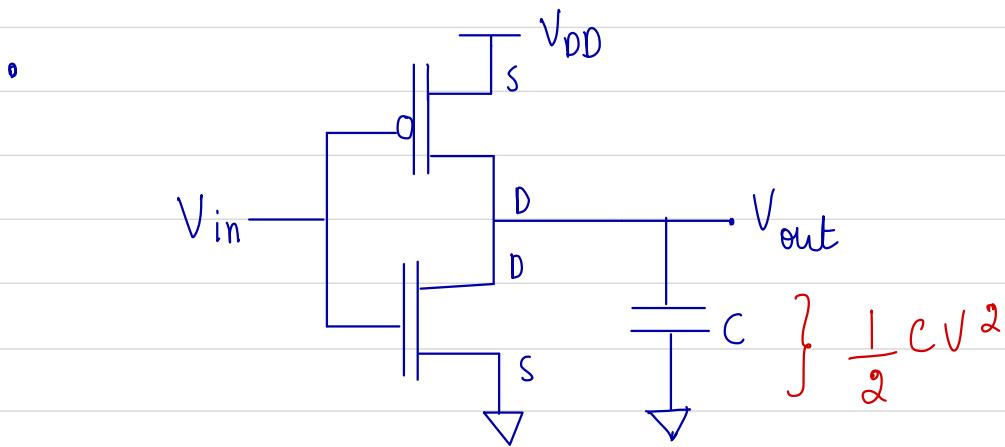
when V_{in} is neither V_{DD} or $0V$ (dynamic case):

→ A path exists from V_{DD} to V_{SS} through PUN & PDN. - A continuous current flows, leads to dynamic power consumption.

→ If w_{load} & w_{driver} (aspect ratios of Load & driver) are large, dynamic power consumption

increases. At the same time t_{rise} & t_{fall} decreases.

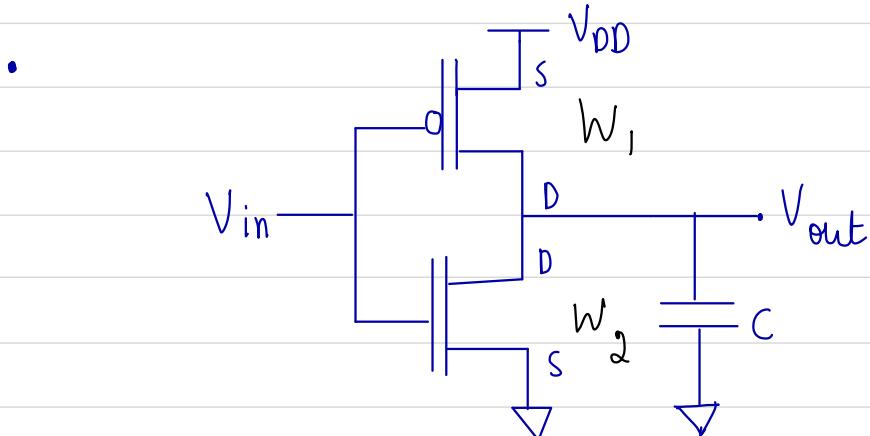
NOTE :



→ When the input is logic '1' the stored energy $\frac{1}{2} CV^2$ is released.

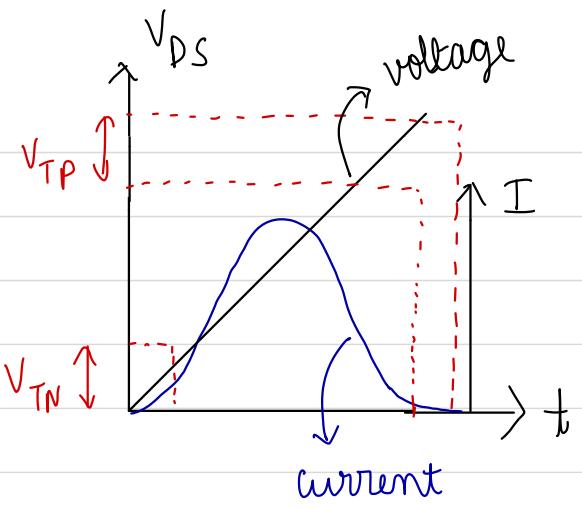
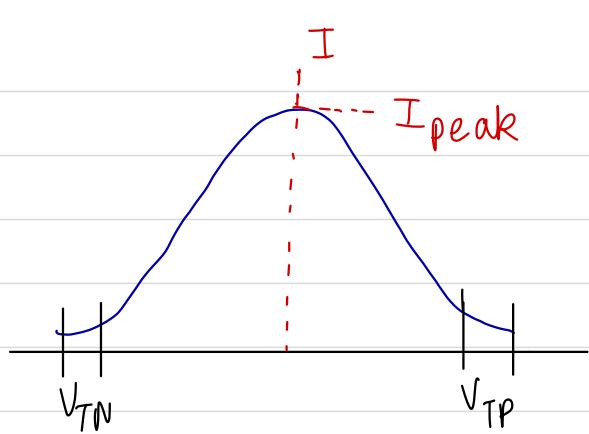
→ So we can reduce either C or V to reduce voltage

→ By reducing voltage we reduce power by square factor.

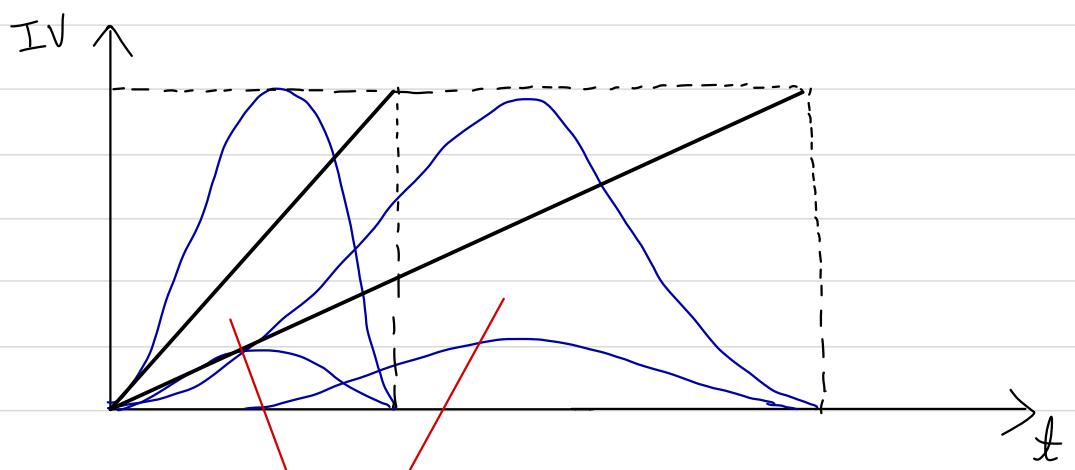


→ If $W_1 = 2W$ & $W_2 = W$, let $T = 1 \text{ nsec}$ if widths are doubled then current increases, i.e. drive strength increases.

→ If $W_1 = 4W$ & $W_2 = 2W$, then $T = 0.5 \text{ nsec}$



→ As rise time is increased, more energy is wasted.



Static energy dissipated

Under static conditions $I_{\text{load}} = I_{\text{driver}}$

$$\Rightarrow K_P \left(\frac{W}{L} \right)_{\text{load}} \frac{(V_{GSL} - V_{tL})^2}{2} = K_N \left(\frac{W}{L} \right)_{\text{driver}} \frac{(V_{GSD} - V_{tD})^2}{2}$$

$$\Rightarrow K_L \frac{(V_{GSL} - V_{tL})^2}{2} = K_D \frac{(V_{GSD} - V_{tD})^2}{2}$$

Let us assume $|V_{tL}| = |V_{tD}| \quad \& \quad V_{in} = \frac{V_{DD}}{2}$, then,

Substituting $V_{GSL} = V_{GSD} = 0.5 \cdot V_{DD}$ in the above equation we find that, $K_L = K_D$.

\Rightarrow This implies that we can design a CMOS inverter with $t_{rise} = t_{fall}$ if $K_D = K_L$ i.e $K_D / K_L = 1$. And under these conditions when $V_{in} = \frac{V_{DD}}{2}$, $V_{out} = \frac{V_{DD}}{2}$. This means $NMH = NML$,

For a CMOS inverter if $K_D = K_L$ then,

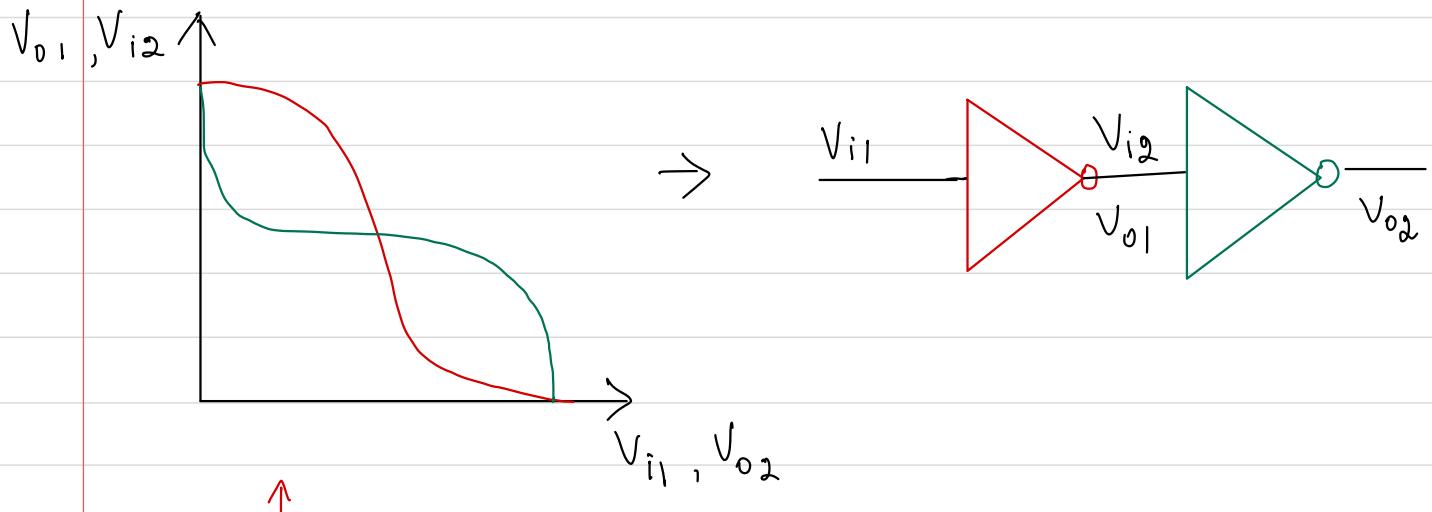
$$\rightarrow t_{rise} = t_{fall}$$

$$\rightarrow NMH = NML$$

$$\rightarrow V_{in} = \frac{V_{DD}}{2} \quad \Rightarrow \quad V_{out} = \frac{V_{DD}}{2}$$

By manipulating the ratio of K_D to K_L we can change the logic transition point, t_{rise} , t_{fall} , NMH & NML .

Regenerative property of a logic gate:



Transfer characteristics of NOT gate cascaded.

NOTE: Only resistors & parasitic resistance of active device can dissipate power.

Power dissipation types: Static, dynamic, Leakage

Static power consumption:

- Power dissipated in the circuit due to a constant current flowing from V_{DD} to GND when inputs & outputs are not changing.
- Non productive & ideally must be 0.

Dynamic power consumption:

- In MOSFET based logic gates, the logic value is stored in parasitic capacitance at the input or output.
- When the output toggles due to evaluation on the function, the output capacitor

charges or discharges.

- Though the capacitor is a charge storage device, the energy stored on the output capacitor is wasted.
- The charging & discharging process takes place by the current flowing through the PUN and PDN switches which have parasitic resistance and power is dissipated due to these switch resistance.

Leakage power:

- Due to very small current flowing through the device due to reverse biased junctions eg: Sub - threshold conduction, substrate leakage.

Design Power Metrics:

- Power
- Energy per transition
- Area
- Delay.
- All these should be as small as possible, typically when you try to reduce one of them, others tend to increase. There should be a tradeoff.

Power consumption:

- Decides the regulation of the supply source.
- Larger power variations need better power regulation.

- Decides the width of the power rails (power rail resistance should be as low as possible, otherwise power is dissipated in these rails and supply rail voltage drops - ground bounce).

Energy:

- Very important parameter for mobile devices.
- Battery storage capacity (which is fixed & limited) decides how long the computer can be used without recharging.
- Smaller energy consumption per transition, battery lasts longer or more computations can be made.
- Computations involve toggling of values. Use algorithms that need less number of transitions, optimize the synthesized logic (reduce number of gates, fanout)
- Reduce parasitic capacitances.

Power consumption

- Static – Depends on the circuit or Logic Family (eg. Ratioed or non-ratioed)
- Dynamic – Proportional to $C \cdot V^2$
- Leakage – Depends on Process Technology

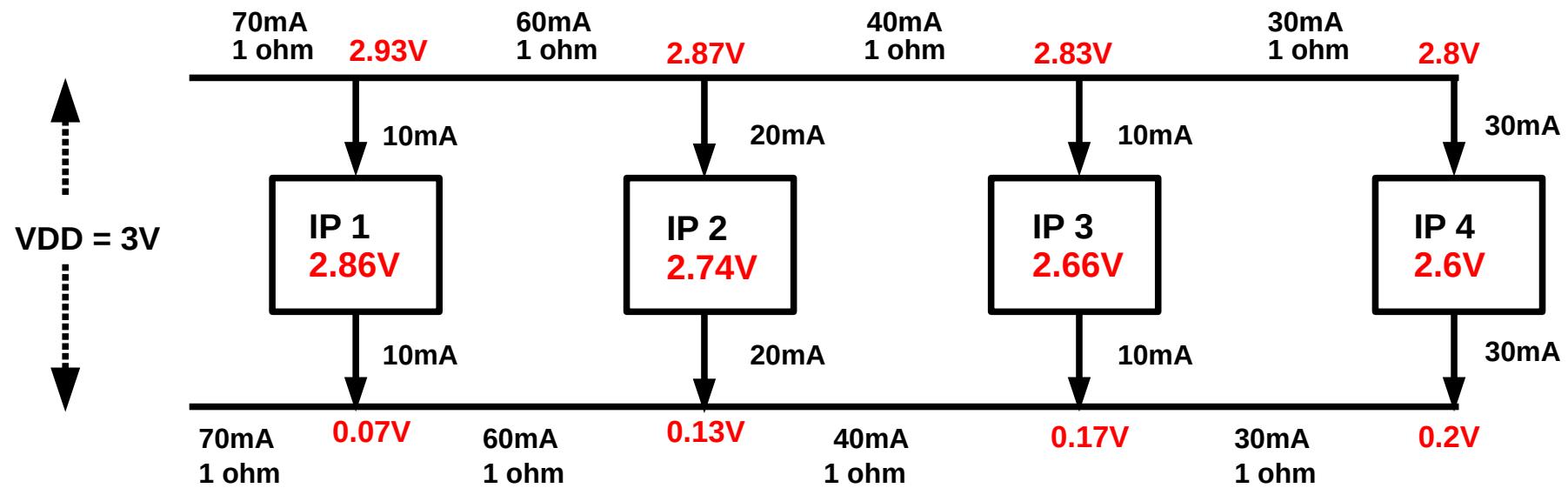
To reduce Power and Energy consumption:

- Reduce the number of transitions – Dynamic power consumption is due to charging and discharging of outputs ie. toggling of output by choosing appropriate
 - algorithm (eg. Booths multiplication with higher radix)
 - architecture (eg. Carry Save Adders)
 - Optimized RTL both pre and post synthesis
- Choose appropriate Process Technology
 - Low Supply voltage (Smaller VDD) – Power consumed is proportional to square of the supply voltage
 - Low parasitic capacitance - Power consumed is proportional to Capacitance
 - Low leakage
- Reduce rise and fall time of inputs and outputs – higher these values higher will be the energy consumed due to longer period of short circuit power consumption.
 - Optimize the sizing of MOSFETs
 - Optimize the Layout style – less parasitic capacitance and power supply rail resistance etc.

Comparison of logic families

	Perfect VOL ?	Perfect VOH ?	Static Power Consumption when V_i is a constant value = '1'	Dynamic Power Consumption (Due to (dis)charging of input and output capacitance)	Ratioed Logic	Input Capacitance
Passive Resistance	No	Yes	Yes	Small	Yes	Small
Enhancement NMOS	No	No	Yes	Small	Yes	Small
Depletion NMOS	No	Yes	Yes	Small	Yes	Small
Enhancement PMOS (Pseudo NMOS)	No	Yes	Yes	Small	Yes	Small
CMOS	Yes	Yes	No	Larger	No	Larger

Ground bounce:



Ground bounce affects:

- logic voltage level,
- drive strength,
- delay,
- noise margin
- computed value

- Digital supply lines are very noisy due to switching currents
- Reduce interconnect resistance
- Reduce power requirement
- Separate the Analog and Digital Ground