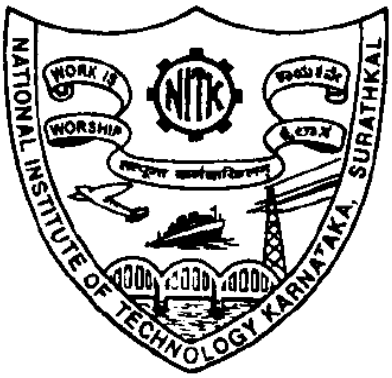
VLSI DESIGN LABORATORY

(Subject Code: EC-302)



Report submission

by

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List of Experiments

1. Study the VI characteristics of NMOS Transistor
2. Study of MOS inverter with passive resistance load.
3. Study of MOS inverter with active load-NMOS and PMOS (pseudo NMOS load)
4. Study of CMOS inverter.
5. Study of CMOS gates
6. CMOS Inverter Layout and Characterization.
7. Generation of a Standard Cell library.

Part 1

Experiment 1: Study the VI characteristics of NMOS Transistor

Objective:

Study the Input and Output characteristics of NMOS Transistor, effects of L, W, VTO, LAMBDA, VSB, and temperature on the behavior of the transistor.

Procedure:

a) Plot the input and output characteristics by sweeping VDS, VGS for a given L and W.

b) Vary W from a value equal to half the feature size to 10 times the feature size, repeat part (a), study the behaviour with variation in W.

c) Vary L from a value equal to half the feature size to 10 times the feature size, repeat part (a). Study the behaviour with variation in L.

d) Vary VTO within a reasonable range, repeat part (a), study the behaviour with variation in VTO.

e) Vary LAMBDA within a reasonable range, repeat part (a), study the behaviour with variation in LAMBDA.

f) Vary VSB within a reasonable range, repeat part (a), study the change in VTO, and the behaviour of transistor.

g) Vary temperature within a reasonable range, repeat part (a), study the change in VTO, and the behaviour of transistor.

Observations:

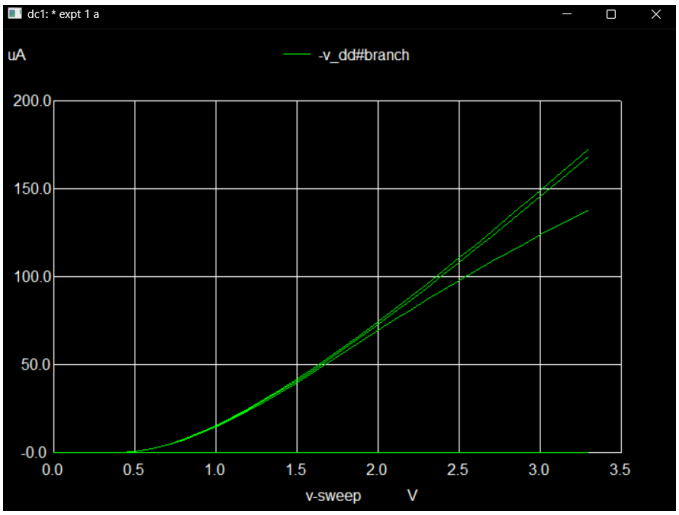
a) Code:

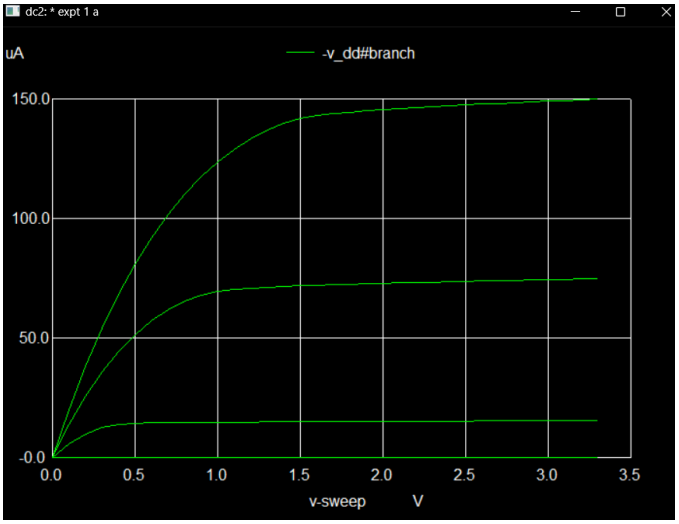
```
* Expt 1 a

* including model files
.include ./t14y_tsmc_025_level3.txt

* netlist
m1 vdd in 0 0 cmosn l=1u w=0.5u

* power sources excitation
v_dd vdd 0 3.3
v_in in 0 3.3

* implementation
.control
dc v_in 0 3.3 0.1 v_dd 0 3.3 1
run
setplot dc1
plot -v_dd#branch
dc v_dd 0 3.3 0.1 v_in 0 3.3 1
run
setplot dc2
plot -v_dd#branch
.endc

.end
```

Here, we have plotted VGS and VDS with respect to the current. L = 1um, W = 0.5um.

We vary VGS from 0 to 3.3 V in increments of 0.1V with VDS=0, 1, 2, and 3 V respectively.

Next, we vary VDS from 0 to 3.3 V in increments of 0.1V with VGS=0, 1, 2, and 3 V respectively.





b) Code:

* **Expt 1 b**

* include model files

.include ./t14y_tsmc_025_level3.txt

* spice netlist

m1 drain gate 0 0 cmosn l=1u w=0.5u

* excitation sources

vdd drain 0 dc 3.3

vgg gate 0 dc 3.3

* desired responses

.dc vdd 0 3.3 0.1 vgg 0 3.3 1

* implementation

.control

foreach wid 0.25u 0.5u 5u

alter m1 w = $wid

run

end

.endc

```
* plot
.control
foreach iter 1 2 3
setplot dc$iter
plot -vdd#branch
end
.endc

.end
```

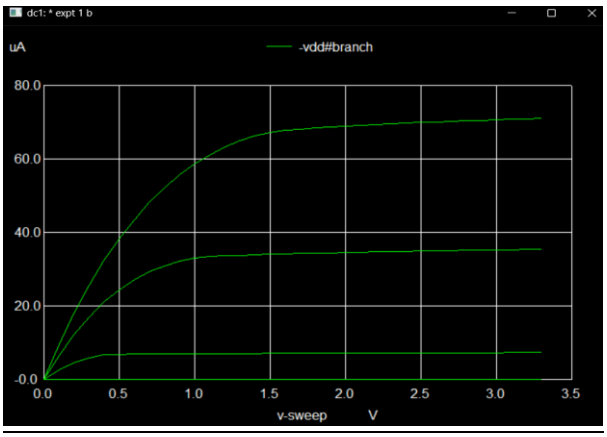
Here, we vary the width of NMOS transistor from 0.25um to 5um. L is kept constant at 1um. We observe the following values:

Width of NMOS transistor (um)	ID (uA)
0.25	71
0.5	150
5	1570

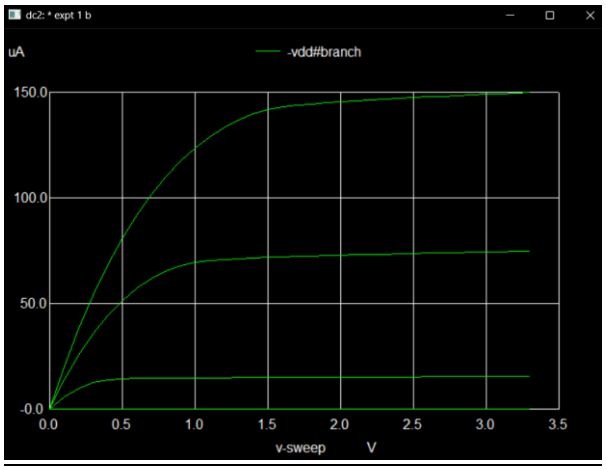
We observe that the drain current is linearly varying with an increase in the width of the NMOS transistor. Therefore, the drain current is directly proportional to the width of the NMOS transistor.

Plots of the above are as shown below:

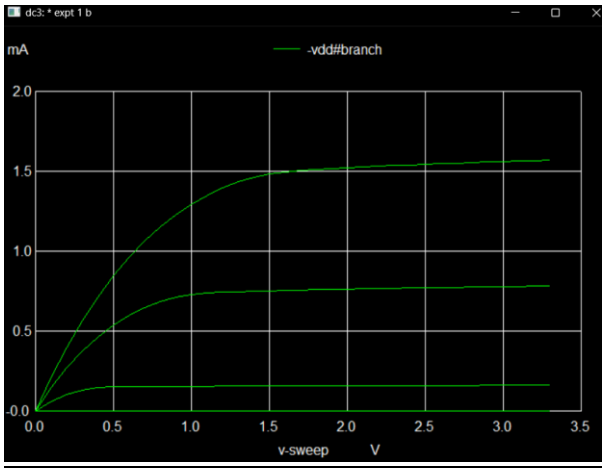
Plots:



W = 0.25um



W = 0.5 um



W = 5um

c) Code:

```
* Expt 1 c

* include model files
.include ./t14y_tsmc_025_level3.txt

* spice netlist
m1 drain gate 0 0 cmosn l=1u w=0.5u

* excitation sources
vdd drain 0 dc 3.3
vgg gate 0 dc 3.3

* desired responses
.dc vdd 0 3.3 0.1 vgg 0 3.3 1
```

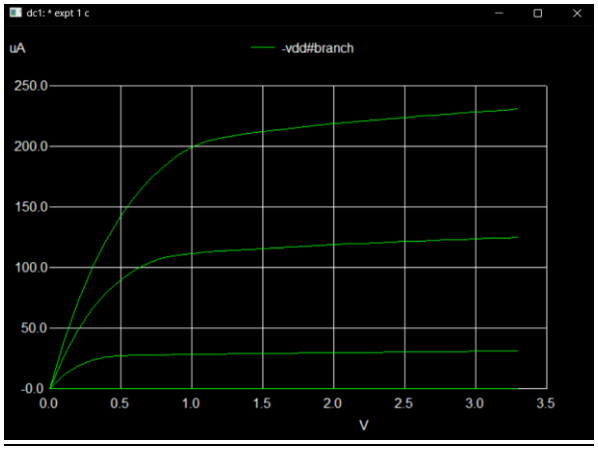
```
* implementation
.control
foreach len 0.5u 1u 10u
alter m1 l = $len
run
end
.endc

* plot
.control
foreach iter 1 2 3
setplot dc$iter
plot -vdd#branch
end
.endc

.end
```

Here, we vary the length of the NMOS transistor from 0.5um to 10um. L is kept constant at 1um. We observe the following values:

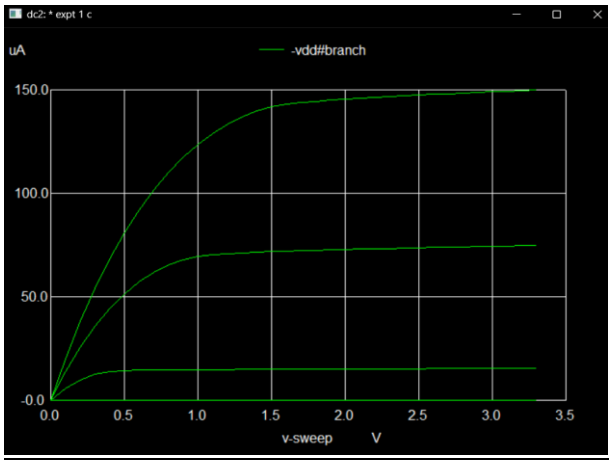
Length of NMOS transistor (um)	ID (uA)
0.5	230
1	150
10	22.4

We observe that the drain current linearly decreases with an increase in the length of the NMOS transistor. Therefore, the drain current is inversely proportional to the length of the NMOS transistor.

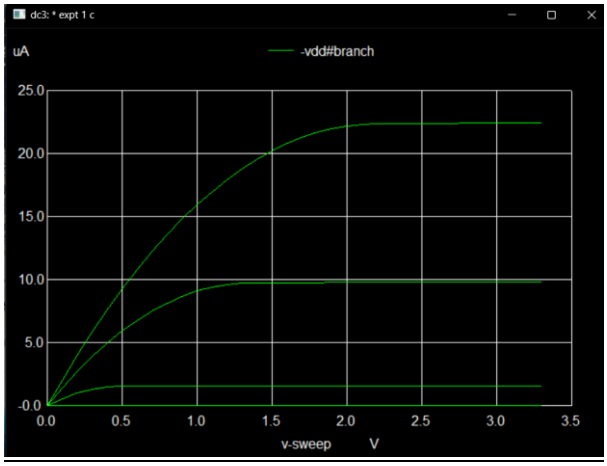
Plots of the above are as shown below:



L = 0.5um



L = 1um



L = 10um

d) Code:

*** Expt 1 d**

.MODEL nfet1 NMOS LEVEL=1 VTO=0.5

.MODEL nfet2 NMOS LEVEL=1 VTO=1.0

```
.MODEL nfet3 NMOS LEVEL=1 VTO=1.5

* MOSFETS
m0 drain0 gate 0 0 nfet1 w=0.5u l=1u ad=6.84p pd=10.8u as=6.84p ps=10.8u
m1 drain1 gate 0 0 nfet2 w=0.5u l=1u ad=6.84p pd=10.8u as=6.84p ps=10.8u
m2 drain2 gate 0 0 nfet3 w=0.5u l=1u ad=6.84p pd=10.8u as=6.84p ps=10.8u

* RESISTANCES
R0 dd drain0 0.0001
R1 dd drain1 0.0001
R2 dd drain2 0.0001

* SUPPLY VOLTAGES
v_dd dd 0 dc 3.3
v_gg gate 0 dc 3.3

* VARIATION OF VOLTAGES
.dc v_gg 0 3.3 0.1 v_dd 0 3.3 1
.dc v_dd 0 3.3 0.1 v_gg 0 3.3 1

.control
run
setplot dc1
plot (v(dd)-v(drain0))/0.0001
plot (v(dd)-v(drain1))/0.0001
plot (v(dd)-v(drain2))/0.0001
*plot (v(dd)-v(drain0))/0.0001 (v(dd)-v(drain1))/0.0001 (v(dd)-v(drain2))/0.0001
setplot dc2
plot (v(dd)-v(drain0))/0.0001
plot (v(dd)-v(drain1))/0.0001
plot (v(dd)-v(drain2))/0.0001
.endc
.end
```

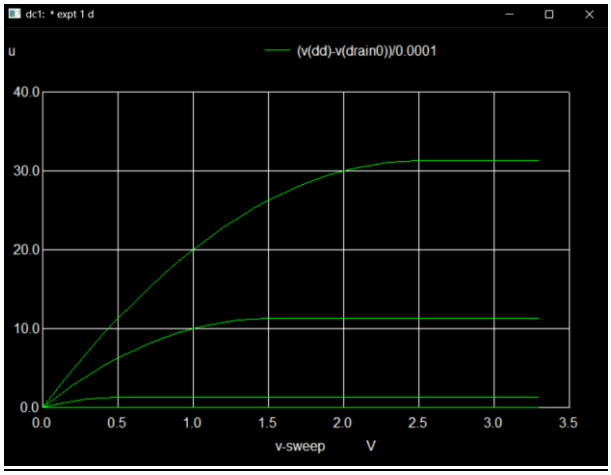
Here, we are varying VTO, which is zero bias threshold voltage.

For VGS = 3V

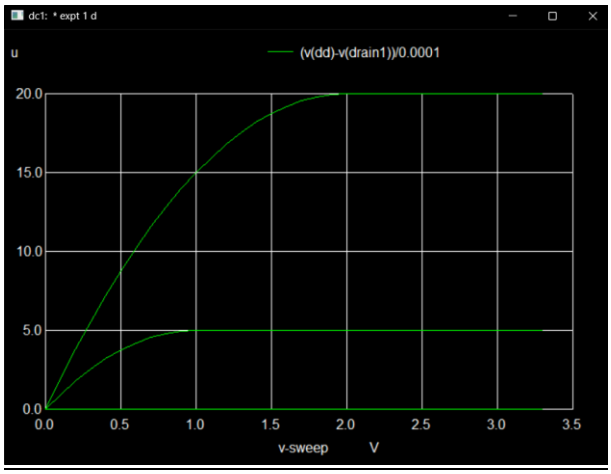
VTO (V)	ID (uA)
0.5	31.25
1	20
1.5	11.25

We observe that the drain current decreases with an increase in VTO. Therefore, the drain current is inversely proportional to the VTO of the NMOS transistor.

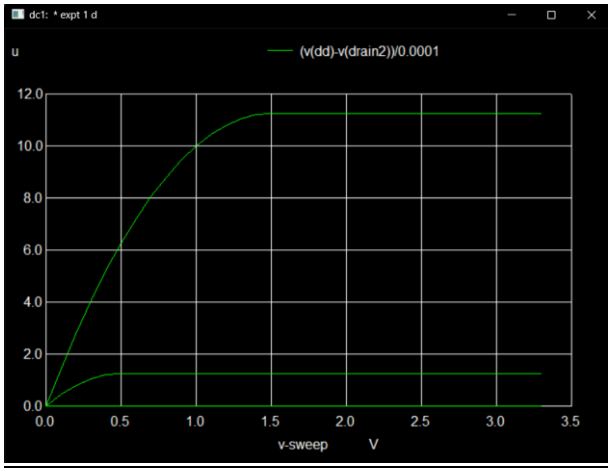
Plots of the above are as shown below:



VTO = 0.5V



VTO = 1V



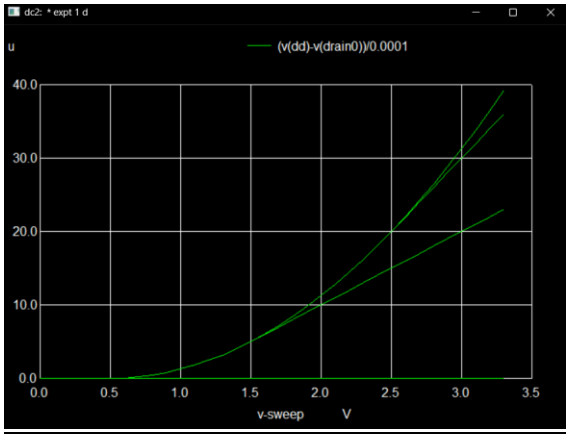
VTO = 1.5V

For VDS = 3V

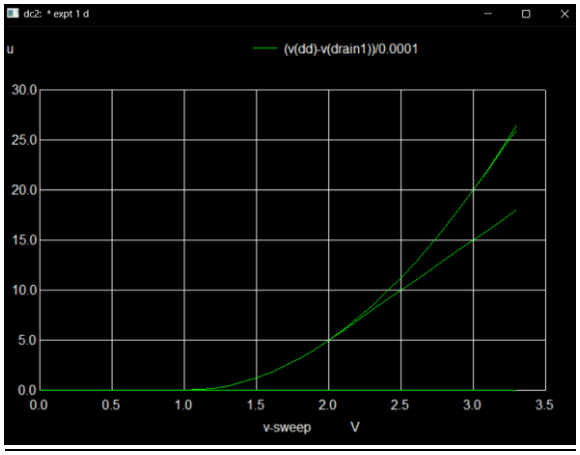
VTO (V)	ID (uA)
0.5	40
1	26
1.5	16

We observe that the drain current decreases with an increase in VTO. Therefore, the drain current is inversely proportional to the VTO of the NMOS transistor.

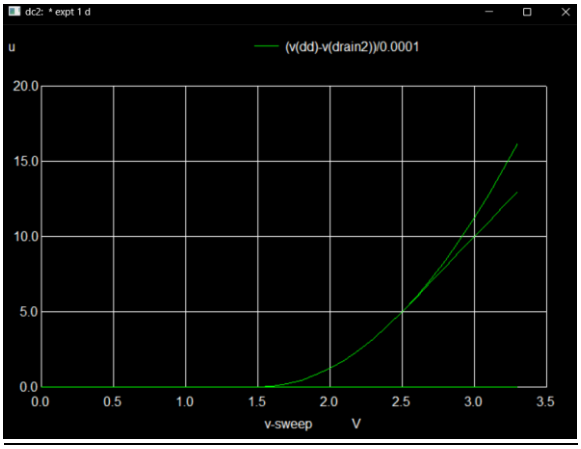
Plots of the above are as shown below:



VTO = 0.5V



VTO = 1V



VTO = 1.5V

e) Code:

***Expt 1 e**

m0 drain0 gate 0 0 nfet1 w=6.4u l=1.8u ad=6.84p pd=10.8u as=6.84p ps=10.8u

m1 drain1 gate 0 0 nfet2 w=6.4u l=1.8u ad=6.84p pd=10.8u as=6.84p ps=10.8u

m2 drain2 gate 0 0 nfet3 w=6.4u l=1.8u ad=6.84p pd=10.8u as=6.84p ps=10.8u

R0 dd drain0 0.0001

R1 dd drain1 0.0001

R2 dd drain2 0.0001

.MODEL nfet1 NMOS LEVEL=1 LAMBDA=0.3

.MODEL nfet2 NMOS LEVEL=1 LAMBDA=0.5

.MODEL nfet3 NMOS LEVEL=1 LAMBDA=0.9

* supply voltages

Vdd dd 0 dc 5

Vgg gate 0 dc 5

* analysis request

.dc vgg 0 5 0.1 vdd 0 5 1

.dc vdd 0 5 0.1 vgg 0 5 1

.control

run

setplot dc1

plot (v(dd)-v(drain0))/0.0001

plot (v(dd)-v(drain1))/0.0001

plot (v(dd)-v(drain2))/0.0001

*plot (v(dd)-v(drain0))/0.0001 (v(dd)-v(drain1))/0.0001 (v(dd)-v(drain2))/0.0001

setplot dc2

plot (v(dd)-v(drain0))/0.0001

plot (v(dd)-v(drain1))/0.0001

plot (v(dd)-v(drain2))/0.0001

.endc

.end

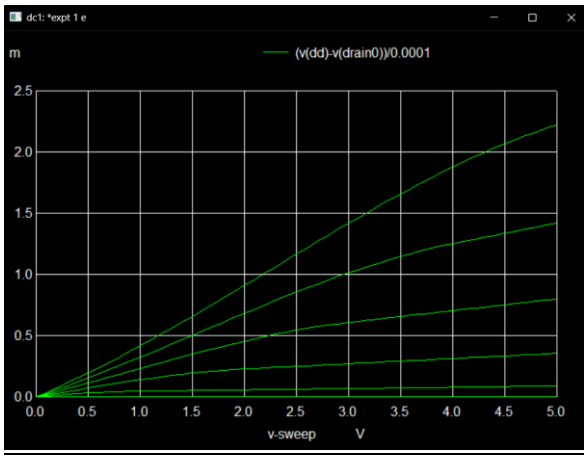
Here, we vary lambda, which is channel length modulation. When lambda increases, the channel length decreases. When channel length decreases, drain current Id increases because the channel has lesser resistance.

Therefore, drain current is directly proportional to lambda.

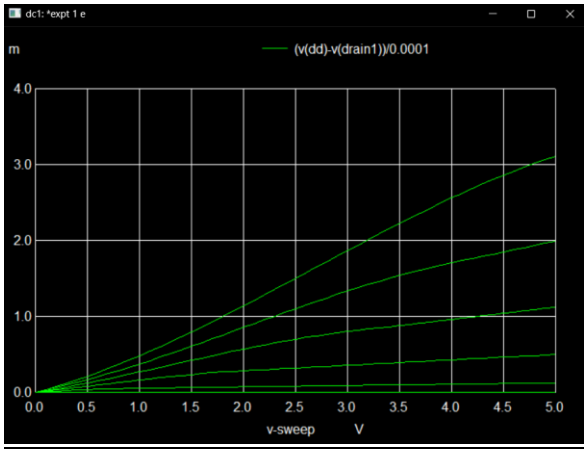
Vdd = 5V

Lambda	ID (mA)
0.3	2.23
0.5	3.10
0.9	4.89

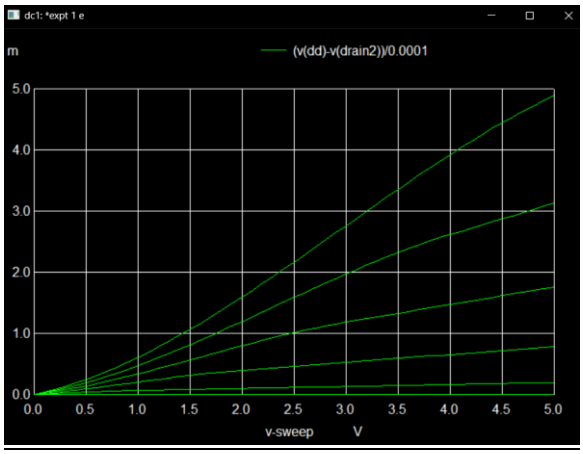
Plots of the above are as shown below:



Lambda = 0.3



Lambda = 0.5



Lambda = 0.9

f) Code:

*** Expt 1 f**

*model files

.include ./t14y_tsmc_025_level3.txt

m1 drain gate source bulk cmosn l=1u w=0.5u

vdd drain 0 3.3

vgg gate 0 3.3

vss source 0 0

vbb bulk 0 3.3

.dc vgg 0 3.3 0.1

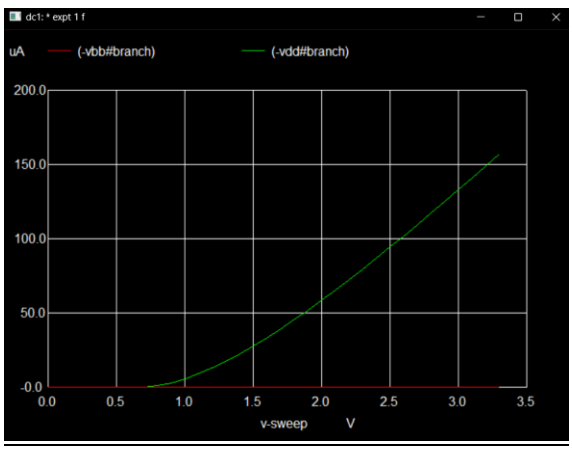
```
* implementation
.control
foreach vbulk -2 -1 0 1 2
alter vbb = $vbulk
run
end
.endc

.control
foreach iter 1 2 3 4 5
setplot dc$iter
plot (-vdd#branch) (-vbb#branch)
end
.endc

.end
```

Here, we are varying VSB, which is the source to bulk voltage.

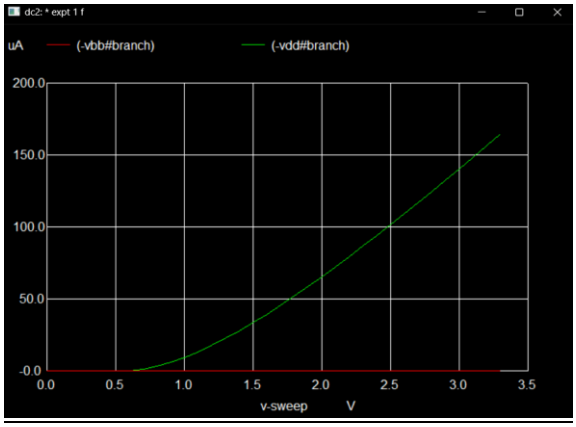
Case	VBB (V)	VSB (V)	IB (A)	VTO (V)	ID (uA)
1	-2	2	0	1.094	157
2	-1	1	0	0.928	165
3	0	0	0	0.831	174
4	1	-1	22A	-	0
5	2	-2	250A	-	0

We see that for negative VSB, drain current is very low. For positive VSB, as VSB increases, drain current decreases. Therefore, VSB is inversely proportional to drain current.

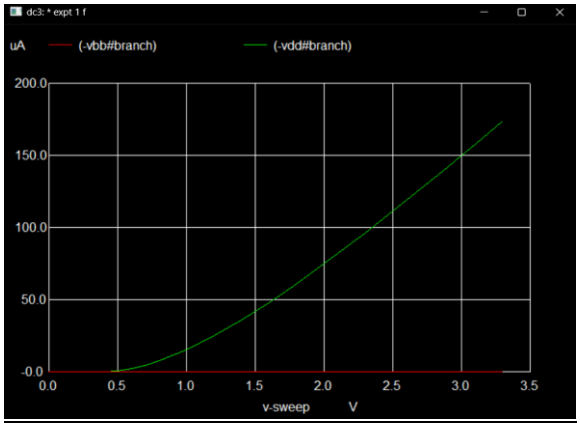
Plots of the above are as shown below:



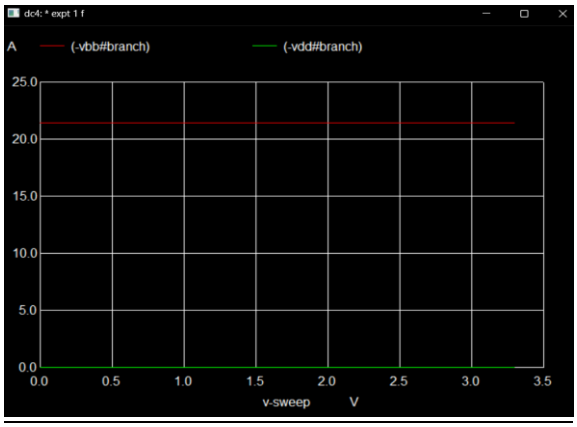
Case 1



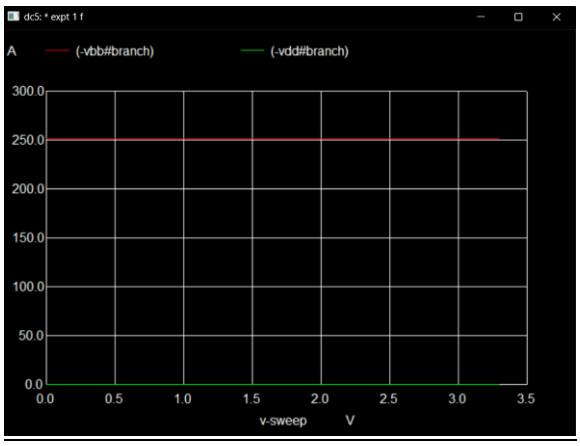
Case 2



Case 3



Case 4



Case 5

g) Code:

*** Expt 1 g**

```
* MODELS
.MODEL nfet nmos LEVEL=1

*define mosfet
 m0 drain gate 0 0 nfet w=0.5u l=1u ad=6.84p pd=10.8u as=6.84p ps=10.8u

* SUPPLY
vdd drain 0 dc 3.3
vgg gate 0 dc 3.3

* VARIATION
.dc vdd 0 3.3 0.1 vgg 0 3.3 1

* IMPLEMENTATION
.control
run
setplot dc1
plot -vdd#branch
set temp=50
run
setplot dc2
plot -vdd#branch
set temp=100
run
setplot dc3
plot -vdd#branch
.endc
.end
```

Here, we vary the temperature.

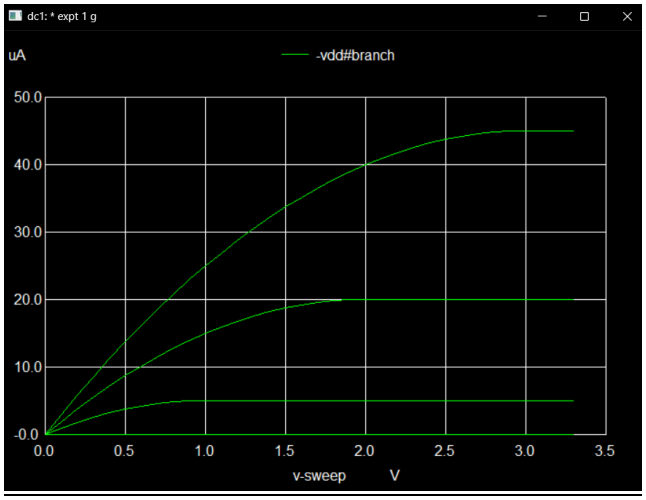
VDD = 3V

It is observed that an increase in temperature decreases mobility. This causes a decrease in drain current.

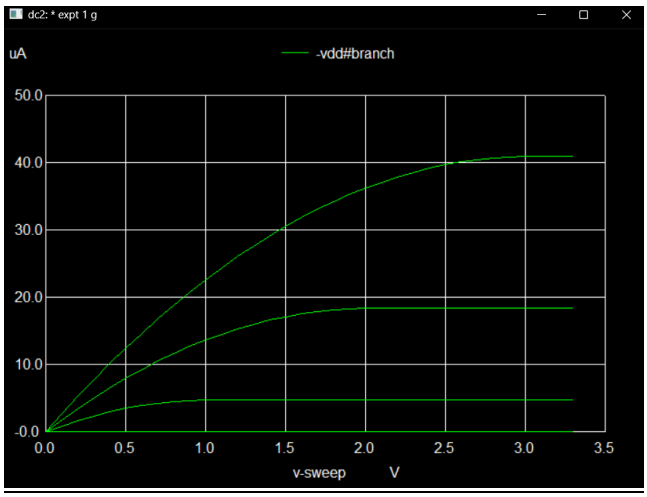
Therefore, the temperature is inversely proportional to the drain current.

Temperature (Celsius)	ID (uA)
27	45
50	41
100	34

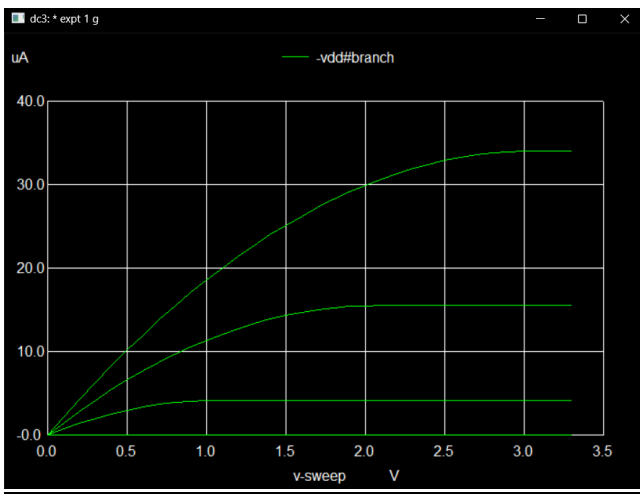
Plots of the above are as shown below:



T = 27 Celsius



T = 50 Celsius



T = 100 Celsius

Experiment 2: Study of MOS inverter with passive resistive load.

Objective:

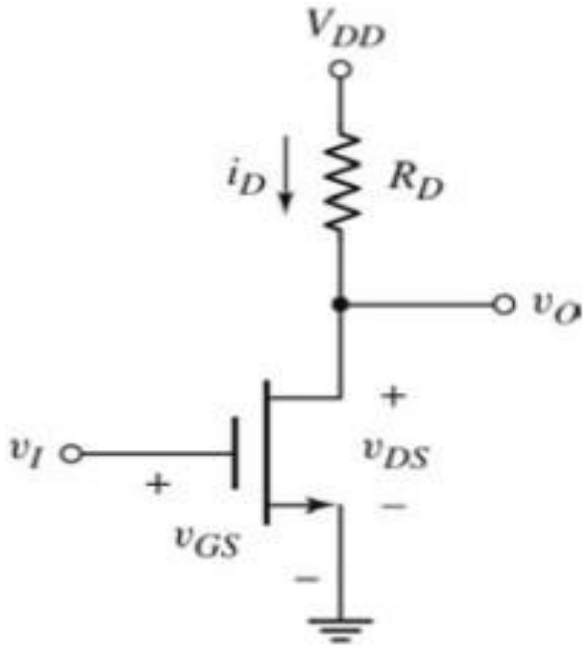
Study the transfer function, Noise margin, effect on risetime, falltime, propagation delay, power and energy consumed of a MOS Inverter for various L, W of the transistor, load capacitance and rise/fall time of input.

Procedure:

Plot the transfer function and transient response; for various combinations of values of Resistance R, L and W of NMOS transistor. Study the effect of variation of R, W/L ratio of pulldown transistor on risetime, fall time, propagation delay, and power consumed. Estimate the value theoretically and verify with simulated result and justify. Identify the region of operation of driver transistor during the transition of the output. Study the variation in IDS of driver transistor, current through load resistance RL; the charge and discharge current through the load capacitance CL with the transition of output.

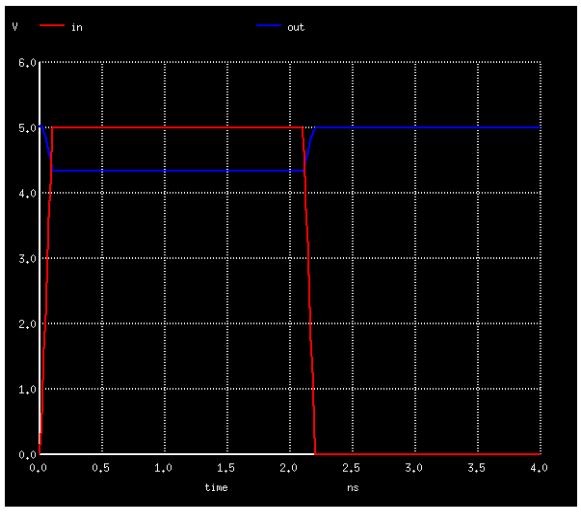
Observations:

Circuit diagram:

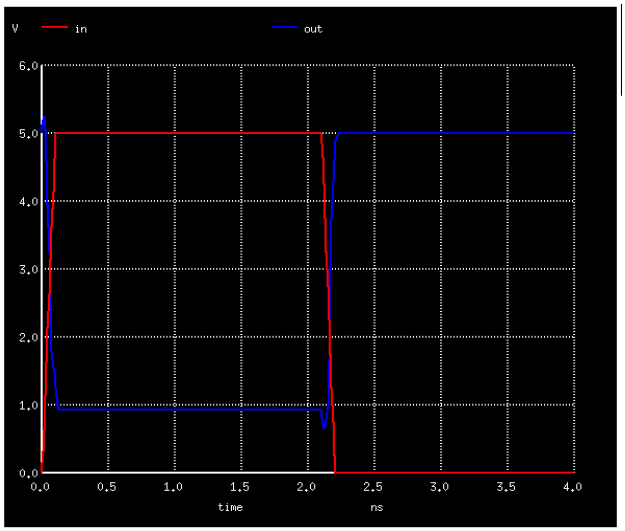


```
* nmos with resistive load
.include ./t14y_tsmc_025_level3.txt
m1 out in vss 0 cmosn l=1u w=1u
r0 out vdd 1k

* power source
v_dd vdd 0 5
v_ss vss 0 0

v_in in 0 5 pulse(0 5 0 0.1n 0.1n 2n 4n)

* .tran 1n 100n

.control
    foreach res 1k 10k 50k
        alter r0=$res
        tran 0.01n 4n
        run
    end
    foreach iter 1 2 3
        setplot tran$iter
        plot in, out
        meas tran vmax MAX out from=0.5ns to=2.5ns
        meas tran vmin MIN out from=0.01ns to=0.5ns

        let V10=Vmin+ ((Vmax-Vmin)*0.1)
        let V50=Vmin+ ((Vmax-Vmin)*0.5)
        let V90=Vmin+ ((Vmax-Vmin)*0.9)

        meas tran trise trig out val=V10 rise=1 targ out val=V90 rise=1
        meas tran tfall trig out val=V90 fall=1 targ out val=V10 fall=1

        meas tran tphl trig in val=V50 rise=1 targ out val=V50 fall=1
        meas tran tplh trig in val=V50 fall=1 targ out val=V50 rise=1

        print V10
        print V50
        print V90
        print trise
        print tfall
        print tphl
        print tplh
    end
.endc
.end
```

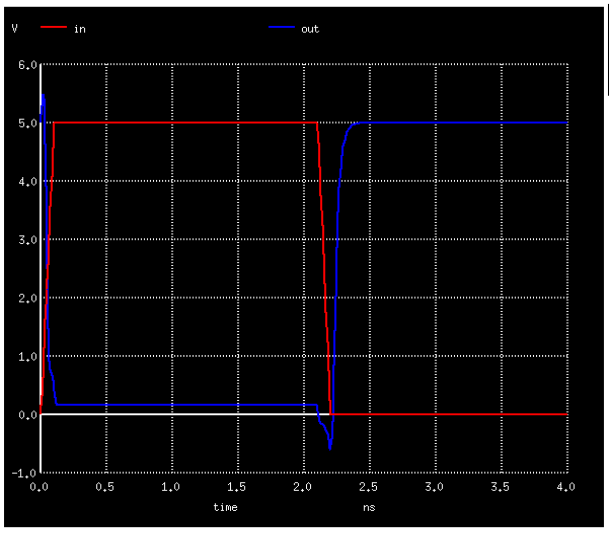
Varying Resistance:



R=1k ohm



R=10k ohm



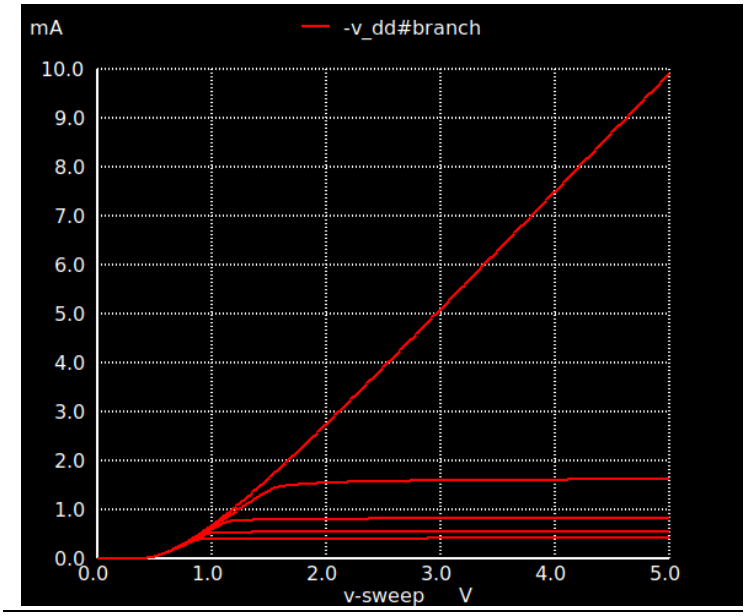
R= 50k ohm

For Varying Resistance:

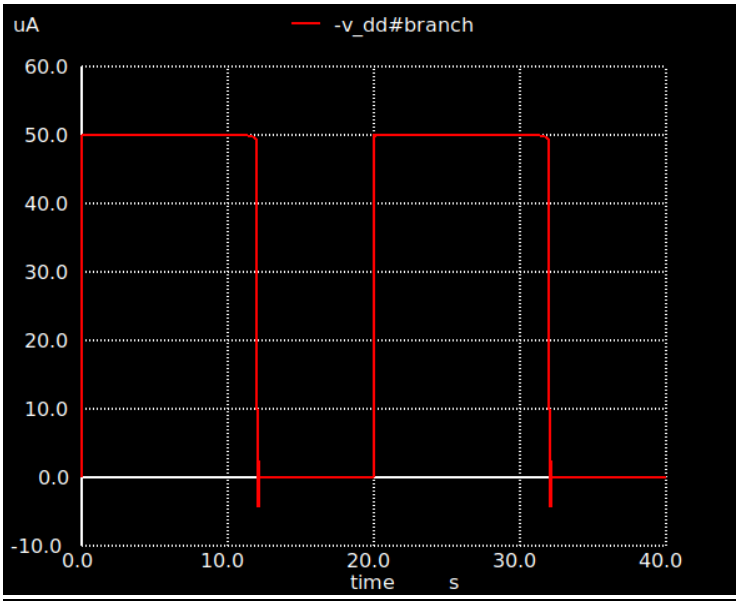
RL(ohm)	Vmax(V)	Vmin(V)	trise(ps)	tfall(ps)	tphl(ps)	tplh(ps)	tp(ps)
1k	5	4.34	69.7	67.9	-27.15	35.9	4.20
10k	5	0.93	66.9	65.4	-2.72	23.8	10.6
50k	4.99	0.17	45.1	49.9	-5.61	93.25	43.8

We observe from the table above that as RL increases, Vmax remains nearly constant and Vmin decreases.

For resistive load, the plot of Id vs Vin:



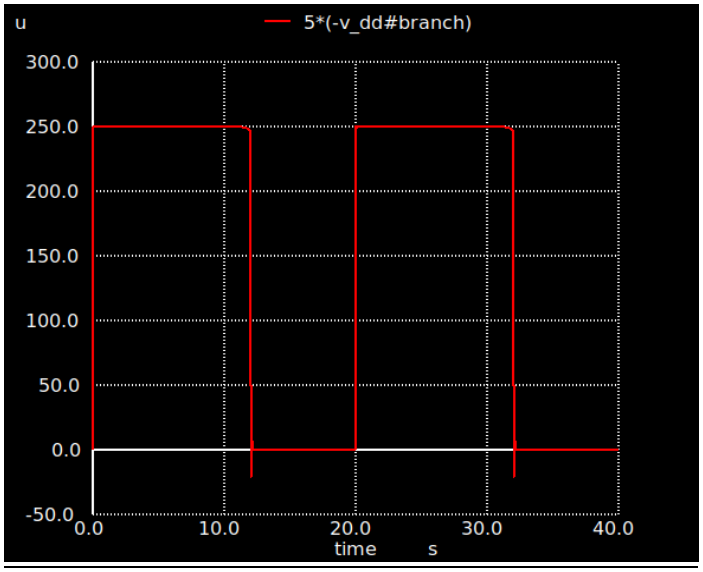
For capacitive load, the plot of Id vs Vin:



Analysis:

Characteristics	Value
Rise Time	1.363408e-01 s
Fall Time	7.425317e-03 s
Propagation Delay	3.895189e-01 s
Energy	4.808058e-04 J

Power plot:



Noise Margin Analysis:

For Resistive Load:

Resistance (ohm)	**1k**	**5k**	**10k**
VOL (V)	2.339	1.990	0.930
VOH (V)	4.995	4.975	4.950

For Capacitive Load:

VOL = 1.564V
VOH = 4.678V

Varying NMOS Width:

Width (in µ)	**0.5**	**2**	**5**
Vol (in V)	2.035	0.4291	0.1627
Voh (in V)	4.95	4.95	4.95
Rise Time (in s)	2.774e-10	2.876e-10	3.280e-10
Fall Time (in s)	2.325e-10	7.809e-11	5.9e11
Propagation Delay (in s)	8.786e-11	8.48e-11	1.038e-10
Average Power (in W)	7.75e-4	1.269e-3	1.4e-3

Regions of Operation inferred from the VTC Curve:

- When the input voltage is set to Vdd, the NMOS is in the linear region.
- When the input voltage is set to logic 0, the NMOS is off.
- Perfect VOH is obtained, VOL is close to 0.

Conclusion:

As Load Resistance increases:
- VTC shifts towards left
- The gain of the transition region in the VTC increases
- VOL decreases as R becomes larger than Resistance offered by nmos.
- Rise time and fall time of transient response decreases.

As W/L ratio increases:
- VTC shifts towards left
- NML decreases and NMH increases
- TPLH increases and TPHL decreases
- The gain of the transition region in the VTC increases
- VOL decreases as Resistance offered by nmos decreases.
- Rise time and fall time of transient response decreases.

Experiment 3: Study of MOS inverter with active load - NMOS and PMOS (pseudo NMOS load)

Objective:

For a MOS Inverter with active load NMOS and PMOS (pseudo NMOS load), study the transfer function, Noise margin, effect on risetime, falltime, propagation delay, power and energy consumed with variation in L and W of the pullup and pulldown transistors. Also power and energy consumed with non-ideal step input.

Procedure:

a) Plot the transfer function and transient response; for various combinations of values of L and W of both driver and load transistors. Study the effect of W/L ratio of pullup and pulldown transistors on risetime, falltime, propagation delay, power consumed. Estimate the value theoretically and verify with simulated result and justify.

b) For an inverter with equal rise and fall time plot the transient response by varying the risetime and falltime of the input. Study the variations in power and energy consumed per transition. Estimate the value theoretically and verify with simulated result and justify.

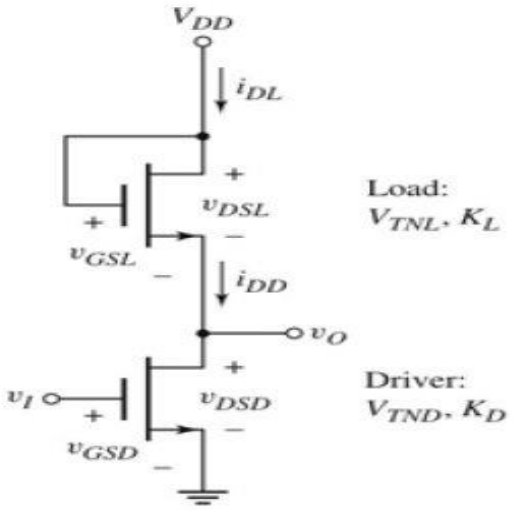
c) Plot the transient response for an inverter with equal rise and fall time with various capacitive loads at the output (i.e. estimate the input capacitance of the inverter and try with different fanout loads.) Prepare a table of risetime, falltime, propagation delay, power consumed for various loads for ideal and non-ideal step inputs.

d) Compute the amount of continuous power and dynamic power dissipated.

Observations:

For NMOS inverter with active load NMOS:

Circuit Diagram:

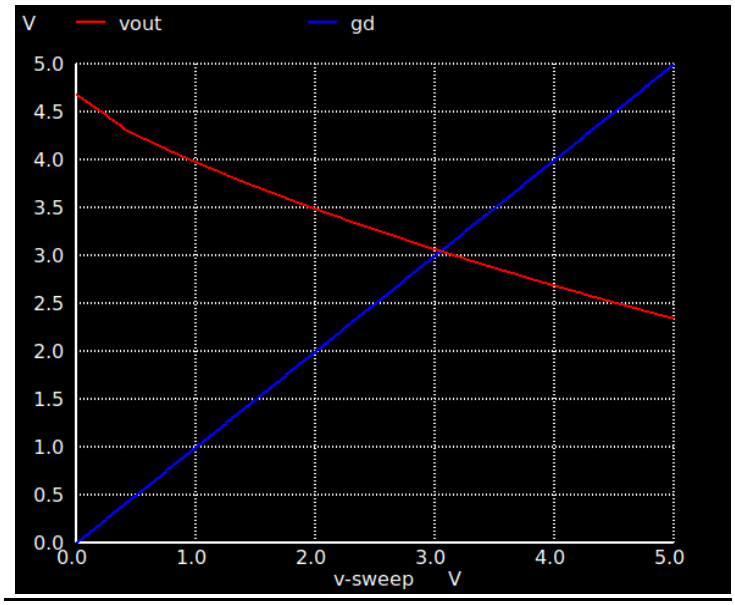


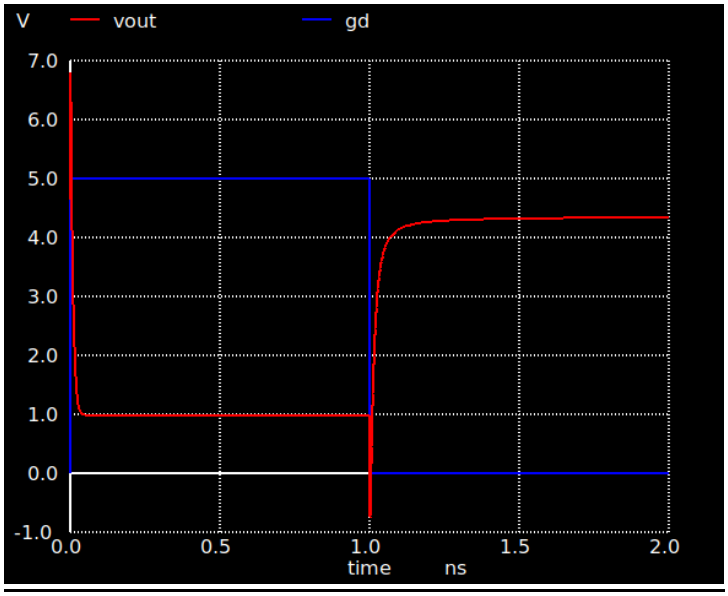
NMOS Load

Code:

```
*NMOS Inverter

.include ./t14y_tsmc_025_level3.txt

m_load sl sl vout 0 cmosn l=0.5u w=25u
m_driver vout gd 0 0 cmosn l=0.5u w=10u

v_dd sl 0 5
v_test vtest vout 0
v_in gd 0 PULSE(0 5 0 0 0 1n 2n)

.control
   dc v_in 0 5 0.01
   setplot dc1
   plot vout gd

        tran 0.01ns 4ns
        setplot tran1
        plot vout gd
        plot -5*v_dd#branch

.endc

.end
```

Plots:





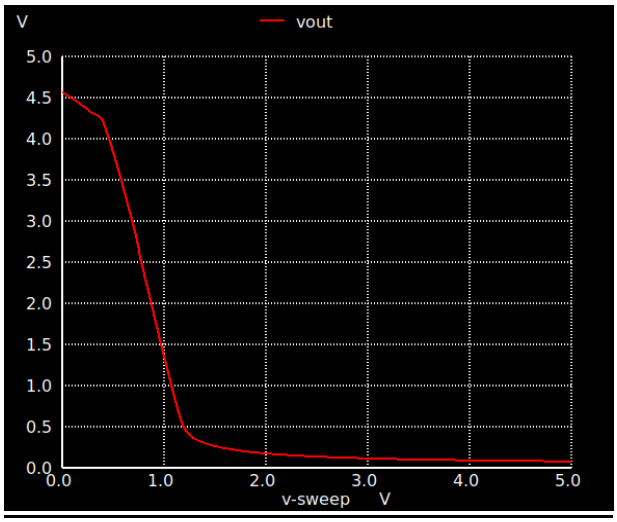
Code varying length, width and calculating various parameters:

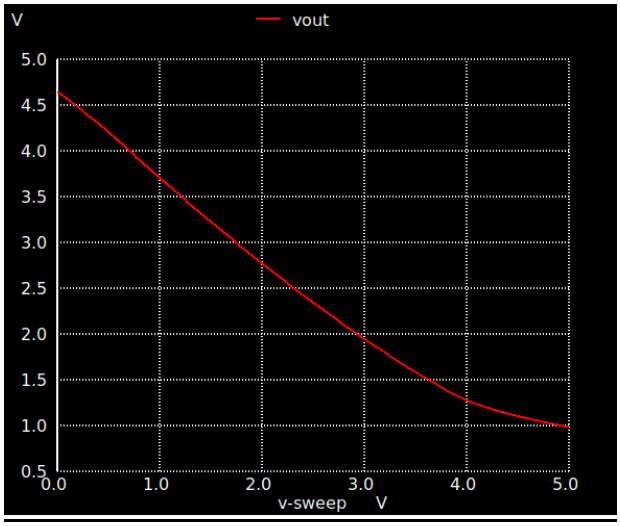
```
*NMOS Inverter
.include ./t14y_tsmc_025_level3.txt

m_load sl sl vout 0 cmosn l=0.5u w=25u
m_driver vout gd 0 0 cmosn l=0.5u w=10u

v_dd sl 0 5
v_test vtest vout 0
v_in gd 0 PULSE(0 5 0 0 0 1n 2n)

.control
	foreach width 1u 10u 100u
		alter @m_load[w] = $width
		dc v_in 0 5 0.01
	end
	foreach width 1u 10u 100u
		alter @m_driver[w] = $width
		dc v_in 0 5 0.01
	end
	foreach length 1u 10u 100u
		alter @m_load[l] = $length
		dc v_in 0 5 0.01
	end
	foreach length 1u 10u 100u
		alter @m_driver[l] = $length
		dc v_in 0 5 0.01
	end
	foreach iter 1 2 3 4 5 6 7 8 9 10 11 12
		setplot dc$iter
		plot vout
```

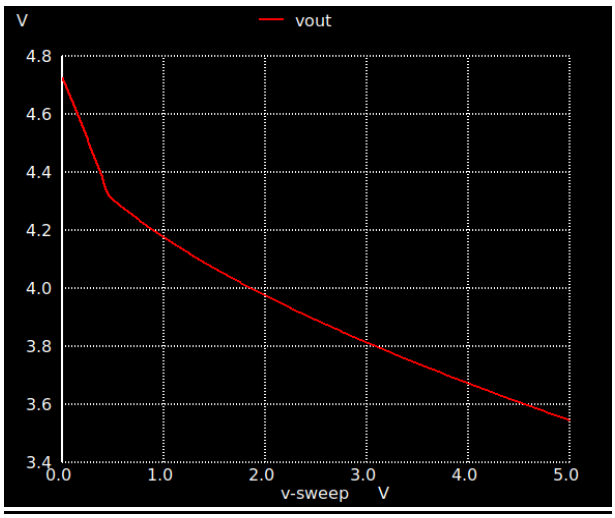
```
            hardcopy img/plot2_$iter vout
        end
        alter @m_load[l] = 0.5u
        alter @m_load[w] = 10u
        alter @m_driver[l] = 0.5u
        alter @m_driver[w] = 10u

        tran 1p 2n
        setplot tran12
        plot vout, gd
        plot 5*v_test#branch

        meas tran Vmax MAX vout from=0.01n to=4n
        meas tran Vmin MIN vout from=0.01n to=4n

    let v10 = Vmin + 0.1*(Vmax - Vmin)
    let v50 = Vmin + 0.5*(Vmax - Vmin)
    let v90 = Vmin + 0.9*(Vmax - Vmin)
    print v10, v50, v90

    meas tran trise trig vout val=v10 rise=1 targ vout val=v90 rise=1
    print trise
    meas tran tfall trig vout val=v90 fall=1 targ vout val=v10 fall=1
    print tfall

    meas tran tphl trig gd val=2.5 rise=1 targ vout val=v50 fall=1
    meas tran tplh trig gd val=2.5 fall=1 targ vout val=v50 rise=1
    print tphl
    print tplh
    let tp = (tphl+tplh)/2
    print tp

.endc
.end
```

Plots:

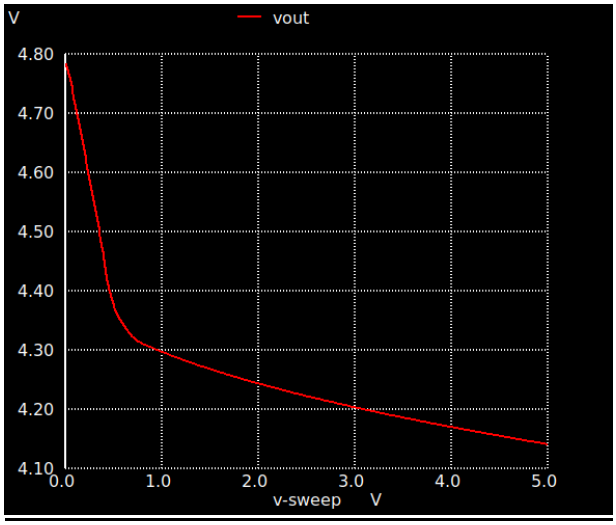
Varying width of load:

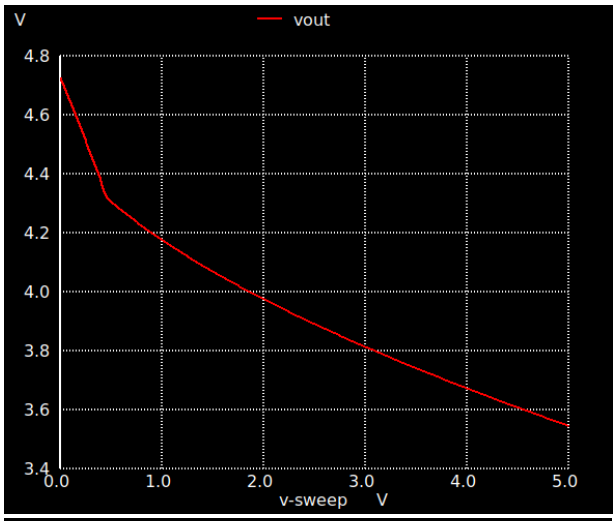


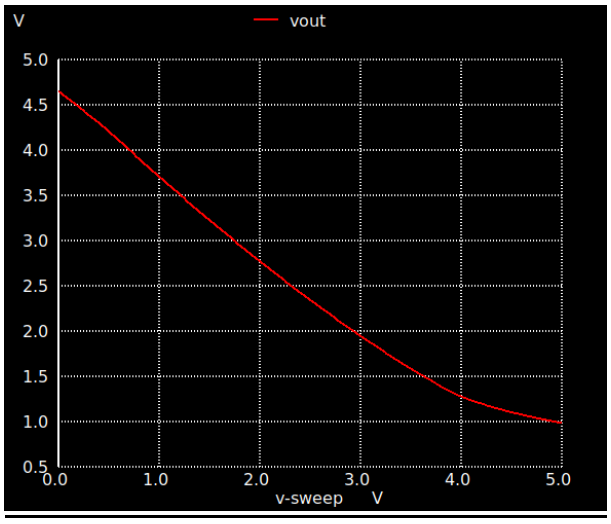




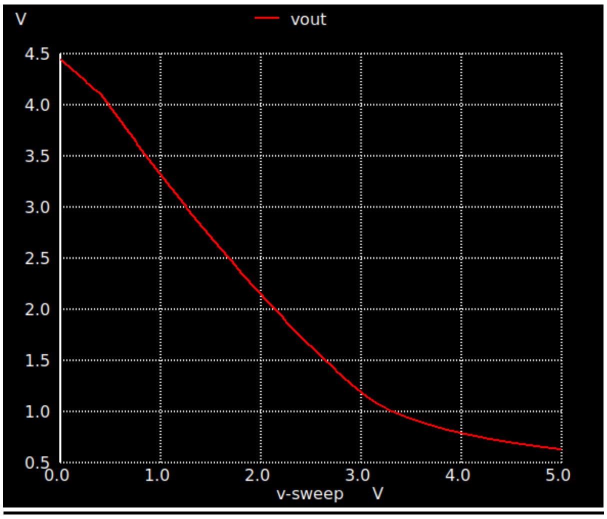
Varying width of driver:

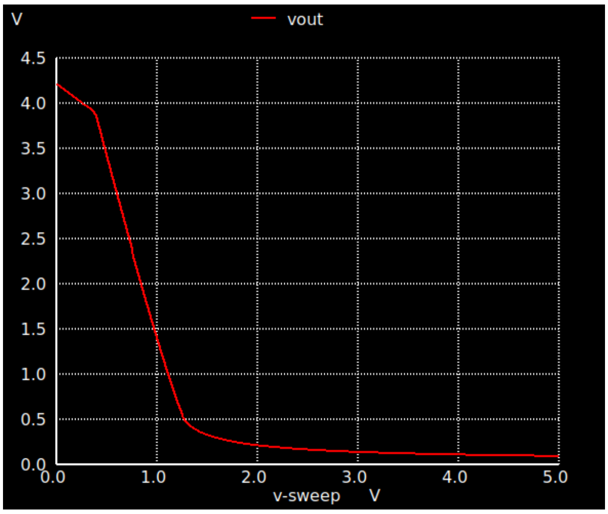


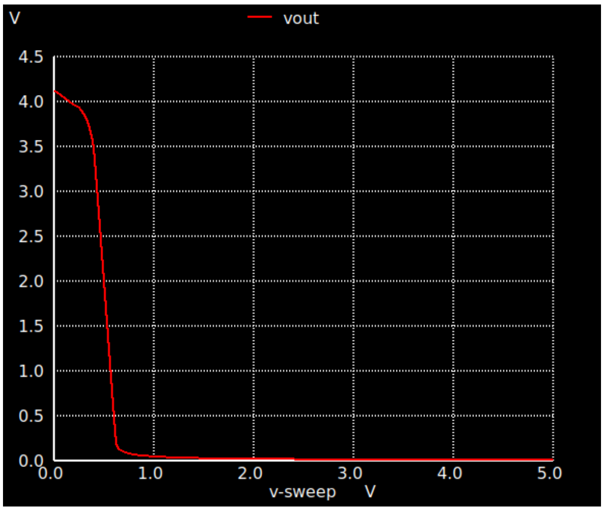




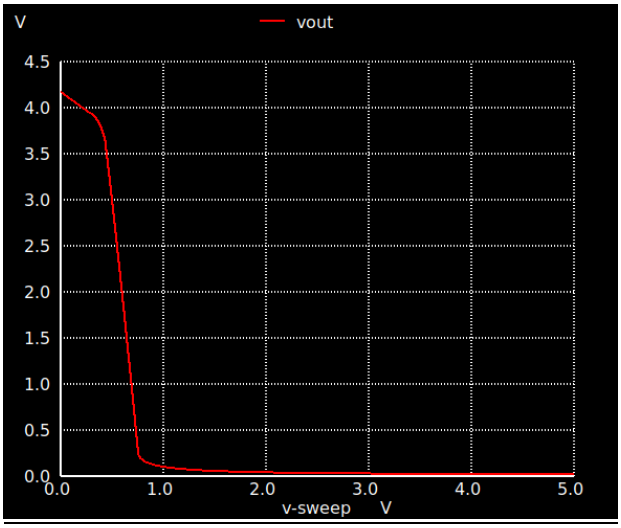
Varying length of load:

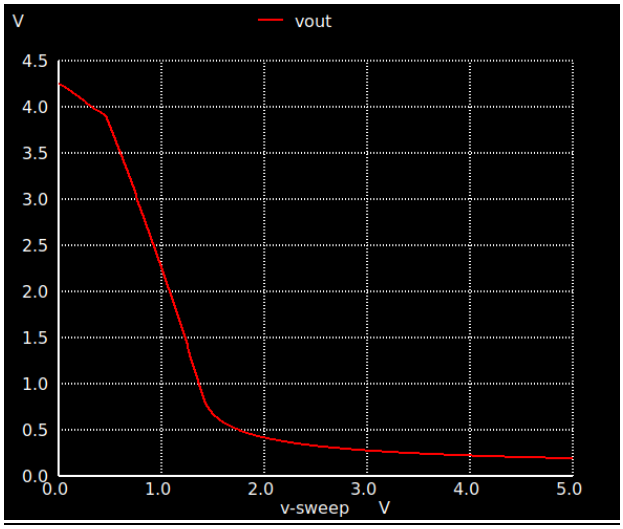


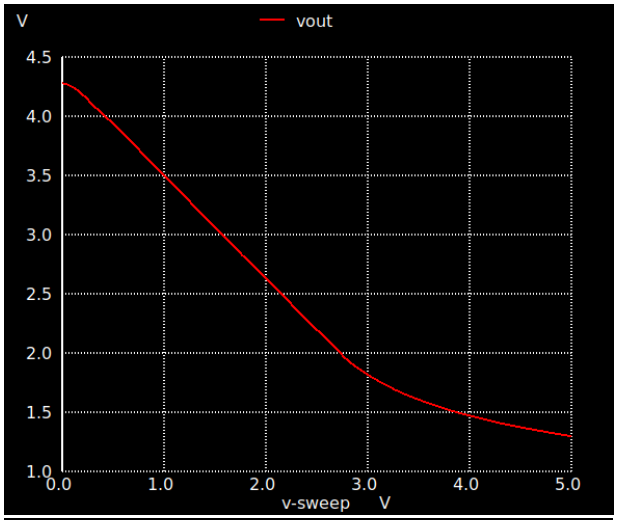




Varying length of the driver:



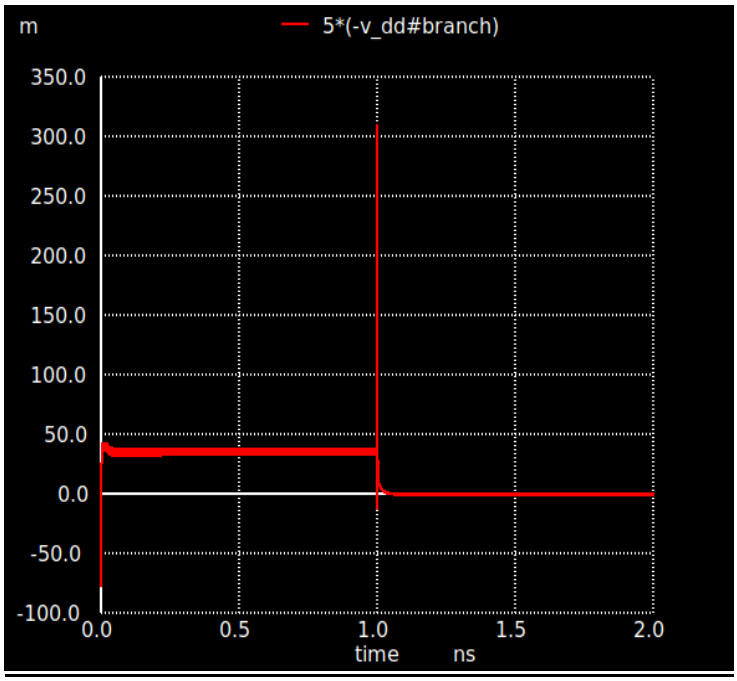




Analysis:

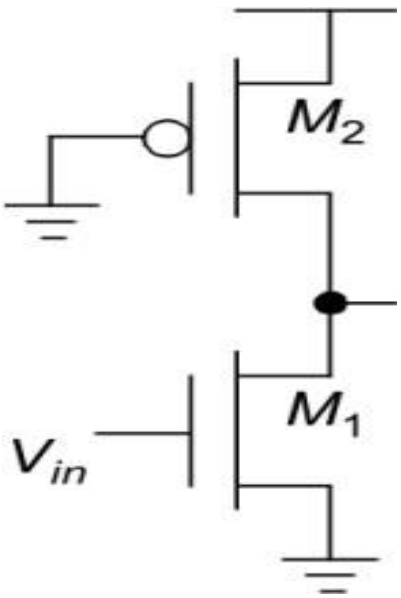
Characteristics	**Value**
Rise Time	4.797626e-11 s
Fall Time	9.955073e-10 s
Propagation Delay	1.401907e-11 s
Energy	5.092565e-13 J

Power plot:



For NMOS inverter with pseudo NMOS (PMOS) load:

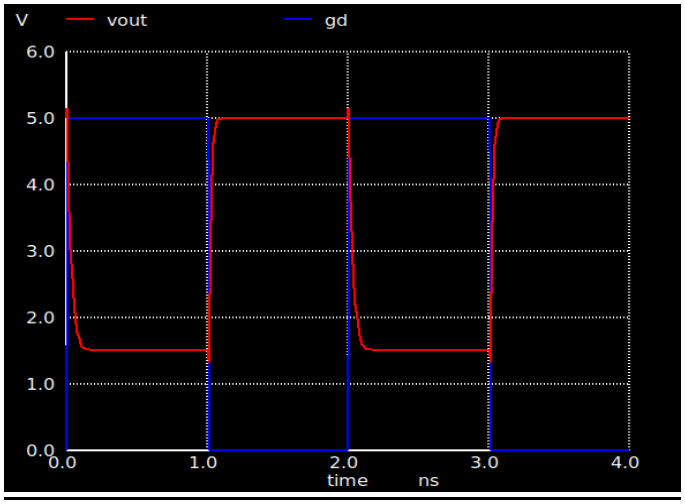
Circuit Diagram:

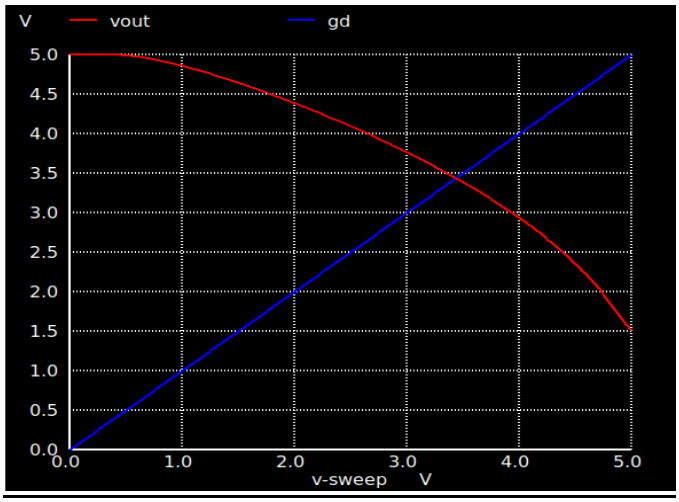


Code:

```
*NMOS Inverter

.include ./t14y_tsmc_025_level3.txt

m_load vtest 0 sl sl cmosp l=0.5u w=25u
m_driver vout gd 0 0 cmosn l=0.5u w=10u

v_dd sl 0 5
v_test vtest vout 0
v_in gd 0 PULSE(0 5 0 0 0 1n 2n)

.control
   dc v_in 0 5 0.01
   setplot dc1
   plot vout gd

        tran 0.01ns 4ns
        setplot tran1
        plot vout gd
        plot -5*v_dd#branch
.endc
.end
```

Plots:





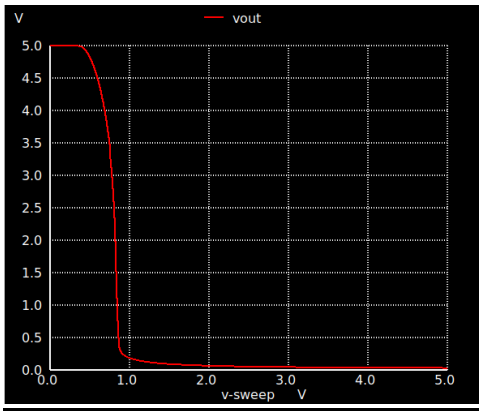
Code varying length, width and calculating various parameters:

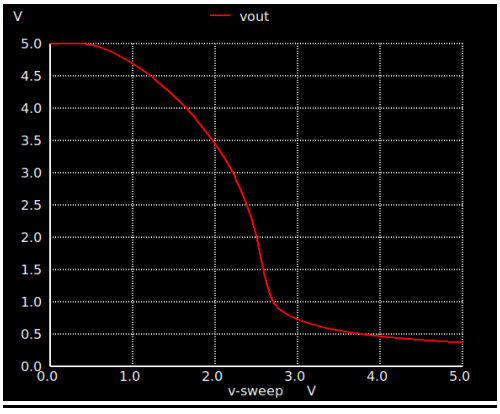
```
*NMOS Inverter
.include ./t14y_tsmc_025_level3.txt

m_load sl sl vout 0 cmosn l=0.5u w=25u
m_driver vout gd 0 0 cmosn l=0.5u w=10u

v_dd sl 0 5
v_test vtest vout 0
v_in gd 0 PULSE(0 5 0 0 0 1n 2n)

.control
	foreach width 1u 10u 100u
		alter @m_load[w] = $width
		dc v_in 0 5 0.01
	end
	foreach width 1u 10u 100u
		alter @m_driver[w] = $width
		dc v_in 0 5 0.01
	end
	foreach length 1u 10u 100u
		alter @m_load[l] = $length
		dc v_in 0 5 0.01
	end
	foreach length 1u 10u 100u
		alter @m_driver[l] = $length
		dc v_in 0 5 0.01
	end
	foreach iter 1 2 3 4 5 6 7 8 9 10 11 12
		setplot dc$iter
		plot vout
		hardcopy img/plot2_$iter vout
	end
	alter @m_load[l] = 0.5u
	alter @m_load[w] = 10u
	alter @m_driver[l] = 0.5u
	alter @m_driver[w] = 10u

	tran 1p 2n
	setplot tran12
	plot vout, gd
	plot 5*v_test#branch

	meas tran Vmax MAX vout from=0.01n to=4n
	meas tran Vmin MIN vout from=0.01n to=4n
```

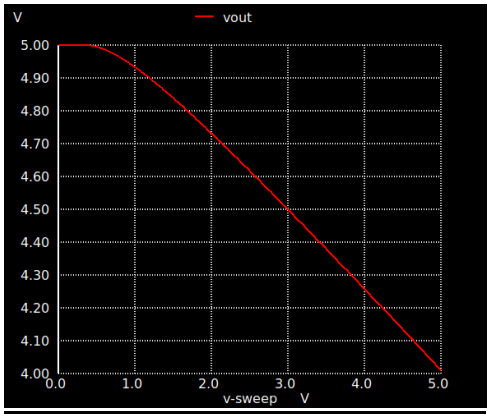
```
    let v10 = Vmin + 0.1*(Vmax - Vmin)
    let v50 = Vmin + 0.5*(Vmax - Vmin)
    let v90 = Vmin + 0.9*(Vmax - Vmin)
    print v10, v50, v90

    meas tran trise trig vout val=v10 rise=1 targ vout val=v90 rise=1
    print trise
    meas tran tfall trig vout val=v90 fall=1 targ vout val=v10 fall=1
    print tfall

    meas tran tphl trig gd val=2.5 rise=1 targ vout val=v50 fall=1
    meas tran tplh trig gd val=2.5 fall=1 targ vout val=v50   rise=1
    print tphl
    print tplh
    let tp = (tphl+tplh)/2
    print tp
.endc
.end
```

Plots:

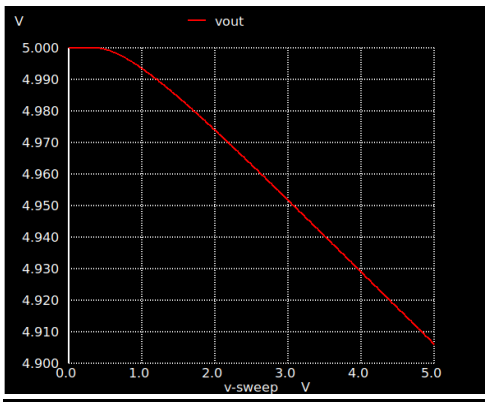
Varying width of load:

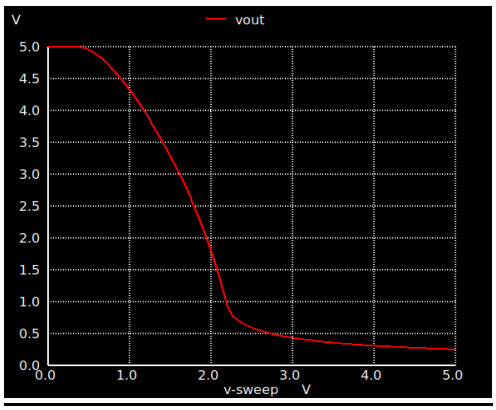


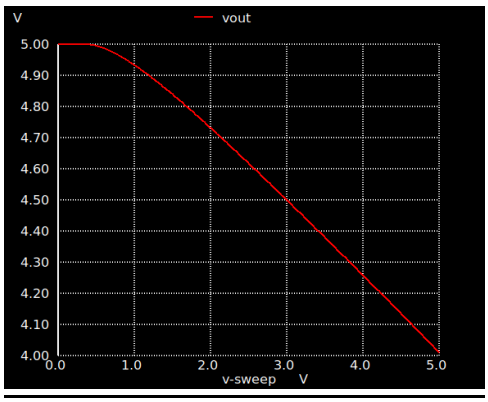




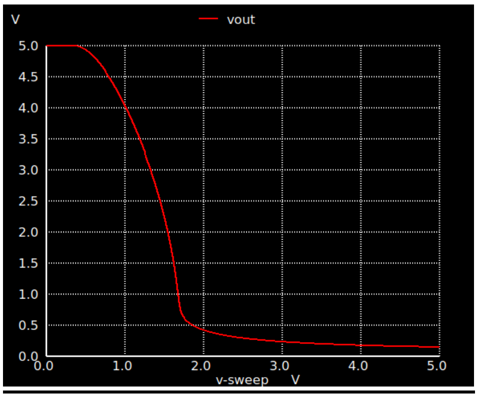
Varying width of the driver:

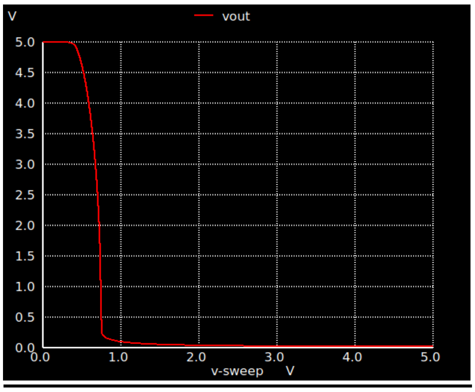


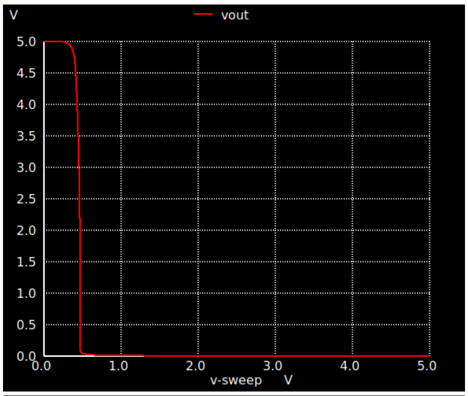




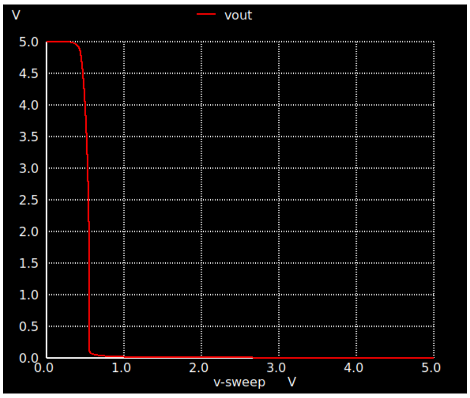
Varying length of load:

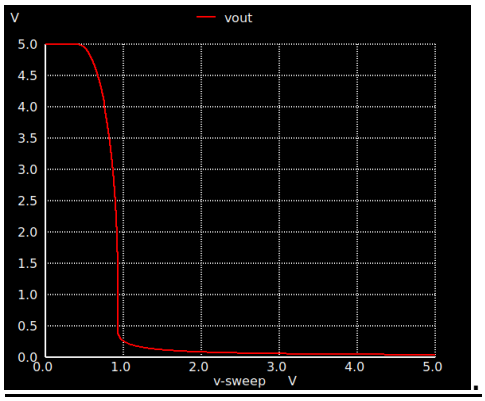


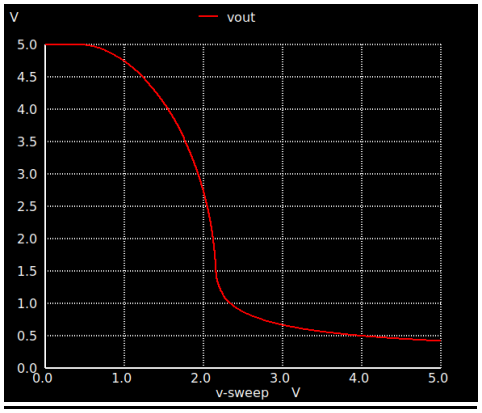




Varying length of driver:



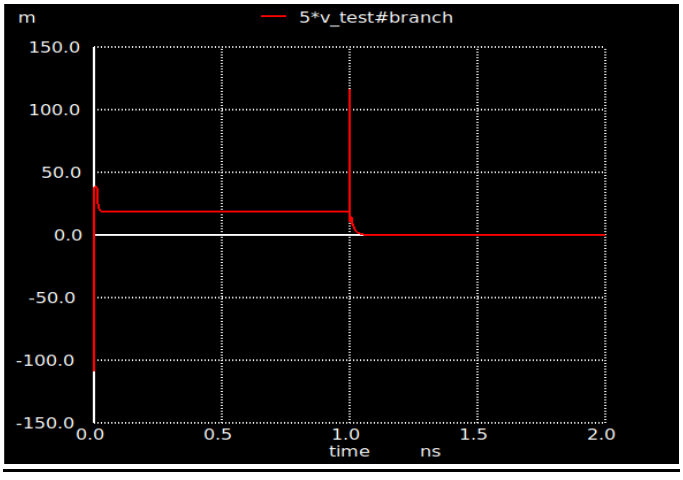




Analysis:

Characteristics	**Value**
Rise Time	2.992617e-11 s
Fall Time	9.969917e-10 s
Propagation Delay	1.226702e-11 s
Energy	1.908499e-11 J

Power plot:



Theory:

In this experiment, we replace the passive resistor used in the pull up network in experiment 2 with an active nmos load and pseudo nmos load (PMOS).
In NMOS with active NMOS load, the NMOS in the PUN is always on and is in saturation region. When the input is low, the bottom NMOS is off, hence there is no current in the circuit. When the input is high, both the transistors fight to pull down the output. VOL and VOH are not perfect here.
Next, we replace the active NMOS load with a pseudo NMOS load i.e. a PMOS whose gate is grounded.
Since we have grounded the gate of the PMOS, it is always on. Based on the input the output would be pulled up or pulled down.

Conclusion:

As W/L of NMOS increases:
- VTC shifts towards left
- TPLH increases and TPHL decreases
- The gain of the transition region in the VTC increases.
- VOL decreases as R becomes smaller than Resistance offered by pmos.
- Rise/Fall time reduces.
- NML decreases and NMH increases

As W/L of PMOS LOAD decreases:
- VTC shifts towards left
- NML decreases and NMH increases
- TPLH increases and TPHL decreases
- Rise/Fall time reduces.
- VOL decreases as Resistance offered by pmos increases.
- The gain of the transition region in the VTC increases

Experiment 4: Study of CMOS inverter

Objective:

Study the transfer function, Noise margin, effect on risetime, falltime, propagation delay. power and energy consumed of a CMOS Inverter with variation in L. and W of the pullup and pulldown transistors. Also power and energy consumed with non ideal step input.

Procedure:

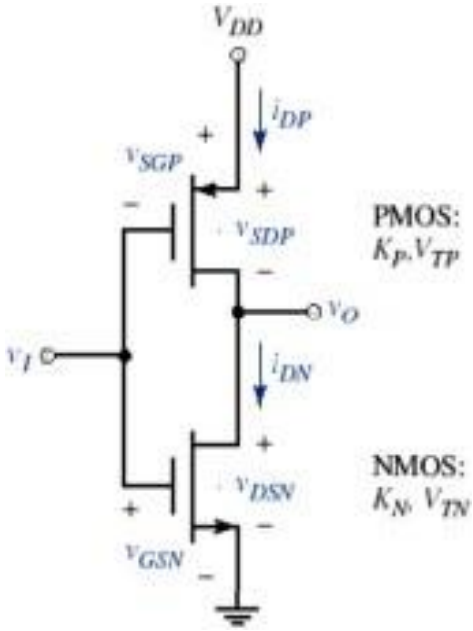
a) Plot the transfer function and transient response; for various combinations of values of L and W of both NMOS and PMOS transistors. Study the effect of W/L ratio of pullup and pulldown transistors on risetime, falltime, propagation delay, power consumed. Estimate the value theoretically and verify with simulated result and justify.

b) Plot the transient response for an ideal CMOS inverter with equal rise and fall time by varying the risetime and falltime of the input. Study the variations in power and energy consumed per transition. Estimate the value theoretically and verify with simulated result and justify.

c) Plot the transient response for an ideal CMOS inverter with equal rise and fall time with various capacitive loads at the output (i.e. estimate the input capacitance of the inverter and try with different fanout loads.) Prepare a table of risetime, falltime, propagation delay, power consumed for various loads for ideal and non-ideal step inputs.

Observations:

Circuit Diagram:



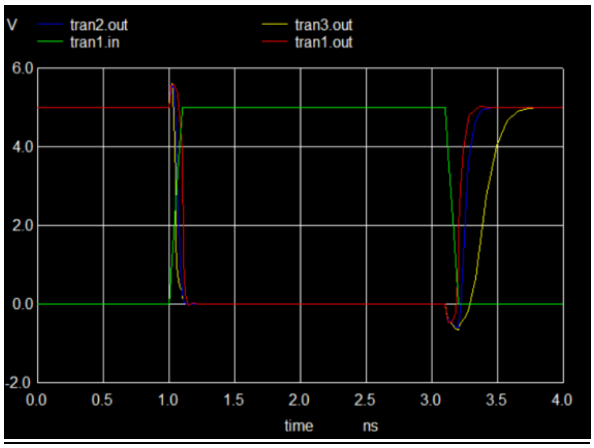
i) Effect of W/L ratio on output of CMOS inverter

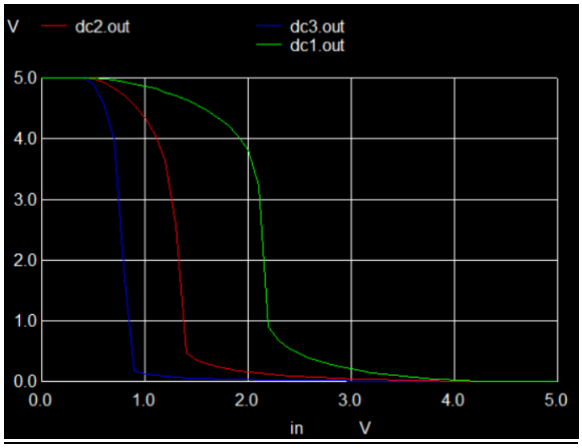
Code:

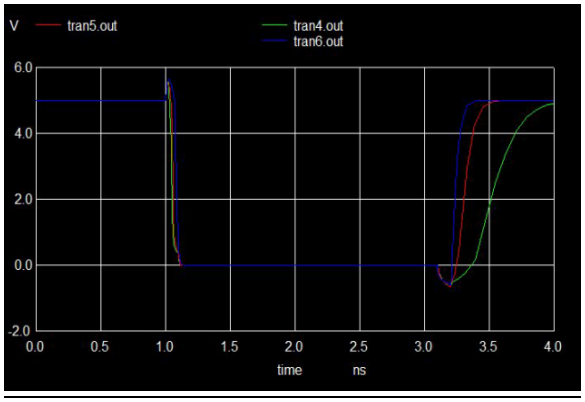
```
.include ./t14y_tsmc_025_level3.txt

mp out in vdd vdd cmosp l=1u w=0.5u
mn out in 0 0 cmosn l=1u w=0.5u
v_dd vdd 0 dc 5
vin in 0 dc 2.5 pulse(0 5 1n 0.1n 0.1n 2n 4n)

*varying width of pdn
.control
foreach wid 0.25u 1u 5u
alter mn w = $wid
run
tran 0.1ns 4n
dc vin 0 5 0.1
end
.endc

.control
foreach iter 1 2 3
setplot dc$iter
setplot tran$iter
.endc

*plotting the output
.control
plot
tran1.in tran1.out tran2.out tran3.out
plot
dc1.out dc2.out dc3.out vs in
.endc

*varying width of pun
.control
foreach wid 0.25u 1u 5u
alter mp w = $wid
run
tran 0.1ns 4n
dc vin 0 5 0.1
end
.endc

.control
foreach iter 4 5 6
setplot dc$iter
```

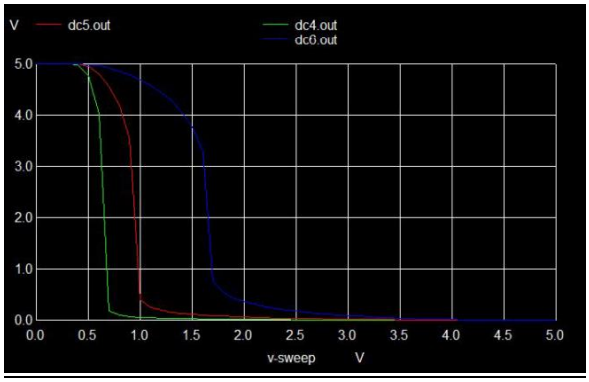
```
setplot trans$iter
.endc

*plotting the output
.control
plot
tran4.out tran5.out tran6.out
plot
dc4.out dc5.out dc6.out vs in
.endc
.end
```

Plots:







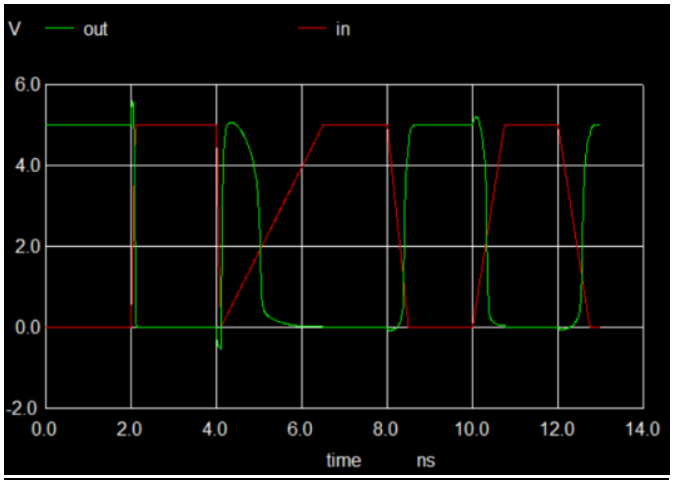


ii) Risetime and Falltime

Code:

```
.include ./t14y_tsmc_025_level3.txt
m1 out in 0 0 cmosn w=0.5u l=1u
m2 out in vdd vdd cmosp w=0.5u l=1u
v_dd vdd 0 dc 5
vin in 0 pwl(0 0 2n 0 2.1n 5 4n 5 4.1n 0 6.5n 5 8n 5 8.5n 0 10n 0 10.75n 5 12n 5 12.75n 0)
.control
tran 0.01ns 13n
run
plot out in
end
.endc
```

Plots:

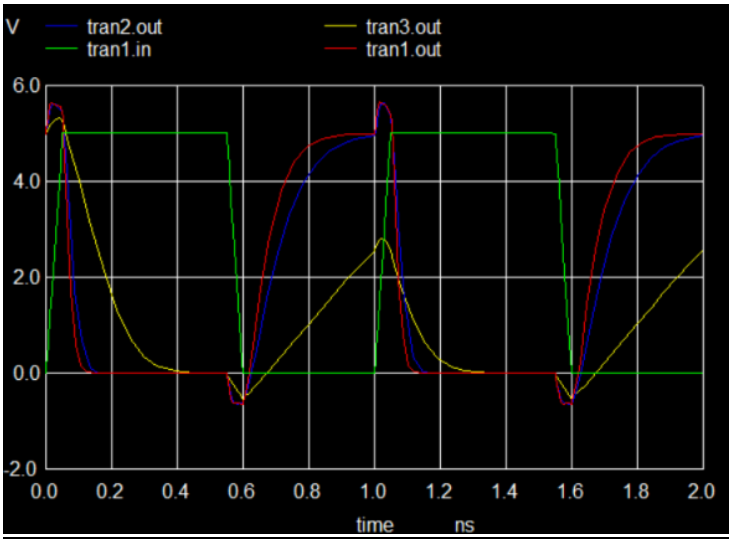


iii) Behaviour of varying load capacitance

Code:

```
.include ./t14y_tsmc_025_level3.txt
m1 out in 0 0 cmosn w=2u l=1u
m2 out in vdd vdd cmosp w=2u l=1u
c1 out 0 1u
v_dd vdd 0 dc 5
vin in 0 pulse(0 5 0 0.05n 0.05n 0.5n 1n)

.control
foreach cap 0.005p 0.01p 0.05p
alter c1=$cap
tran 0.1ns 2n
run
end
.endc
.control
plot
tran1.in tran1.out tran2.out tran3.out
.endc
.end
```

Plot:



Analysis:

Characteristics	Value
Rise Time	2.963833e-11 s
Fall Time	9.973074e-10 s
Propagation Delay	1.001395e-11 s
Energy	1.317490e-12 J

Regions of Operation inferred from the VTC Curve

- When the input voltage is less than VTN, the NMOS is off and the PMOS is in linear region.
- Beyond VTN and before an intermediate value, NMOS is in saturation and PMOS is in linear region.
- On increasing Vin further, both the NMOS and PMOS enter saturation.
- After thus, NMOS enters linear region and PMOS stays in saturation.
- Beyond VTP, PMOS turns off and NMOS stays in linear region.

Conclusion:

- CMOS inverters are better than NMOS, PMOS, and resistor load based inverter.
- V_{OH} is equal to VDD in CMOS inverter.
- Rise time can be made equal to fall time.
- At Vin=VDD/2, Vout=VDD/2

Experiment 5: Study of CMOS gates

Objective:

Study the behavior transfer function, Noise margin, effect on risetime, falltime, propagation delay, power and energy consumed of CMOS gates like Nand, Nor, functions like AOI (2 input AND gate, 2 input OR gate), and 2 input XOR gate with variation in L and W of the pullup and pulldown transistors. Also, power and energy consumed with non-ideal step input. Study the effect of VSB due to series connected transistors.

Procedure:

Similar to CMOS inverter experiment. Test with different input combinations and check the change in rise-time, falltime etc with test patterns.

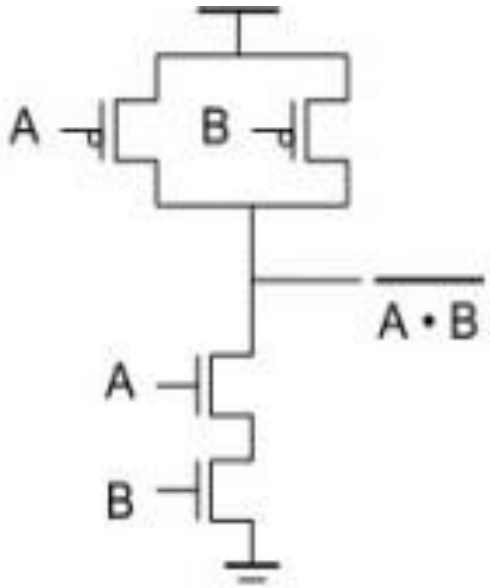
To study the effect of VSB due to series connected transistors:

- connect the substrate of all NMOS to GND and all PMOS to VDD, simulate the circuit.
- connect the source of each transistor to substrate contact of respective transistor, and simulate.
- The first simulation gives you effect of Vsb on series connected transistors.
- Plot the switching waveforms at different nodes and compare.

Observations:

NAND:

Circuit diagram:

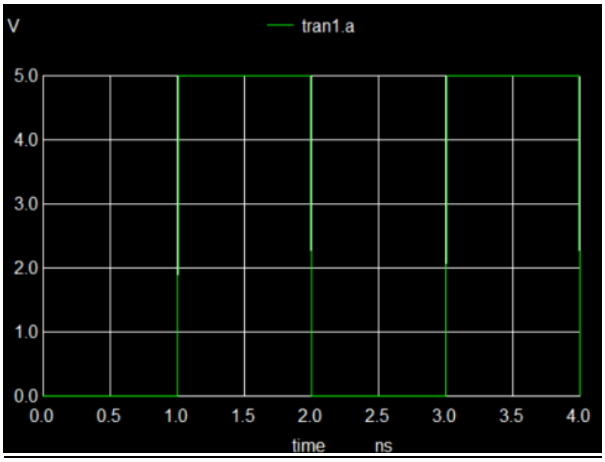


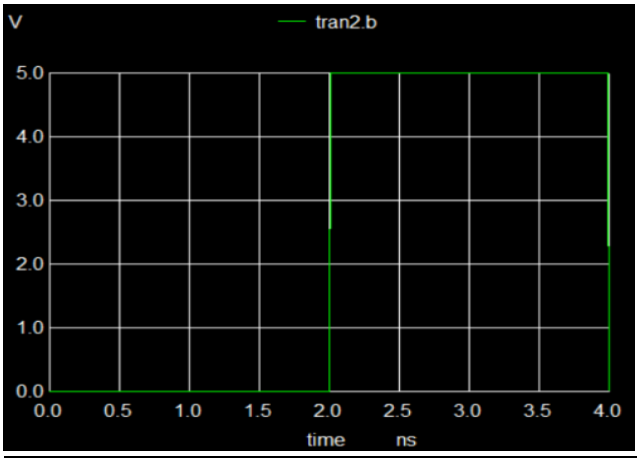
Varying Width of PDN Transistor:

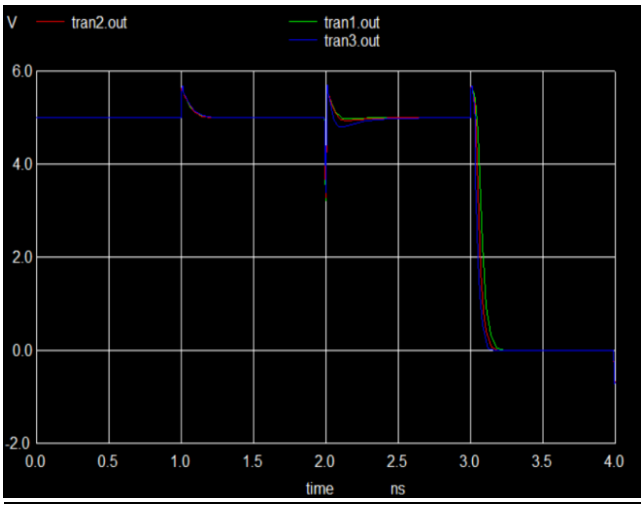
Code:

```
.include ./t14y_tsmc_025_level3.txt
mpa out a vdd vdd cmosp w=2u l=1u
mpb out b vdd vdd cmosp w=2u l=1u
mna x a 0 0 cmosn w=1u l=1u
mnb out b x 0 cmosn w=1u l=1u
va a 0 5 pwl(0n 0 1n 0 1.01n 5 1.99n 5 2n 0 3n 0 3.01n 5 2.99n 5 4n 0) r=0
vb b 0 5 pwl(0n 0 2n 0 2.01n 5 3.99n 5 5 4n 0) r=0
v_dd vdd 0 5

.control
foreach wid 1u 2u 5u
alter mna w=$wid
alter mnb w=$wid
tran 0.1n 4n
end
.endc

.control
foreach iter 1 2 3
setplot tran$iter
end
.endc

.control
plot tran1.a
plot tran2.b
plot tran1.out tran2.out tran3.out
.endc
.end
```

Plots:







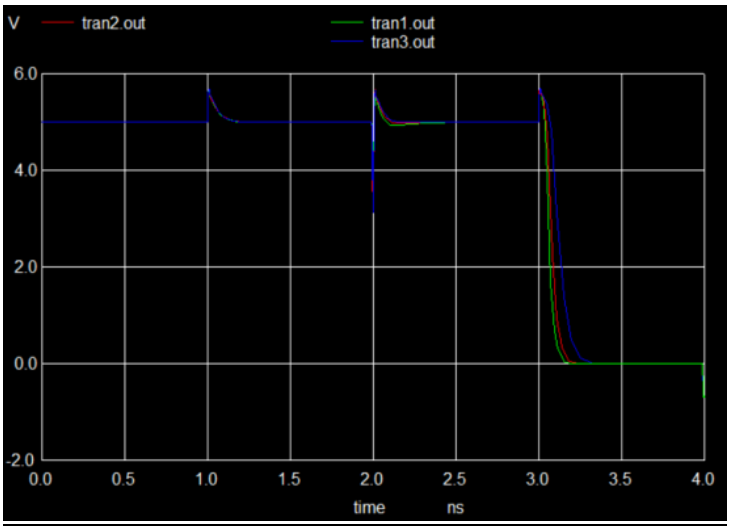
Varying Width of PUN Transistor:

Code:

```
.include ./t14y_tsmc_025_level3.txt
mpa out a vdd vdd cmosp w=2u l=1u
mpb out b vdd vdd cmosp w=2u l=1u
mna x a 0 0 cmosn w=1u l=1u
mnb out b x 0 cmosn w=1u l=1u
va a 0 5 pwl(0 0 1n 0 1.01n 5 1.99n 5 2n 0 3n 0 3.01n 5 3.99n 5 4n 0) r=0
vb b 0 5 pwl(0 0 2n 0 2.01n 5 3.99n 5 4n 0) r=0
v_dd vdd 0 5

.control
foreach wid 1u 2u 5u
alter mpa w=$wid
alter mpb w=$wid
tran 0.1ns 4n
end
.endc

.control
```

```
foreach iter 1 2 3
setplot tran$iter
end
.endc

.control
plot tran1.out tran2.out tran3.out
.endc
.end
```

Plots:

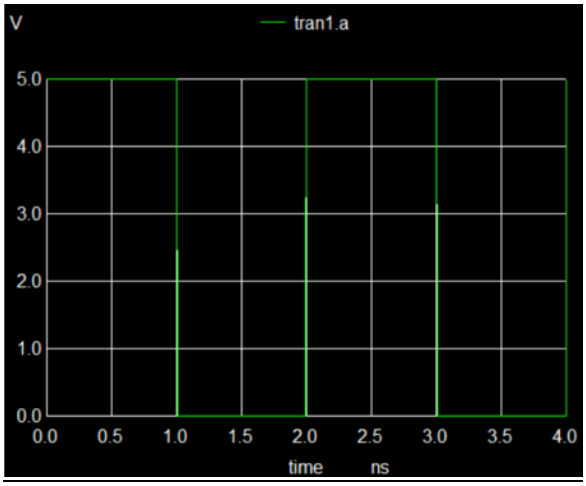


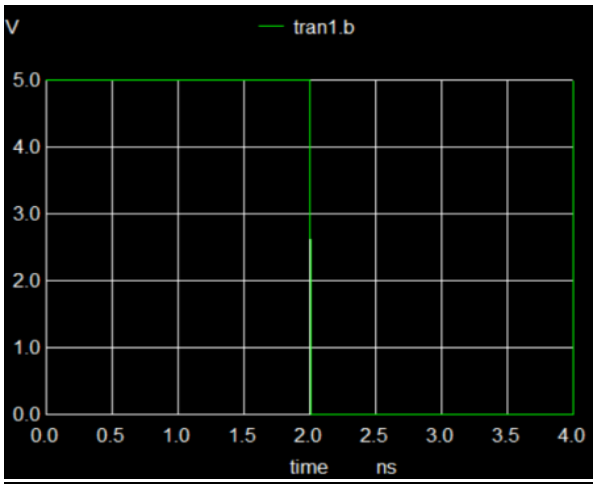
Varying input sequence:

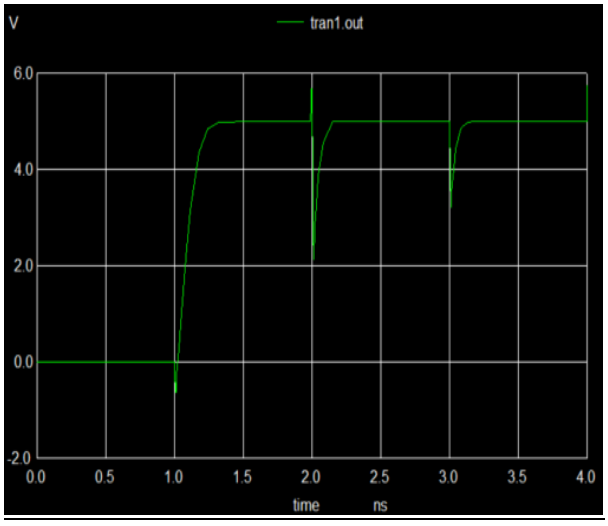
Code:

```
.include ./t14y_tsmc_025_level3.txt
mpa out a vdd vdd cmosp w=2u l=1u
mpb out b vdd vdd cmosp w=2u l=1u
mna x a 0 0 cmosn w=1u l=1u
mnb out b x 0 cmosn w=1u l=1u
va a 0 5 pwl(0 5 1n 5 1.01n 0 1.99n 0 2n 5 3n 5 3.01n 0 3.99n 0 4n 0) r=0
vb b 0 5 pwl(0 5 2n 5 2.01n 0 3.99n 0 4n 0) r=0
v_dd vdd 0 5

.tran 0.1n 4n

.control
run
.endc

.control
plot tran1.a tran1.b tran1.out
.endc
.end
```

Plots:



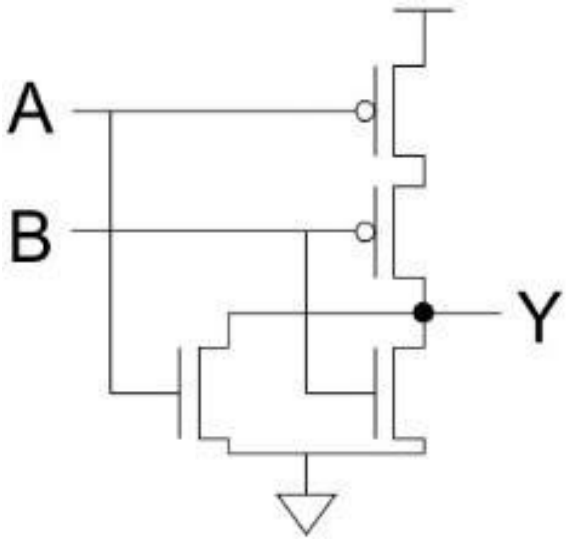




As we increase the width of the PDN transistors, the fall time reduces and hence the transition time also reduces. As the width of the PUN transistors increase, fall time increases. The transition time also depends on the input sequence given to the circuit. And also there are some fluctuations in the output voltage when there are transitions in the input voltage.

NOR:

Circuit diagram:

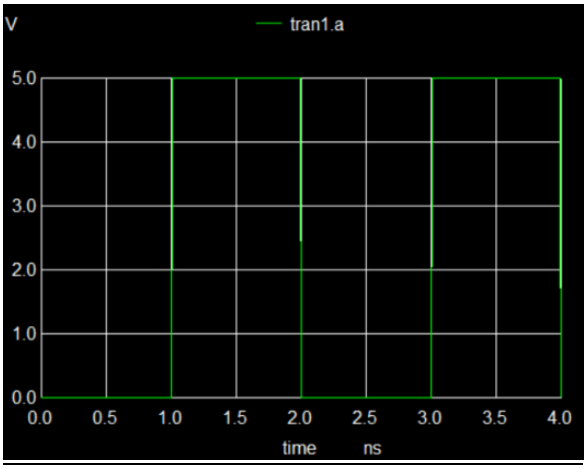


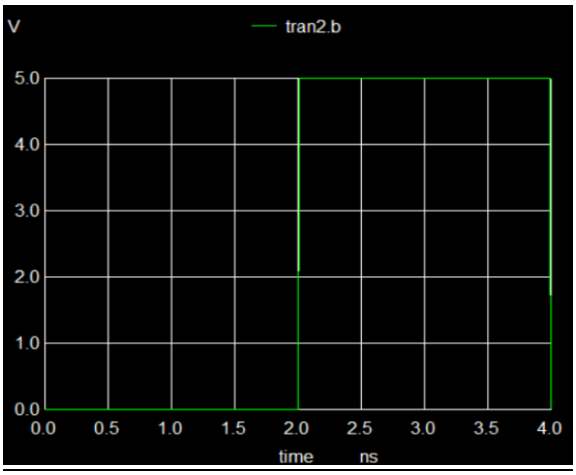
Varying Width of PDN Transistors:

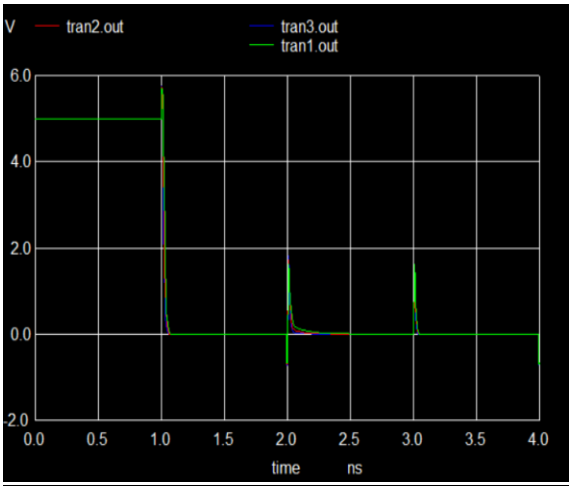
Code:

```
.include ./t14y_tsmc_025_level3.txt
mpa out a x vdd cmosp w=2u l=1u
mpb x b vdd vdd cmosp w=2u l=1u
mna out a 0 0 cmosn w=1u l=1u
mnb out b 0 0 cmosn w=1u l=1u
va a 0 5 pwl(0 0 1n 0 1.01n 5 1.99n 5 2n 0 3n 0 3.01n 5 3.99n 5 4n 0)r=0
vb b 0 5 pwl(0 0 2n 0 2.01n 5 3.99n 5 4n 0)r=0
v_dd vdd 0 5

.control
foreach wid 1u 2u 5u
alter mna w=$wid
alter mnb w=$wid
tran 0.1ns 4n
end
.endc

.control
foreach iter 1 2 3
setplot tran$iter
end
.endc

.control
plot tran1.a
plot tran2.b
plot tran1.out tran2.out tran3.out
.endc
.end
```

Plots:


V
tran1.a
5.0
4.0
3.0
2.0
1.0
0.0
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0
time ns


V
tran2.b
5.0
4.0
3.0
2.0
1.0
0.0
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0
time ns

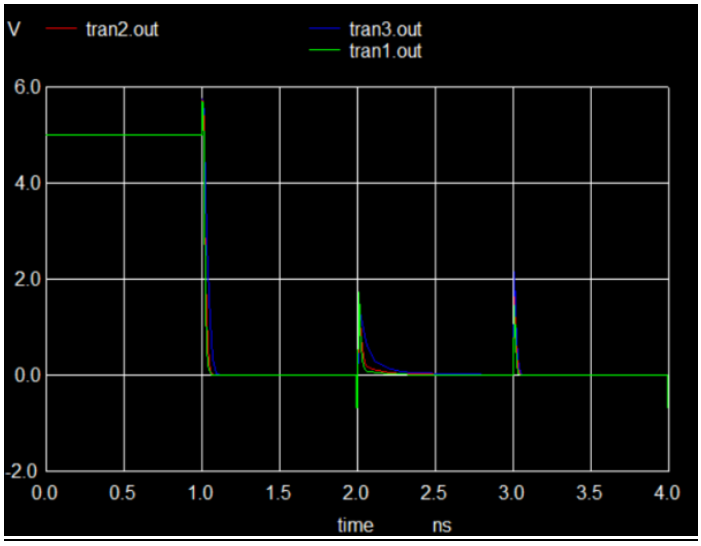

V
tran2.out
tran3.out
tran1.out
6.0
4.0
2.0
0.0
-2.0
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0
time ns

Varying Width of PUN Transistors:

Code:

```
.include ./t14y_tsmc_025_level3.txt
mpa out a x vdd cmosp w=2u l=1u
mpb x b vdd vdd cmosp w=2u l=1u
mna out a 0 0 cmosn w=1u l=1u
mnb out b 0 0 cmosn w=1u l=1u
va a 0 5 pwl(0 0 1n 0 1.01n 5 1.99n 5 2n 0 3n 0 3.01n 5 3.99n 5 4n 0)r=0
vb b 0 5 pwl(0 0 2n 0 2.01n 5 3.99n 5 4n 0)r=0
v_dd vdd 0 5

.control
foreach wid 1u 2u 5u
alter mpa w=$wid
alter mpb w=$wid
tran 0.1ns 4n
end
.endc

.control
foreach iter 1 2 3
setplot tran$iter
end
.endc

.control
plot tran1.out tran2.out tran3.out
.endc
.end
```

Plots:

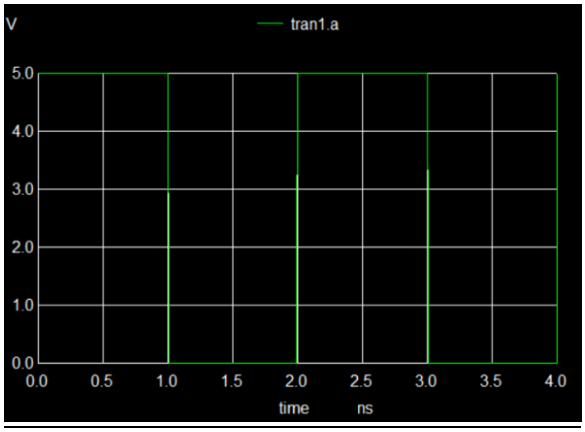


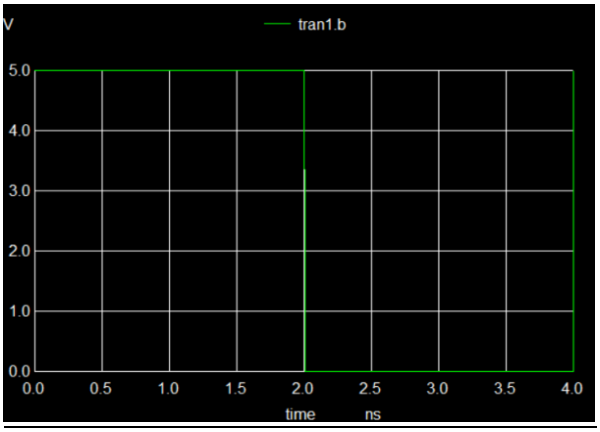
Varying Input Sequence:

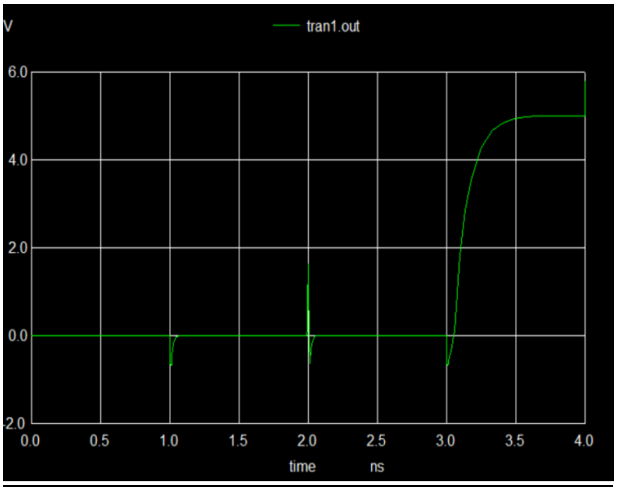
Code:

```
.include ./t14y_tsmc_025_level3.txt
mpa out a x vdd cmosp w=2u l=1u
mpb x b vdd vdd cmosp w=2u l=1u
mna out a 0 0 cmosn w=1u l=1u
mnb out b 0 0 cmosn w=1u l=1u
va a 0 5 pwl(0 5 1n 5 1.01n 0 1.99n 0 2n 5 3n 5 3.01n 0 3.99n 0 4n 0) r=0
vb b 0 5 pwl(0 5 2n 5 2.01n 0 3.99n 0 4n 0) r=0
v_dd vdd 0 5

.control
tran 0.1ns 4n
run
.endc

.control
plot tran1.a
plot tran1.b
plot tran1.out
.endc
.end
```

Plots:



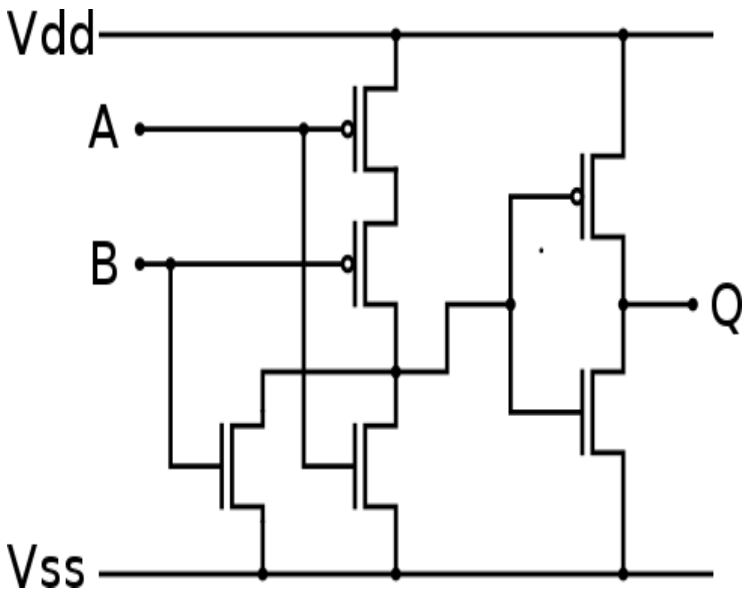




As the width of the PDN transistors increases, the rise time decreases and hence the transition time decreases. As the width of the PUN transistors increases, the rise time also increases, but not as much when compared to the NAND gate. The transition time also depends on the input sequence given. We can also see fluctuations in the output when the input transitions.

AND:

Circuit Diagram:

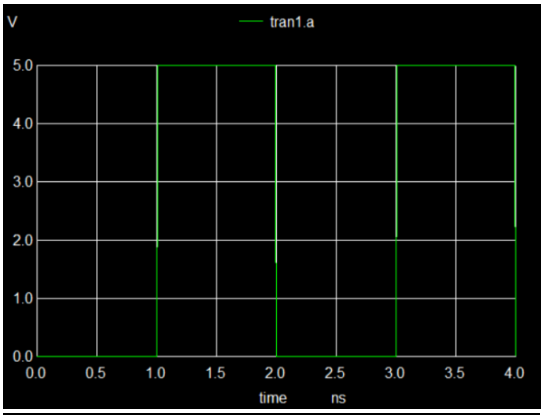


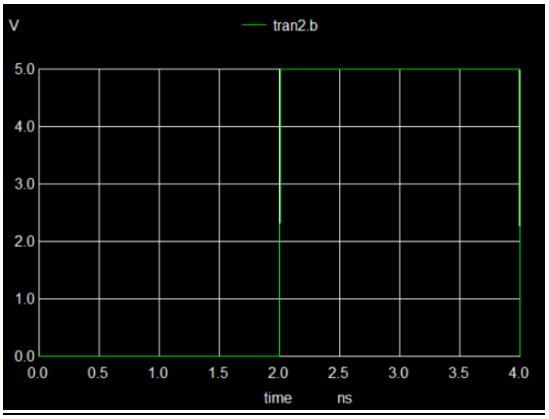
Varying Width of Driver Transistors:

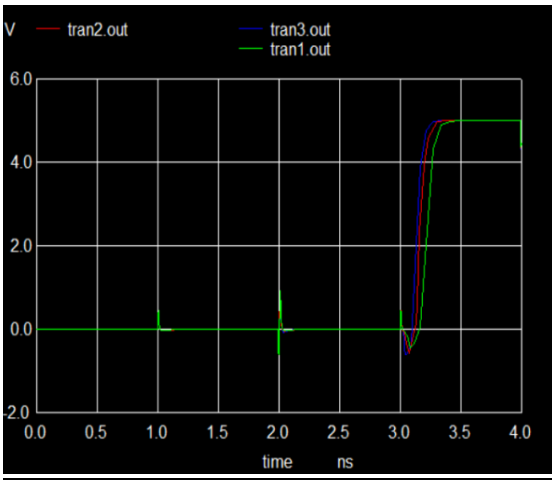
Code:

```
.include ./t14y_tsmc_025_level3.txt
mpa out1 a vdd vdd cmosp w=2u l=1u
mpb out1 b vdd vdd cmosp w=2u l=1u
mna x a 0 0 cmosn w=1u l=1u
mnb out1 b x 0 cmosn w=1u l=1u
m1 out out1 0 0 cmosn w=0.5u l=1u
m2 out out1 vdd vdd cmosp w=0.5u l=1u
va a 0 5 pwl(0 0 1n 0 1.01n 5 1.99n 5 2n 0 3n 0 3.01n 5 3.99n 5 4n 0)r=0
vb b 0 5 pwl(0 0 2n 0 2.01n 5 3.99n 5 4n 0)r=0
v_dd vdd 0 5

.control
foreach wid 1u 2u 5u
alter mna w = $wid
alter mnb w = $wid
tran 0.1ns 4n
end
.endc

.control
foreach iter 1 2 3
setplot tran$iter
end
.endc

.control
plot tran1.a
plot tran2.b
plot tran1.out tran2.out tran3.out
.endc
.end
```

Plots:







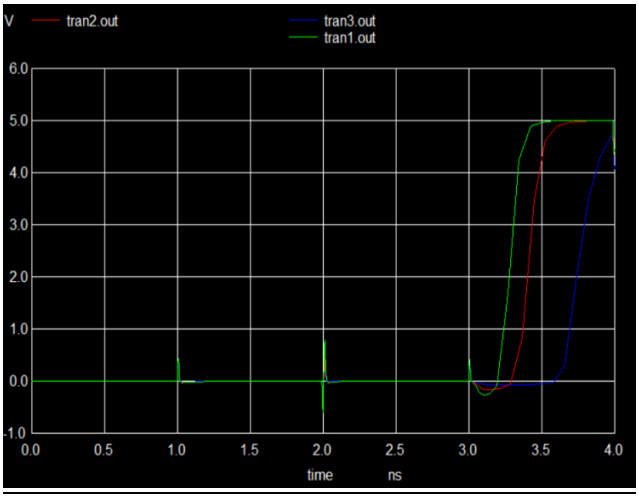
Varying Width of Inverter Transistors:

Code:

```
.include ./t14y_tsmc_025_level3.txt
mpa out1 a vdd vdd cmosp w=2u l=1u
mpb out1 b vdd vdd cmosp w=2u l=1u
mna x a 0 0 cmosn w=1u l=1u
mnb out1 b x 0 cmosn w=1u l=1u
m1 out out1 0 0 cmosn w=0.5u l=1u
m2 out out1 vdd vdd cmosp w=0.5u l=1u
va a 0 5 pwl(0 0 1n 0 1.01n 5 1.99n 5 2n 0 3n 0 3.01n 5 3.99n 5 4n 0)r=0
vb b 0 5 pwl(0 0 2n 0 2.01n 5 3.99n 5 4n 0)r=0
v_dd vdd 0 5

.control
foreach wid 1u 2u 5u
alter m1 w = $wid
tran 0.1ns 4n
end
.endc

.control
foreach iter 1 2 3
```

```
setplot tran$iter
end
.endc

.control
plot tran1.out tran2.out tran3.out
.endc
.end
```

Plots:



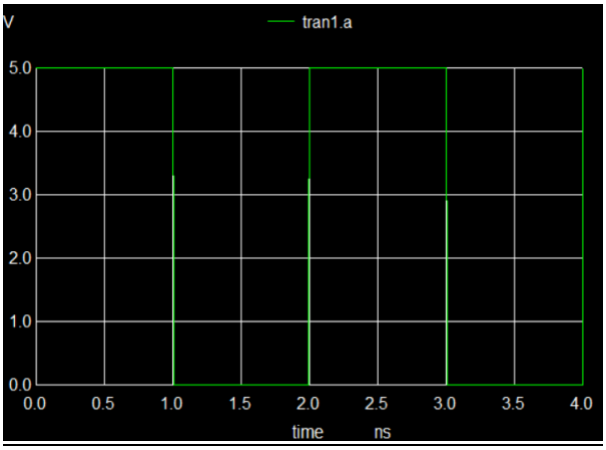
Varying Input Sequence:

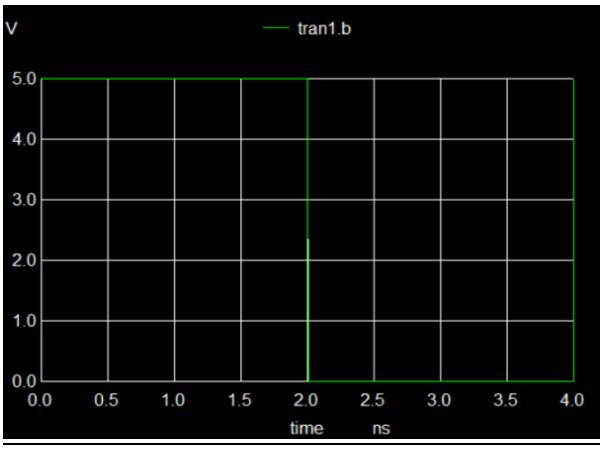
Code:

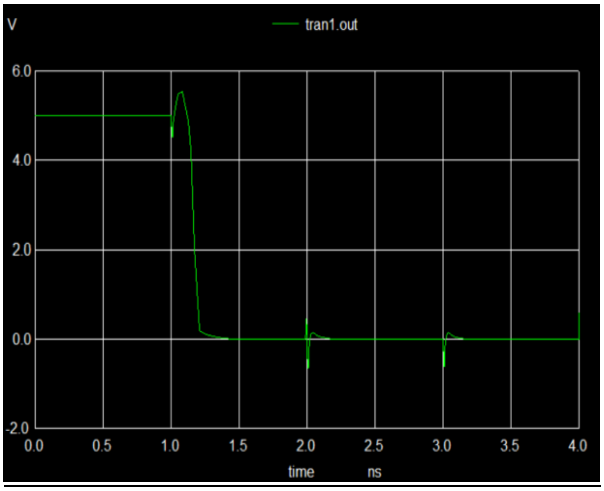
```
.include ./t14y_tsmc_025_level3.txt
mpa out1 a vdd vdd cmosp w=2u l=1u
mpb out1 b vdd vdd cmosp w=2u l=1u
mna x a 0 0 cmosn w=1u l=1u
mnb out1 b x 0 cmosn w=1u l=1u
m1 out out1 0 0 cmosn w=0.5u l=1u
m2 out out1 vdd vdd cmosp w=0.5u l=1u
va a 0 5 pwl(0 5 1n 5 1.01n 0 1.99n 0 2n 5 3n 5 3.01n 0 3.99n 0 4n 0) r=0
vb b 0 5 pwl(0 5 2n 5 2.01n 0 3.99n 0 4n 0) r=0
v_dd vdd 0 5

.tran 0.1n 4n

.control
run
.endc

.control
plot tran1.a
plot tran1.b
plot tran1.out
.endc
```

.end

Plots:



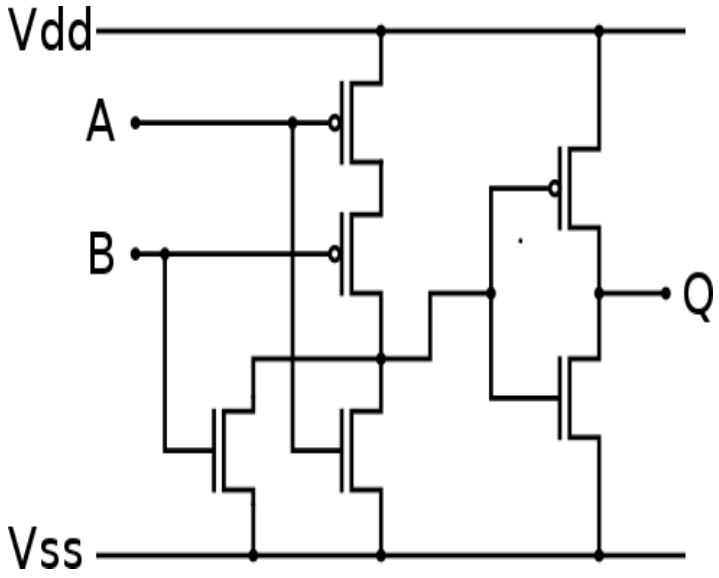




As the width of the AND gates PUN transistors increases, the rise time decreases and hence the transition time also decreases. As the width in the inverter PDN increases, the rise time also increases drastically. The circuit also takes a longer time to fall when going from a 1 1 state to another state.

OR:

Circuit Diagram:



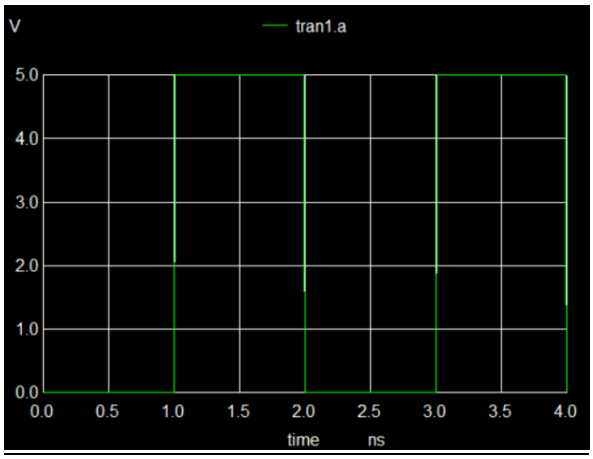
Varying Width of Transistors in OR Gate:

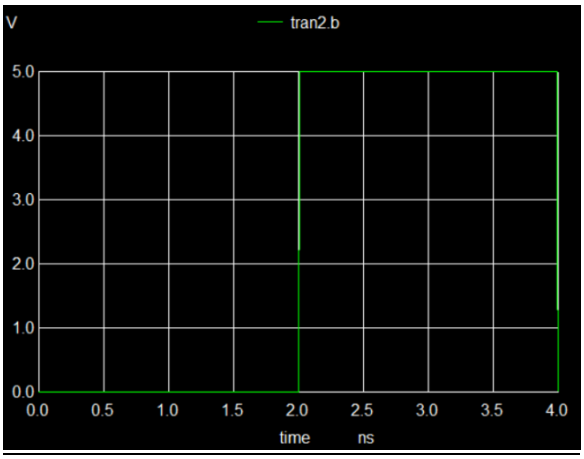
Code:

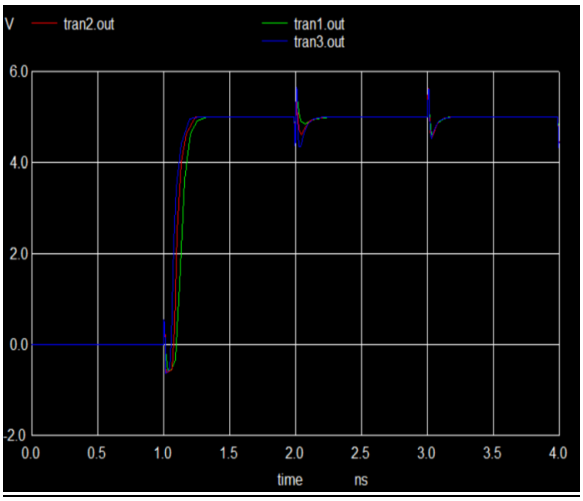
```
.include ./t14y_tsmc_025_level3.txt
mna out1 a 0 0 cmosn w=1u l=1u
mnb out1 b 0 0 cmosn w=1u l=1u
mpa out1 a x vdd cmosp w=2u l=1u
mpb x b vdd vdd cmosp w=2u l=1u
m1 out out1 0 0 cmosn w=0.5u l=1u
m2 out out1 vdd vdd cmosp w=0.5u l=1u
va a 0 5 pwl(0 0 1n 0 1.01n 5 1.99n 5 2n 0 3n 0 3.01n 5 3.99n 5 4n 0) r=0
vb b 0 5 pwl(0 0 2n 0 2.01n 5 3.99n 5 4n 0) r=0
v_dd vdd 0 5

.control
foreach wid 1u 2u 5u
alter mna w = $wid
alter mnb w = $wid
tran 0.1ns 4n
end
.endc

.control
foreach iter 1 2 3
setplot tran$iter
end
.endc
```

```
.control
plot tran1.a
plot tran2.b
plot tran1.out tran2.out tran3.out
.endc
.end
```

Plots:





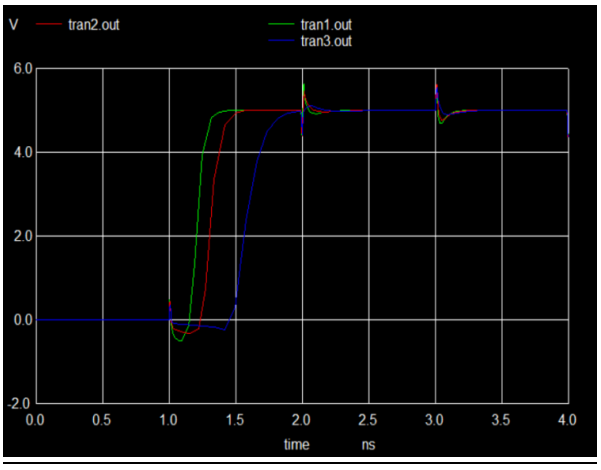


Varying Transistors of Inverter:

Code:

```
.include ./t14y_tsmc_025_level3.txt
mna out1 a 0 0 cmosn w=1u l=1u
mnb out1 b 0 0 cmosn w=1u l=1u
mpa out1 a x vdd cmosp w=2u l=1u
mpb x b vdd vdd cmosp w=2u l=1u
m1 out out1 0 0 cmosn w=0.5u l=1u
m2 out out1 vdd vdd cmosp w=0.5u l=1u
va a 0 5 pwl(0 0 1n 0 1.01n 5 1.99n 5 2n 0 3n 0 3.01n 5 3.99n 5 4n 0) r=0
vb b 0 5 pwl(0 0 2n 0 2.01n 5 3.99n 5 4n 0) r=0
v_dd vdd 0 5

.control
foreach wid 1u 2u 5u
alter m1 w = $wid
tran 0.1n 4n
end
.endc

.control
foreach iter 1 2 3
setplot tran$iter
end
.endc
.control
plot tran1.out tran2.out tran3.out
.endc
.end
```

Plots:

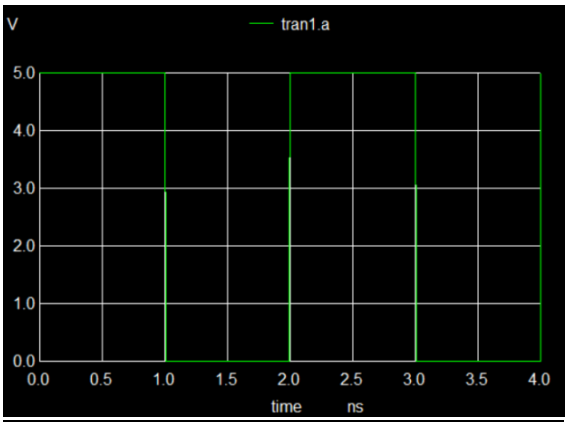


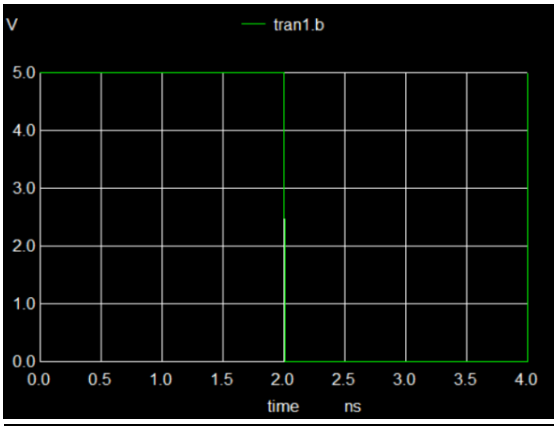
Changing Input Sequence:

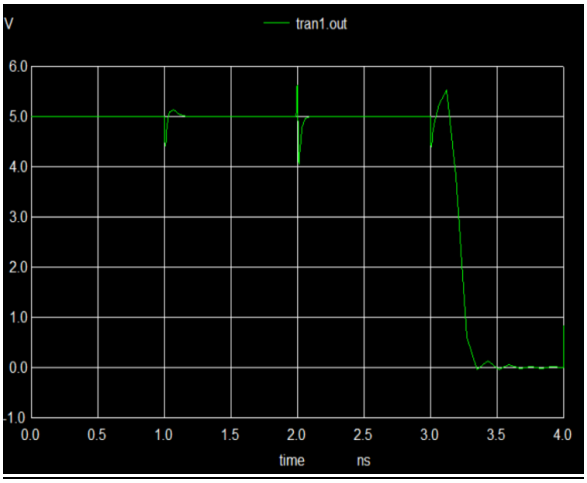
Code:

```
.include ./t14y_tsmc_025_level3.txt
mna out1 a 0 0 cmosn w=1u l=1u
mnb out1 b 0 0 cmosn w=1u l=1u
mpa out1 a x vdd cmosp w=2u l=1u
mpb x b vdd vdd cmosp w=2u l=1u
m1 out out1 0 0 cmosn w=0.5u l=1u
m2 out out1 vdd vdd cmosp w=0.5u l=1u
va a 0 5 pwl(0 5 1n 5 1.01n 0 1.99n 0 2n 5 3n 5 3.01n 0 3.99n 0 4n 0) r=0
vb b 0 5 pwl(0 5 2n 5 2.01n 0 3.99n 0 4n 0) r=0
v_dd vdd 0 5

.control
tran 0.1n 4n
run
.endc

.control
plot tran1.a
plot tran1.b
plot tran1.out
.endc
.end
```

Plots:







As the width of the PDN transistors in the OR circuit increases, the rise time decreases, and hence the transition time also decreases. As the width of the PDN transistor in the Inverter increases, the rise time increases drastically. And the propagation delay is very high at almost half of the pulse width. We can see that the circuit takes time to fall from high to low and also there is undershoot when going to 0 0 state from other states.

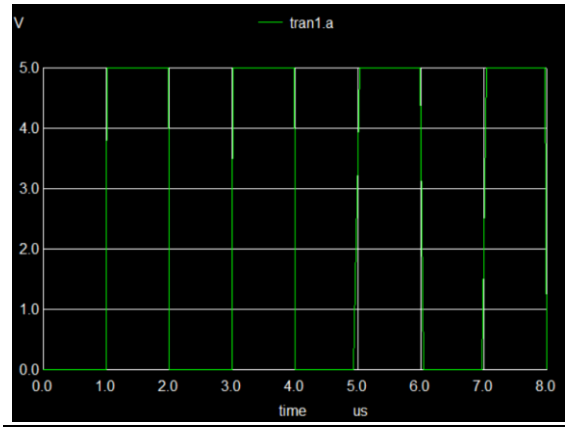
XOR:

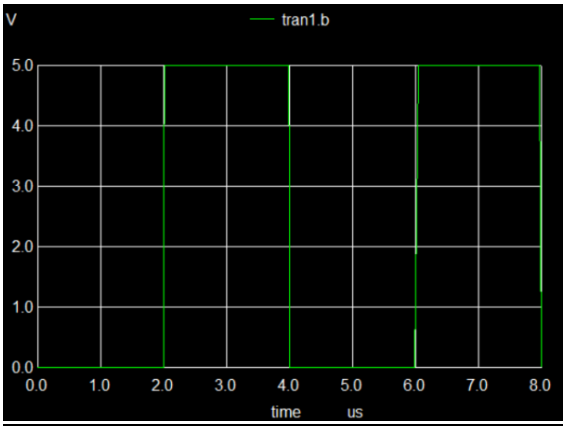
Code:

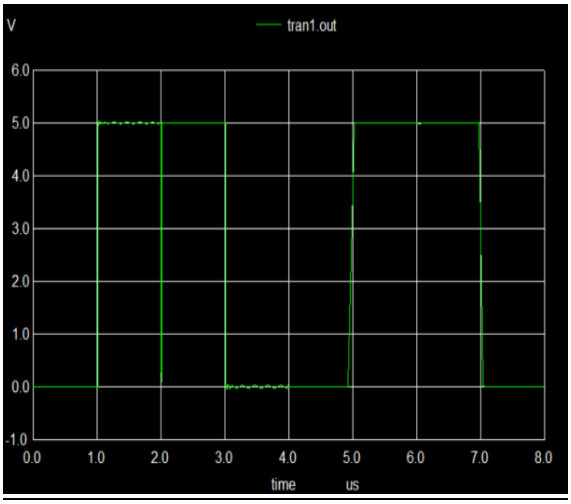
```
.include ./t14y_tsmc_025_level3.txt
mnia x a 0 0 cmosn w=0.5u l=1u
mpia x a vdd vdd cmosp w=1.5u l=1u
mnib y b 0 0 cmosn w=0.5u l=1u
mpib y b vdd vdd cmosp w=1.5u l=1u
m1d1 p1 b 0 0 cmosn w=1u l=1u
m1d2 z x p1 0 cmosn w=1u l=1u
m1u1 z b vdd vdd cmosp w=1.5u l=1u
m1u2 z x vdd vdd cmosp w=1.5u l=1u
m2d1 p2 a 0 0 cmosn w=1u l=1u
m2d2 w y p2 0 cmosn w=1u l=1u
m2u1 w a vdd vdd cmosp w=1.5u l=1u
m2u2 w y vdd vdd cmosp w=1.5u l=1u
m3d1 p3 z 0 0 cmosn w=1u l=1u
m3d2 out w p3 0 cmosn w=1u l=1u
m3u1 out z vdd vdd cmosp w=1.5u l=1u
m3u2 out w vdd vdd cmosp w=1.5u l=1u
c1 z 0 1p
c2 w 0 1p
v_dd vdd 0 5
va a 0 5 pwl(0 0 1u 0 1.01u 5 1.99u 5 2u 0 3u 0 3.01u 5 3.99u 5 4u 0) r=0
vb b 0 5 pwl(0 0 2u 0 2.01u 5 3.99u 5 4u 0) r=0

.control
tran 0.1u 8u
run
```

```
.endc

.control
plot tran1.a
plot tran1.b
plot tran1.out
.endc
.end
```

Plots:







The Results obtained have perfect VOL and VOH resulting in accurate outputs except for the overshoots and time delay. The overshoots are due to the capacitances while the time delays are because the signal takes time in propagating to the load capacitance.

Part 2

Experiment 6: CMOS Inverter Layout and Characterization

Objective:

To learn layout, extract, LVS and characterization processes in the design flow with CMOS inverter as an example.

Procedure:

a) Design a CMOS Inverter for a specified value of risetime and falltime with a specified drive strength. Write a spice netlist for that CMOS inverter.

b) Layout the CMOS inverter, save it in a mag file. Provide sufficient width to the power rails.

c) Using the extresis and extract commands, extract the circuit parameters, parasitics into a .ext file.

d) Using the exttospice command convert the .ext file into a spice netlist.

e) Using the netgen command, compare the extracted spice netlist with the original netlist to verify that the laid out circuit indeed represents the original spice netlist.

f) Simulate the extracted spice netlist using NgSPICE. Compute the risetime and the falltime of this inverter with the design specifications. Justify the difference if any.

g) Compute the area occupied by the cell.

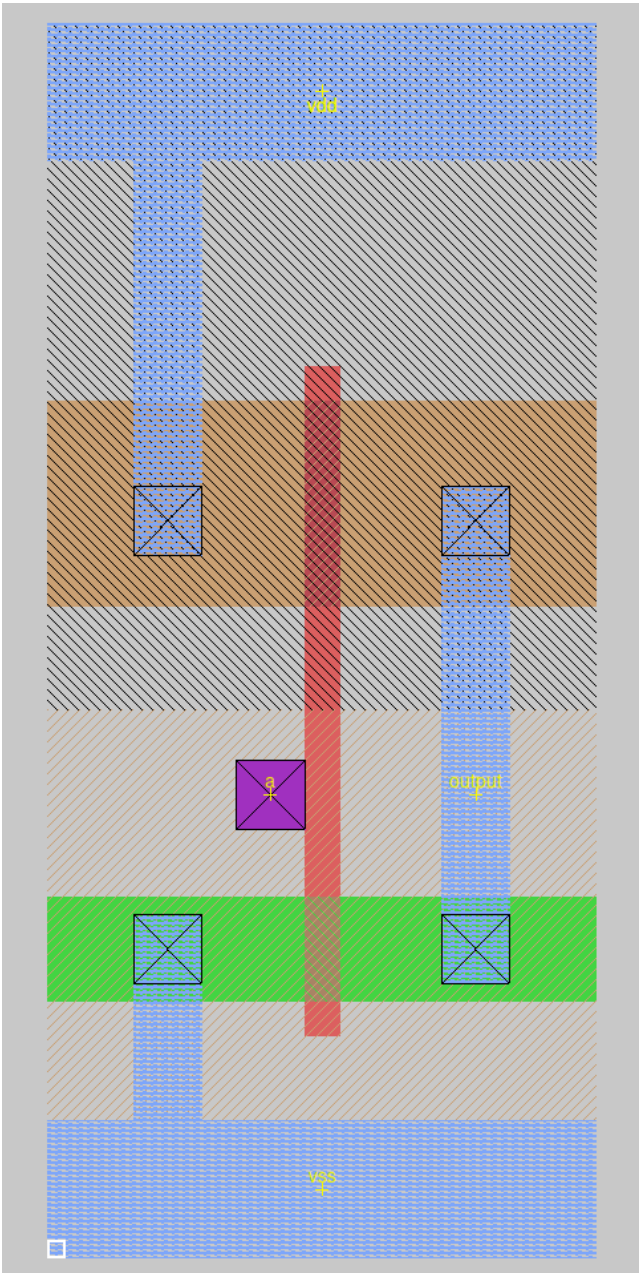
h) Try to minimize the area and improve the speed for the same load by using optimal layout techniques and create a standard cell for the inverter.

i) Find the power consumed per transition of output for various loads, continuous power dissipated.

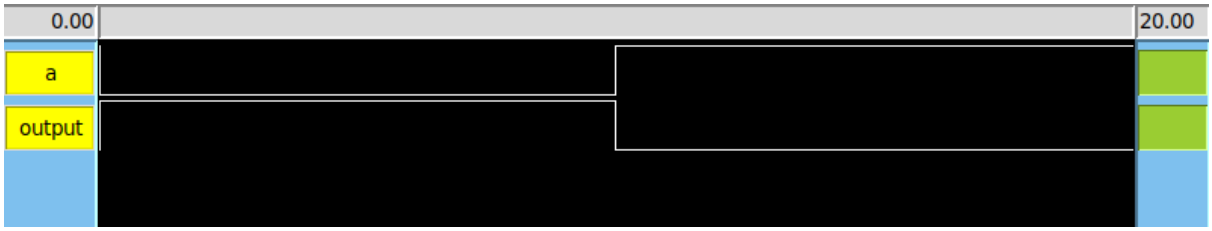
j) Tabulate all your observations like area of the cell, input capacitance, output capacitance, rise and fall time power dissipated for various loads.

Observations:

Layout:



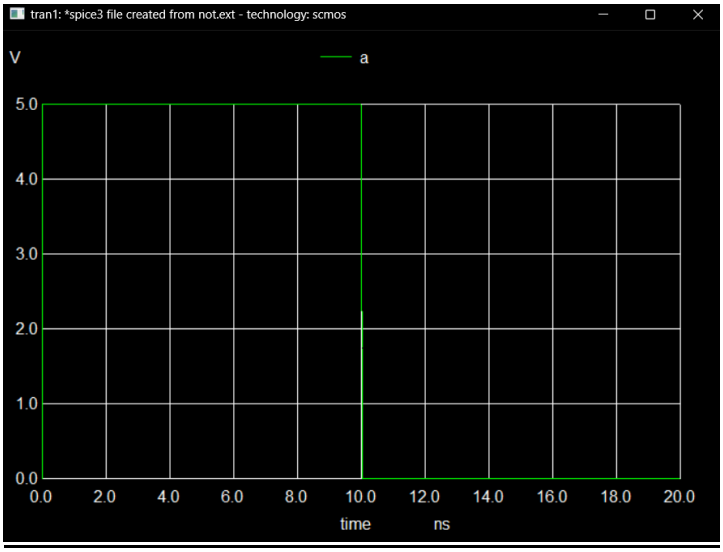
IRSIM simulation:

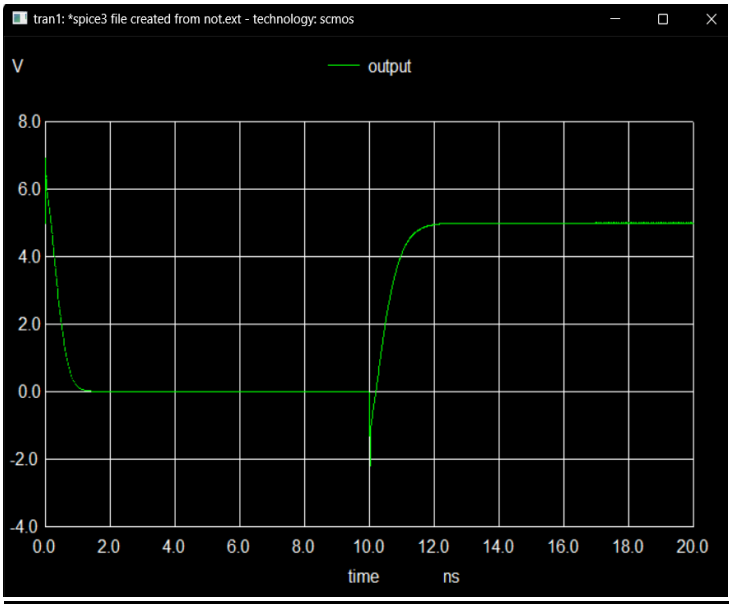


Spice code generated:

```
*SPICE3 file created from not.ext - technology: scmos

.include ./t14y_tsmc_025_level3.txt
.option scale=1u
*netlist



M1000 output a vdd w_0_32# cmosp w=12 l=2
+  ad=180 pd=54 as=180 ps=54
M1001 output a vss w_0_8# cmosn w=6 l=2
+  ad=90 pd=42 as=90 ps=42
*C0 a w_0_8# 4.84fF
*C1 output w_0_8# 2.07fF
*C2 w_0_32# a 2.38fF
*C3 vss 0 12.03fF
*C4 vdd 0 12.03fF



v_dd vdd 0 5
v_ss vss 0 0

v_ina a 0 pulse(0 5 0 0 0 10n 20n)

.control
tran 0.01n 20n
setplot tran1
plot a
plot output
.endc
.end
```

Plots:

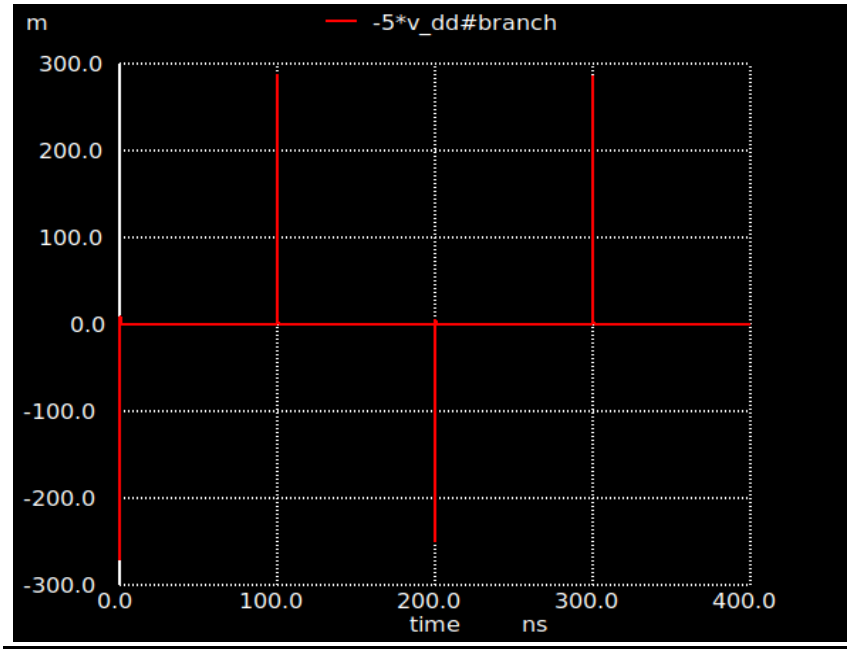




Analysis:

Characteristics	Value
Rise Time	1.00307e-07 s
Fall Time	7.178547e-10 s
Propagation Delay	5.622745e-10 s
Energy	2.175819e-13 J

Power plot:



Conclusion:

- With the decrease in total area of the Inverter layout the output becomes more and more ideal.
- Value of capacitances decrease with the size

Experiment 7: Generation of a Standard Cell library

Objective:

To create a standard cell library of CMOS Gates - Two input NOT, NAND, NOR, AND, OR gates.

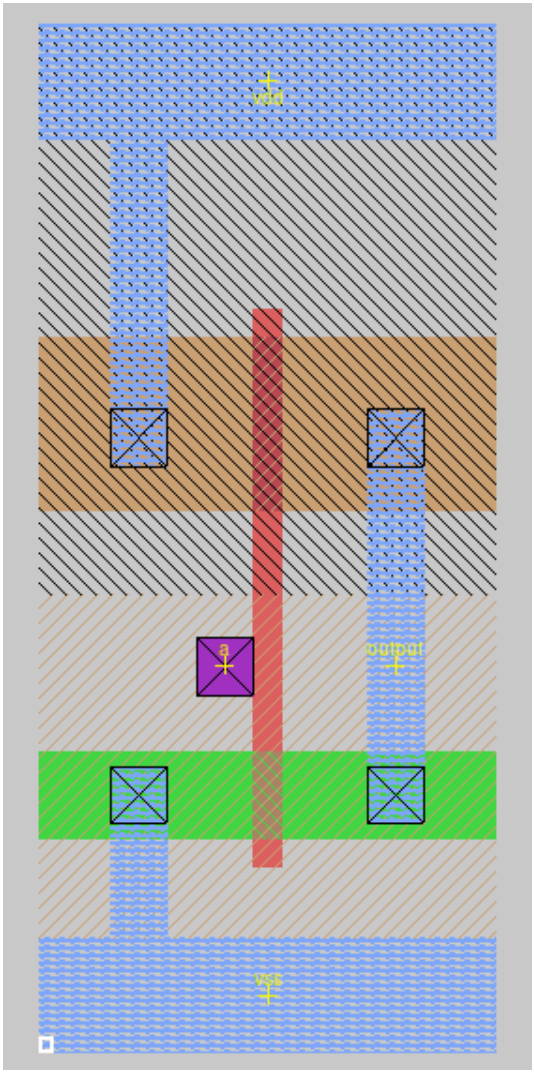
Procedure:

Similar to experiment 6.

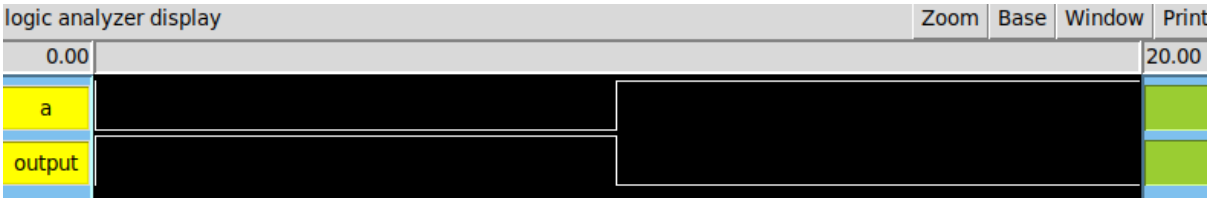
Observations:

a) NOT Gate:

Layout:



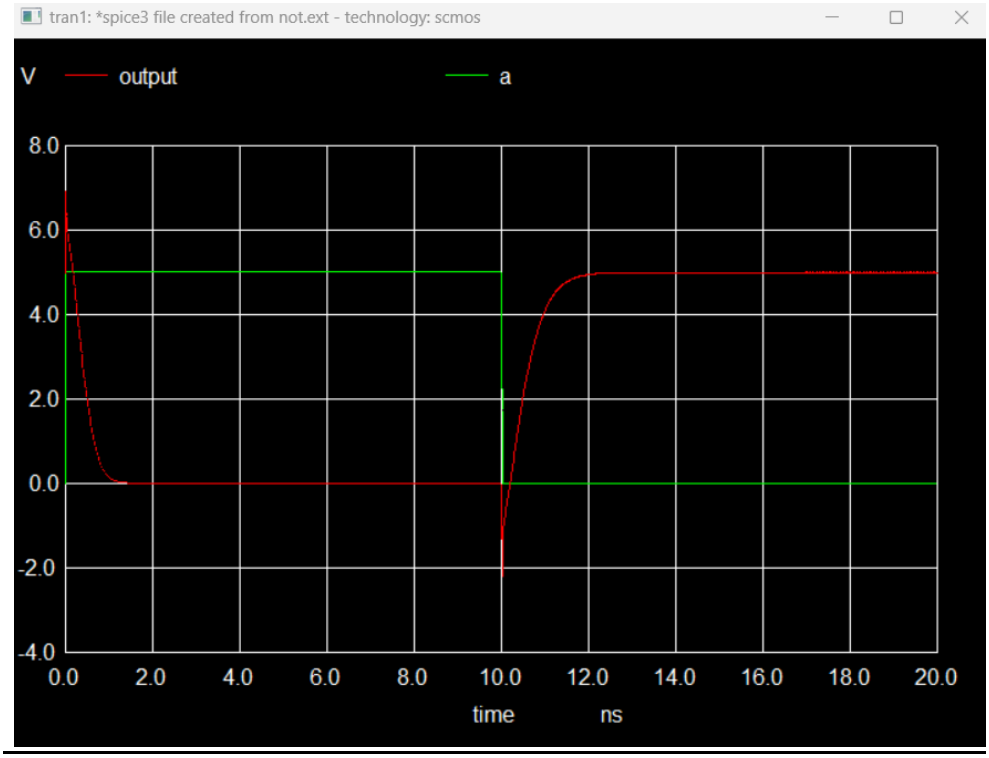
IRSIM simulation:



Ngspice Netlist:

```
*SPICE3 file created from not.ext - technology: scmos

.include ./t14y_tsmc_025_level3.txt
.option scale=1u
*netlist


M1000 output a vdd w_0_32# cmosp w=12 l=2
+  ad=180 pd=54 as=180 ps=54
M1001 output a vss w_0_8# cmosn w=6 l=2
+  ad=90 pd=42 as=90 ps=42
*C0 a w_0_8# 4.84fF
*C1 output w_0_8# 2.07fF
*C2 w_0_32# a 2.38fF
*C3 vss 0 12.03fF
*C4 vdd 0 12.03fF


v_dd vdd 0 5
v_ss vss 0 0

v_ina a 0 pulse(0 5 0 0 0 10n 20n)

.control
tran 0.01n 20n
setplot tran1
plot a output
.endc
.end
```

Plot:

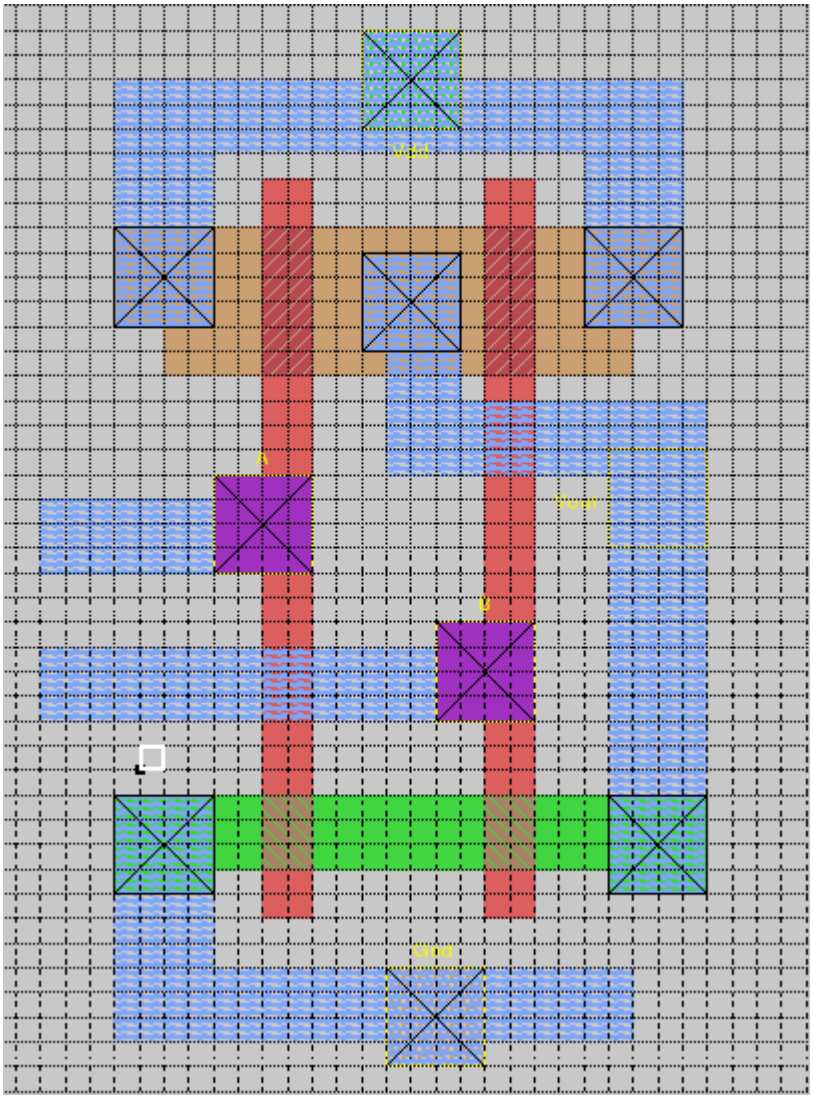


Analysis:

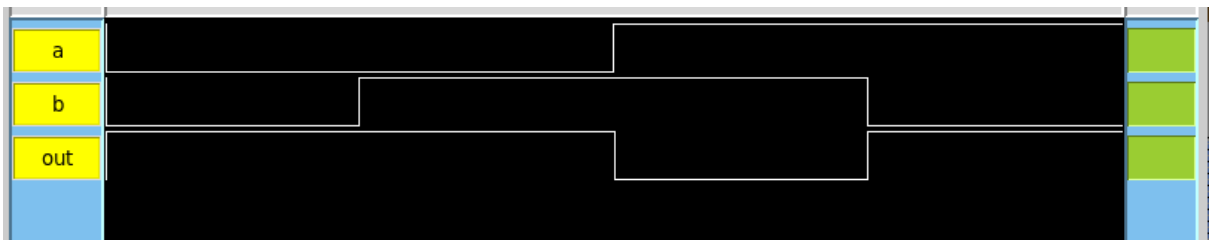
Characteristics	**Value**
Rise Time	1.00307e-07 s
Fall Time	7.178547e-10 s
Propagation Delay	5.622745e-10 s
Energy	2.175819e-13 J

b)NAND Gate

Layout:



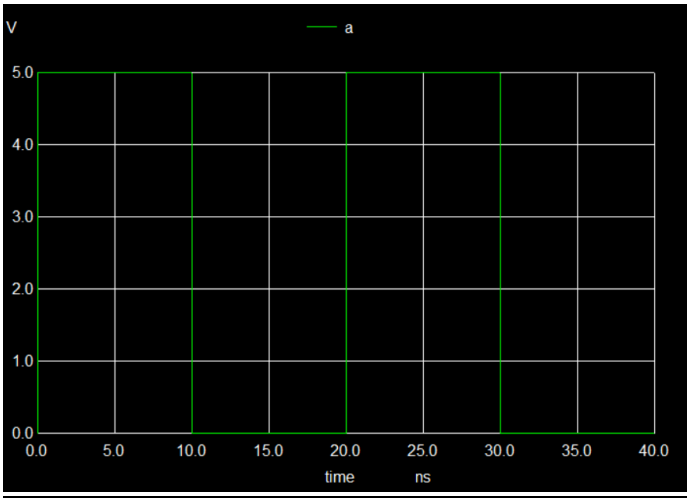
IRSIM simulation:

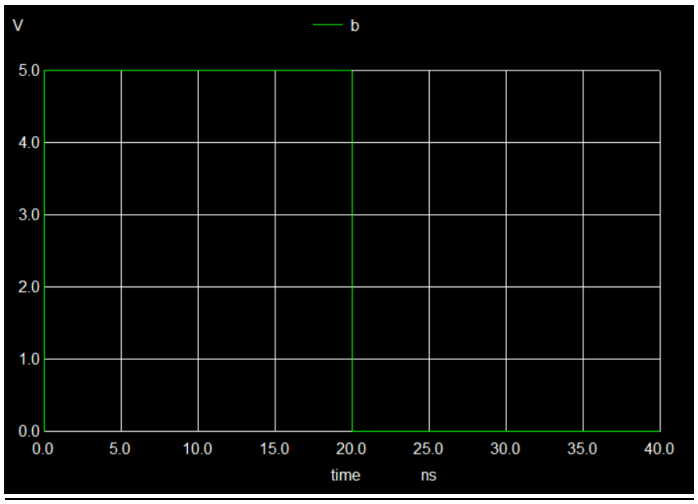


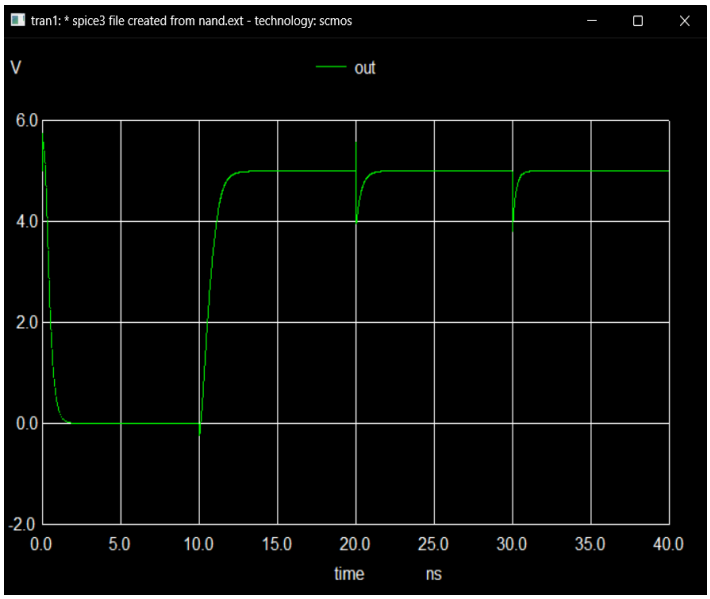
Ngspice Netlist:

```
* SPICE3 file created from nand.ext - technology: scmos

.option scale=1u

.include ./t14y_tsmc_025_level3.txt
M1000 vdd b out vdd cmosp w=8 l=2
+  ad=80 pd=52 as=48 ps=28
M1001 out b a_7_0# vss cmosn w=4 l=2
+  ad=20 pd=18 as=24 ps=20
M1002 a_7_0# a vss vss cmosn w=4 l=2
+  ad=0 pd=0 as=20 ps=18
M1003 out a vdd vdd cmosp w=8 l=2
+  ad=0 pd=0 as=0 ps=0
*C0 vss Gnd 3.15fF
*C1 b Gnd 5.00fF
*C2 a Gnd 5.00fF

v_dd vdd 0 5
v_ss vss 0 0

v_ina a 0 pulse(0 5 0 0 0 10n 20n)
v_inb b 0 pulse(0 5 0 0 0 20n 40n)
.control
tran 0.01n 40n
setplot tran1
plot a
plot b
plot out
.endc

.end
```

Plots:


V
a
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
time
ns


V
b
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
time
ns

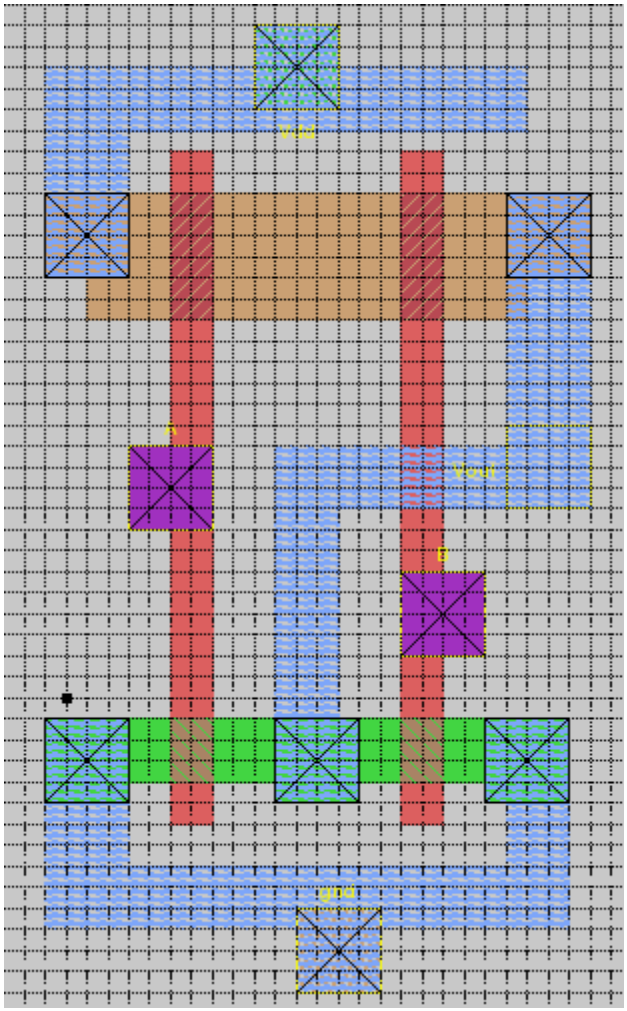

tran1: * spice3 file created from nand.ext - technology: scmos
V
out
6.0
4.0
2.0
0.0
-2.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
time
ns

Analysis:

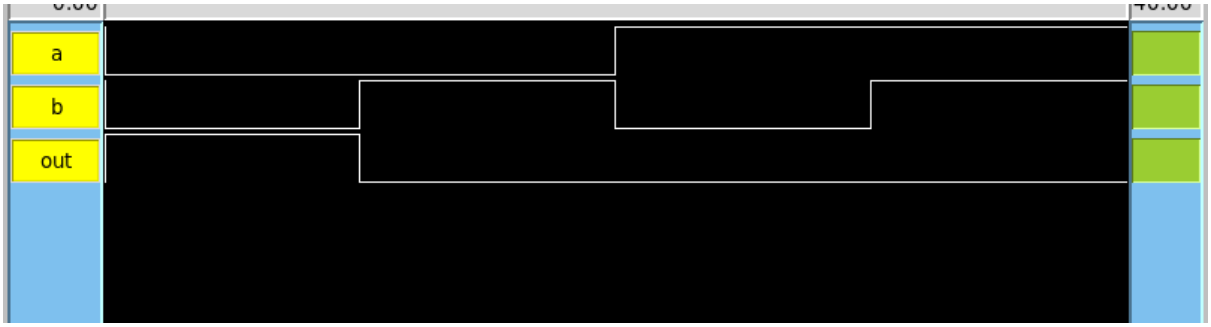
Characteristics	**Value**
Rise Time	2.03935e-08 s
Fall Time	1.132681e-09 s
Propagation Delay w.r.t input A	9.602641e-10 s
Propagation Delay w.r.t input B	9.03974e-09 s
Energy	1.490572e-12 J

c)NOR gate

Layout:



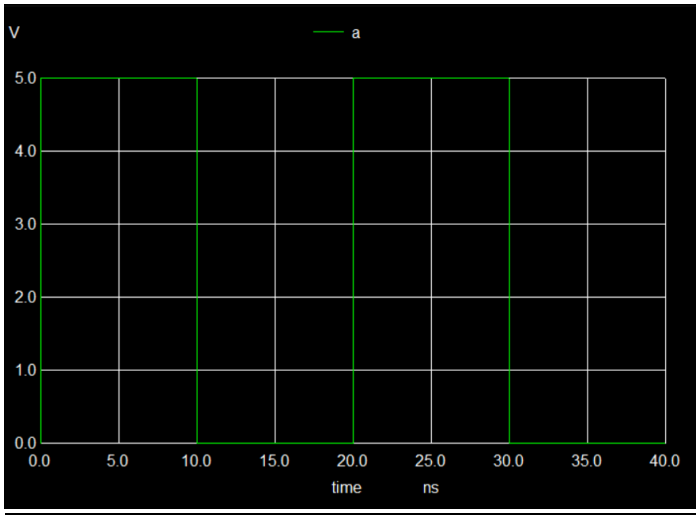
IRSIM simulation:

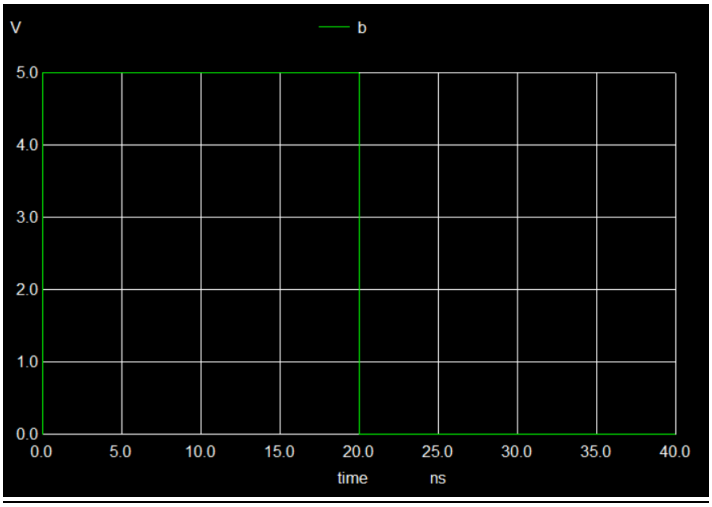


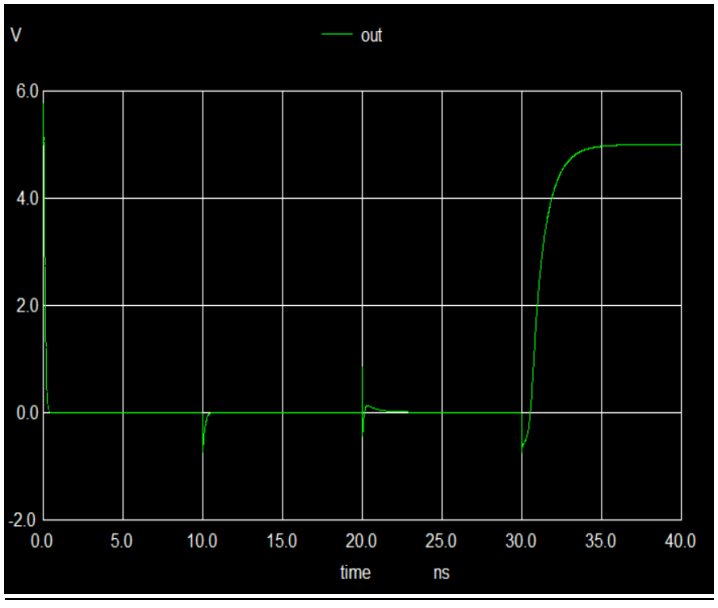
Ngspice Netlist:

```
*running NOR gate extracted from Layout
.include ./t14y_tsmc_025_level3.txt
.option scale=1u
*netlist

M1000 out b a_7_37# vdd cmosp w=20 l=2
+ad=100 pd=50 as=120 ps=52
M1001 a_7_37# a vdd vdd cmosp w=20 l=2
+ad=0 pd=0 as=116 ps=66
M1002 vss b out vss cmosn w=10 l=2
+ad=116 pd=76 as=60 ps=32
M1003 out a vss vss cmosn w=10 l=2
+ad=0 pd=0 as=0 ps=0

*C0 gnd Gnd 6.39FF
*C1 out Gnd 4.70fF
*C2 b Gnd 7.06fF
*C3 a Gnd 7.06fF
*C4 vdd Gnd 5.64fF

v_dd vdd 0 5
v_ss vss 0 0

v_ina a 0 pulse(0 5 0 0 0 10n 20n)
v_inb b 0 pulse(0 5 0 0 0 20n 40n)
.control
tran 0.01n 40n
setplot tran1
plot a
plot b
plot out
.endc

.end
```

Plots:


V
a
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
time
ns


V
b
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
time
ns

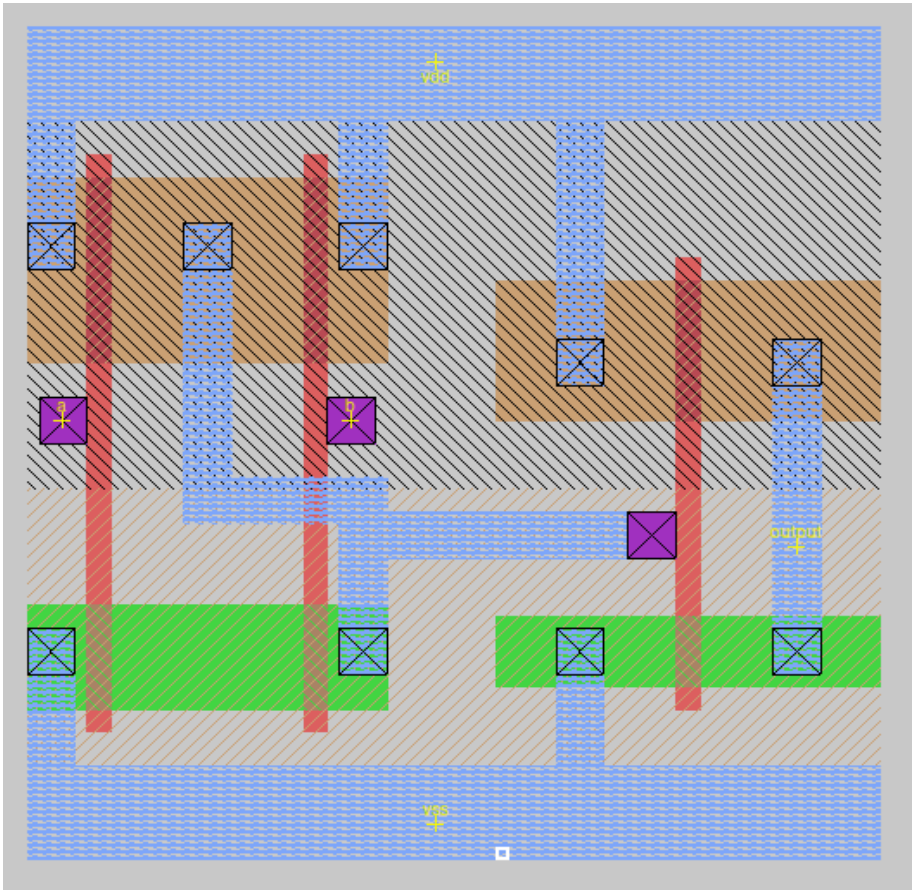

V
out
6.0
4.0
2.0
0.0
-2.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
time
ns

Analysis:

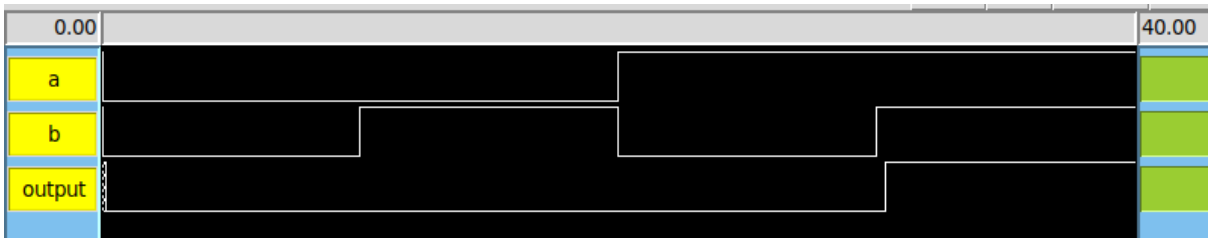
Characteristics	Value
Rise Time	2.00036e-08 s
Fall Time	4.804346e-11 s
Propagation Delay w.r.t input A	1.025317e-08 s
Propagation Delay w.r.t input B	5.253169e-09 s
Energy	2.30979e-14 J

d) AND Gate

Layout:

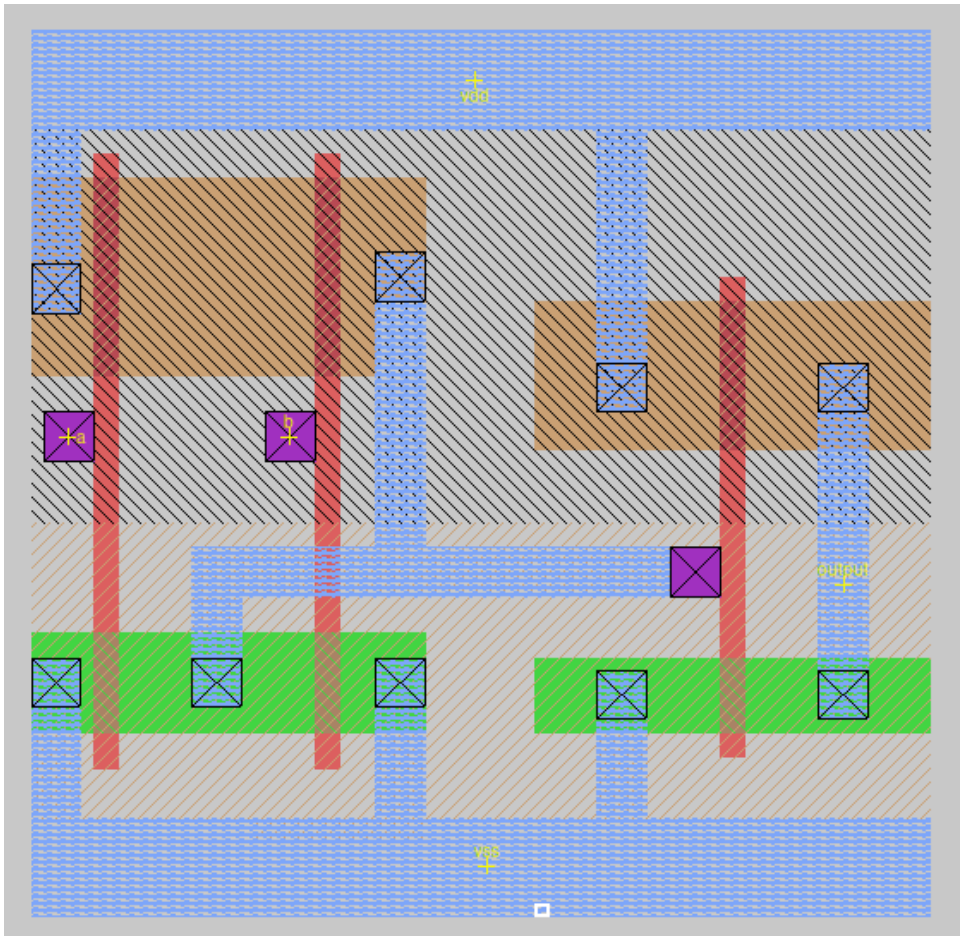


IRSIM simulation:

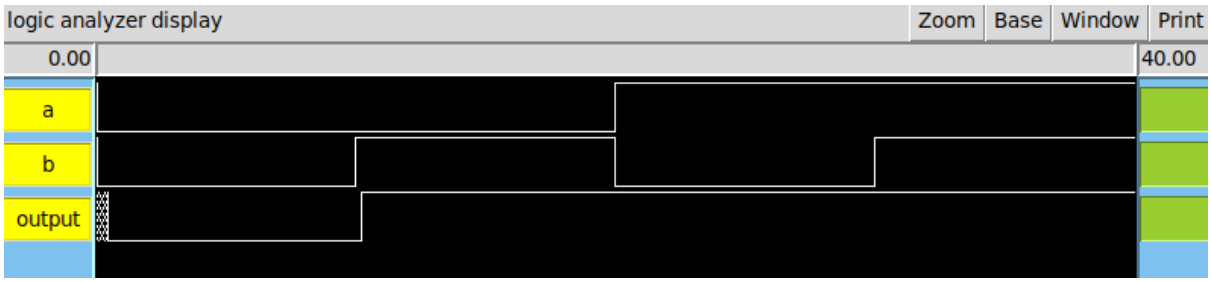


e) OR Gate

Layout:



IRSIM simulation:



Conclusion:

Layouts were created for various 2 and 3 inputs gate. However ideal behaviour was rarely observed due to additional parasitic capacitance.