BEC601

Model Question Paper-1 with effect from 2022(CBCS Scheme)

USN | | | | | | | | | | |

6th Semester B.E. Degree Examination

Subject Title – Embedded Systems Design

TIME: 03 Hours **Max. Marks: 100**

Note: Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

		Module -1	*Bloom's Taxonomy Level	COs	Marks
Q.01	a	Define Embedded System. Classify an embedded system based on (i) generation (ii) Complexity (iii) Triggering	L1	CO1	10
	b	Explain the following: (i) Optocoupler (ii) Zig-Bee (iii) Wi-Fi (iv)SPI bus (v) USB	L2	CO1	10
		OR			
Q.02	a	List the features of the following : (i)I2C Bus (ii)IrDA (iii)1-wire Interface (iv)keyboard (v)UART	L1	CO1	10
	b	Illustrate the architectural block diagram of embedded system and mention the components used.	L2	CO1	10
		Module-2			
Q. 03	a	Discuss the Operational and Non-Operational Quality Attributes of an Embedded System.	L2	CO2	10
	b	Compare (i) DFG and CDFG models with an example. (ii) C v/s Embedded C (iii) Compiler v/s Cross-Compiler	L2	CO2	10
		OR			
Q.04	a	Explain the assembly language based embedded firmware development with a diagram and mention its advantages and disadvantages.	L2	CO2	10
	b	Demonstrate coin operated telephone system with a FSM , function of states and state transition diagram.	L2	CO2	10
		Module-3			
Q. 05	a	Explain monolithic and micro kernels with suitable example for each.	L2	CO3	06
	b	Discuss the terms tasks, process and threads.	L2	CO3	08
	c	Three processes with process IDs P1, P2 and P3 with estimated completion time 10,5,7 ms respectively enter the ready queue together in order P1, P2 , P3. Calculate waiting time and turn around time for each process and average waiting time and TAT.(Assume there is no I/O waiting for the processes.	L3	CO3	06
		OR			
Q. 06	a	Write a note on IAP [In Application Programming] and In System Programming.	L2	CO3	04
	b	Demonstrate a block schematic of IDE environment for embedded system design and explain their functions in brief. - 08	L2	CO3	08
	c	Illustrate the concept of 'deadlock' with a neat diagram. Mention the different conditions which favors a deadlock situation.	L3	CO3	08
		Module-4			
Q. 07	a	List the different registers of ARM CORTEX – M3 and mention their use. Explain the use of R13, R14 and R15 registers.	L1,L2	CO4	08

	b	Summarize the CPSR configuration. Illustrate how to access different subdivisions of PSR.	L2	CO4	06
	c	Explain exceptions and interrupts of ARM CORTEX – M3.	L2	CO4	06
		OR			
Q. 08	a	Describe with a block schematic, explain the function of various units in ARM Cortex M3 processor architecture in brief.	L1,L2	CO4	10
	b	Discuss any 5 applications of ARM cortex M3 based on its features.	L2	CO4	05
	c	Explain all the processor modes of ARM Cortex M3 along with a diagram.	L2	CO4	05
		Module-5			
Q. 09	a	Explain the following 32 bit instructions with an example for each : ADC, BIC, LSL and PUSH.	L2	CO5	08
	b	Describe CMSIS with diagram and its functions, organization and scope.	L2	CO5	07
	c	Write an ALP to add the first 10 integer numbers using Cortex M3 processor.	L3	CO5	05
		OR			
Q. 10	a	Explain the operation of following instruction with syntax and an example for each : (i)ADD.W (ii)LDMIA (iii)BEQ (iv) LSR (v)IF-THEN	L2	CO5	10
	b	Explain different rotate and reverse instructions of Cortex M3 with example for each.	L3	CO5	10

*Bloom's Taxonomy Level: Indicate as L1, L2, L3, L4, etc. It is also desirable to indicate the COs and POs to be attained by every bit of questions.