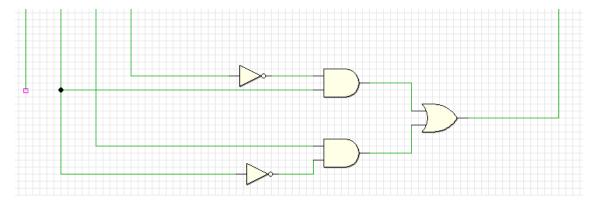
1.1. Diseño de un Convertidor BCD – 7 Segmentos.

X3	X2	X1	X0	Α	В	С	D	E	F	G	DP
0	0	0	0	1	1	1	0	0	0	0	0
0	0	0	1	1	1	1	0	0	0	0	0
0	0	1	0	1	1	1	0	0	1	1	0
0	0	1	1	1	0	1	1	0	1	1	0
0	1	0	0	1	1	1	1	1	1	1	0
0	1	0	1	0	1	1	0	0	0	0	0
0	1	1	0	1	0	1	1	1	1	1	0
0	1	1	1	1	1	1	0	0	0	0	0
1	0	0	0	X	X	X	X	X	X	X	0
1	0	0	1	X	X	X	X	X	X	x	0
1	0	1	0	x	x	X	x	×	x	x	0
1	0	1	1	X	X	X	X	X	X	x	0
1	1	0	0	X	X	X	X	X	X	X	0
1	1	0	1	X	X	X	X	X	х	X	0
1	1	1	0	X	X	X	X	X	X	x	0
1	1	1	1	X	X	X	X	X	X	X	0

SM (Suma Mínima) → Segmento G

X1 X0\ X3 X2	00	01	11	10
00	0	1	х	Х
01	0	0	x	x
11	1	0	x	Х
10	1	1	х	х

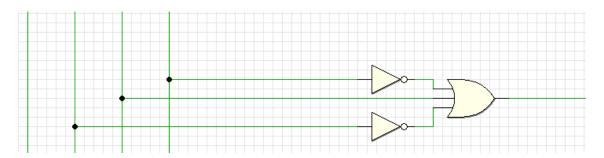
Función lógica: X0'X2+X1X2'



PM (Producto Mínimo) → Segmento A

X1 X0\ X3 X2	00	01	11	10
00	1	1	х	x
01	1	0	х	X
11	1	1	х	X
10	1	1	х	х

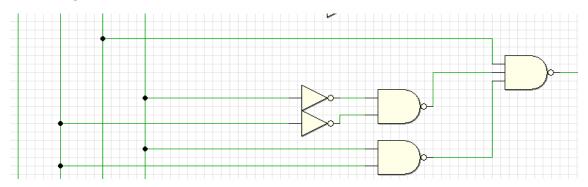
Función lógica: X0'+X2'+X1



NAND → Segmento B

X1 X0\ X3 X2	00	01	11	10
00	4	1)	1 x	x
01		1	1 x	х
11		0	1 x	x
10		1	0 x	х

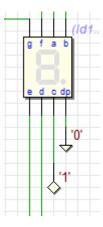
Función lógica: X1'+X0'X2'+X0X2 = X1' \cdot (X0'+X2) \cdot (X0'+X2') \cdot (X0+X2')



 $NOR \rightarrow Segmento C$

X1 X0\ X3 X2	00	01	11	10
00	1	1	X	X
01	1	1	x	x
11	1	1	x	X
10	1	1	x	x

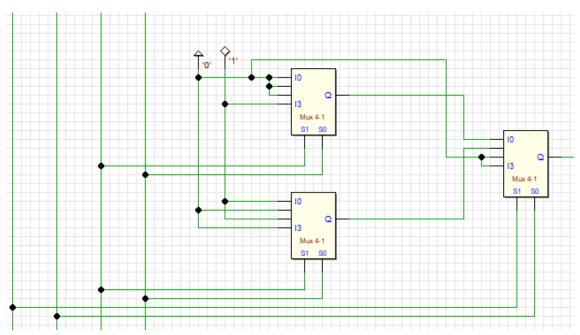
Función lógica: 1



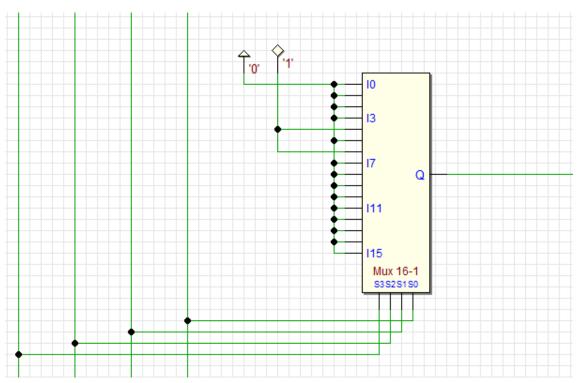
MUX4-1 \rightarrow Segmento D

X1 X0\ X3 X2	00	01	11	10
00	0	1	x	x
01	0	0	x	x
11	1	0	x	x
10	0	1	x	x

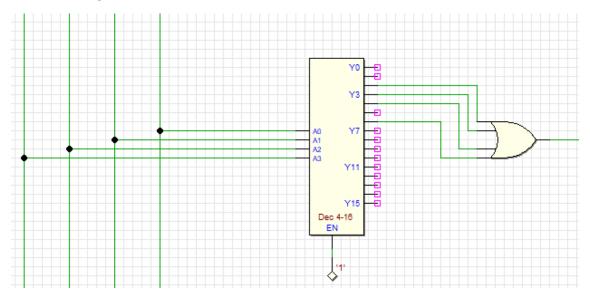
Función lógica: X0'X2+X1X0X2'



MUX16-1 → Segmento E



DEC4-16 → Segmento F



1.3. Implementación y Animación del Convertidor BCD -7 Segmentos

