Marwan Abdelwahab

813-452-8922 | marwanabdelwahab09@gmail.com | linkedin.com/in/marwan-abdelwahab | github.com/Mar85562

Education

University of South Florida – Tampa, FL **Graduation: May 2026**

Bachelor of Science in Computer Engineering ***GPA: 3.94/4.0****, Dean's List x6*

- **Relevant Coursework:** Computer System Design, Computer Architecture, Hardware Accelerators for ML, CMOS VLSI Design, Operating Systems, Electrical Systems, Electronic Materials, VLSI Testing, Data Structures and Algorithms, Intro to AI, Computer Logic and design, Discrete Structures, Program Design

Experience

Teaching Assistant - Computer Logic & Design **January 2025 – Present**

USF CSE Department *Tampa, FL*

- Supported instruction for **100+** students by grading assignments and exams, providing detailed written and verbal feedback that clarified misconceptions and contributed to a **10%** improvement in class averages
- Conducted weekly office hours guiding students through logic design concepts, **Verilog** debugging, and circuit simulations, increasing overall project completion rates
- Designed and delivered demonstrations on **Linux** and **VS Code** workflows, boosting student confidence in applying professional tools to academic projects.

Operations Assistant **May 2024 – Present**

USF Housing & Residential Education *Tampa, FL*

- Managed campus-wide housing key inventory for over **2000** keys and lock workflow systems, maintaining **100%** tracking accuracy across **15+** residential communities
- Coordinated **5** mailroom clerks per shift during peak semester occupancy, improving package processing efficiency by **25%** and reducing resident complaints significantly
- Processed ad hoc maintenance requests, lockouts, and room changes in collaboration with facilities and security teams, cutting response times by **20%**

Projects & Research

Electronics Team Lead | *Society of Aeronautics and Rocketry at USF* **August 2024 – Present**

- Directed a 5-member team to deliver a real-time **Data Acquisition** system for rocket engine tests, ensuring safe cross-team integration with propulsion and mechanical subsystems
- Designed and validated **3** custom **PCBs** for power distribution, signal conditioning, and sensor interfacing, achieving a **20%** reduction in noise and consistent data integrity across **5+** system tests
- Programmed **FreeRTOS-based** firmware in **C++** on **ESP32** microcontrollers to acquire and synchronize data from **3** sensor types (pressure, load cells, thermocouples), improving telemetry reliability and reducing latency by **15%** during live tests

Undergraduate Researcher | *SEES Lab (Secure, Efficient, and Evolvable Systems)* **June 2025 - Present**

- Researched **generative AI** for hardware design by applying large language models to automate **RTL** code generation and verification workflows, advancing methods for AI-assisted circuit designs
- Developing a novel hierarchical **Verilog** dataset aiming at **50–70** designs with varying complexity to establish a standardized evaluation platform for benchmarking **state-of-the-art LLMs** in hardware design
- Designed and executed experiments using **Yosys**, **OpenLane**, and **Sky130** to analyze functionality, complexity, and **PPA** trade-offs of **LLM-generated** hardware modules
- Strengthened research methodology and academic presentation skills through the **CRA UR2PhD** program, contributing toward future peer-reviewed publications in **AI** and **EDA**

RISCV SoC with ML Accelerator | *ASIC Design, Verilog, OpenLane* **April 2025 - Present**

- Designed a single-cycle **RISC-V CPU** in Verilog and integrated a custom ML coprocessor for vector dot-product acceleration, developing instruction decoding, ALU, and control modules
- Verified functionality of implemented instructions through **15+** assembly test programs and waveform analysis, ensuring correct execution and accelerator memory-mapped access
- Synthesized the design using **Yosys** and **OpenLane**, producing a **DRC/LVS-clean GDSII** layout on the **Sky130 PDK** and evaluating preliminary area, timing, and power metrics

Technical Skills

Languages: Python, C/C++, Verilog HDL, SystemVerilog, TCL, RISC-V, HTML/CSS, SQL
Frameworks/Technologies: RTL Design, ASIC Design/Flow, RTOS, Embedded Systems, UART/I2C/SPI, PyTorch, PCB Design. Sky130 PDK
Developer Tools: Git/Github, Cadence Virtuouso, AMD Vivado, OpenLane, Yosys, EasyEDA, VS Code, Arduino IDE, Google Colab, Oscilloscope, Logic Analyzer