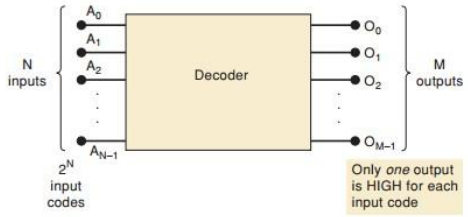
Digital Sytems

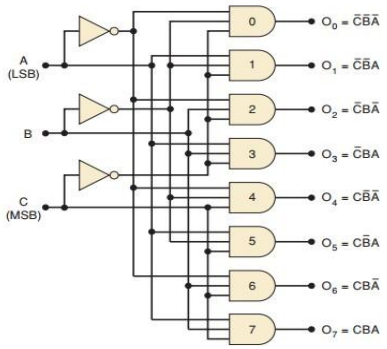
MSI Circuits

Decoders

- A decoder is a logic circuit that accepts a set of inputs that represents a binary number and activates only the output that corresponds to that input number.
- Decoder circuit looks at its inputs, determines which binary number is present there, and activates the one output that corresponds to that number; all other outputs remain inactive.



Decoders

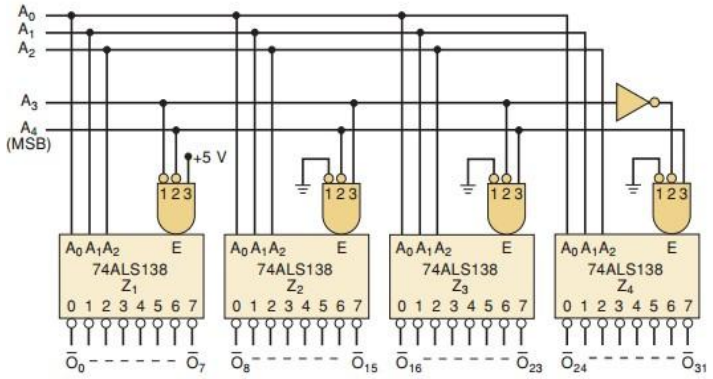


ENABLE Inputs

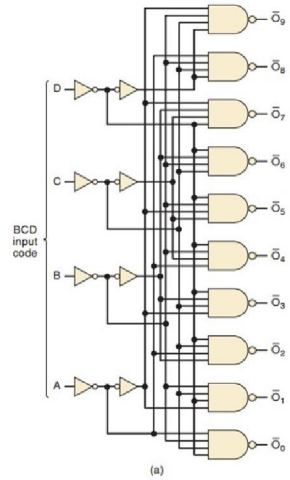
- Some decoders have one or more ENABLE inputs that are used to control the operation of the decoder.
- With ENABLE held LOW, all of the outputs will be forced to the LOW state regardless of the levels at the A, B, C inputs.Thus,the decoder is enabled only if ENABLE is HIGH.

Decoders

(a) Which output will be activated for $A_4A_3A_2A_1A_0$ = 01101 ?
(b) What range of input codes will activate the Z_4 chip?

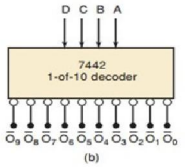


BCD-to-Decimal Decoder



The logic diagram for a 7442 BCD-to-decimal decoder. It is also available as a 74LS42 and a 74HC42.

BCD-to-Decimal Decoder



(b) Logic symbol

Inputs D	C	B	A	Active Output
L	L	L	L	$\overline{O}_0$
L	L	L	H	$\overline{O}_1$
L	L	H	L	$\overline{O}_2$
L	L	H	H	$\overline{O}_3$
L	H	L	L	$\overline{O}_4$
L	H	L	H	$\overline{O}_5$
L	H	H	L	$\overline{O}_6$
L	H	H	H	$\overline{O}_7$
H	L	L	L	$\overline{O}_8$
H	L	L	H	$\overline{O}_9$
H	L	H	L	None
H	L	H	H	None
H	H	L	L	None
H	H	L	H	None
H	H	H	L	None
H	H	H	H	None

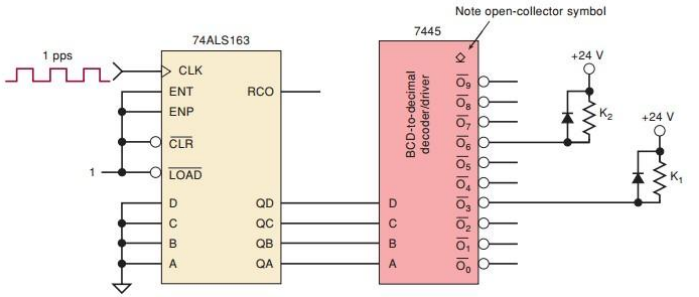
H = HIGH Voltage Level
L = LOW Voltage Level

(c)

- The logic symbol and the truth table for the 7442 are also shown in the figure. Note that this decoder does not have an enable input.

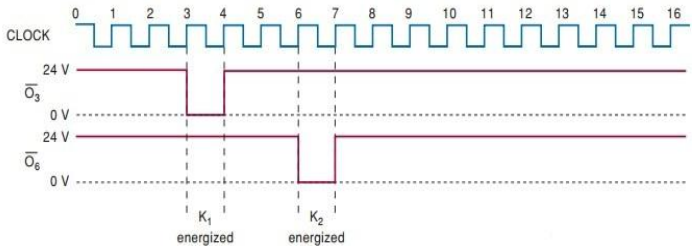
Decoder Applications

Decoders are used whenever outputs are to be activated with specific input levels provided by the outputs of a counter or a register.



Decoder Applications

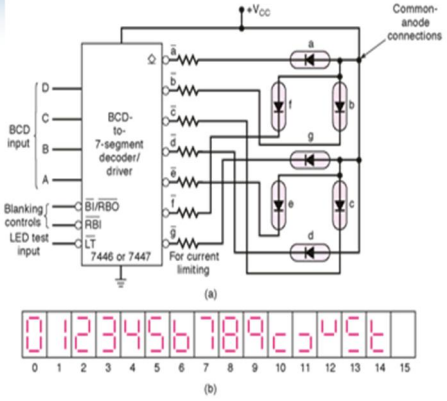
Counter/decoder combination used to provide timing and sequencing operations .



7-Segment LED

(a) 7-segment arrangement; (b) active segments for each digit.

BCD-to-7-segment Decoder/Driver

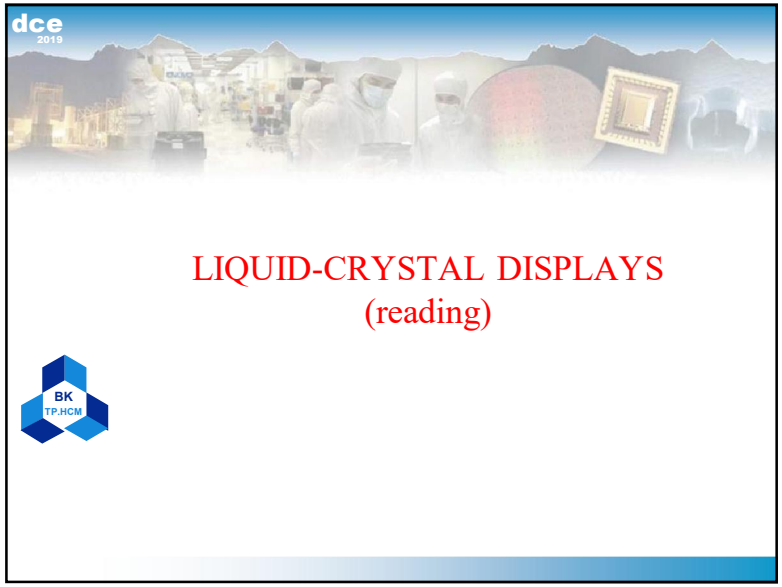


(a) BCD-to-7-segment decoder/driver driving a common-anode 7-segment LED display; (b) segment patterns for all possible input codes.

- A BCD-to-7-segment decoder/driver is used to take a four-bit BCD input and provide the outputs that will pass current through the appropriate segments to display the decimal digit
- The logic for this decoder is complicated because each output is activated for more than one combination of inputs.

Common-Anode Vs Common-Cathode LED Displays

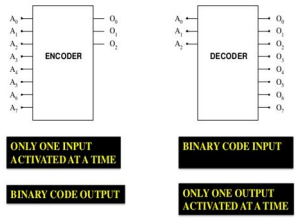
- The LED display used in the previous is a common-anode type because the anodes of all of the segments are tied together to Vcc
- Another type of 7-segment LED display uses a common-cathode arrangement where the cathodes of all of the segments are tied together and connected to ground. This type of display must be driven by a BCD-to-7-segment decoder/driver with active HIGH outputs that apply a HIGH voltage to the anodes of those segments that are to be activated

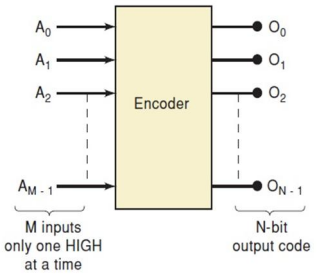


LIQUID-CRYSTAL DISPLAYS
(reading)

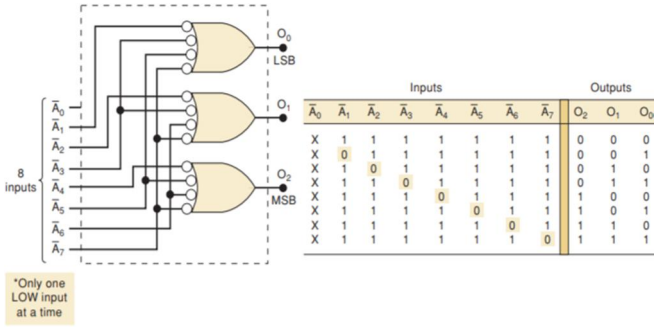
Introduction of Encoders

ENCODERS AND DECODERS





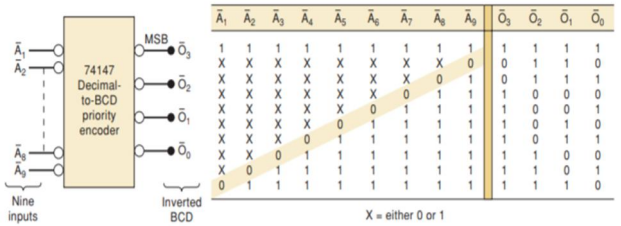
INTRODUCTION OF ENCODERS



Inputs								Outputs		
$\bar{A}_0$	$\bar{A}_1$	$\bar{A}_2$	$\bar{A}_3$	$\bar{A}_4$	$\bar{A}_5$	$\bar{A}_6$	$\bar{A}_7$	O_2	O_1	O_0
X	0	1	1	1	1	1	1	0	0	0
X	1	0	1	1	1	1	1	0	0	1
X	1	1	0	1	1	1	1	0	1	0
X	1	1	1	0	1	1	1	0	1	1
X	1	1	1	1	0	1	1	1	0	0
X	1	1	1	1	1	0	1	1	0	1
X	1	1	1	1	1	1	0	1	1	0

An octal-to-binary encoder (8-line-to-3-line encoder) accepts eight input lines and produces a three-bit output code depending on the active input.

Priority encoder

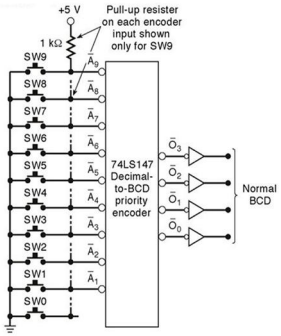


$\bar{A}_1$	$\bar{A}_2$	$\bar{A}_3$	$\bar{A}_4$	$\bar{A}_5$	$\bar{A}_6$	$\bar{A}_7$	$\bar{A}_8$	$\bar{A}_9$	$\bar{O}_3$	$\bar{O}_2$	$\bar{O}_1$	$\bar{O}_0$
1	1	1	1	1	1	1	1	1	1	1	1	1
X	X	X	X	X	X	X	X	0	0	1	1	0
X	X	X	X	X	X	X	0	1	0	1	1	1
X	X	X	X	X	X	0	1	1	1	0	0	0
X	X	X	X	X	0	1	1	1	1	0	0	1
X	X	X	X	0	1	1	1	1	1	0	1	0
X	X	X	0	1	1	1	1	1	1	0	1	1
X	X	0	1	1	1	1	1	1	1	1	0	0
X	0	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	0

X = either 0 or 1

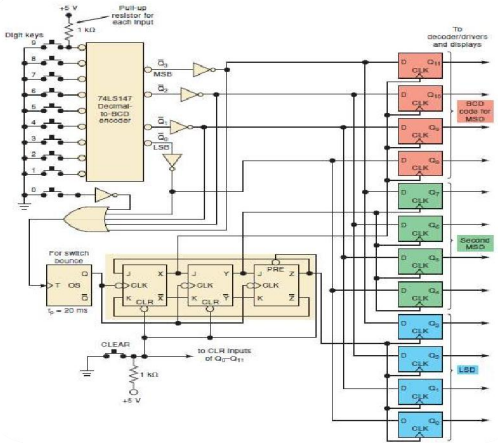
- Priority Encoders: when two or more inputs are activated, the output code will correspond to the highest-numbered input.
- 74147 decimal-to-bcd priority encoder: having 9 active LOW input representing the decimal digit 1 through 9.
  - Producing the INVERTED BCD code corresponding to the highest order activated inputs.

Switch encoder



Decimal-to-BCD Switch Encoder

Switch encoder

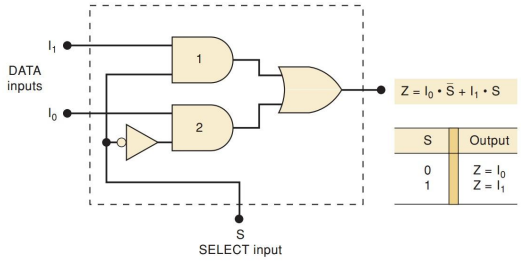


Circuit For Keyboard Entry Of Three-digit Number Into Storage Registers

Multiplexers (Data Selectors)

- **Basic Two-Input Multiplexer**
- **Quad Two-Input MUX (74ALS157/HC157)**
- **Four-Input Multiplexer**
- **Eight-Input Multiplexer**

Basic Two-Input Multiplexer

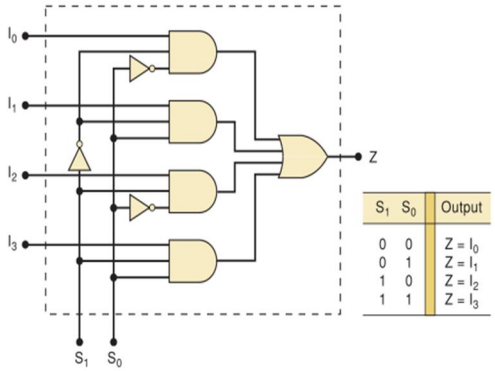


The Boolean expression for the output $Z = I_0\bar{S} + I_1S$

With *S* = 0 this expression becomes: $Z = I_0 \cdot 1 + I_1 \cdot 0 = I_0$ [gate 2 enabled]

With *S* = 1 the expression becomes: $Z = I_0 \cdot 0 + I_1 \cdot 1 = I_1$ [gate 1 enabled]

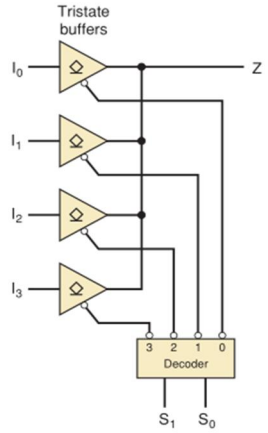
Four-Input Multiplexer



S_1	S_0	Output
0	0	$Z = I_0$
0	1	$Z = I_1$
1	0	$Z = I_2$
1	1	$Z = I_3$

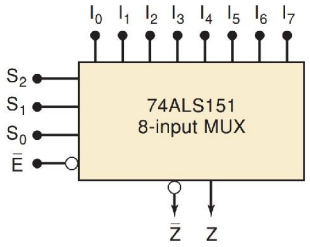
Four-Input Multiplexer

- This approach uses tristate buffers to select one of the signals.
- The decoder ensures that only one buffer can be enabled at any time.
- S_1 and S_0 are used to specify which of the input signals is allowed to pass through its buffer and arrive at the output.



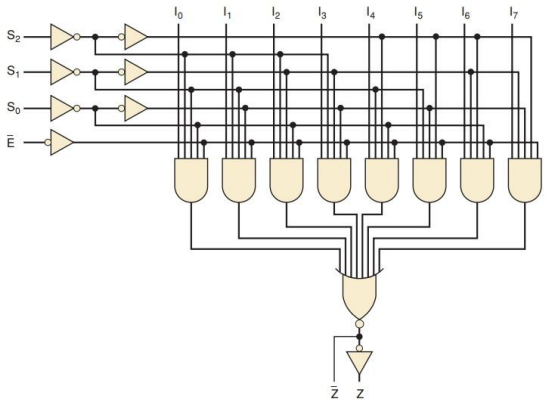
Eight-Input Multiplexer

- This multiplexer has an **enable input** and provides both the normal and the inverted outputs.



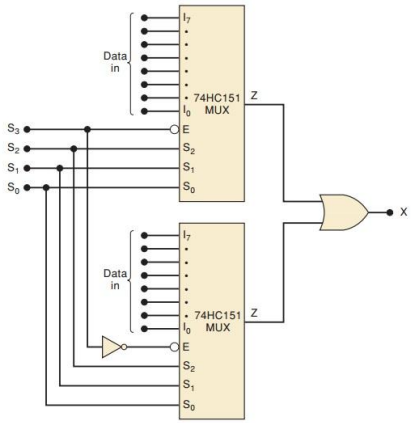
Inputs				Outputs	
$\overline{E}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\overline{I_0}$	I_0
L	L	L	H	$\overline{I_1}$	I_1
L	L	H	L	$\overline{I_2}$	I_2
L	L	H	H	$\overline{I_3}$	I_3
L	H	L	L	$\overline{I_4}$	I_4
L	H	L	H	$\overline{I_5}$	I_5
L	H	H	L	$\overline{I_6}$	I_6
L	H	H	H	$\overline{I_7}$	I_7

Eight-Input Multiplexer



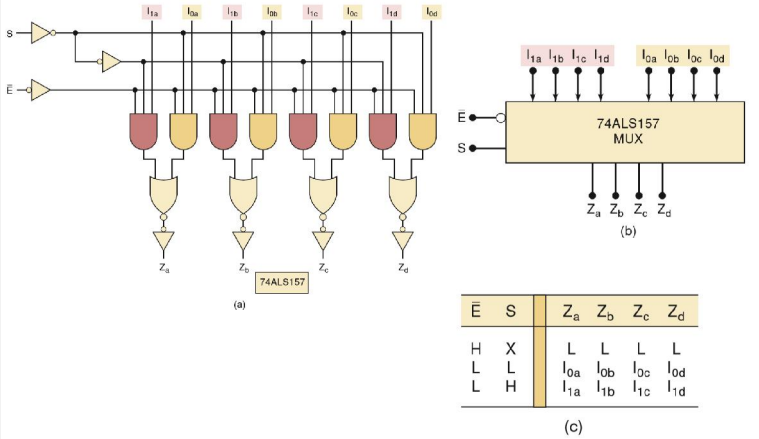
The logic diagram for the 74ALS151 (74HC151) eight-input multiplexer.

Eight-Input Multiplexer



Two 74HC151s combined to form a 16-input multiplexer.

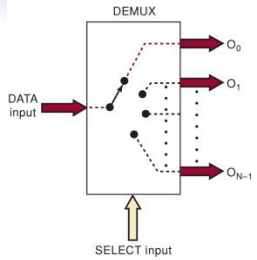
Quad Two-Input MUX (74ALS157/HC157)



$\bar{E}$	S	Z_a	Z_b	Z_c	Z_d
H	X	L	L	L	L
L	L	I_{0a}	I_{0b}	I_{0c}	I_{0d}
L	H	I_{1a}	I_{1b}	I_{1c}	I_{1d}

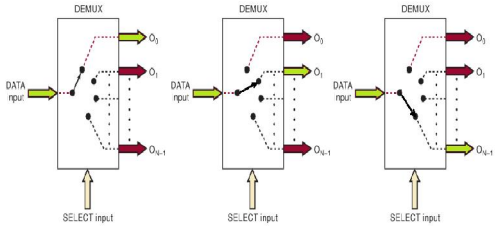
(c)

Demultiplexer

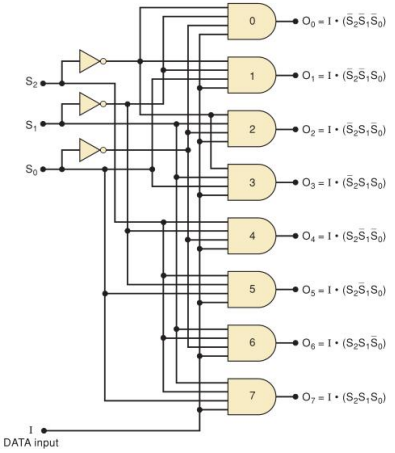


Demultiplexer (DEMUX): reverse operation of multiplexer

=> takes a single input and distributes it over several outputs



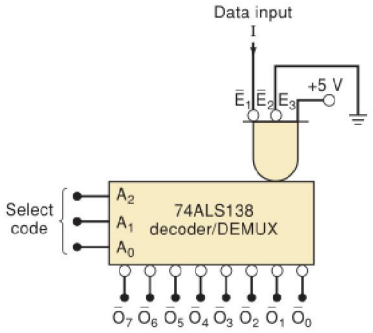
1-Line-to-8-Line Demux



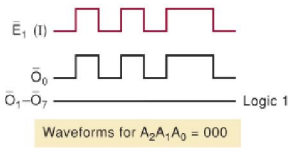
For example:
When $S_0S_1S_2$=000
+ only AND gate 0 is enabled.
+ data input I will appear at output O_0.

SELECT code			OUTPUTS							
S_2	S_1	S_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
0	0	0	0	0	0	0	0	0	0	I
0	0	1	0	0	0	0	0	0	I	0
0	1	0	0	0	0	0	0	I	0	0
0	1	1	0	0	0	0	I	0	0	0
1	0	0	0	0	0	I	0	0	0	0
1	0	1	0	0	I	0	0	0	0	0
1	1	0	0	I	0	0	0	0	0	0
1	1	1	I	0	0	0	0	0	0	0

1-Line-to-8-Line Demux



-E_2' and E_3 are always held in their active states.
=> The output follow the signal on E_1'.



Waveforms for $A_2A_1A_0$ = 000

-Case $A_2A_1A_0$=000: Only O_0' output is actived.

Security Monitoring System

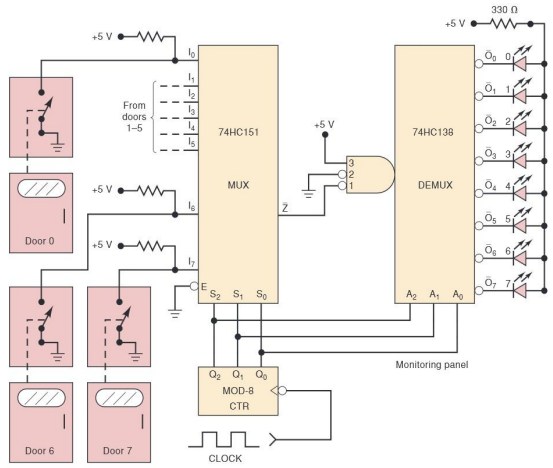
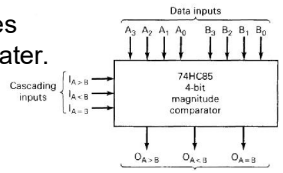


FIGURE 9-31 Security monitoring system.

MAGNITUDE COMPARATOR

- A combination logic circuit that indicates which of 2 binary quantity inputs is greater.
  - The 74HC85 compares 2 unsigned 4-bit binary number.
  - The 74HC85 has 3 active-HIGH outputs (for 3 states of result)

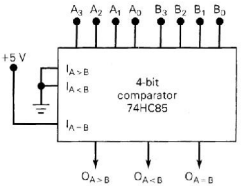


TRUTH TABLE

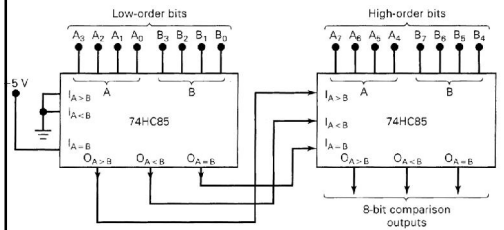
COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

CASCADING INPUT



(a)



(b)

- Expand the comparison operation to more than 4 bits
- The inputs are labeled the same as the outputs.
- When 2 comparators are to be cascaded, the output of the lower-order one is connected to the input of higher-order one.

APPLICATION

- Useful in control applications where a binary number represent the physical variable.

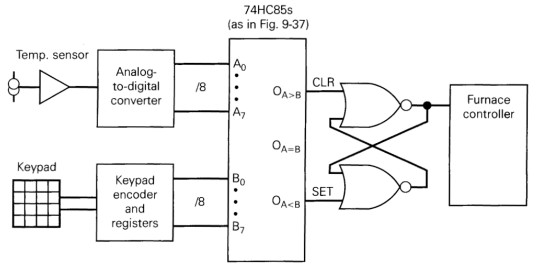
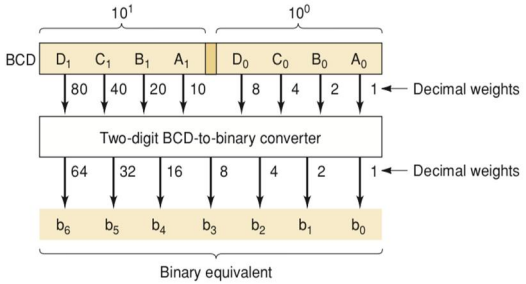


FIGURE 9-38 Magnitude comparator used in a digital thermostat.

CODE CONVERTERS

- BASIC IDEA



CODE CONVERTERS

- Conversion Process

BCD Bit	Decimal Weight	Binary Equivalent						
		b_6	b_5	b_4	b_3	b_2	b_1	b_0
A_0	1	0	0	0	0	0	0	1
B_0	2	0	0	0	0	0	1	0
C_0	4	0	0	0	0	1	0	0
D_0	8	0	0	0	1	0	0	0
A_1	10	0	0	0	1	0	1	0
B_1	20	0	0	1	0	1	0	0
C_1	40	0	1	0	1	0	0	0
D_1	80	1	0	1	0	0	0	0

CODE CONVERTERS

- EXAMPLE

Convert 01010010 (BCD for decimal 52) to binary. Repeat for 10010101 (decimal 95).

Solution

Write down the binary equivalents for all the 1s in the BCD
Then add them all together in binary.

01010010 (BCD)
→0000010 (binary for 2)
→0001010 (binary for 10)
→+ 0101000 (binary for 40)
0110100 (binary for 52)

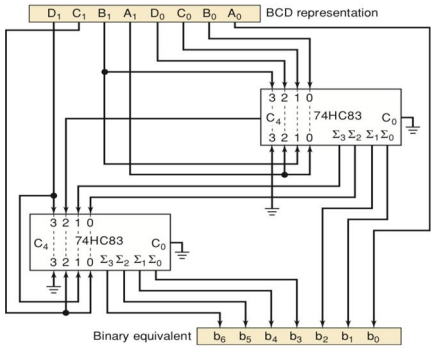
10010101 (BCD)
→0000001 (binary for 1)
→0000100 (binary for 4)
→0001010 (binary for 10)
→+ 1010000 (binary for 80)
1011111 (binary for 95)

BCD Bit	Decimal Weight	Binary Equivalent						
		b_6	b_5	b_4	b_3	b_2	b_1	b_0
A_0	1	0	0	0	0	0	0	1
B_0	2	0	0	0	0	0	1	0
C_0	4	0	0	0	0	1	0	0
D_0	8	0	0	0	1	0	0	0
A_1	10	0	0	0	1	0	1	0
B_1	20	0	0	1	0	1	0	0
C_1	40	0	1	0	1	0	0	0
D_1	80	1	0	1	0	0	0	0

CODE CONVERTERS

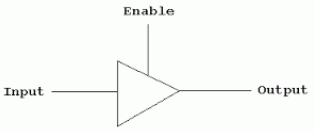
Circuit Implementation

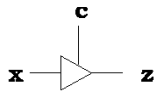
Clearly, one way to implement the logic circuit that performs this conversion process is to use binary adder circuits. Figure 9-40 shows how two 74HC83



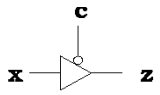
Tristate buffer

Enable	Input	Output
0	0	Disconnected
0	1	Disconnected
1	0	0
1	1	1



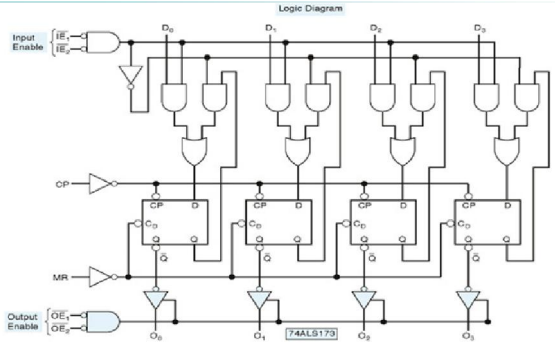


tri–state buffer with active high control



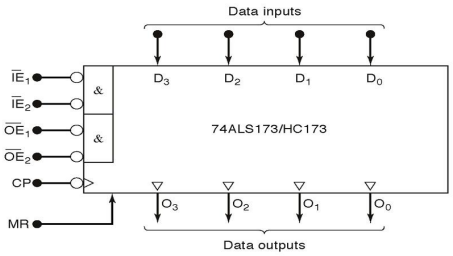
tri–state buffer with active low control

74ALS173 tristate register



Inputs					FF Outputs
MR	CP	$\overline{IE}_1$	$\overline{IE}_2$	D_n	Q
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

74ALS173 tristate register

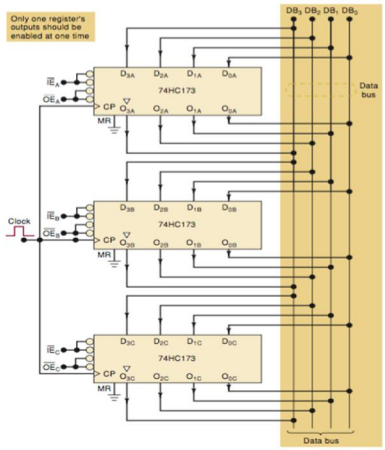


Note:
▽ indicates a tristate output

Data Bus Operation for register-to-register data transfer:

In this arrangement:

- Corresponding outputs of each register are connected to the same data bus line *(e.g., O3A, O3B, and O3C are connected to DB3).*
- The three registers have their outputs connected together.
- Only one register have its outputs enabled and that the other two register outputs re-main in the Hi-Z state.
- Corresponding register inputs are also tied to the same bus line. the levels on the bus will always be ready to be transferred to one or more of the registers depending on the *IE* inputs.



Describe the input signal requirements for transferring [A] → [C]:

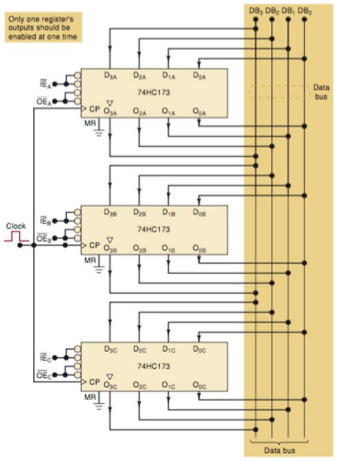
First, only register A should have its outputs enabled:

- OEA =0, OEB =OEC =1

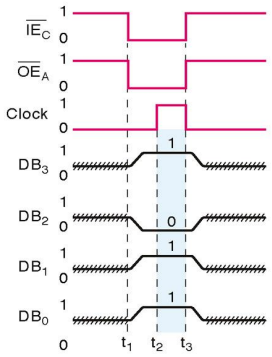
Next, only register C should have its inputs enabled:

- IEC =0 IEA =IEB =1

Finally, a clock pulse is required to transfer the data from the bus into the register C flip-flops.



Bus Signals



NOTES:

= floating (Hi-Z)

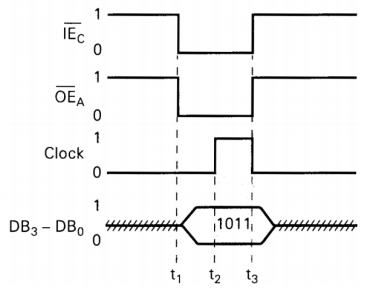
t_1: Register A outputs are enabled. Its data are placed on the data bus lines.

t_2: The PGT of the clock transfers valid data from data bus into register C.

t_3: Register A outputs are disabled and data bus lines return to Hi-Z state.

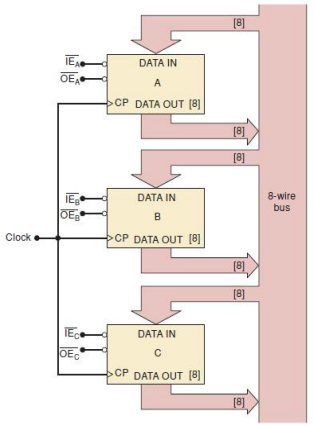
Simplified Bus Timing Diagram:

Use only a single timing waveform to represent the complete set of bus lines.



Simplified Bus Representation:

The numbers in brackets([]) indicate the number of bits register and number of lines data bus



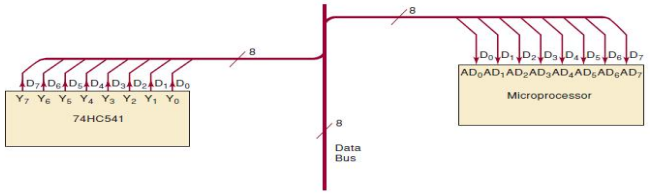
Simplified representation of bus arrangement.

Simplified Bus Representation:

Bundle method:

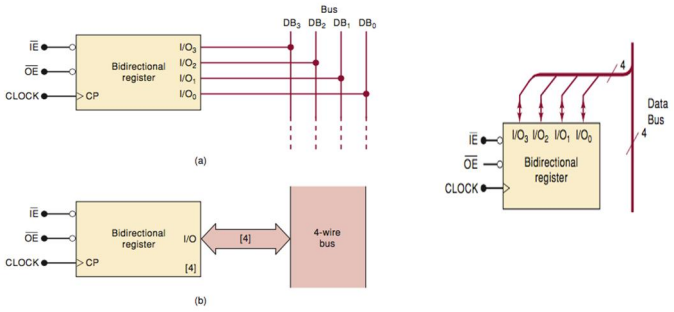
A single line denotes the data bus

"/8" denotes an eight-line data bus



Bidirectional Busing:

Bidirectional register connected to data bus



- Some devices have both inputs and outputs connected to the data bus.
  - ➢ Inputs and outputs are connected together internal to the chip
    - ❖Reduce the number of IC pins
    - ❖Reduce number of connections to the bus