Digital Systems Review

Tran Ngoc Thinh
HCMC University of Technology
http://www.cse.hcmut.edu.vn/~tnthinh

Kmap

- The minimum SOP

$$F(D,C,B,A) = \sum(0,1,2,4,5,7,9,12) + \sum d(10,11,14,15)$$

a) D'B' + C'BA' + DC'A + D'CA
b) D'B' + DB + C'BA' + DC'A + D'CA + DCA'
c) C'BA' + CB'A' + D'CA + C'B'A
d) D'B' + C'BA' + DCA' + DC'A + D'CA
e) CB'A' + C'B'A + D'CA + D'C'A'

Boolean Algebra

- Find the SOP minimum form :
  - **F (DCBA) = ∑(0,1,2,8,11,12) + d(3,9,13)**
    A. A'B' + A'C'+ B'D
    B. D'C' + DB' + C'A
    C. D'C + DB + C'A

  - **X = B(A+C) + C((AB)'.A)'**
    A. F = A'C + BC
    B. F = AB + A'C
    C. F = ABC + A'C
    D. F = AB + BC + A'C
    E. F = 1

Boolean Algebra

1)Choose a FALSE statement:

a) An AND gate can be used as a merging circuit
b) A NOR gate can be used as a enable/disable circuit
c) A XNOR gate can be used as a selectable inversion circuit
d) All above statements are FALSE

2) Convert these numbers: 275_{10} and 641_{10} into BCD format and perform a BCD addition.

a) 100010110110_{BCD}
b) 100110110110_{BCD}
c) 100100010110_{BCD}
d) 100100010100_{BCD}

Design

- A combinational circuit with 4 inputs A, B, C, D and 1 output X. Output X = A' when and only if B, C are at level 0 (LOW) or C=D. With remaining cases, output X = 0. The Boolean algebra for the output X is:

a) A'.(B.C + C'.D' + C.D)'

b) A'.(B'.C' + C'.D' + C.D)

c) A' + (B' + C').(C'.D' + C.D)

d) A' + (B'.C' + (C ⊕ D))

e) A'.(B.C + (C ⊕ D)')

Arithmetic

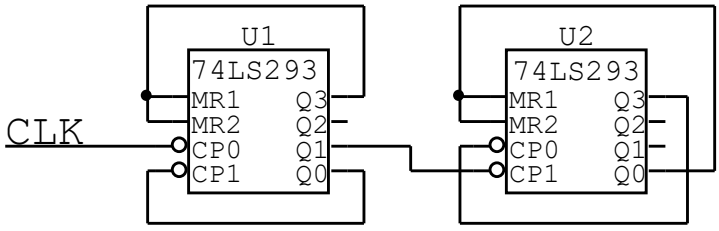
1. The fast carry or look-ahead carry circuits found in most 4-bit parallel-adder circuits

a. add a 1 to complemented inputs
b. increase ripple delay
c. reduce propagation delay
d. determine sign and magnitude

2) How many bits would be required to represent decimal numbers from -32,768 to + 32,767?

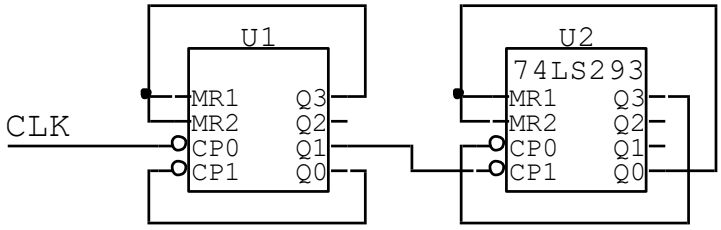
a) 16
b) 15
c) 14
d) 13

Counter 74293 (1)



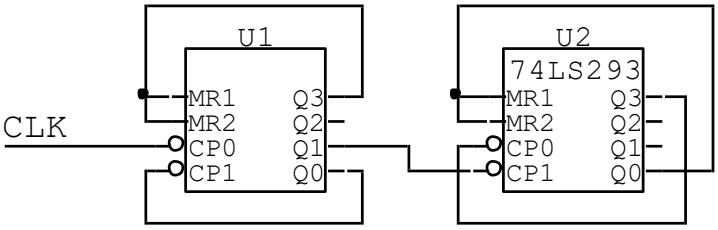
- Determine the frequency at Q3 of U2, *Given* f_{CLK}= **100 KHz**
  A. 6.25 KHz
  B. ≈ 7.14 KHz
  C. ≈ 3.57 KHz
  D. 3.125 KHz
  E. 1.5625 KHz

Counter 74293 (2)



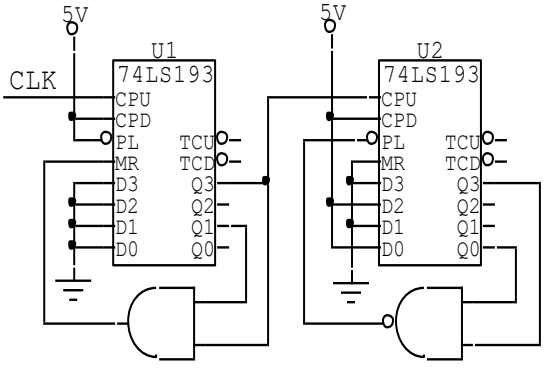
- Assume that the initial value of the counter **$Q_3Q_2Q_1Q_0$ (U1) = 0011** and **$Q_3Q_2Q_1Q_0$ (U2) = 1100**. Determine the state of **$Q_3Q_2Q_1Q_0$ (U2)** after next 5 clock cycles of CLK.
  A. 0000
  B. 1110
  C. 0111
  D. 1101

Counter 74293 (3)

- 

- Determine MOD of the counter
  A. 8
  B. 16
  C. 32
  D. 56
  E. 64

Counter

- 

- MOD?
- 40
- 45
- 50
- 90

MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⎍	H	Count Up
L	H	H	⎍	Count Down

Registers

1. In contrast to a binary counter, how many extra Flip-Flops does a ring counter use if both counters are MOD-8?
   a. 3
   b. 4
   c. 5
   d. 6

2. In contrast to a binary counter, how many extra Flip-Flops does a Johnson counter use if both counters are MOD-8?
   a) 4
   b) 3
   c) 2
   d) 1

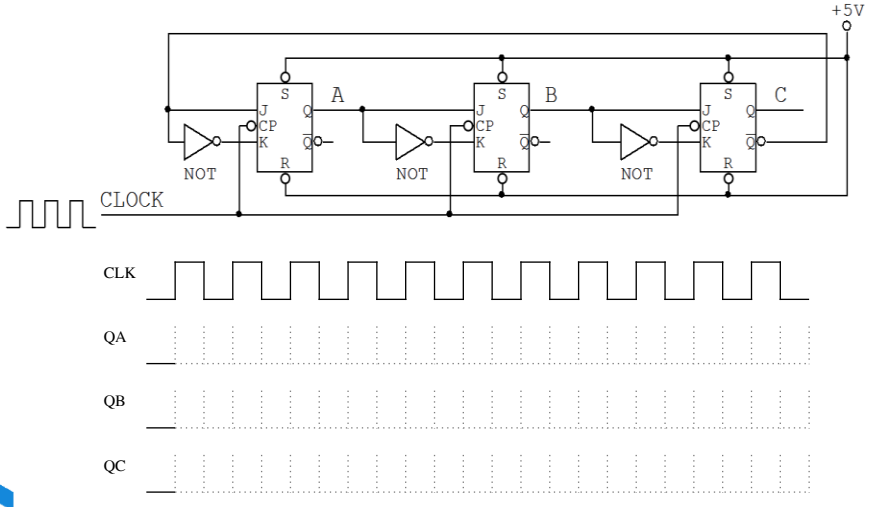
Registers

1. Given 8-bit shift register X = 10101111 and Data input at HIGH(1) connected with MSB bit, after shift right 6 clock cycles, the value of register X is:
   a. 10101111
   b. 11111110
   c. 11101011
   d. 11111111

2. Given 8-bit shift register X = 10101111 and 8-bit shift register Y = 00000000, MSB bit of X connects with LSB bit of Y. After shift left six(6) clock cycles, the value of register Y is:
   a) 10101111
   b) 10111100
   c) 00101011
   d) 11101011

Timing diagram

- Sketch a timing diagram showing the waveforms of Qa, Qb, Qc and Qd as following circuit. Note that CP (clock), S (preset), R (reset).



MSI Circuits

1) What are the outputs of a 7485 four-bit magnitude comparator when the inputs are A = 0001 and B = 0100?

A) A<B is 0 A=B is 1 A>B is 1
B) A<B is 0 A=B is 1 A>B is 0
C) A<B is 1 A=B is 0 A>B is 0
D) A<B is 0 A=B is 0 A>B is 1

2) Which device is used in computer hardware to interpret the binary code of the computer instruction?

A) decoder
B) multiplexer
C) encoder
D) demultiplexer

Design

- Construct an 8-to-1 MUX using any number of 4-to-1 and 2-to-1 MUXs as building blocks. Use the smallest number of component MUXs that you can.
- .

Decoder Example (1)

- Draw the diagram to show how to realize the functions $F(W,X,Y) = \sum(1,3,5,6)$ and $G(W,X,Y) = \sum(2,3,4,7)$ using only a single 74LS138 and two NAND gates.
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Decoder Example (2)

- Draw the diagram to show how to realize the functions F(A,B,C,D) = ∑(2,4,6,14) using only one 74LS138 and one NAND gates.

MUX Example (1)

- Draw the diagram to show how to realize the functions F(W,X,Y) = ∏(3,4,5,6,7) using only a 74LS151.
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MUX Example (2)

- Draw the diagram to show how to realize the functions F(A,B,C,D) = ∑(2,4,6,14) using only a 74LS151.
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MUX homework

- Draw the diagram to show how to realize the functions F(A,B,C,D) = ∑(1,5,7,8,9,13,14) (with B, C, and D as the control inputs) using only a 74LS151.