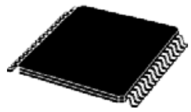
VNH5019A-E

Automotive fully integrated H-bridge motor driver

Features

Type	$R_{DS(on)}$	I_{out}	V_{ccmax}
VNH5019A-E	18 mΩ typ (per leg)	30 A	41 V

- ECOPACK®: lead free and RoHS compliant
- Automotive Grade: compliance with AEC guidelines
- Output current: 30 A
- 3 V CMOS compatible inputs
- Undervoltage and overvoltage shutdown
- High-side and low-side thermal shutdown
- Cross-conduction protection
- Current limitation
- Very low standby power consumption
- PWM operation up to 20 khz
- Protection against:
  – Loss of ground and loss of V_{CC}
- Current sense output proportional to motor current
- Charge pump output for reverse polarity protection
- Output protected against short to ground and short to V_{CC}



MultiPowerSO-30™

Description

The VHN5019A-E is a full bridge motor driver intended for a wide range of automotive applications. The device incorporates a dual monolithic high-side drivers and two low-side switches. The high-side driver switch is designed using STMicroelectronics' well known and proven proprietary VIPower® M0 technology that allows to efficiently integrate on the same die a true Power MOSFET with an intelligent signal/protection circuit.

The three dice are assembled in MultiPowerSO-30 package on electrically isolated lead-frames. This package, specifically designed for the harsh automotive environment offers improved thermal performance thanks to exposed die pads. The input signals IN_A and IN_B can directly interface to the microcontroller to select the motor direction and the brake condition.

The $DIAG_A/EN_A$ or $DIAG_B/EN_B$, when connected to an external pull-up resistor, enable one leg of the bridge. They also provide a feedback digital diagnostic signal. The CS pin allows to monitor the motor current by delivering a current proportional to its value when CS_DIS pin is driven low or left open. The PWM, up to 20 KHz, lets us to control the speed of the motor in all possible conditions. In all cases, a low-level state on the PWM pin turns-off both the LS_A and LS_B switches. When PWM rises to a high-level, LS_A or LS_B turn-on again depending on the input pin state.

Output current limitation and thermal shutdown protects the concerned high-side in short to ground condition.

The short to battery condition is revealed by the overload detector or by thermal shutdown that latches off the relevant low-side.

Active V_{CC} pin voltage clamp protects the device against low energy spikes in all configurations for the motor.

CP pin provides the necessary gate drive for an external n-channel PowerMOS used for reverse polarity protection.

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1 Block diagram and pin description

Figure 1. Block diagram

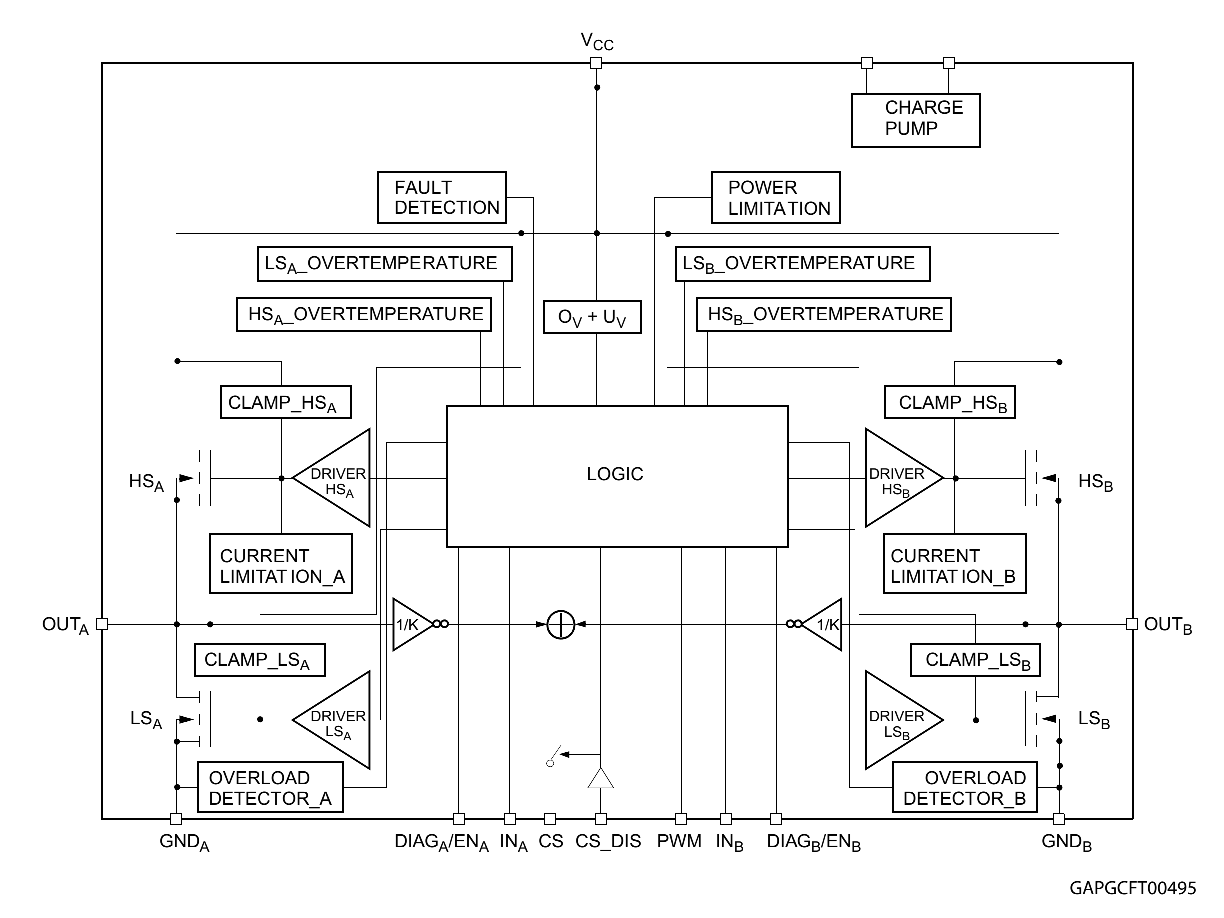


Figure 2. Configuration diagram (top view)

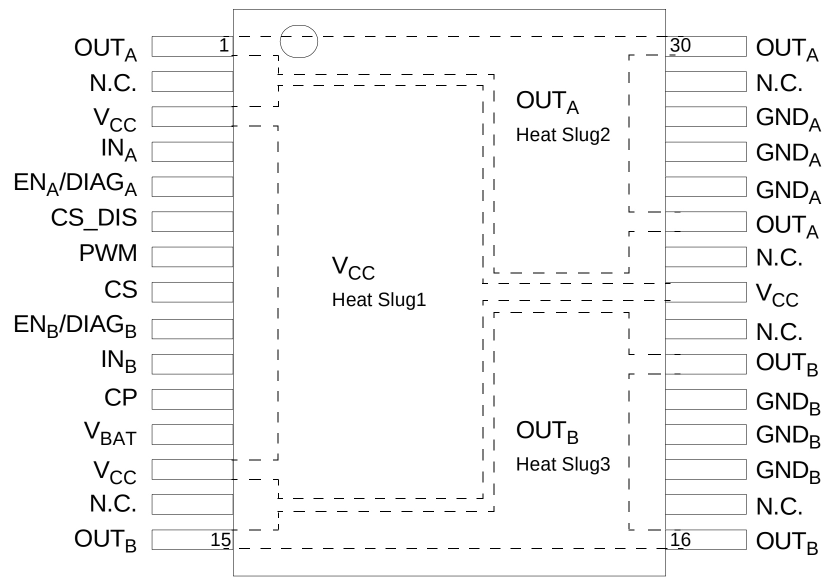


Table 1. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	OUTx	INPUTx, PWM DIAGx/ENx CS_DIS
Floating	Not allowed	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 10 kΩ resistor

Table 2. Pin definitions and functions

Pin	Symbol	Function
1, 25, 30	OUT$_A$, Heat Slug2	Source of high-side switch A / drain of low-side switch A, power connection to the motor
2,14,17, 22, 24,29	N.C.	Not connected
3, 13, 23	V$_{CC}$, Heat Slug1	Drain of high-side switches and connection to the drain of the external PowerMOS used for the reverse battery protection
12	V$_{BAT}$	Battery connection and connection to the source of the external PowerMOS used for the reverse battery protection
5	EN$_A$/DIAG$_A$	Status of high-side and low-side switches A; open drain output. This pin must be connected to an external pull-up resistor. When externally pulled low, it disables half-bridge A. In case of fault detection (thermal shutdown of a high-side FET or excessive ON-state voltage drop across a low-side FET), this pin is pulled low by the device (see *Table 13: Truth table in fault conditions (detected on OUTA)*)

Table 2. Pin definitions and functions (continued)

Pin	Symbol	Function
6	CS_DIS	Active high CMOS compatible pin to disable the current sense pin
4	IN_A	Clockwise input. CMOS compatible
7	PWM	PWM input. CMOS compatible.
8	CS	Output of current sense. This output delivers a current proportional to the motor current, if CS_DIS is low or left open. The information can be read back as an analog voltage across an external resistor.
9	EN_B/$DIAG_B$	Status of high-side and low-side switches B; Open drain output. This pin must be connected to an external pull up resistor. When externally pulled low, it disables half-bridge B. In case of fault detection (thermal shutdown of a high-side FET or excessive ON-state voltage drop across a low-side FET), this pin is pulled low by the device (see *Table 13: Truth table in fault conditions (detected on OUTA)*.
10	IN_B	Counter clockwise input. CMOS compatible
11	CP	Connection to the gate of the external MOS used for the reverse battery protection
15, 16, 21	OUT_B, Heat Slug3	Source of high-side switch B / drain of low-side switch B, power connection to the motor
26, 27, 28	GND_A	Source of low-side switch A and power ground[1]
18, 19, 20	GND_B	Source of low-side switch B and power ground[1]

1. GNDA and GNDB must be externally connected together

Table 3. Block descriptions[1]

Name	Description
Logic control	Allows the turn-on and the turn-off of the high-side and the low-side switches according to the *Table 12*.
Overvoltage + undervoltage	Shut down the device outside the range [4.5 V to 24 V] for the battery voltage.
High-side, low-side and clamp voltage	Protect the high-side and the low-side switches from the high-voltage on the battery line in all configuration for the motor.
High-side and low-side driver	Drive the gate of the concerned switch to allow a proper $R_{DS(on)}$ for the leg of the bridge.
Linear current limiter	Limits the motor current, by reducing the high-side switch gate-source voltage when short-circuit to ground occurs.
High-side and low-side overtemperature protection	In case of short-circuit with the increase of the junction's temperature, it shuts down the concerned driver to prevent its degradation and to protect the die.
Low-side overload detector	Detects when low-side current exceeds shutdown current and latches off the concerned low-side.

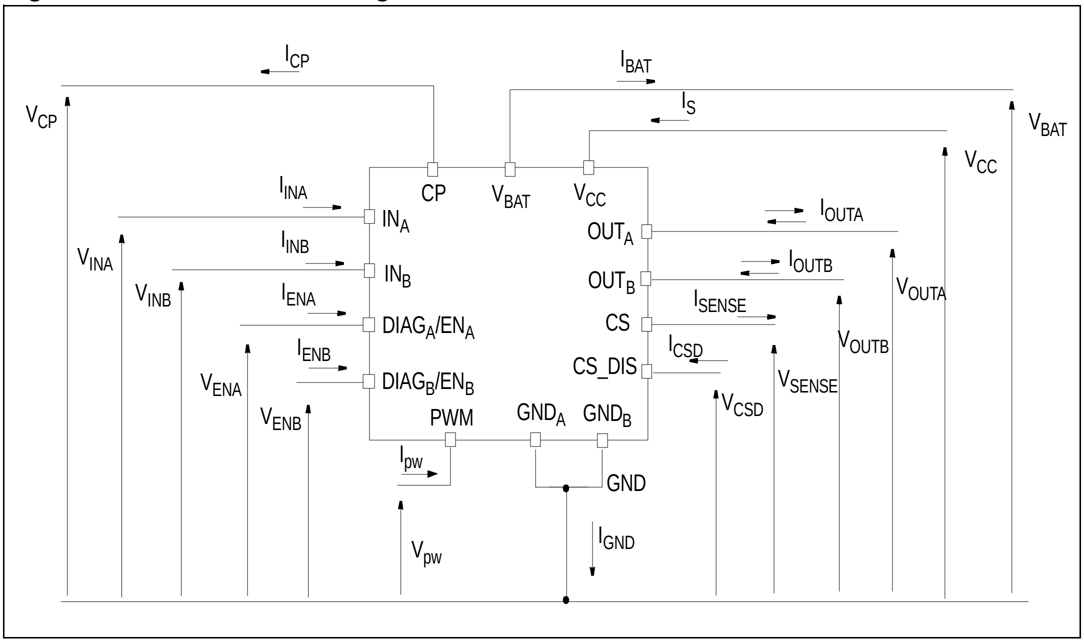
Table 3. Block descriptions[(1)] (continued)

Name	Description
Charge pump	Provides the voltage necessary to drive the gate of the external PowerMOS used for the reverse polarity protection
Fault detection	Signalizes an abnormal condition of the switch (output shorted to ground or output shorted to battery) by pulling down the concerned ENx/DIAGx pin.
Power limitation	Limits the power dissipation of the high-side driver inside safe range in case of short to ground condition.

1. See *Figure 1*

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document.

Table 4. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{BAT}	Maximum battery voltage(1)	-16 +41	V V
V_{CC}	Maximum bridge supply voltage	+ 41	V
I_{max}	Maximum output current (continuous)	30	A
I_R	Reverse output current (continuous)	-30	A
I_{IN}	Input current (IN_A and IN_B pins)	+/- 10	mA
I_{EN}	Enable input current ($DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins)	+/- 10	mA
I_{pw}	PWM input current	+/- 10	mA
I_{CP}	CP output current	+/- 10	mA
I_{CS_DIS}	CS_DIS input current	+/- 10	mA

Table 4. Absolute maximum rating (continued)

Symbol	Parameter	Value	Unit
V_{CS}	Current sense maximum voltage	V_{CC} - 41 $+V_{CC}$	V V
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 kΩ, C = 100 pF)	2	kV
T_c	Case operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

1. This applies with the n-channel MOSFET used for the reverse battery protection. Otherwise V_{BAT} has to be shorted to V_{CC}.

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case HSD	1.7	°C/W
	Thermal resistance junction-case LSD	3.2	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	See *Figure 18*	°C/W

2.3 Electrical characteristics

Values specified in this section are for 8 V < V_{CC} < 21 V, -40 °C < T_j < 150 °C, unless otherwise specified.

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating bridge supply voltage		5.5		24	V
I_S	Supply current	OFF-state with all fault cleared and ENx = 0 V (standby): $IN_A = IN_B$ = PWM = 0; T_j = 25 °C; V_{CC} = 13 V $IN_A = IN_B$ = PWM = 0 OFF-state (no standby): $IN_A = IN_B$ = PWM = 0; ENx = 5 V		10	15 60 6	µA µA mA
		ON-state: IN_A or IN_B = 5 V, no PWM IN_A or IN_B = 5 V, PWM = 20 kHz		4	8 8	mA mA
R_{ONHS}	Static high-side resistance	I_{OUT} = 15 A; T_j = 25 °C		12.0		mΩ
		I_{OUT} = 15 A; T_j = - 40 °C to 150 °C			26.5	
R_{ONLS}	Static low-side resistance	I_{OUT} = 15 A; T_j = 25 °C		6.0		mΩ
		I_{OUT} = 15 A; T_j = - 40 °C to 150 °C			11.5	
V_f	High-side free-wheeling diode forward voltage	I_f = 15 A, T_j = 150 °C		0.6	0.8	V
$I_{L(off)}$	High-side OFF-state output current (per channel)	T_j = 25 °C; $V_{OUTX} = EN_X$ = 0 V; V_{CC} = 13 V			3	µA
		T_j = 125 °C; $V_{OUTX} = EN_X$ = 0 V; V_{CC} = 13 V			5	

Table 7. Logic inputs (IN_A, IN_B, EN_A, EN_B, PWM, CS_DIS)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level input voltage	Normal operation ($DIAG_X/EN_X$ pin acts as an input pin)			0.9	V
V_{IH}	High-level input voltage	Normal operation ($DIAG_X/EN_X$ pin acts as an input pin)	2.1			V
I_{INL}	Low-level input current	V_{IN} = 0.9 V	1			µA
I_{INH}	High-level input current	V_{IN} = 2.1 V			10	µA
V_{IHYST}	Input hysteresis voltage	Normal operation ($DIAG_X/EN_X$ pin acts as an input pin)	0.15			V

Table 7. Logic inputs (IN_A, IN_B, EN_A, EN_B, PWM, CS_DIS) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5	6.3	7.5	V
		I_{IN} = -1 mA	-1.0	-0.7	-0.3	
V_{DIAG}	Enable low-level output voltage	Fault operation ($DIAG_X/EN_X$ pin acts as an output pin); I_{EN} = 1 mA			0.4	V

Table 8. Switching (V_{CC} = 13 V, R_{LOAD} = 0.87 Ω, Tj = 25 °C)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f	PWM frequency		0		20	kHz
$t_{d(on)}$	HSD rise time	Input rise time < 1µs (see *Figure 9*)			250	µs
$t_{d(off)}$	HSD fall time	Input rise time < 1µs (see *Figure 9*)			250	µs
t_r	LSD rise time	(see *Figure 8*)		1	2	µs
t_f	LSD fall time	(see *Figure 8*)		1	2	µs
t_{DEL}	Delay time during change of operating mode	(see *Figure 7*)	200	400	1600	µs
t_{rr}	High-side free wheeling diode reverse recovery time	(see *Figure 10*)		110		ns
I_{RM}	Dynamic cross-conduction current	I_{OUT} = 15 A (see *Figure 10*)		2		A

Table 9. Protection and diagnostic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{USD}	V_{CC} undervoltage shutdown			4.5	5.5	V
$V_{USDhyst}$	V_{CC} undervoltage shutdown hysteresis			0.5		V
V_{OV}	V_{CC} overvoltage shutdown		24	27	30	V
I_{LIM_H}	High-side current limitation		30	50	70	A
I_{SD_LS}	Low-side shutdown current		70	115	160	A
V_{CLPHS}(1)	High-side clamp voltage (V_{CC} to OUT_A = 0 or OUT_B = 0)	I_{OUT} = 15 A	43	48	54	V
V_{CLPLS}(1)	Low-side clamp voltage (OUT_A = V_{CC} or OUT_B = V_{CC} to GND)	I_{OUT} = 15 A	27	30	33	V
T_{TSD}(2)	Thermal shutdown temperature	V_{IN} = 2.1 V	150	175	200	°C

Table 9. Protection and diagnostic (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T_{TSD_LS}	Low-side thermal shutdown temperature	$V_{IN} = 0$ V	150	175	200	°C
T_{TR}(3)	Thermal reset temperature		135			°C
T_{HYST}(3)	Thermal hysteresis		7	15		°C

1. The device is able to pass the ESD and ISO pulse requirements as specified in the *Table 15*.
2. T_{TSD} is the minimum threshold temperature between HS and LS
3. Valid for both HSD and LSD

Table 10. Current sense (8 V < V_{CC} < 21 V)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
K_0	I_{OUT}/I_{SENSE}	$I_{OUT} = 3$ A, $V_{SENSE} = 0.5$ V, $T_j = -40$ °C to 150°C	4670	7110	10110	
dK_0/K_0	Analog current sense ratio drift	$I_{OUT} = 3$ A; $V_{SENSE} = 0.5$ V, $T_j = -40$ °C to 150 °C	-19		19	%
K_1	I_{OUT}/I_{SENSE}	$I_{OUT} = 8$ A, $V_{SENSE} = 1.3$V, $T_j = -40$ °C to 150°C	6060	7030	8330	
dK_1/K_1	Analog current sense ratio drift	$I_{OUT} = 8$ A; $V_{SENSE} = 1.3$V, $T_j = -40$ °C to 150 °C	-14		14	%
K_2	I_{OUT}/I_{SENSE}	$I_{OUT} = 15$ A, $V_{SENSE} = 2.4$ V, $T_j = -40$ °C to 150°C	6070	6990	7810	
dK_2/K_2	Analog current sense ratio drift	$I_{OUT} = 15$ A; $V_{SENSE} = 2.4$ V, $T_j = -40$ °C to 150 °C	-12		12	%
K_3	I_{OUT}/I_{SENSE}	$I_{OUT} = 25$ A, $V_{SENSE} = 4$ V, $T_j = -40$ °C to 150°C	6000	6940	7650	
dK_3/K_3	Analog current sense ratio drift	$I_{OUT} = 25$ A; $V_{SENSE} = 4$ V, $T_j = -40$ °C to 150 °C	-12		12	%
V_{SENSE}	Max analog sense output voltage	$I_{OUT} = 15$ A, $R_{SENSE} = 1.1$ kΩ	5			V
I_{SENSEO}	Analog sense leakage current	$I_{OUT} = 0$ A, $V_{SENSE} = 0$ V, $V_{CSD} = 5$ V, $V_{IN} = 0$ V, $T_j = -40$ to 150°C	0		5	µA
		$I_{OUT} = 0$ A, $V_{SENSE} = 0$ V, $V_{CSD} = 0$ V, $V_{IN} = 5$ V, $T_j = -40$ to 150°C	0		100	
$t_{DSENSEH}$	Delay response time from falling edge of CS_DIS pin	$V_{IN} = 5$ V, $V_{SENSE} < 4$ V, $I_{OUT} = 8$ A, $I_{SENSE} = 90\%$ of $I_{SENSEmax}$ (see fig *Figure 13*)			50	µs
$t_{DSENSEL}$	Delay response time from rising edge of CS_DIS pin	$V_{IN} = 5$ V, $V_{SENSE} < 4$ V, $I_{OUT} = 8$ A, $I_{SENSE} = 10\%$ of $I_{SENSEmax}$ (see fig *Figure 13*)			20	µs

Table 11. Charge pump

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CP}	Charge pump output voltage	$EN_X = 5$ V	$V_{CC} + 5$		$V_{CC} + 10$	V
		$EN_X = 5$ V, $V_{CC} = 4.5$ V		10.5		
I_{BAT}	Charge pump standby current	$EN_A = EN_B = 0$ V		200		nA

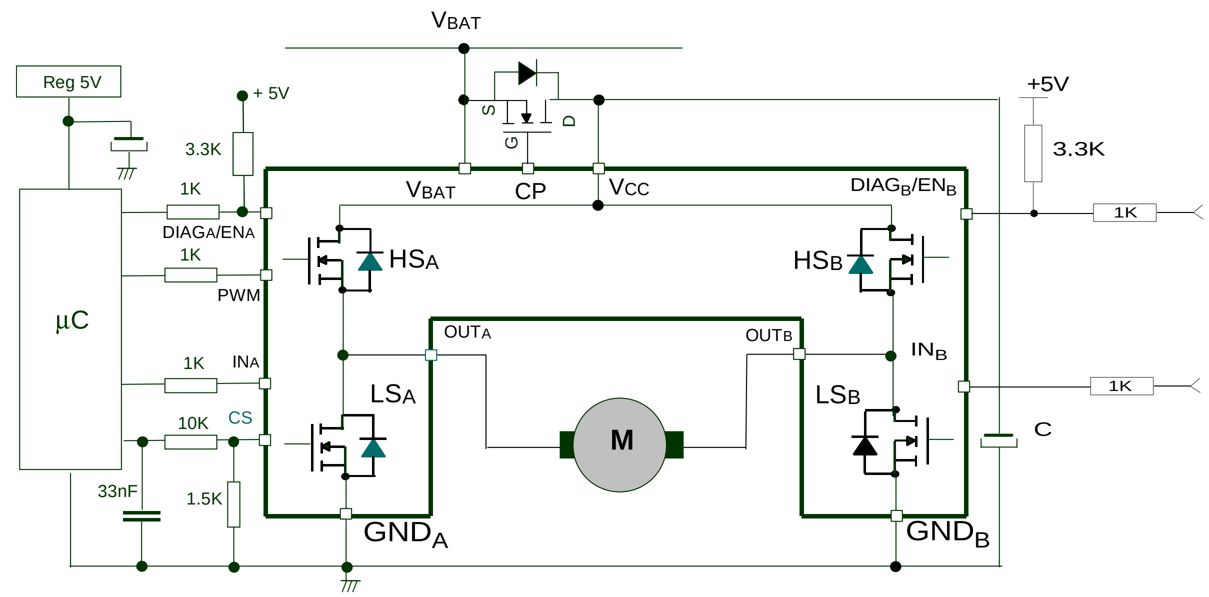
2.4 Waveforms and truth table

In normal operating conditions the $DIAG_X/EN_X$ pin is considered as an input pin by the device. This pin must be externally pulled-high
PWM pin usage: in all cases, a “0” on the PWM pin turns-off both LS_A and LS_B switches. When PWM rises back to “1”, LS_A or LS_B turn-on again depending on the input pin state.

Table 12. Truth table in normal operating conditions

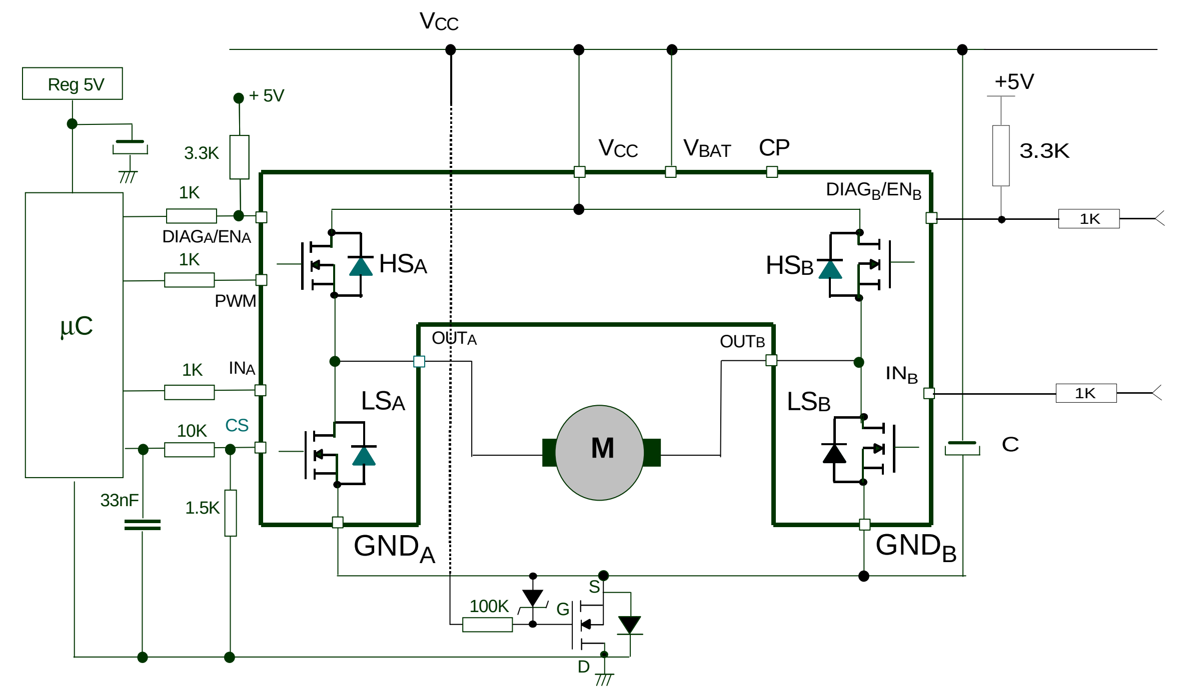
IN_A	IN_B	$DIAG_A/EN_A$	$DIAG_B/EN_B$	OUT_A	OUT_B	CS ($V_{CSD} = 0$ V)	Operating mode
1	1	1	1	H	H	High imp.	Brake to V_{CC}
1	0	1	1	H	L	$I_{SENSE} = I_{OUT}/K$	Clockwise (CW)
0	1	1	1	L	H	$I_{SENSE} = I_{OUT}/K$	Counterclockwise (CCW)
0	0	1	1	L	L	High imp.	Brake to GND

Figure 4. Typical application circuit for DC to 20 kHz PWM operation with reverse battery protection (option A)



Note:
The external N-channel Power MOSFET used for the reverse battery protection should have the following characteristics:
- BVdss > 20 V (for a reverse battery of -16 V);
- $R_{DS(on)}$ < 1/3 of H-bridge total $R_{DS(on)}$
- Standard Logic Gate Driving

Figure 5. Typical application circuit for DC to 20 kHz PWM operation with reverse battery protection (option B)



Note:
The value of the blocking capacitor (C) depends on the application conditions and defines voltage and current ripple onto supply line at PWM operation. Stored energy of the motor inductance may flyback into the blocking capacitor, if the bridge driver goes into 3-state. This causes a hazardous overvoltage if the capacitor is not big enough. As basic orientation, 500 μF per 10 A load current is recommended.

Table 13. Truth table in fault conditions (detected on OUT_A)

<table>
<tr><th>IN_A</th><th>IN_B</th><th>$DIAG_A/EN_A$</th><th>$DIAG_B/EN_B$</th><th>OUT_A</th><th>OUT_B</th><th>CS (V_{CSD}=0V)</th></tr>
<tr><td rowspan="2">1</td><td>1</td><td rowspan="5">0</td><td rowspan="4">1</td><td rowspan="5">OPEN</td><td>H</td><td rowspan="2">High impedance</td></tr>
<tr><td>0</td><td>L</td></tr>
<tr><td rowspan="2">0</td><td>1</td><td>H</td><td>I_{OUTB}/K</td></tr>
<tr><td>0</td><td>L</td><td rowspan="2">High impedance</td></tr>
<tr><td>X</td><td>X</td><td>0</td><td>OPEN</td></tr>
<tr><td></td><td></td><td colspan="2">Fault Information</td><td colspan="2">Protection Action</td><td></td></tr>
</table>

Note: In normal operating conditions the $DIAG_X/EN_X$ pin is considered as an input pin by the device. This pin must be externally pulled high.

In case of a fault condition the $DIAG_X/EN_X$ pin is considered as an output pin by the device.

The fault conditions are:

- overtemperature on one or both high-sides (for example, if a short to ground occurs as it could be the case described in line 1 and 2 in the *Table 14*);
- Short to battery condition on the output (saturation detection on the low-side Power MOSFET).

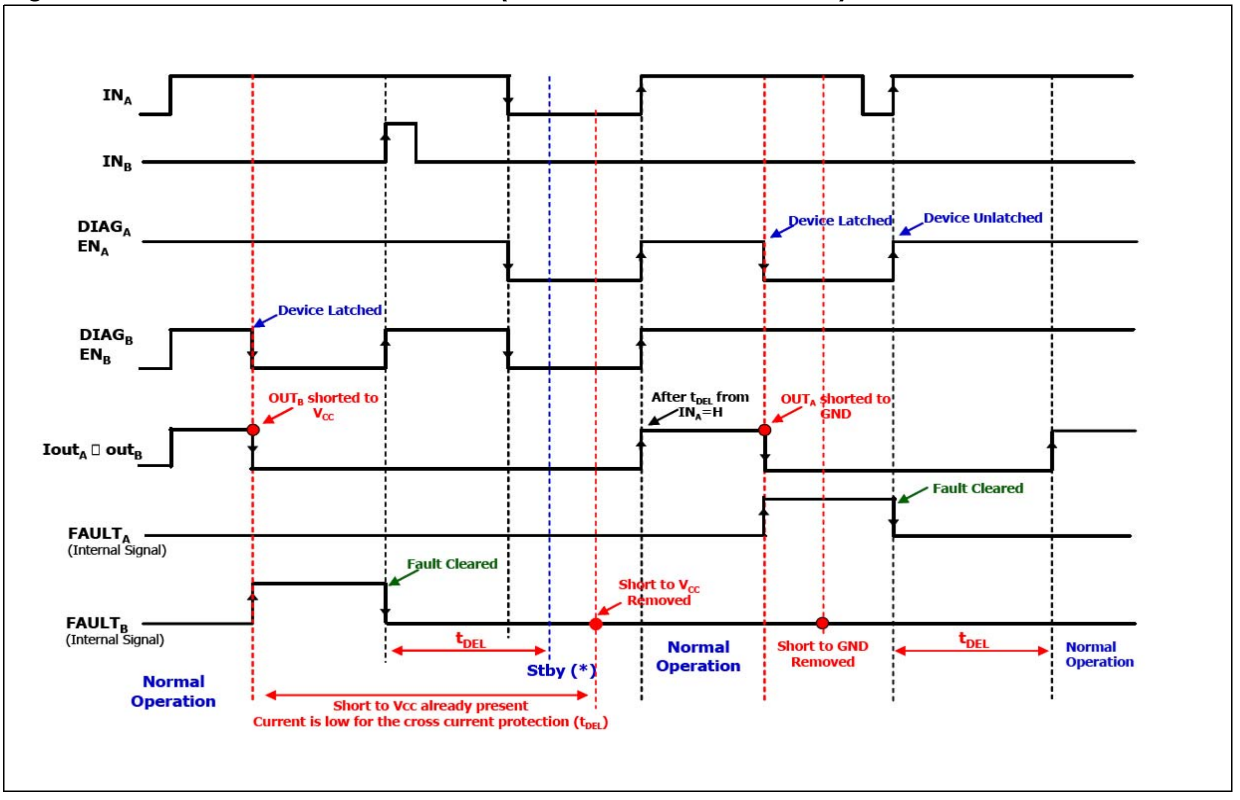
Possible origins of fault conditions may be:

- OUT_A is shorted to ground. It follows that, high-side A is in overtemperature state.
- OUT_A is shorted to V_{CC}. It follow that, low-side Power MOSFET is in saturation state.

When a fault condition is detected, the user can know which power element is in fault by monitoring the IN_A, IN_B, $DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins.

In any case, when a fault is detected, the faulty leg of the bridge is latched off. To turn-on the respective output (OUT_X) again, the input signal must rise from low-level to high-level.

Figure 6. Behavior in fault condition (how a fault can be cleared)



Note: In case of the fault condition is not removed, the procedure for unlatching and sending the device in Stby mode is:

- Clear the fault in the device (toggle: INA if ENA=0 or INB if ENB=0)

- Pull low all inputs, PWM and Diag/EN pins within tDEL.

If the Diag/En pins are already low, PWM=0, the fault can be cleared simply toggling the input. The device enters in stby mode as soon as the fault is cleared.

Table 14. Electrical transient requirements (part 1)

ISO T/R 7637/1 Test Pulse	Test level				
	I	II	III	IV	Delay and impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms, 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms, 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs, 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs, 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

Table 15. Electrical transient requirements (part 2)

ISO T/R 7637/1 Test Pulse	Test levels			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Table 16. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.5 Reverse battery protection

Against reverse battery condition the charge pump feature allows to use an external N-channel MOSFET connected as shown in the typical application circuit (see *Figure 4*).

As alternative option, a N-channel MOSFET connected to GND pin can be used (see typical application circuit in figure *Figure 5*).

With this configuration we recommend to short V_{BAT} pin to V_{CC}.

The device sustains no more than -30 A in reverse battery conditions because of the two body diodes of the Power MOSFETs. Additionally, in reverse battery condition the I/Os of VNH5019A-E is pulled-down to the V_{CC} line (approximately -1.5 V). Series resistor must be inserted to limit the current sunk from the microcontroller I/Os. If I_{Rmax} is the maximum target reverse current through microcontroller I/Os, series resistor is:

$$R = \frac{V_{IOs} - V_{CC}}{I_{Rmax}}$$

Figure 7. Definition of the delay times measurement

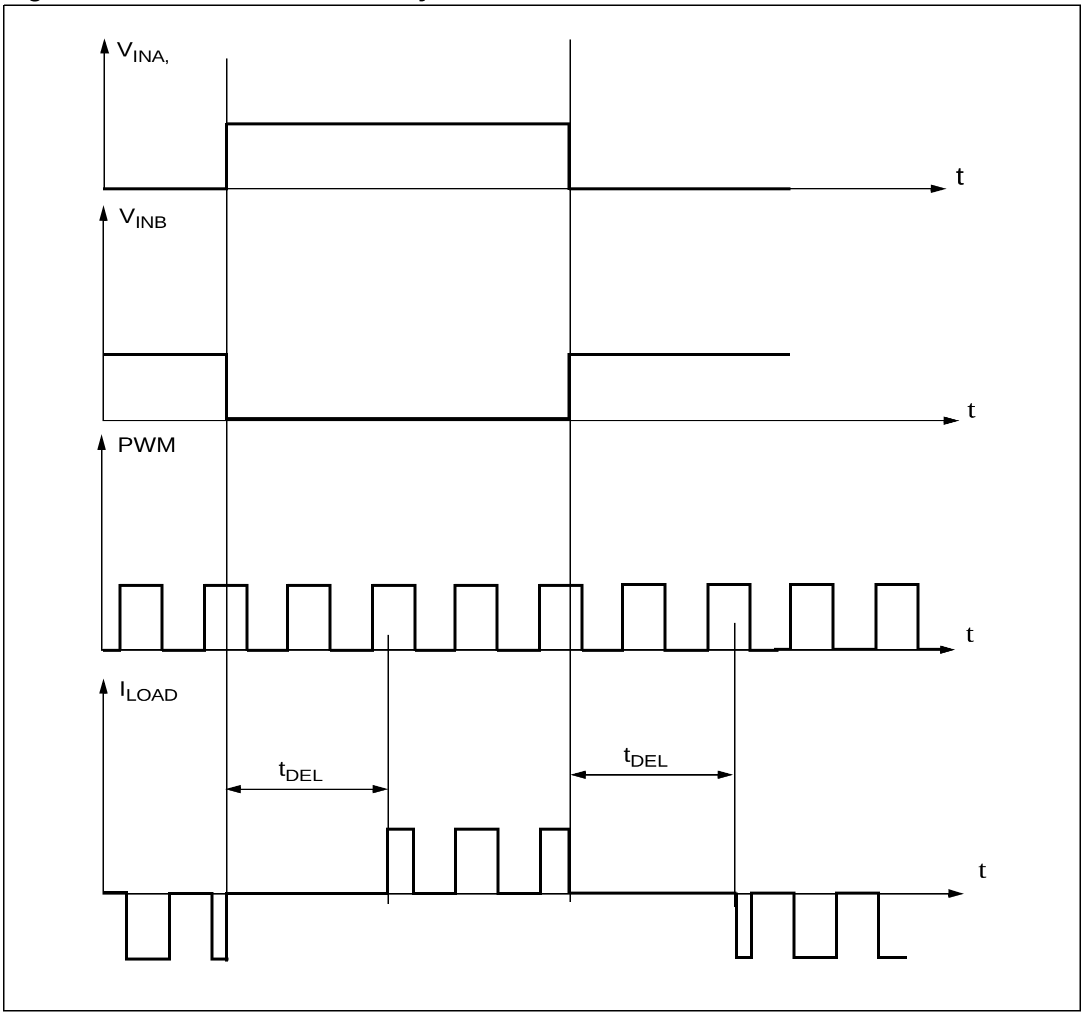


Figure 8. Definition of the low-side switching times

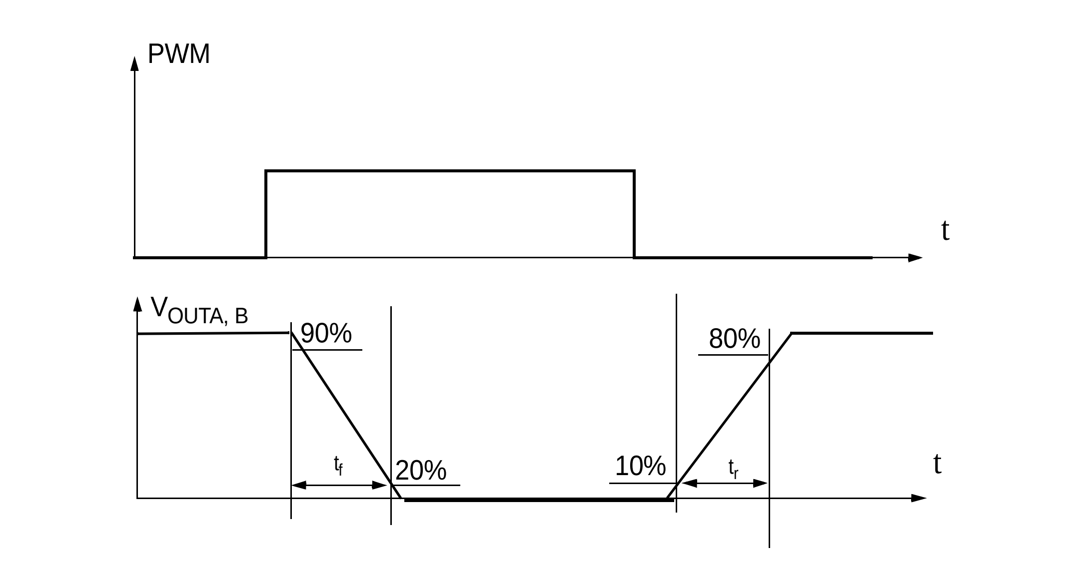


Figure 9. Definition of the high-side switching times

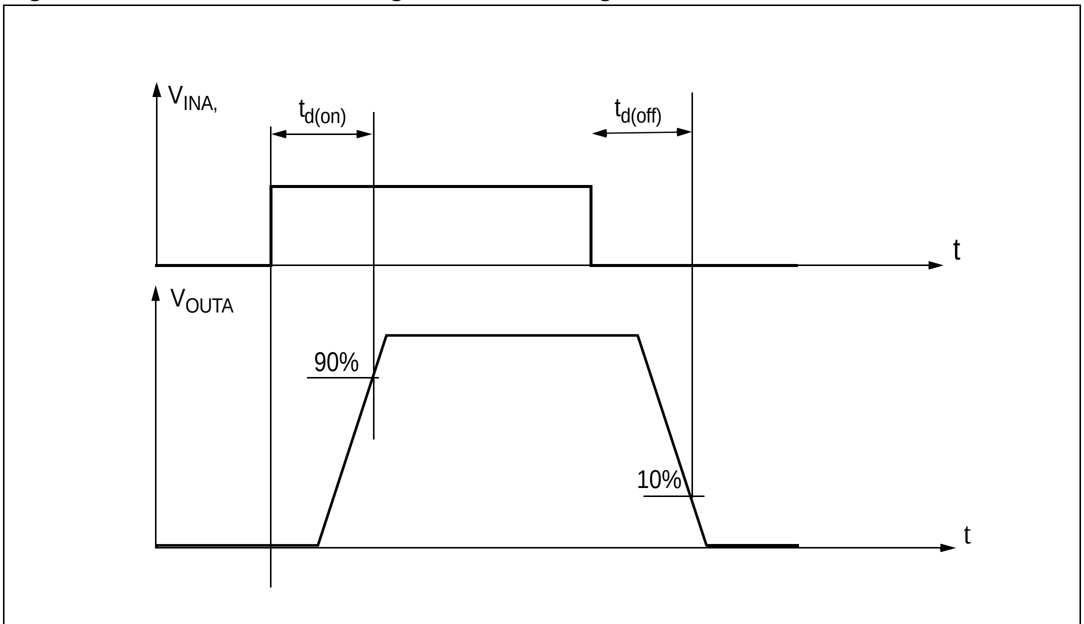


Figure 10. Definition of dynamic cross conduction current during a PWM operation

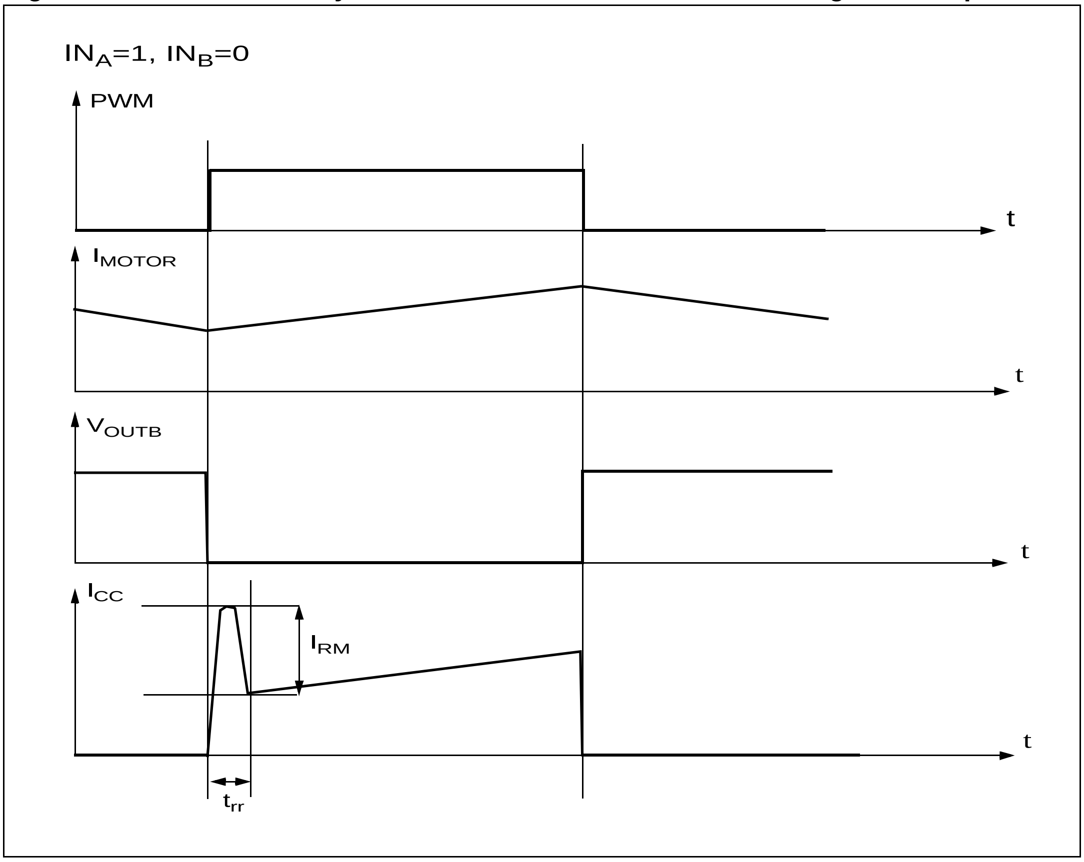


Figure 11. Waveforms in full bridge operation (part 1)

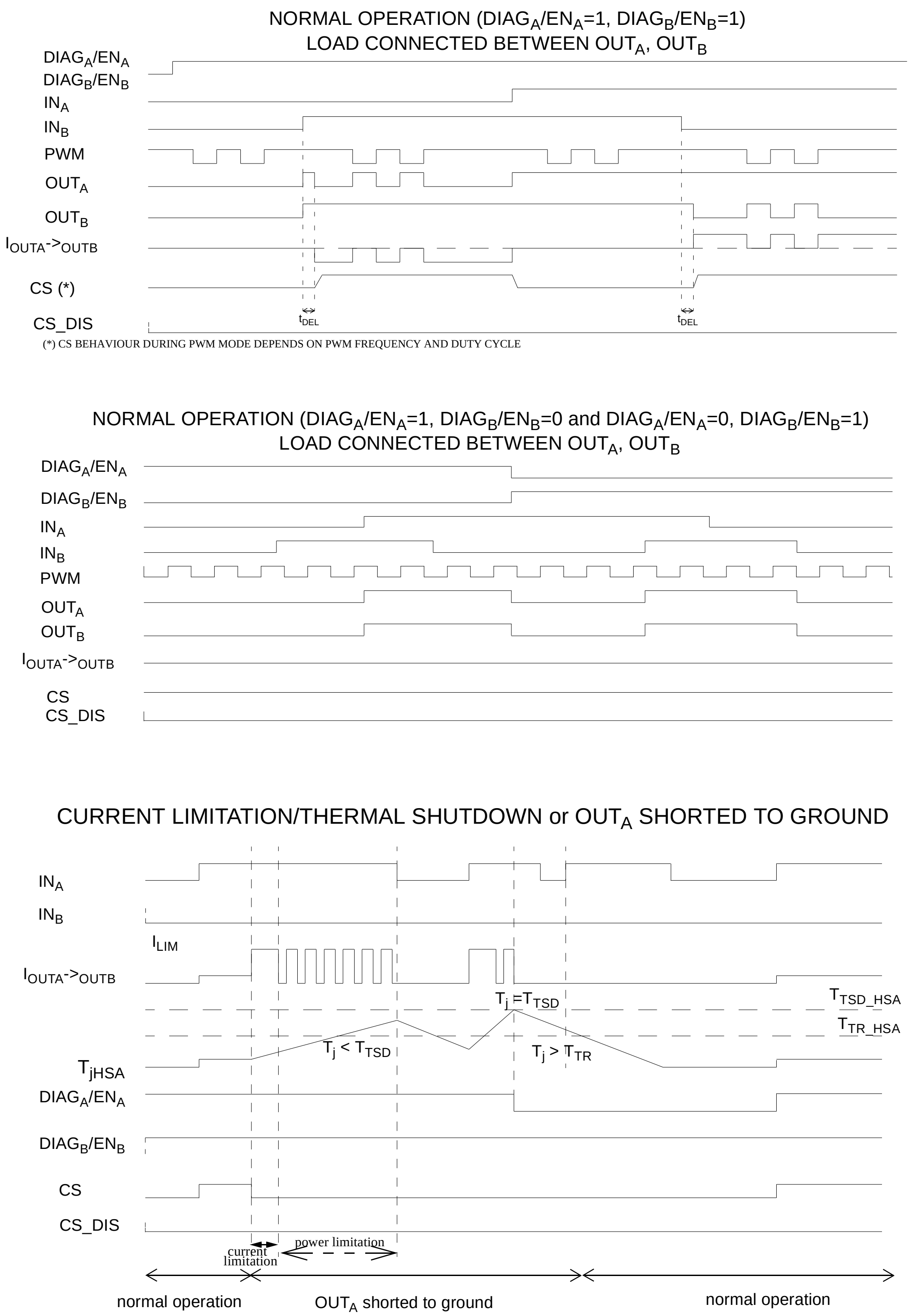


Figure 12. Waveforms in full bridge operation (part 2)

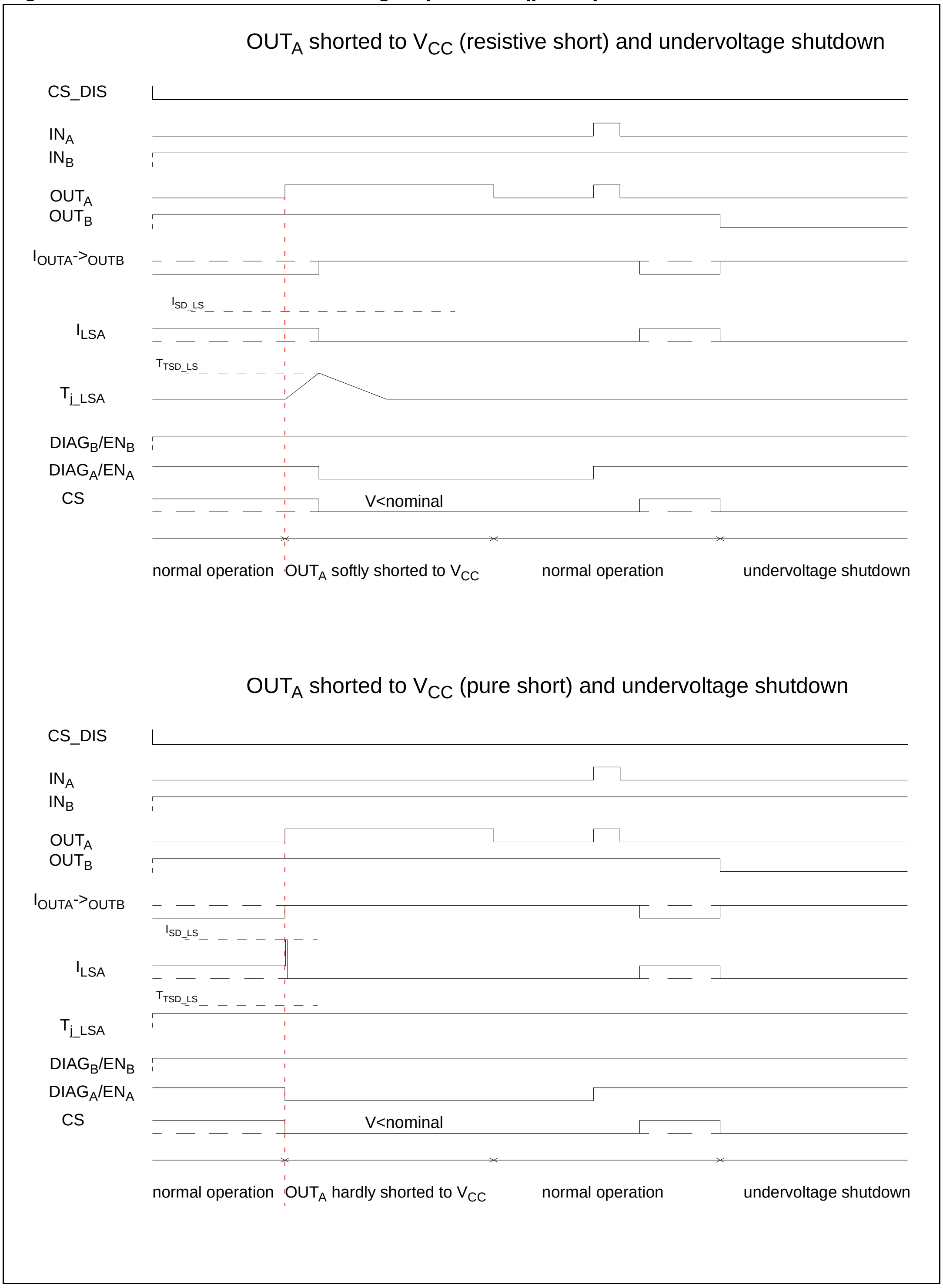
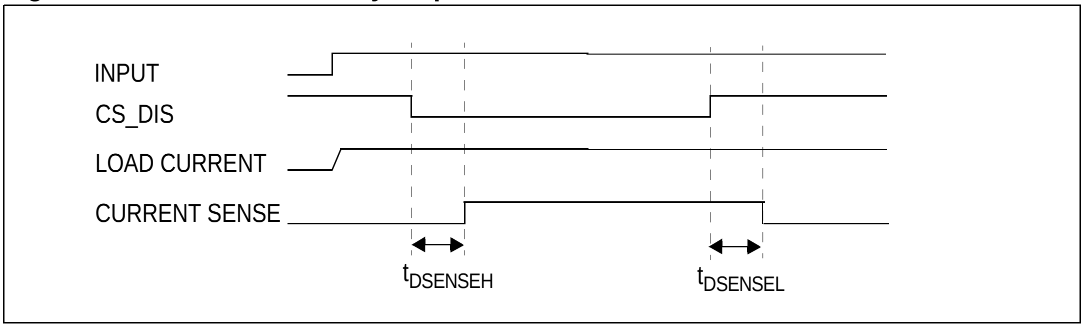
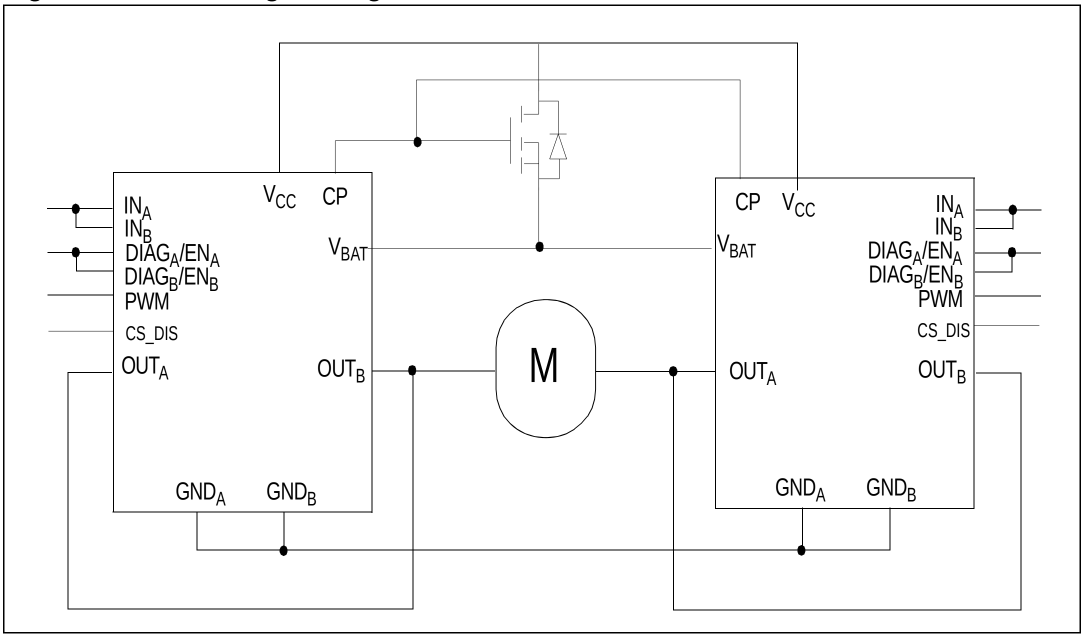


Figure 13. Definition of delay response time of sense current



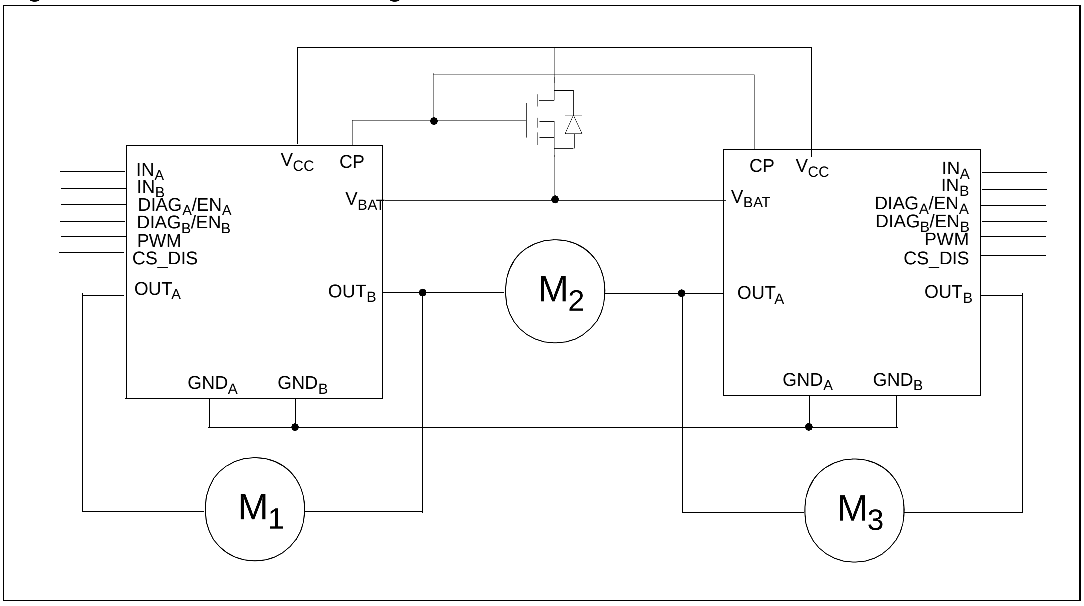
The VNH5019A-E can be used as a high power half-bridge driver achieving an on- resistance per leg of 9.5 mΩ. The figure below shows the suggested configuration:

Figure 14. Half-bridge configuration



The VNH5019A-E can easily be designed in multi-motors driving applications such as seat positioning systems where only one motor must be driven at a time. $DIAG_X/EN_X$ pins allow to put unused half-bridges in high-impedance. The figure below shows the suggested configuration:

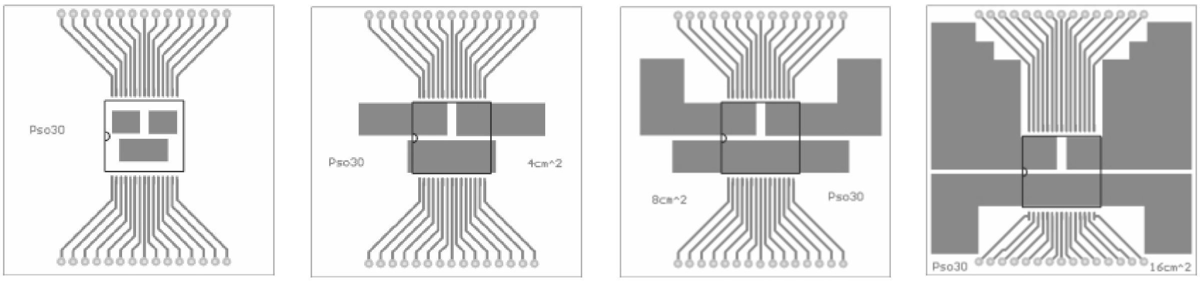
Figure 15. Multi-motors configuration



3 Package and PCB thermal data

3.1 MultiPowerSO-30 thermal data

Figure 16. MultiPowerSO-30™ PC board



Note:
Layout condition of Rth and Zth measurements (PCB FR4 area= 58 mm x 58 mm, PCB thickness=2 mm, Cu thickness=35 mm, Copper areas: from minimum pad lay-out to 16 cm²).

Figure 17. Chipset configuration

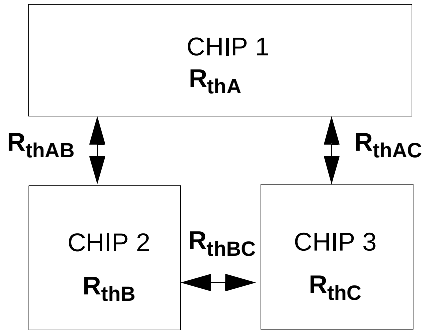
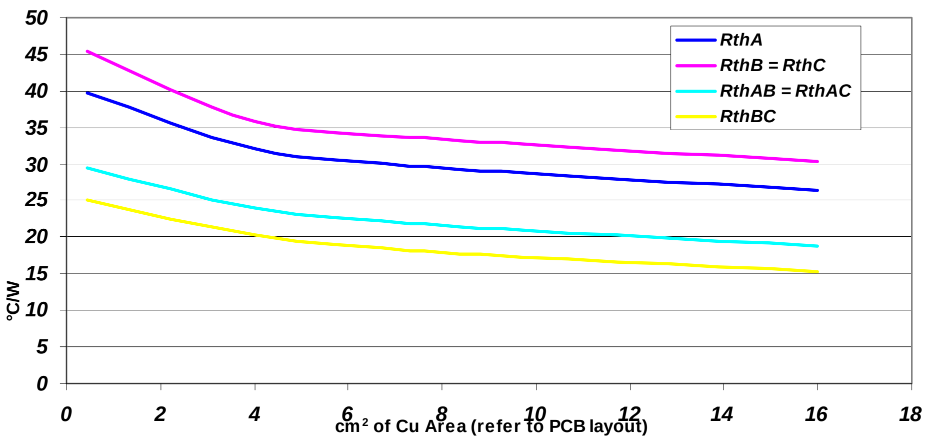


Figure 18. Auto and mutual $R_{thj-amb}$ vs PCB copper area in open box free air condition



3.1.1 Thermal calculation in clockwise and anti-clockwise operation in steady-state mode

Table 17. Thermal calculation in clockwise and anti-clockwise operation in steady-state mode

Chip 1	Chip 2	Chip 3	Tjchip1	Tjchip2	Tjchip3
ON	OFF	ON	$P_{dchip1} \cdot R_{thA} + P_{dchip3} \cdot R_{thAC} + T_{amb}$	$P_{dchip1} \cdot R_{thAB} + P_{dchip3} \cdot R_{thBC} + T_{amb}$	$P_{dchip1} \cdot R_{thAC} + P_{dchip3} \cdot R_{thC} + T_{amb}$
ON	ON	OFF	$P_{dchip1} \cdot R_{thA} + P_{dchip2} \cdot R_{thAB} + T_{amb}$	$P_{dchip1} \cdot R_{thAB} + P_{dchip2} \cdot R_{thB} + T_{amb}$	$P_{dchip1} \cdot R_{thAC} + P_{dchip2} \cdot R_{thBC} + T_{amb}$
ON	OFF	OFF	$P_{dchip1} \cdot R_{thA}+ T_{amb}$	$P_{dchip1} \cdot R_{thAB} + T_{amb}$	$P_{dchip1} \cdot R_{thAC} + T_{amb}$
ON	ON	ON	$P_{dchip1} \cdot R_{thA} + (P_{dchip2} + P_{dchip3}) \cdot R_{thAB} + T_{amb}$	$Pdchip2 \cdot R_{thB} + P_{dchip1} \cdot R_{thAB} + P_{dchip3} \cdot R_{thBC} + T_{amb}$	$P_{dchip1} \cdot R_{thAB} + P_{dchip2} \cdot R_{thBC} + P_{dchip3} \cdot R_{thC} + T_{amb}$

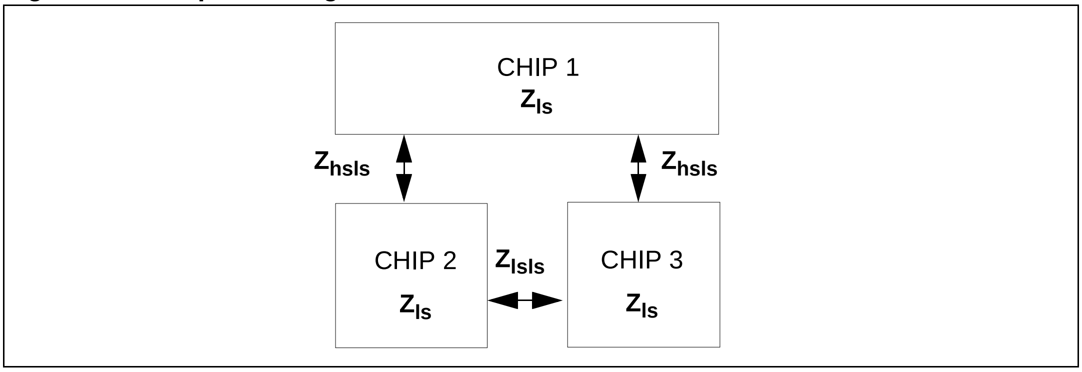
3.1.2 Thermal calculation in transient mode

$T_{hs}= P_{dhs} \cdot Z_{hs} + Z_{hsls} \cdot (Pd_{lsA} + Pd_{lsB}) + T_{amb}$

$T_{lsA}= Pd_{lsA} \cdot Z_{ls} + Pd_{hs} \cdot Z_{hsls} + Pd_{lsB} \cdot Z_{hsls} + T_{amb}$

$T_{lsB}= Pd_{lsB} \cdot Z_{ls} + Pd_{hs} \cdot Z_{hsls} + Pd_{ls}A \cdot Z_{hsls} + T_{amb}$

Figure 19. Chipset configuration



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Figure 20. MultiPowerSO-30 HSD thermal impedance junction ambient single pulse

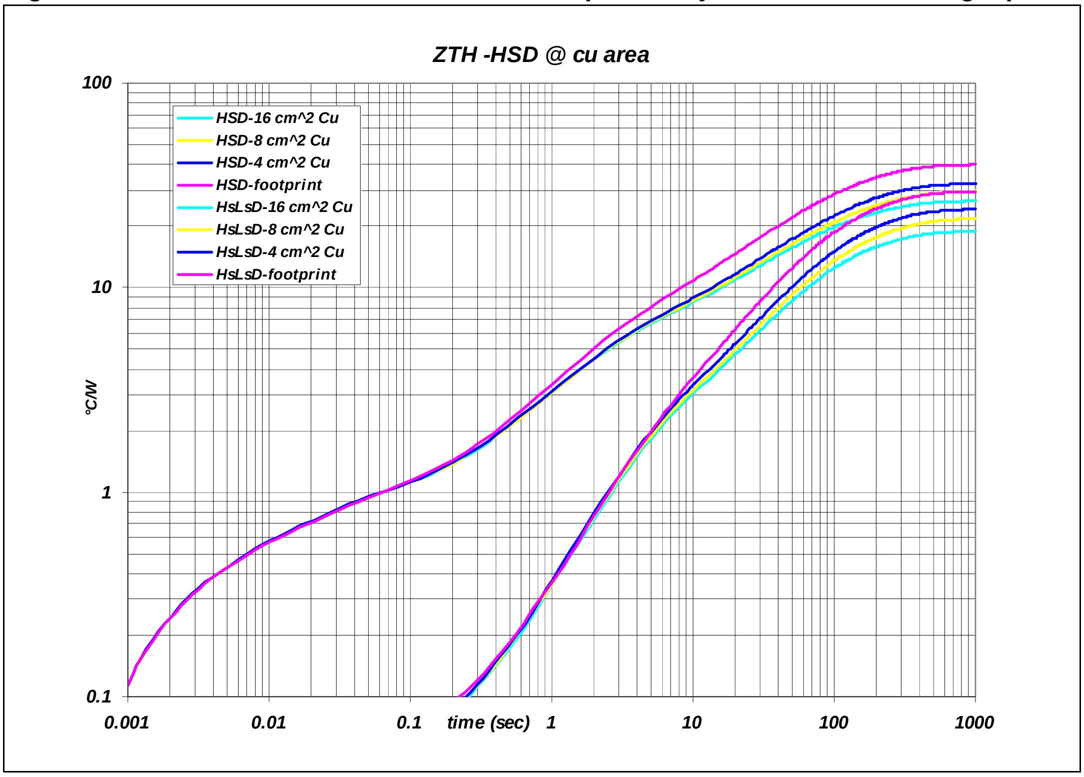


Figure 21. MultiPowerSO-30 LSD thermal impedance junction ambient single pulse

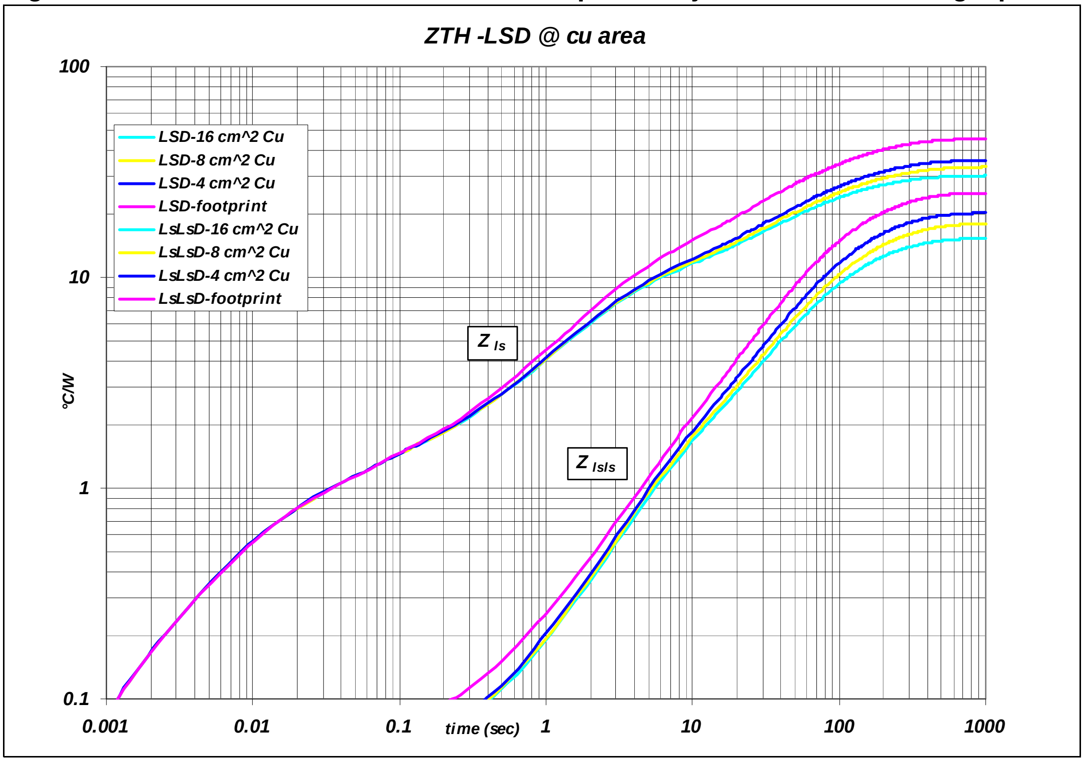


Figure 22. Thermal fitting model of an H-bridge in MultiPowerSO-30

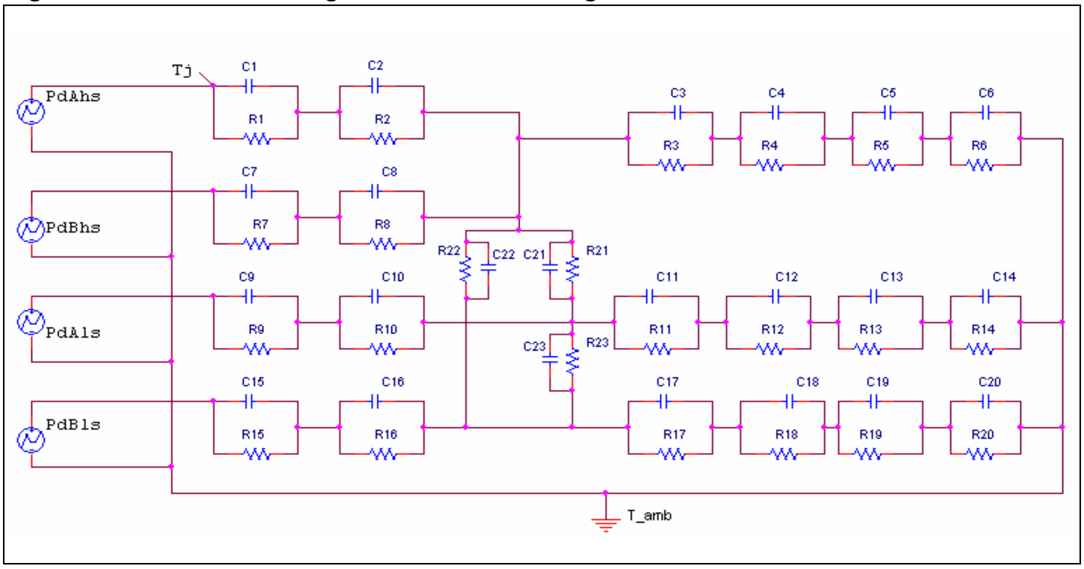


Table 18. Thermal parameters(1)

Area/island (cm^2)	Footprint	4	8	16
R1 = R7 (°C/W)	0.1			
R2 = R8 (°C/W)	0.3			
R3 = R10 = R16 (°C/W)	0.5			
R4 (°C/W)	6			
R5 (°C/W)	30	24	24	24
R6 (°C/W)	56	52	42	32
R9 = R15 (°C/W)	0.05			
R11 = R17 (°C/W)	0.7			
R12 = R18 (°C/W)	10			
R13 = R19 (°C/W)	36	26	26	26
R14 = R20 (°C/W)	56	42	36	28
R21 = R22 (°C/W)	35	25	25	25
R23 (°C/W)	160	150	150	150
C1 = C7 = C9 = C15 (W.s/°C)	0.005			
C2 = C8 (W.s/°C)	0.01			
C3 (W.s/°C)	0.03			
C4 (W.s/°C)	0.4			
C5 (W.s/°C)	1.5	2	2	2
C6 (W.s/°C)	3	4	5	6
C10 = C16 (W.s/°C)	0.015			
C11 = C17 (W.s/°C)	0.05			
C12 = C18 (W.s/°C)	0.3			
C13 = C19 (W.s/°C)	1.2	2	2	2
C14 = C20 (W.s/°C)	2.5	3	4	5
C21 = C22 = C23 (W.s/°C)	0.01	0.008	0.008	0.008

1. The blank space means that the value is the same as the previous one.

4 Package and packing information

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.2 MultiPowerSO-30 mechanical data

Figure 23. MultiPowerSO-30 package dimensions

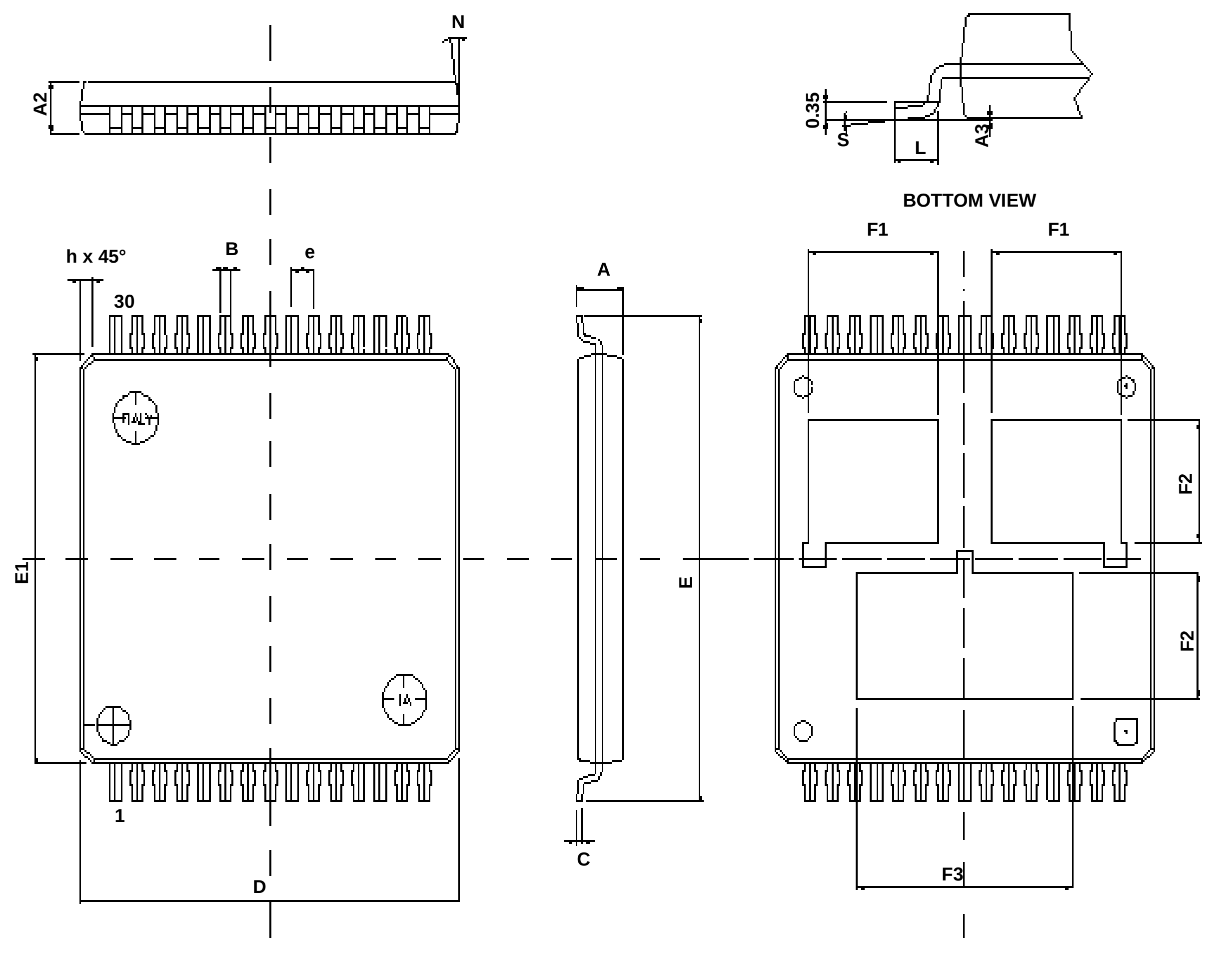
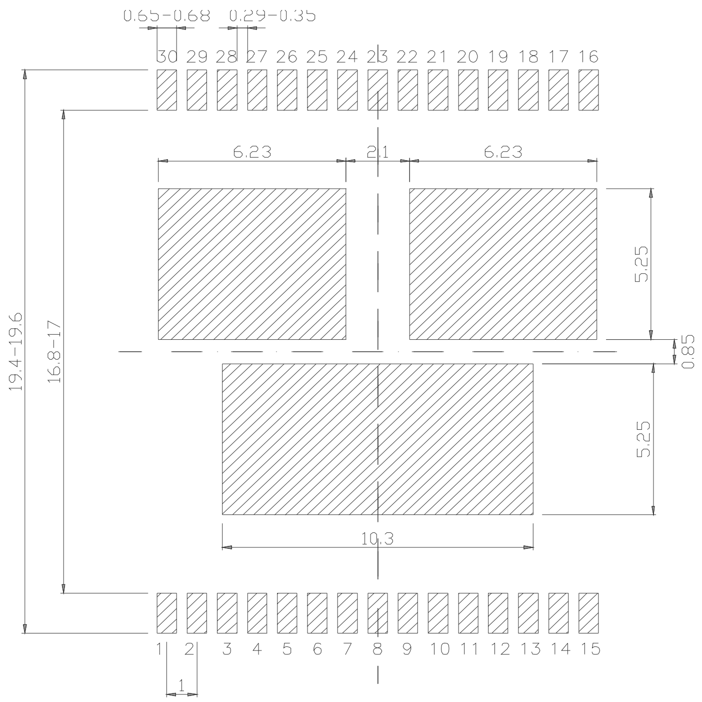


Table 19. MultiPowerSO-30 mechanical data

Symbol	Data book mm		
	Min.	Typ.	Max.
A			2.35
A2	1.85		2.25
A3	0		0.1
B	0.42		0.58
C	0.23		0.32
D	17.1	17.2	17.3
E	18.85		19.15
E1	15.9	16	16.1
e		1	
F1	5.55		6.05
F2	4.6		5.1
F3	9.6		10.1
L	0.8		1.15
N			10°
S	0°		7°

4.3 MultiPowerSO-30 suggested land pattern

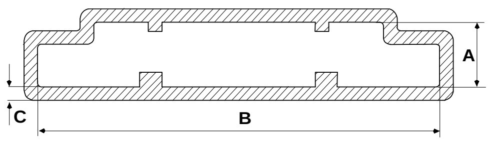
Figure 24. MultiPowerSO-30 suggested pad layout



4.4 MultiPowerSO-30 packing information

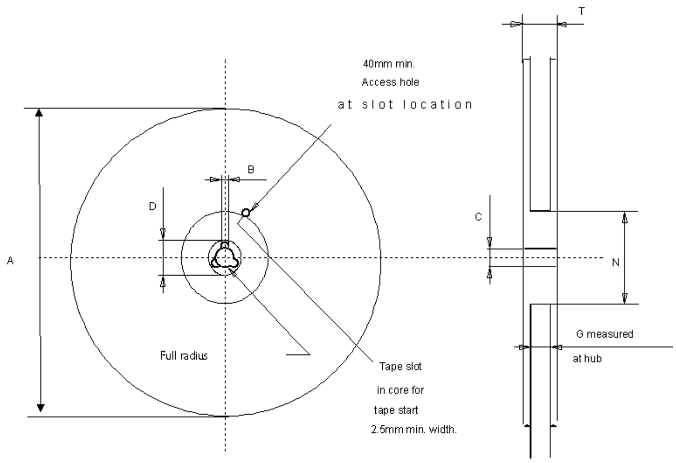
The devices can be packed in tube or tape and reel shipments (see *Table 20: Device summary* for packaging quantities).

Figure 25. MultiPowerSO-30 tube shipment (no suffix)



Dimension	mm
Base q.ty	29
Bulk q.ty	435
Tube length (± 0.5)	532
A	3.82
B	23.6
C (± 0.13)	0.8

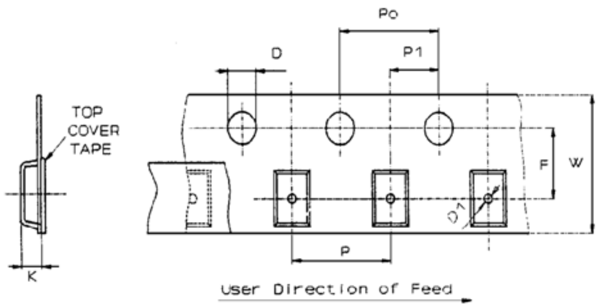
Figure 26. MultiPowerSO-30 tape and reel shipment (suffix "TR")



Reel dimensions

SO-28 tube shipment (no suffix)

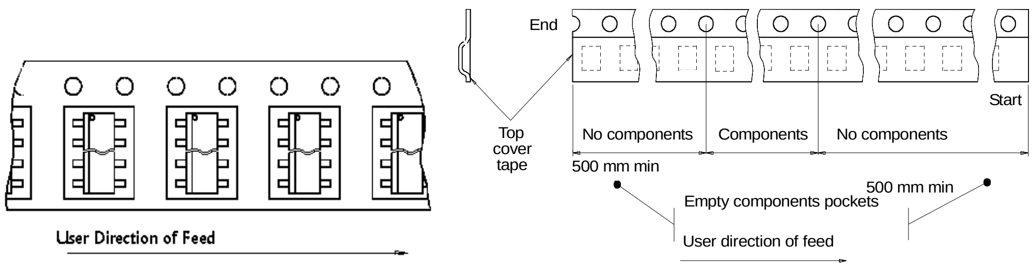
Dimension	mm
Base q.ty	1000
Bulk q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
D (min)	20.2
G (+ 2 / -0)	32
N (min)	100
T (max)	38.4



Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Description	Dimension	mm
Tape width	W	32
Tape hole spacing	P0 (± 0.1)	4
Component spacing	P	24
Hole diameter	D (± 0.1/-0)	1.5
Hole diameter	D1 (min)	2
Hole position	F (± 0.1)	14.2
Compartment Depth	K (max)	2.2
Hole Spacing	P1 (± 0.1)	2



5 Order codes

Table 20. Device summary

Package	Order codes	
	Tube	Tape and reel
MultiPowerSO-30	VNH5019A-E	VNH5019TR-E

6 Revision history

Table 21. Document revision history

Date	Revision	Changes
22-Jan-2008	1	Initial release.
04-Nov-2009	2	Uploaded corporate template by using V3 version Added *Table 5: Thermal data* *Section 2.1: Absolute maximum ratings* – Added text *Table 6: Power section* – I_S: added max value for $IN_A = IN_B = PWM = 0$; $T_j = 25$ °C; V_{CC}=13V in Test conditions, deleted $IN_A = IN_B = PWM = 0$ – V_f: changed Test conditions, changed typ/max value – I_{RM}: deleted and copied in *Table 8: Switching (V_{CC} = 13 V, R_{LOAD} = 0.87 W, Tj = 25 °C)* whole row *Table 8: Switching (V_{CC} = 13 V, R_{LOAD} = 0.87 W, Tj = 25 °C)* – t_{DEL}: changed min/typ/max value – Copied I_{RM} row by *Table 6: Power section* Updated *Table 10: Current sense (8 V < V_{CC} < 21 V)* *Table 11: Charge pump* – V_{CP}: changed min/max value for EN_X = 5 V, changed typ value for EN_X = 5 V, V_{CC} = 4.5 V Updated *Figure 11: Waveforms in full bridge operation (part 1)* Updated *Figure 12: Waveforms in full bridge operation (part 2)* Added *Chapter 4*
16-Dec-2009	3	Updated following tables: – *Table 6: Power section* – *Table 9: Protection and diagnostic* – *Table 10: Current sense (8 V < V_{CC} < 21 V)* Added *Figure 6: Behavior in fault condition (how a fault can be cleared)* Added *Chapter 3: Package and PCB thermal data*
06-Apr-2010	4	Updated *Table 5: Thermal data*. *Table 6: Power section*: – I_S: updated test condition and max value Updated table notes on *Table 9: Protection and diagnostic*. *Table 10: Current sense (8 V < V_{CC} < 21 V)*: – dK_0/k_0, dK_1/k_1, dK_3/k_3: updated minimum end maximum values.
19-Apr-2010	5	Updated *Table 10: Current sense (8 V < V_{CC} < 21 V)*.
25-May-2010	6	Updated *Features* list. Updated *Table 6: Power section*.
02-Sep-2010	7	Updated *Table 5: Thermal data*.

Table 21. Document revision history (continued)

Date	Revision	Changes
22-Dec-2011	8	Updated *Figure 1: Block diagram* Added *Table 1: Suggested connections for unused and not connected pins* Updated *Table 3: Block descriptions* *Table 8: Switching (V_{CC} = 13 V, R_{LOAD} = 0.87 W, Tj = 25 °C)*: – T_{TSD}, T_{TR}, T_{HYST}: added note – T_{TSD_LS}: added row Updated *Table 13: Truth table in fault conditions (detected on OUTA)* Updated *Figure 11: Waveforms in full bridge operation (part 1)* and *Figure 12: Waveforms in full bridge operation (part 2)*
19-Sep-2013	9	Updated Disclaimer.

AEDB-9140 Series

Three Channel Optical Incremental Encoder Modules with Codewheel, 100 CPR to 500 CPR

AVAGO TECHNOLOGIES

Data Sheet

Description

The AEDB-9140 series are three channel optical incremental encoder modules offered with a codewheel. When used with a codewheel, these low cost modules detect rotary position. Each module consists of a lensed LED source and a detector IC enclosed in a small plastic package. Due to a highly collimated light source and a unique photodetector array, these modules are extremely tolerant to mounting misalignment.

The AEDB-9140 has two channel quadrature outputs plus a third channel index output. This index output is a 90 electrical degree high true index pulse which is generated once for each full rotation of the codewheel.

The AEDB-9140 is designed for use with a codewheel which has an optical radius of 11.00 mm (0.433 inch).

The quadrature signals and the index pulse are accessed through five 0.46 mm square pins located on 1.27 mm(pitch) centers.

Features

- Two Channel Quadrature Output with Index Pulse
- Resolution from 100 CPR to 500 CPR (Counts Per Revolution)
- Low Cost
- Easy to Mount
- No Signal Adjustment required
- Small Size
- Operating Temperature: -10°C to 85°C
- TTL Compatible
- Single 5V Supply

Applications

The AEDB-9140 provide sophisticated motion control detection at a low cost, making them ideal for high volume applications. Typical applications include printers, plotters, tape drives, and industrial and factory automation equipment.

Note: Avago Technologies encoders are not recommended for use in safety critical applications. Eg. ABS braking systems, power steering, life support systems and critical care medical equipment. Please contact sales representative if more clarification is needed.

Ordering Information

AEDB-9140 Option [ ] [ ][ ]

Resolutions (Cycle/Rev)	Shaft Diameter*
C - 100 CPR E - 200 CPR F - 256 CPR G - 360 CPR H - 400 CPR A - 500 CPR	02 - 3mm 04 - 5/32 in 05 - 3/16 in 06 - 1/4 in 11 - 4mm 12 - 6mm 13 - 8mm 14 - 5mm

Three Channel Encoder Modules with Codewheel, 11 mm Optical Radius

* Please contact factory for other shaft diameters

Available Options

		Shaft Diameter Options							
Part No	**CPR**	**02**	**04**	**05**	**06**	**11**	**12**	**13**	**14**
AEDB-9140	C		•		•		•	•	
	E				•	•	•		•
	F		•				•		•
	G				•		•		•
	H				•				•
	A	•	•	•	•	•	•	•	•

Theory of Operation

The AEDB-9140 are emitter/detector modules. Coupled with a codewheel, these modules translate the rotary motion of a shaft into a three-channel digital output.

As seen in Figure 1, the modules contain a single Light Emitting Diode (LED) as its light source. The light is collimated into a parallel beam by means of a single polycarbonate lens located directly over the LED. Opposite the emitter is the integrated detector circuit. This IC consists of multiple sets of photodetectors and the signal processing circuitry necessary to produce the digital waveforms.

The codewheel rotates between the emitter and detector, causing the light beam to be interrupted by the pattern of spaces and bars on the codewheel.

The photodiodes which detect these interruptions are arranged in a pattern that corresponds to the radius and design of the code-wheel. These detectors are also spaced such that a light period on one pair of detectors corresponds to a dark period on the adjacent pair of detectors.

The photodiode outputs are then fed through the signal processing circuitry resulting in A, Abar, B, Bbar, I and Ibar. Comparators receive these signals and produce the final outputs for channels A and B. Due to this integrated phasing technique, the digital output of channel A is in quadrature with that of channel B (90 degrees out of phase).

Block Diagram

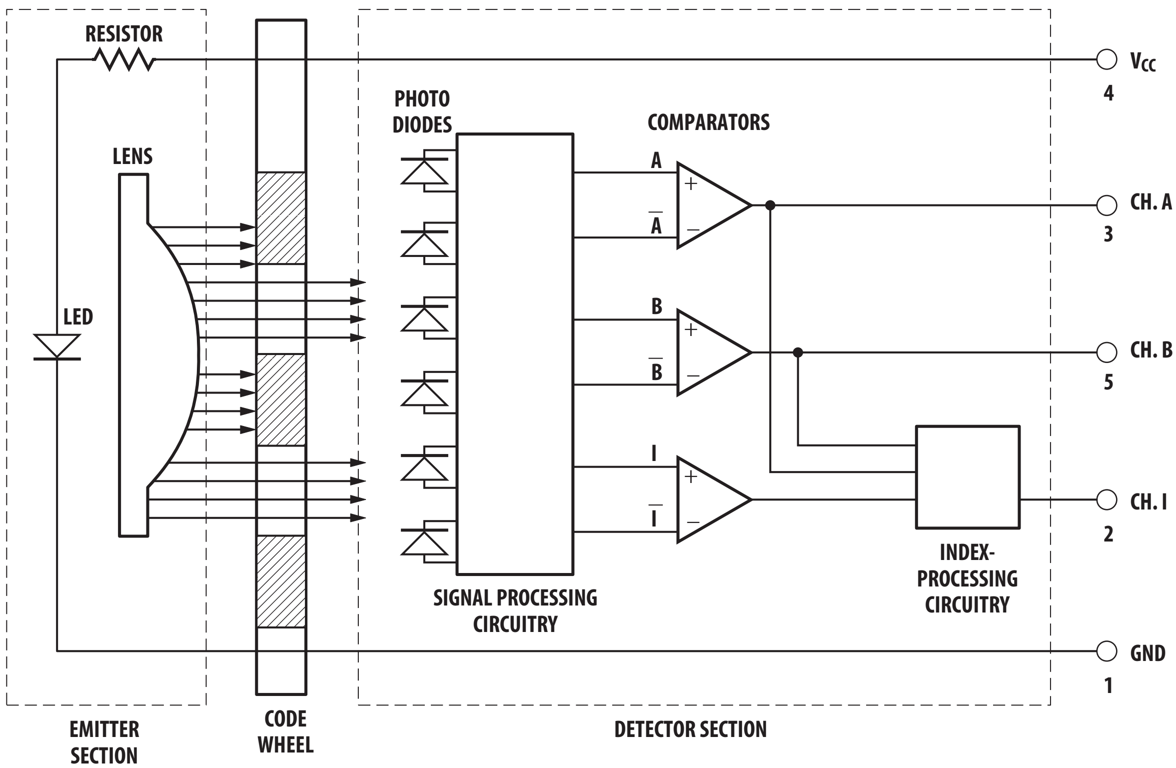


Figure 1.

Output Waveforms

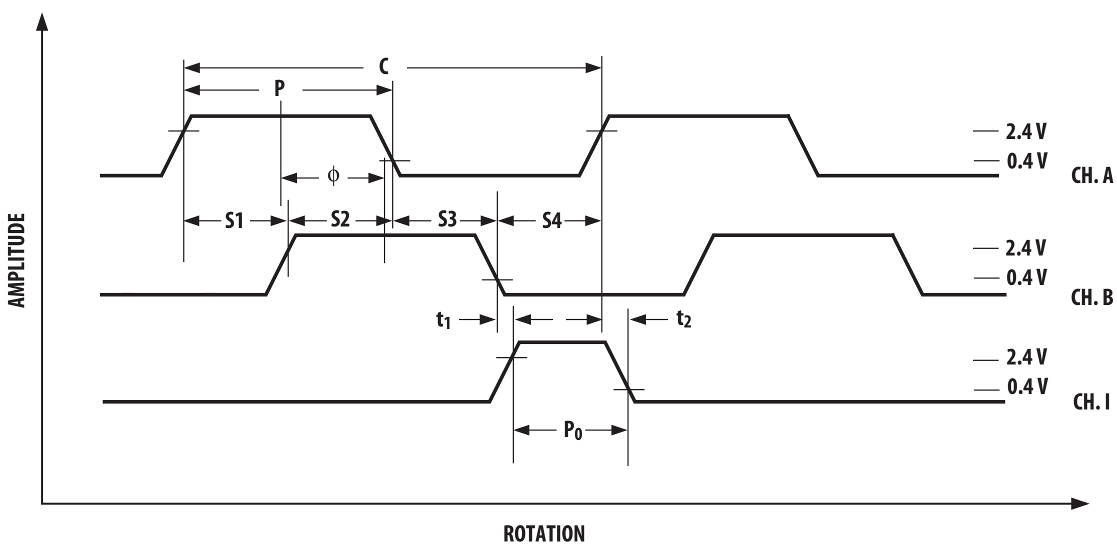


Figure 2.

Definitions

Note: Refer to Figure 2

Count (N): The number of bar and window pairs or counts per revolution (CPR) of the codewheel.

One Cycle (C): 360 electrical degrees (°e), 1 bar and window pair.

One Shaft Rotation: 360 mechanical degrees, N cycles.

Position Error ($\Delta\Theta$): The normalized angular difference between the actual shaft position and the position indicated by the encoder cycle count.

Cycle Error (ΔC): An indication of cycle uniformity. The difference between an observed shaft angle which gives rise to one electrical cycle, and the nominal angular increment of 1/N of a revolution.

Pulse Width (P): The number of electrical degrees that an output is high during 1 cycle. This value is nominally 180°e or 1/2 cycle.

Pulse Width Error (ΔP): The deviation, in electrical degrees, of the pulse width from its ideal value of 180°e.

State Width (S): The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are 4 states per cycle, each nominally 90°e.

State Width Error (ΔS): The deviation, in electrical degrees, of each state width from its ideal value of 90°e.

Phase (f): The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B.

This value is nominally 90°e for quadrature output.

Phase Error ($\Delta\phi$): The deviation of the phase from its ideal value of 90°e.

Direction of Rotation: When the codewheel rotates in the clockwise direction viewing from top of the module (direction from V to G), channel A will lead channel B. If the codewheel rotates in the opposite direction, channel B will lead channel A.

Optical Radius (Rop): The distance from the codewheel's center of rotation to the optical center (O.C) of the encoder module.

Index Pulse Width (Po): The number of electrical degrees that an index is high during one full shaft rotation. This value is nominally 90°e or 1/4 cycle.

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Storage Temperature	T_S	-10		85	°C	
Operating Temperature	T_A	-10		85	°C	
Supply Voltage	V_{CC}	-0.5		7	Volts	
Output Voltage	V_O	-0.5		V_{CC}	Volts	
Output Current per Channel, Iout	I_{OUT}	-1.0		18	mA	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Temperature	T_A	-10		85	°C	
Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts	Ripple < 100mVp-p
Load Capacitance	C_L			100	pF	2.7 kΩ pull-up
Frequency	f			100	kHz	Velocity (rpm) x N/60
Shaft Perpendicularity Plus Axial Play				± 0.20(± 0.008)	mm(in.)	Refer to Mounting Consideration
Shaft Eccentricity Plus Radial Play				± 0.04(± 0.0015)	mm(in.)	

Electrical Characteristics

Electrical Characteristics Over the Recommended Operating Range. Typical Values at 25°C.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Supply Current	I_{CC}	30	57	85	mA	
High Level Output Voltage	V_{OH}	2.4			V	Typ. I_{OH} = -0.5 mA
Low Level Output Voltage	V_{OL}			0.4	V	Typ. I_{OL} = 10 mA
Rise Time	t_r		180		ns	C_L = 25 pFR_L = 2.7 kΩ pull-up
Fall Time	t_f		50		ns	

Note: Typical values specified at Vcc = 5.0 V and 25 °C

Encoding Characteristics

Encoding Characteristics Over the Recommended Operating Conditions and Recommended Mounting Tolerances unless otherwise specified.

Parameter		Symbol	Minimum	Typical	Maximum	Units	Notes
Cycle Error		ΔC		3	10	°e	
Pulse Width Error		ΔP		7	30	°e	
Logic State Width Error		ΔS		5	30	°e	
Phase Error		$\Delta\phi$		2	15	°e	
Position Error		$\Delta\Theta$		10	40	min. of arc	
Index Pulse Width		Po	60	90	120	°e	
CH I rise afterCH B or CH A fall	-10°C to + 85°C	t_1	10	100	1000	ns	
CH I fall afterCH A or CH B rise	-10°C to + 85°C	t_2	10	300	1000	ns	

Electrical Interface

To insure reliable encoding performance, the AEDB-9140 three channel encoder modules require 2.7 kΩ (± 10%) pull-up resistors on output pins 2, 3, and 5 (Channels A, I and B) as shown in Figure 3. These pull-up resistors should be located as close to the encoder module as possible (within 4 feet). Each of the three encoder module outputs can drive a single TTL load in this configuration.

Customized Solutions

Customization of codewheel CPR is possible. It has to be based on the encoder LPI table given below:

Part Number	LPI
AEDB-9140 # C	36.7
AEDB-9140 # E	73.5
AEDB-9140 # F	94
AEDB-9140 # G	132.3
AEDB-9140 # H	147
AEDB-9140 # A	183

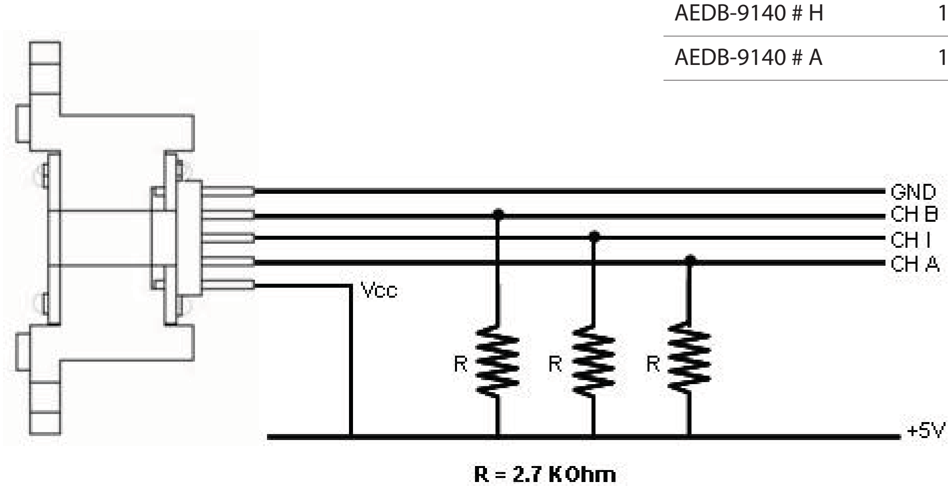


Figure 3.

CPR calculation formula:

CPR = (LPI x 25.4) x 2 x π x ROP

Where:

CPR = Counts Per Revolutions

LPI = Encoder LPI provided in the table

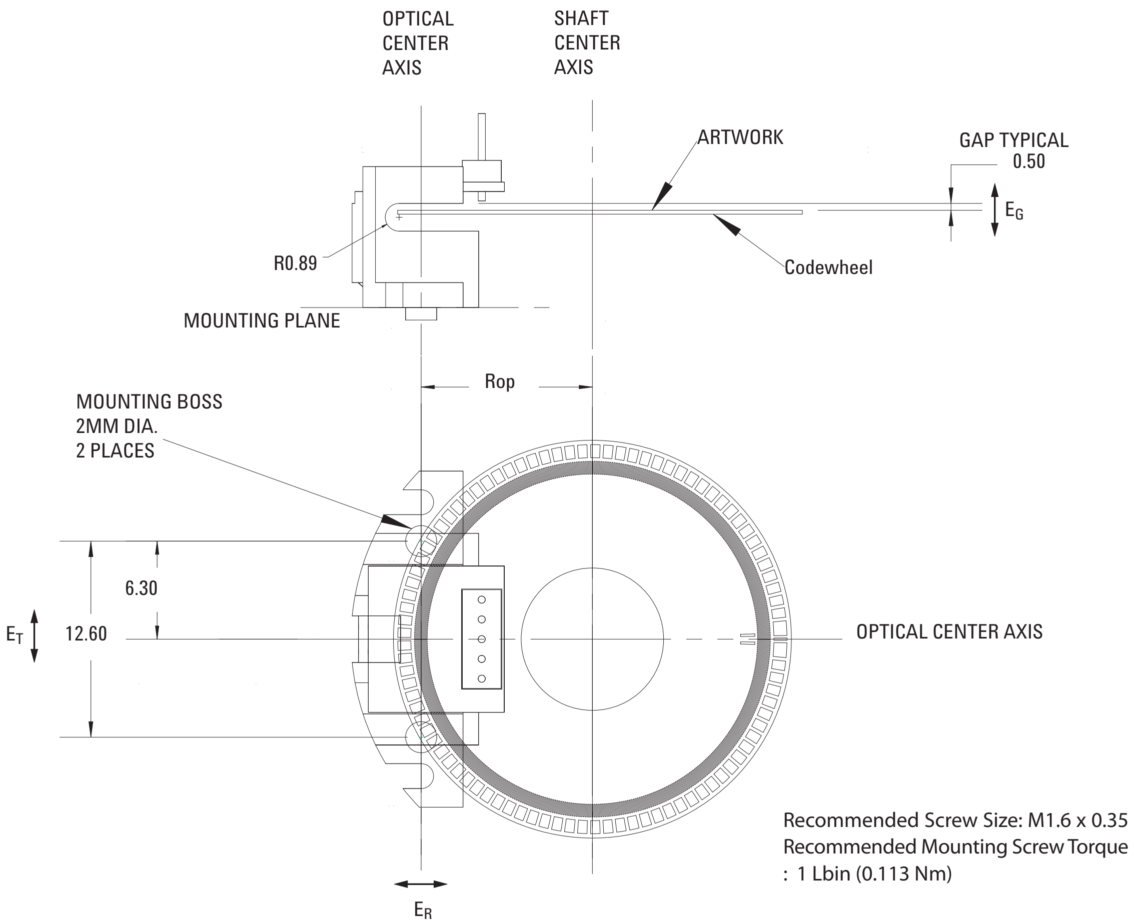
ROP = Encoder Optical Radius in mm

* Recommended maximum Codewheel diameter should not exceed 30mm

Note: The customization of codewheel method is valid from theoretical standpoint. However Avago Technologies strongly recommends a full characterization to be done to determine the actual performance of the encoder with customized codewheel.

Characterization means validating the encoding performance (consist of cycle error, pulse width error, logic state width error, phase error, position error & index pulse width , index channel rise and fall time) over the recommended operating conditions and recommended mounting tolerances.

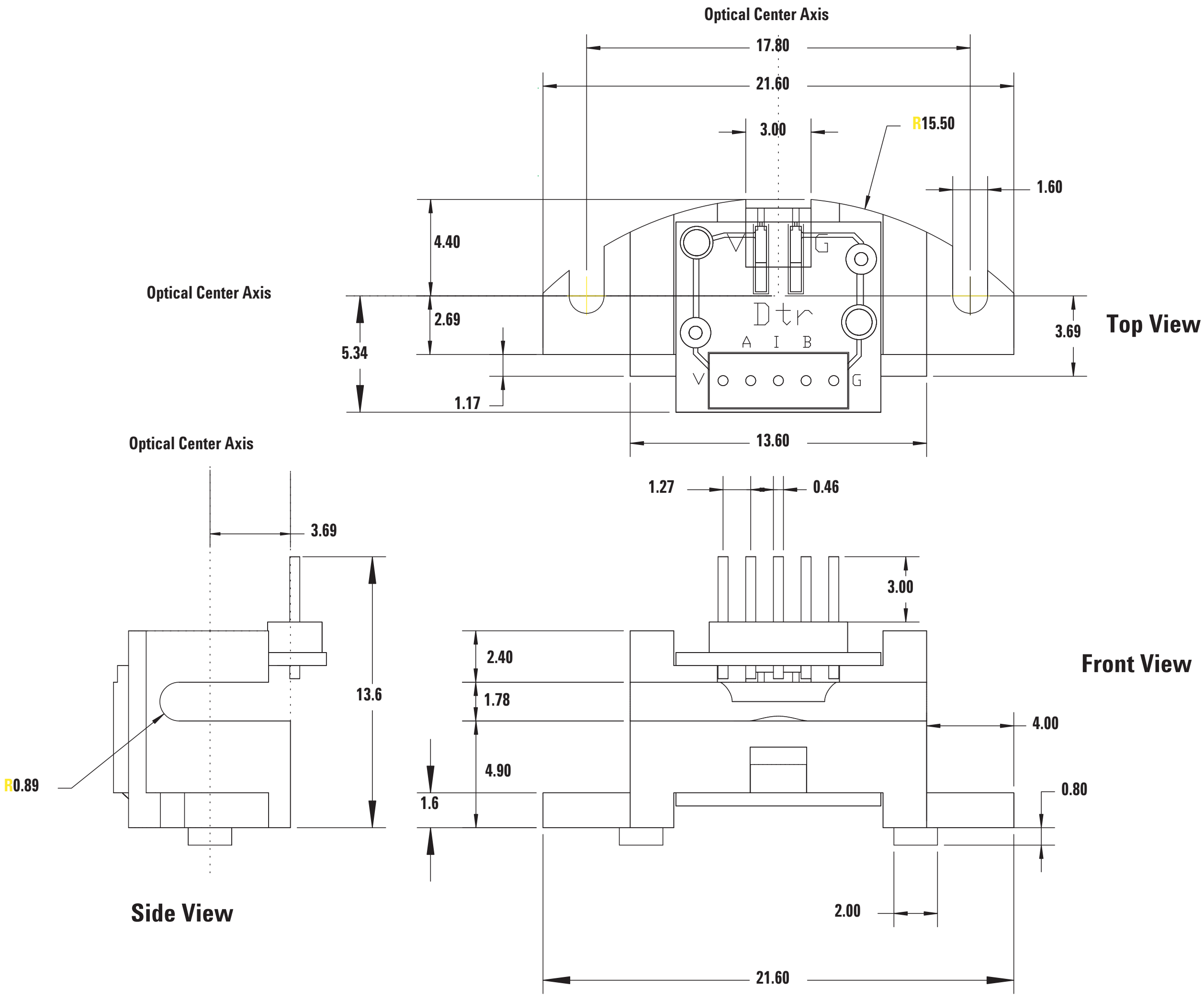
Mounting Considerations



Note:
These dimensions include shaft endplay and codewheel warp. All dimension for mounting the module and codewheel should be measured with respect to two mounting boss, as shown above.

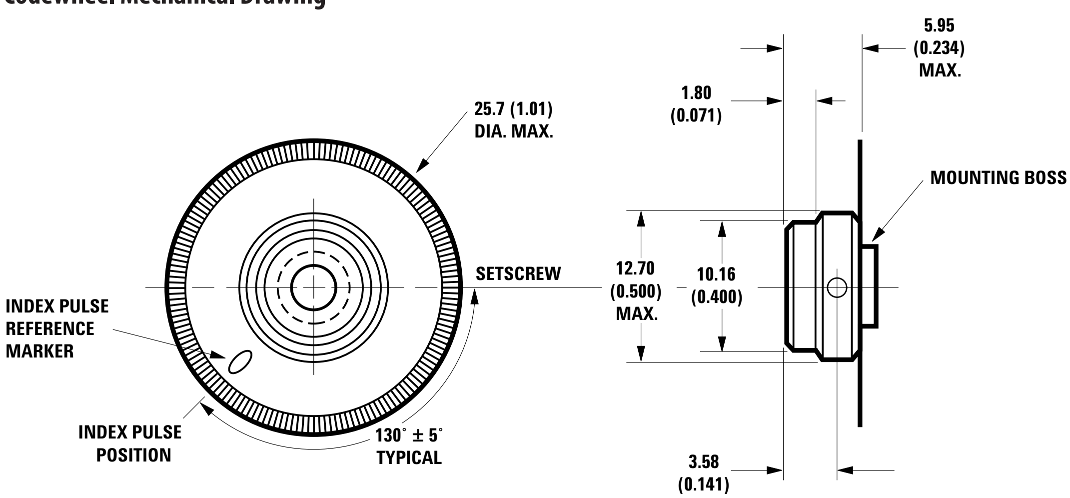
Error		Rop = 11mm	Unit	Notes
E_G	Gap	± 0.20	mm	Recommend to mount the codewheel closer to the detector side (upper side) for optimum encoder performance.
E_R	Radial	± 0.13	mm	
E_T	Tangential	± 0.13	mm	

Package Dimension



TYPICAL DIMENSIONS IN MILLIMETERS

Codewheel Mechanical Drawing



R_{OP} = 11.00 mm (0.433 in.)

DIMENSIONS IN MM (INCHES)

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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