Study of monolithic CMOS pixel sensors in the Belle II experiment upgrade

October 17, 2023

Contents

1 VTX detector **3**

1.1 VTX Layout and mechanical structure 3

1.1.1 iVTX 4

1.1.2 oVTX 6

1.1.3 Thermomechanics and data transmission 8

1.2 Performance simulation 9

1.2.1 Potential VTX geometries 9

1.2.2 Tracking efficiency at low momentum and impact parameter resolution 9

1.2.3 Vertexing resolution 11

1.3 OBELIX chip design 13

1.3.1 Sensor specification 13

1.3.2 Sensor implementation 14

2 Conclusions **17**

1. VTX detector

This chapter focuses on one of the four proposals for the vertex detector upgrade of Belle II, that is VTX. After a brief reference to the reasons behind the vertex detector upgrade, we will go trough VTX concept and layout, designed with a new geometry with respect VXD and also with a different mechanical structure and new pixel sensors (OBELIX), needed to fullfil the new requirements dictated by new environment conditions. Moreover all ongoing studies are supported by continual tests and simulations that we will also take a look at.

1.1 VTX Layout and mechanical structure

In ?? we have introduced in a few words the concept of the *nano-beam* scheme, which could allow to achieve the new fixed target of istantaneous luminosity. This new strategy required a strong focusing of the beams in particular at the IP, resulting in a large amounts of beam induced background and as consequence in a higher dose of radiation in the innermost detector layers. Therefore they have to be robust enough to keep good performance against these new hard conditions. Furthermore to be able to increase the luminosity, SuperKEKB might have to consider an improvement of the final focusing magnets and so a potentially re-design of the interaction region, including the detector but independently of its hit rates and radiation hardness issues.

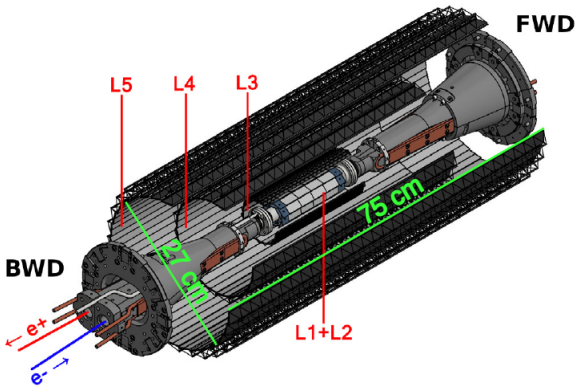

Figure 1.1: Concept of VTX layout with 5 barrel layers, filling the current VXD volume.

VTX project aims to replace the all VXD with a fully pixelated detector based on Depleted Monolithic Active Pixel Sensors (DMPAS) arranged on five layers at different distance from the beam pipe. Actually the radii and the number of the layers are currently subject to several studies and simulations, in order to achieve an optimized arrangement (Figure 1.1). For now two layers are planned in the innermost part (iVTX) and three in the outermost (oVTX). The active lenght of the ladders is expected to vary from 12 to 70 cm to cover the required acceptance of $17° < \theta < 150°$.
As already discussed for other upgrade proposals, it is important to try to reduce the material budget, in order to minimize the multiple Coulomb scattering which particularly affects the very soft particles produced in Belle II collisions. By using a single sensor type, it is expected a reduction of the overall material budget up to 2% of radiation lenght, against the present 3% of VXD, which uses two different sensors such as pixels and strips.

1.1.1 iVTX

The ***internal*VTX** consists of the first two detector layers devised togheter with a self-supported air-cooled all-silicon ladder concept, where four contiguous sensors are diced out of a wafer, thinned and interconnected with post-processed redistribution layers. They are designed to be at 1.4 and 2.2 cm respectively from the beam pipe, and target an individual material budget of about 0.1% radiation lenght. This is actually achivable because the overall surface of these layers is moderate, below 400 cm^2, as well as low sensor power dissipation is expected to be low and the connections needed for the operation to be a few. Precisely for these reasons, air cooling could be a workable system to avoid overheating.

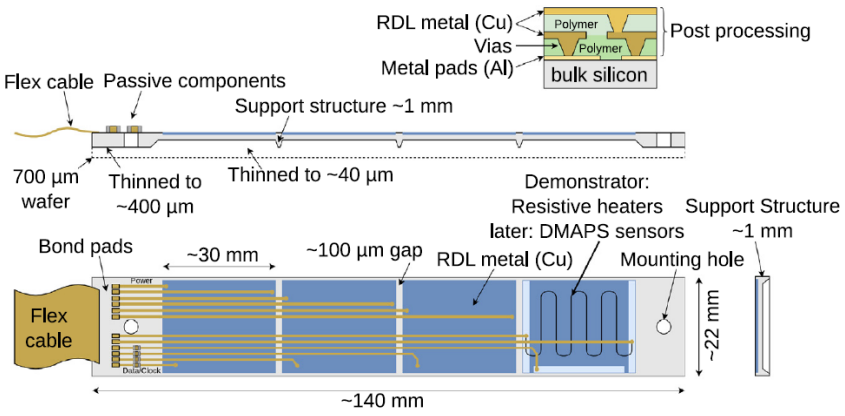

Figure 1.2: Sketch of the all-silicon ladder concept of the iVTX. Four dummy sensors are shown in blue on the silicon support in grey. The yellowish lines instead, indicate power and data transmission lines. Power is delivered to the ladder by a flex cable, which also transmits data to and from the chips in the final one.

The ladder has to be equipped with four of the aforementioned OBELIX chips and thinned to 50 μm except in some border regions, where a few hundreds

of μm are necessary to ensure mechanical stability. In order to interconnect the sensors along the ladder and provide a unique connector at the backward end, during the post-processing metal strips are etched on the redistribution layer (RDL). The latter has the main purpose to route power and data via impedence-controlled transmission lines to a flex cable, added at the end of the ladder. After the RDL processing, the backside of the ladder has to be thinned in accordance with what was previously mentioned. Mounting holes will be added via laser-cutting.

In Figure 1.2 is showing a sketch of the iVTX demonstrator ladder (currently under production), 140 mm long and 22 mm wide (grey). Instead of the actual sensors, it is equipped with four dummies chips with a lenght of about 30 mm (blue), which are used as resistor to mimic the estimated heat load in order to test the air cooling system and more generally to characterized the electrical, mechanical and thermal performance of the ladder. A redistribution layers for power and data is also added to the demonstrator, in order to connect the chips with a flex cable at the end of the ladder (yellowish lines). In addition the wafer is thinned to 400 μm and the sensitive areas down to 40 μm with the purpose to test the mechanical integrity of the whole structure.

R&D

The R&D is ongoing and the full-silicon ladder concept is currently being assessed with industrial partners. First thinned ladders have been produced and characterised with different thickness and geometry.

In addition several tests are focused on evaluating power delivery efficiency, the quality of the signal which travel through the ladder and also the process used to fully assembly it. In Figure 1.3 are shown eye diagrams from simulation with a transfer rate of 640 Mbps, which may imply that 320 Mbps of data rate will be possible.

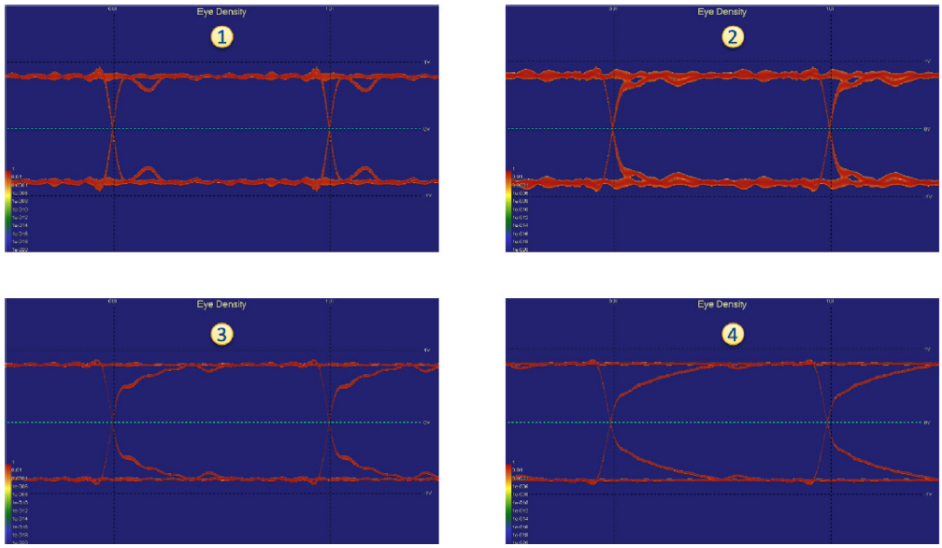

Figure 1.3: Eye diagrams of the iVTX data transmission lines at four different locations on the ladder.

Moreover it has been demonstrated that air at the temperature of 15° and flowing with a speed of 10 m/s succeeds to cool a single inner module, assuming power is uniformly dissipated on the sensor surface. The maximum temperature reached is 20°C.

Through very first estimates it is expected that an equivalent section of 6 tubes with 10 mm of diameter is necessary to expel the heat from the inner layers, roughly equal to 65 W. So it is necessary to design a mechanical structure which forseens the space needed to the tubes in order to bring the air at the IP and also compatible with the new interaction region.

1.1.2 oVTX

The ***outer*VTX** consists of three layers respectively at radii of 39 or 69, 89 and 140 mm from the beam pipe and because of the larger distance required to cover the acceptance, they are not self-support. They follow a more traditional approach, strongly inspired by the designed developed for the ALICE ITS2. Each ladder is water cooled and made of a light carbon fiber support structure, called *truss*, which provide the mechanical integrity. Its structural design is showed in Figure 1.4: 70 cm long and 5.8 g of weight, it is able to support more than 40 sensors in two rows next to each other with a small overlap, earning a material budget of 0.3% X_0 for the first two layer and 0.8%X_0 for the outermost one.

Figure 1.4: Prototype of the layer 5 *truss*, which is the longest, made from thin carbon fibre structures.

For the cooling of the ladder a cold-plate concept is under development (Figure 1.5), on which the sensors are glued and that in turn is installed on the truss. For each row there is a polymide cooling tube that runs over all the sensors and turns back at the other end, so that the heated coolant leaves on the same side. Then two flex print cables connect the two halves of the ladder to the connector.

Figure 1.5: A prototype of the cold-plate for colling. One coolant tube(golden) is connected to the cold plate(black) and turns 180° on the other end (not shown) so that the coolant flows in both directions and thus leaves on the same side it starts.

For layer 3 instead, only one flex print cable in the backward side is considered in order to leave more space in the forward for other possible services and accelerator components. In addition for the third layer two different solutions are under study: at radius of 39 mm e 69 mm respectively. In Figure 1.6 are displayed schematic examples of some hypotheses.

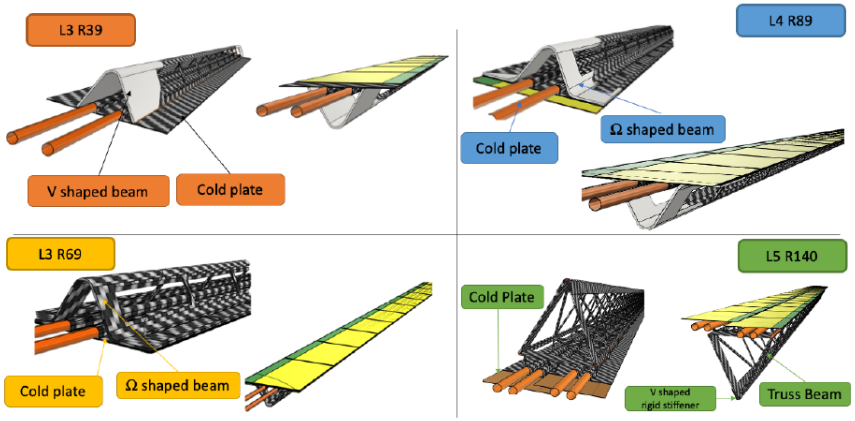

Figure 1.6: Schematic view of possibile solutions for the three outermost layers.

In Figure 1.7 are shown the several substructures described before, that shape a ladder of the outermost layer 5. From bottom to top come in succession the carbon fibre structure, two cold-plates for the two neighbouring sensor rows (Chips, in grey) and the flex cables for power and data transmission (green).

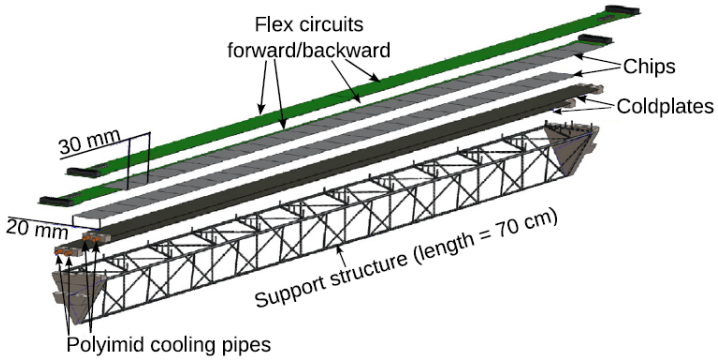

Figure 1.7: An exploding drawing of a fully assembled layer 5 ladder.

R&D

The carbon fiber support structure and flex cable have been designed and fabricated for the last ladder, which is also the longest. Also services for the last two ladders, like electrical connections and cooling, can be provided both on forward and backward sides. A Multiline Power Bus has been realized in

order to power each OBELIX chip along the ladder by a dedicated VDD and GND pair.

After the assembly described in the previous, first thermo-mechanical tests were performed and they show that the first resonance frequency is at 200 Hz, which is safely far from the one of the typical earthquakes in Japan and also that the thermal properties are good.

Trying to reduce as much as possible the material budget, the transmission lines and the flex cables has to be as thin as possible, but also need to ensure safe data transmission. Trace widths are trimmed to fulfill the same maximum voltage drop requirement (200 mV) for all the chips.

For this reason, the outermost ladders long 70 cm are equipped with two flex cables, one from each side of the *truss*. In Figure 1.8 the resulting eye diagram from testing the signal integrity of one of the 35 cm long transmission lines for data transmission rate of 500 Mbps. This result demonstrates that the bandwidth is large enough to allow more then needed 160 Mbps for data transmission.

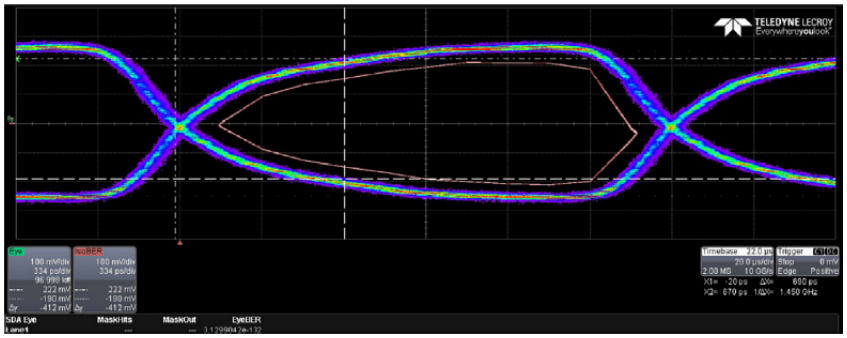

Figure 1.8: Eye diagram for the oVTX transmission line signal integrity of the layer 5 flex cable.

In addition, thermal tests have been performed for the last layer prototypes using kapton heaters to emulate the power dissipation of the chips. The coolant (demineralized water) has been set to a temperature of 10° at the beginning, the environment at 20° with a negative pressure 0f 0.2 bar. Results have been demonstrated that for three different configurations of the flow (such as monodirectional, bi-directional and with an U-turn at one end) the average temperature stands at 24° with a maximum gradient of $\Delta T \approx 4°$ along the full lenght of the ladder.

All these test validate the design of the longest ladder, which is indeed the most challenging, and therefore the possibility to operate the chips safely.

1.1.3 Thermomechanics and data transmission

The proposed VTX detector intends to employ the same sensor type for all the layers in order to use a unique control and power supply system. It is expected to operate at room temperature and for what we have seen in the previous,

the smaller cross section of data cables, the usage of optical fibers and the less complex cooling system might allow a considerable reduction of services with respect to the current VXD. This allows more room for maneuver in the design of the new IR, needed for ramping up the istantaneous luminosity in the future.

As consequence also the design of the mechanical support system, data cables and acquisition system required could be more simple and in particular, the standard PCIe40 acquisition boards used in Belle II match well the data throughput requirement.

1.2 Performance simulation

As we have seen in chapter 2, the experiment aims to reach a new peak of luminosity in further future, but it has to face also the consequences, like the higher level of machine related background and so larger doses of radiation, expecially in the inner layers of the whole detector. For this reason a lot of simulations and studies are focusing on ensuring that the main physics goals of the experiment will be achieved despite the more severe conditions to which it wuold be subjected.

The VTX upgrade program wich foresees for a new silicon vertex detector with high granularity in both space and time, could bring significant improvements in tracking efficiency expecially at low momentum, in the impact parameter resolution and in the robustness against backgrounds.

1.2.1 Potential VTX geometries

As we have already mentioned in the description of the possible VTX layout (subsection 1.1.2), two different VTX geometries are currently under study, which differ only in the position of the third layer (Figure 1.6).

The ***nominal*** geometry is expected to maximize the track impact parameter resolution and it places the third layer at 3.9 cm from the IP. The ***alternative*** geometry instead, aims to improve the K_S^0 reconstruction efficiency and the third layer is located at 6.9 cm from the IP.

Several simulations and investigations are ongoing and they are comparing performance of these two different layout with that of the current Belle II detector (utilizing a full Geant4 simulation of the detector in the study of specific decay modes of interest). Moreover, the different machine backgrounds predictions are also examined in order to consider all effects and correlations.

1.2.2 Tracking efficiency at low momentum and impact parameter resolution

Tracking efficiency at low momentum is one of the areas where the VTX upgrade scenarios show more promising results, particularly for the *soft pions* originated from the decays of $D^{*\pm}$ mesons.

Studies are based on the reconstruction of the decay chain $B^0 \to D^{*-} l^+ \nu$, with $D^{*-} \to \bar{D}^0 \pi^-_{soft}$ and $\bar{D}^0 \to K^+\pi^-$ or $K^+\pi^-\pi^+\pi^-$. All background scenarios metioned in **??** are considered in the evaluation of the *nominal* VTX performance and they are compared with the nominal Belle II geometry in the

intermediate (v2) background hypothesis. In table 1.9 what has been obtained is shown.

	Belle II (v2)	VTX (v1)	VTX (v2)	VTX (v3)
Generated events	32533	32559	32559	30255
Correctly reconstructed signal	10059	16913	16848	15583
Combinatorial	28495	51375	51826	47527
Efficiency	30.9%	51.9%	51.7%	51.5%
Purity	26.1%	24.8%	24.5%	24.7%

Figure 1.9: Reconstruction efficiency and purity for the the decay chain $B^0 \to D^{*-} l^+ \nu$, with $D^{*-} \to \bar{D}^0 \pi^-_{soft}$ and $\bar{D}^0 \to K^+ \pi^-$, for the nominal Belle II detector at the intermediate background conditions and the nominal configuration of VTX in all three background scenarios.

We can see that the VTX reconstruction efficiency[1] in all three background hypotheses, results to be improved of almost a factor 1.7 with respect to the nominal Belle II, with comparable purity[2] . Moreover efficiency remains practically stable in all background conditions, even in the most severe one.

This enhancement in tracking efficiency relies in particular on improved tracking efficiency for the π^-_{soft} mesons, as we can see in Figure 1.10.

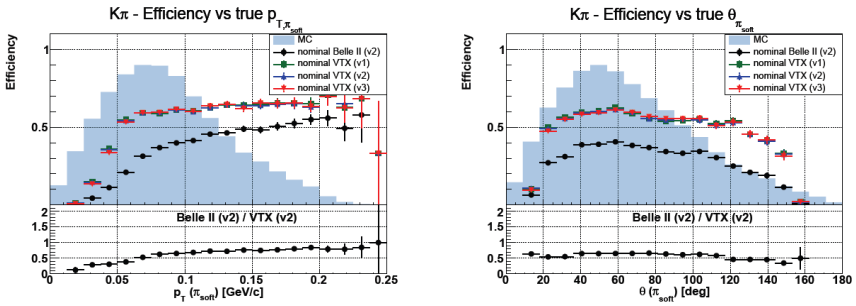

Figure 1.10: Reconstruction efficiency of $B^0 \to D^{*-} l^+ \nu$ as a function of the transverse momentum of the π^-_{soft} (from $D^{*-} \to \bar{D}^0 \pi^-_{soft}$) in the plot on the left and of the polar angle of the π^-_{soft} on the right. The shaded blue histograms represents the momentum spectrum of the π^-_{soft}. The nominal Belle II geometry efficiency in the intermediate background scenario (**v2**) is represents by black dots and it is compared with the nominal VTX configuration in the optimistic (**v1**, green squares), medium (**v2**, blue upward pointing triangles) and pessimistic (**v3**, red downward pointing triangles) background hypotheses. The bottom plots show the ration between nominale Belle II and nominal VTX in the **v2** background scenario.

For all scenarios with nominal VTX, there is a powerful improvement for transverse momenta below 0.05 GeV/c, with respect to the nominal Belle II.

[1] Efficiency is defined as the ration between the number of correctly reconstructed signal events and the total number of candidates.

[2]

Only for p_T greater than 0.2 GeV/c the reconstruction efficiency of Belle II approach those of the VTX.

For p_T higher than 0.3 GeV/c instead, the momentum resolution is dominated by the CDC and there is not a significant enhancement in track momentum resolution in the preceding example.

1.2.3 Vertexing resolution

The studies on vertexing performance have been conducted considering samples of one million $B^0 \to J/\psi K^0_S$ events generated and reconstructed with all the aforementioned combinations. The distributions of the decay vertex resolution σ_z (i.e. the width of the distribution obtained considering the differences between the measured and the true simulated positions) along the z axis of the B decay signal, are shown in Figure 1.11.

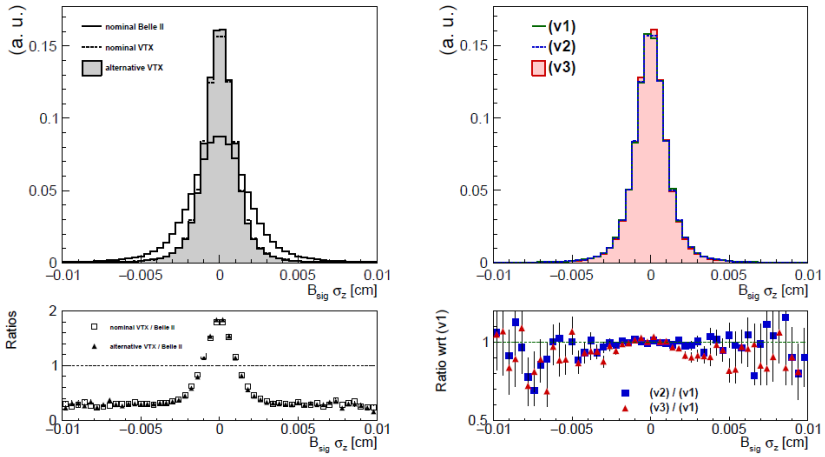

Figure 1.11: On the left: comparison of the B decay vertex resolution along the z axis in $B^0 \to J/\psi K^0_S$ events for the nominal Belle II (solid line), nominal VTX (dotted line) and alternative VTX geometry (filled grey histogram). The bottom plot shows the ratio between the VTX geometries (empty squares the nominal one and filled triangles the alternative) and nominal Belle II.
On the right: B decay vertex resolution along the z axis for the nominal VTX geometry in the three background scenarios: optimistic **v1** (green solid line), intermediate **v2** (blue dotted line) and pessimistic **v3** (red filled histogram). The bottom plot represents the ratio between the two higher background scenarios and the optimistic one.

In table 1.12 a summary of the results that shows that the new geometries achieve a better resolution on the B decay vertex of about 35% on average and they also do not suffer of any significant degradation as the background conditions varies, unlike the nominal Belle II configuration.

The VTX geometries have been demonstrated to achieve better performance also for the vertexing resolution along the x and y axes. Also in these directions they turn out to be almost insensitive to the different levels of background.

B_{sig} z vertex resolution (μm)	Bkg (v1)	Bkg (v2)	Bkg (v3)
Belle II	21.9	23.0	24.9
Nominal VTX	14.5	14.4	14.1
Alternative VTX	14.4	14.3	14.0

Figure 1.12: B_{sig} vertex resolution along the z axis for the three detector geometry and the three background scenarios.

Similar studies for the K_S^0 decay vertex resolution are displayed in Figure 1.13 and in the same way, the upgraded geometries reach a better vertexing resolution with respect to the nominal Belle II detector without any sginifcant degradation as the backgrounds increase. It is importan to notice that in the right plot there is a spurious effect that cause an apparent improvement of performance in the worst case scenario among those considered. This is due to the loss of reconstruction efficiency for candidates with large flight distance (thus affected by poorer vertex resolution).

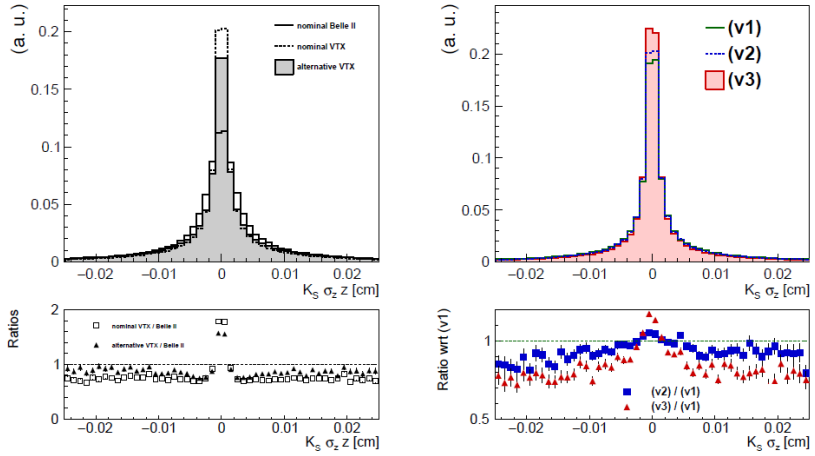

Figure 1.13: On the left: comparison of the K_S^0 decay vertex resolution along the z axis in $B^0 \to J/\psi K_S^0$ events for the nominal Belle II (solid line), nominal VTX (dotted line) and alternative VTX (filled grey histogram). Thebottom plot shows the rattio between the VTX geometries (empty squares for the nominal and filled triangles for the alternative) and nominal Belle II detector. On the right: K_S^0 decay vertex resolution along the z axis for the nominal VTX in the three background scenarios: optimistic **v1** (green solid line), intermediate **v2** (blue dotted line) and pessimistic **v3** (red filled histogram). The bottom plot represents the ratio between the two higher background scenarios and the optimistic one.

1.3 OBELIX chip design

The VTX detector is designed with a single type sensor taylored to the specific needs of Belle II, called OBELIX (Optimized BELle II pIXel sensor) and currently under development, based on fast and high granular Depleted Monolithic Active Pixel Sensor (DMAPS). This new sensor design comes from an evolution of TJ-Monopix 2, whose characterization is the main topic of this thesis, and which will be discussed in chapter 5. Both of them are fabricated in a modified TowerJazz Semiconductor 180 μm CMOS process, that matches particularly well the Belle II requirements. In particular its predecessor is equipped with four different flavors (??), that are distinguished by different type of collection electrode coupling and some little difference in the circuit design. For now their characterization are ongoing and the final decision on which to use for Obelix has not been made.

1.3.1 Sensor specification

A schematic layout of the chip is shown in Figure 1.14. The size of the sensor is expected to be 3 x 1.9 cm^2, with an active area of 3 x 1.6 cm^2 and an additional part in the periphery of about 3 x 0.3 cm^2 dedicated to data pre-processing and triggering. The pixel pitches are designed to be from 30 μm to 40 μm in both direction. As a matter of fact staying in this range is necessary in order to achieve a spatial resolution below 15 μm, wihch is a requirement of the VTX upgrade program.

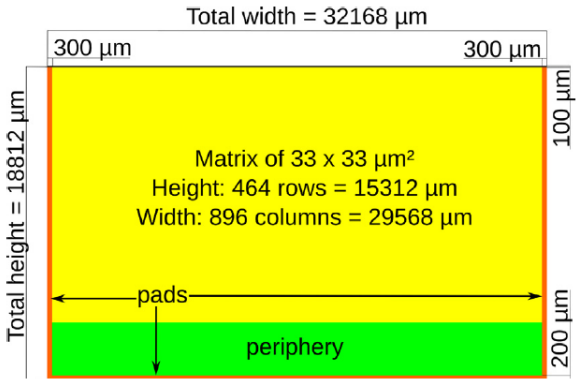

Figure 1.14: OBELIX chip design.

Moreover the sensor thickness has to be below 100 μm to respect the material budget constraint of 0.2%X_0 and as consequence the depleted sensitive region should be lower than 50 μm, perfectly in agreement with the available thickness of MAPS technology. To deal with the target hit rate of 120 MHz/cm^2, the timestamp clock signal can reach down to 25 ns, even if studies have demonstrated that a window of 100 ns (*integration time*) is enough to limit to 320 Mbps the data throughput at the same expected hit rate. All topics faced above allow to realize a sensor with high granularity in both space and time.

With respect to TJ-Monopix 2, which is equipped with a triggerless column-drain readout without memory at the periphery, OBELIX must have a triggered readout architecture, in order to satisfy the needs of Belle II. Moreover the latency is fixed to 5(10) μs and it might operate up to 30 KHz trigger rate.

The expected power consumption instead, is expected to be about 200 mWcm^{-2}, a value which should allow air-cooling for the small area corresponding to the two inner layers and liquid coolant for the outer ones.

Its main design features are summarised in Figure 1.15.

Pixel pitch	30 to 40 μm
Matrix size	512 rows $\times$ 928 to 752 columns
Time stamping	25 to 100 ns precision over 7 bits
Signal Time over threshold	7 bits
Output bandwidth	320 to 640 Mbps
Power dissipation	100 to 200 mW/cm^2
Radiation tolerance	100 MRad and 10^{14} n$_{eq}$/cm^2

Figure 1.15: Designed features of the OBELIX sensor.

	Specification	TJ-Monopix2
Pixel pitch	$< 40\,\mu$m	$< 33\,\mu$m
Sensitive layer thickness	$< 50\,\mu$m	$30\,\mu$m and $100\,\mu$m
Sensor thickness	$< 100\,\mu$m	-
Hit rate capability in the matrix	> 600 MHz cm^{-2}	> 600 MHz cm^{-2}
Hit rate capability at the sensor output	> 120 MHz cm^{-2}	$\gg 100$ MHz cm^{-2}
Trigger delay	$> 10\,\mu$s	-
Trigger rate	30 kHz	-
Overall integration time	< 100 ns	-
(optional) Time precision	< 50 ns	-
Total ionizing dose tolerance	100 kGy/year	1 MGy/year
NIEL fluence tolerance	5×10^{13} n$_{eq}$/cm^2/year	1.5×10^{15} n$_{eq}$/cm^2/year
SEU tolerance	frequently (min^{-1}) flash configuration	-
Matrix dimensions	around 30×16 mm^2	19×19 mm^2
Overall sensor dimensions	around 19×19 mm^2	20×19 mm^2
Powering	through voltage regulators	-
Outputs	one at < 200MHz	one at 160 MHz

Figure 1.16: Comparison between OBELIX requirements and TJ-Monopix 2 features.

1.3.2 Sensor implementation

The technical implementation of the OBELIX sensor have to match all main features listed in table 1.15 . As mentioned above, this new sensor is the development of Tj-Monopix 2, whose characteristics fit the Belle II requirements.

From Tj-Monopix 2 design, the pixel pitch of 33 x 33 μm^2 is maintained, as well as the layout of both digital and analogue parts. Also the Time-Over-Threshold method to digitized the signal is preserved, with a bus width of 7 bit, togheter with the column-drain readout architecture implemented for pairs of columns. Other features which will be explained in depth in chapter 5, have been conserved in the new design like the 3-bit register dedicated to the threshold tuning, but with a larger range of correction. Moreover to aim at the integration time of 100 μs, the clock frequency which defines the precision of ToT and BCID

(that is the timestamp), has been decreased from 40 to 20 MHz. So the current baseline for OBELIX timestamp precision is 50 ns.

However two new modules are added to the implementation, related to the Belle II trigger: the Trigger Logic Unit (TRU) and the Track Trigger Transmitter (TTT).

Trigger Logic Unit (TRU)

The TRU has to select the fired pixel information from the matrix, which are in-time with the triggers sent by the Belle II system. In more details, this module employs two stages of memory in order to manage the data coming from the pixel matrix (Figure 1.17). These components are design in order to minimize power dissipation and to optimize the efficiency even in severe operating conditions: maximum hit rate of 120 MHzcm^{-2}, 30 KHz of trigger rate and 10 μs of trigger delay.

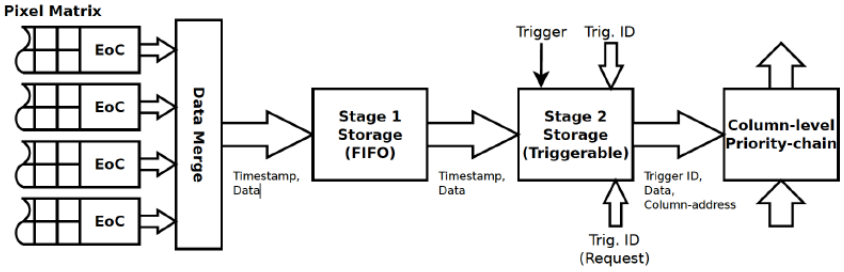

Figure 1.17: Schematic of the Trigger Logic Unit.

The first stage has to store the pixel information during the trigger delay (10 μs). The second memory instead, has the task to compare the BCID of the fired pixel with each trigger time information buffered in a dedicated global memory which keeps track of received triggers. When they have a match, the pixel data is transferred to the Transmission Unit (TXU). Considering the BCID precision time, the time integration of the OBELIX sensor becomes 100 ns.

Track Trigger Transmitter (TTT)

The TTT module divides the matrix in 8 logic regions (this value is still under study) and generates a one-byte word depending on the region that is fired. It is expected taht this information could be transmitted to trigger system within 100 ns and along a line of transmission parallel to the main data output of the sensor. This component behaviour is still under study and it needs of further simulations in correlation with the whole VTX system.

Control Unit (CRU) and power dissipation

The OBELIX sensor, as well as TJ-Monopix 2, is configured by several registers which allow to set crucial features for its operation like threshold settings, masked pixels, time response of the pixel and so on but also define its power consumption. The Control Unit is responsible for receiving these instructions about

the configuration and the trigger information and at the same time sending out data coming from TXU module.

For what concern power dissipation, there are three main features which have the greatest impact: the biasing current flowing into the in-pixel amplifier (i.e. I_{BIAS}), the BCID clock frequency (on which depends the timestamping precision) and the hit rate. In Figure 1.18 is shown the estimations of power dissipation as these parameters vary.

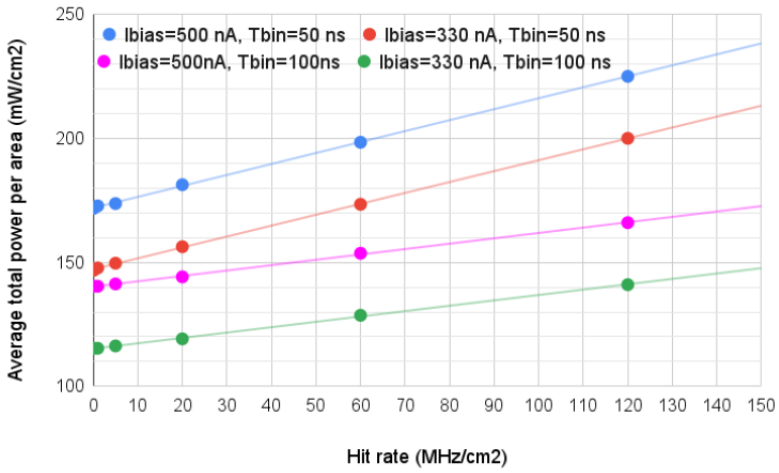

Figure 1.18: OBELIX sensor power dissipation depending on the front edn current (I_{bias}, the BCID frequency (**tbin**) and the hit rate).

As we can see, the power consumption at the maximum hit rate of 120 MHzcm^{-2} exceeds by little more than 10% the power budget of 200 mWcm^{-2} considering the higher precision for the timestamp of 50 ns. Therefore to stay within the power budget it is necessary to find a compromise: reducing timing precision by worsening the BCID precision to 100 ns or decreasing the pre-amplifier biasing current causing a degradation of the time walk.

The first version of the sensor, called OBELIX-1, is being designed and the submission for fabrication is planned in the last month of 2023. A second improved version, OBELIX-2, will be designed based on performance studies on the first version and it is expected that it will be the final sensor needed for the experiment.

2. Conclusions

List of Figures

1.1 Concept of VTX layout with 5 barrel layers, filling the current VXD volume. 3

1.2 Sketch of the all-silicon ladder concept of the iVTX. Four dummy sensors are shown in blue on the silicon support in grey. The yellowish lines instead, indicate power and data transmission lines. Power is delivered to the ladder by a flex cable, which also transmits data to and from the chips in the final one. 4

1.3 Eye diagrams of the iVTX data transmission lines at four different locations on the ladder. 5

1.4 Prototype of the layer 5 *truss*, which is the longest, made from thin carbon fibre structures. 6

1.5 A prototype of the cold-plate for colling. One coolant tube(golden) is connected to the cold plate(black) and turns 180° on the other end (not shown) so that the coolant flows in both directions and thus leaves on the same side it starts. 6

1.6 Schematic view of possibile solutions for the three outermost layers. 7

1.7 An exploding drawing of a fully assembled layer 5 ladder. 7

1.8 Eye diagram for the oVTX transmission line signal integrity of the layer 5 flex cable. 8

1.9 Reconstruction efficiency and purity for the the decay chain $B^0 \to D^{*-} l^+ \nu$, with $D^{*-} \to \bar{D}^0 \pi^-_{soft}$ and $\bar{D}^0 \to K^+ \pi^-$, for the nominal Belle II detector at the intermediate background conditions and the nominal configuration of VTX in all three background scenarios. 10

1.10 Reconstruction efficiency of $B^0 \to D^{*-} l^+ \nu$ as a function of the transverse momentum of the π^-_{soft} (from $D^{*-} \to \bar{D}^0 \pi^-_{soft}$) in the plot on the left and of the polar angle of the π^-_{soft} on the right. The shaded blue histograms represents the momentum spectrum of the π^-_{soft}. The nominal Belle II geometry efficiency in the intermediate background scenario (**v2**) is represents by black dots and it is compared with the nominal VTX configuration in the optimistic (**v1**, green squares), medium (**v2**, blue upward pointing triangles) and pessimistic (**v3**, red downward pointing triangles) background hypotheses. The bottom plots show the ration between nominale Belle II and nominal VTX in the **v2** background scenario. 10

1.11 On the left: comparison of the B decay vertex resolution along the z axis in $B^0 \to J/\psi K^0_S$ events for the nominal Belle II (solid line), nominal VTX (dotted line) and alternative VTX geometry (filled grey histogram). The bottom plot shows the ratio between the VTX geometries (empty squares the nominal one and filled triangles the alternative) and nominal Belle II.
On the right: B decay vertex resolution along the z axis for the nominal VTX geometry in the three background scenarios: optimistic **v1** (green solid line), intermediate **v2** (blue dotted line) and pessimistic **v3** (red filled histogram). The bottom plot represents the ratio between the two higher background scenarios and the optimistic one. 11
1.12 B_{sig} vertex resolution along the z axis for the three detector geometry and the three background scenarios. 12
1.13 On the left: comparison of the K^0_S decay vertex resolution along the z axis in $B^0 \to J/\psi K^0_S$ events for the nominal Belle II (solid line), nominal VTX (dotted line) and alternative VTX (filled grey histogram). Thebottom plot shows the rattio between the VTX geometries (empty squares for the nominal and filled triangles for the alternative) and nominal Belle II detector. On the right: K^0_S decay vertex resolution along the z axis for the nominal VTX in the three background scenarios: optimistic **v1** (green solid line), intermediate **v2** (blue dotted line) and pessimistic **v3** (red filled histogram). The bottom plot represents the ratio between the two higher background scenarios and the optimistic one. 12
1.14 OBELIX chip design. 13
1.15 Designed features of the OBELIX sensor. 14
1.16 Comparison between OBELIX requirements and TJ-Monopix 2 features. 14
1.17 Schematic of the Trigger Logic Unit. 15
1.18 OBELIX sensor power dissipation depending on the front edn current (I_{bias}, the BCID frequency (**tbin**) and the hit rate). . . . 16

List of Tables