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Study of monolithic CMOS pixel sensors in the
Belle II experiment upgrade

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Anno accademico 2022/2023

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1. CMOS MAPS sensors

The fourth chapter aims to introduce the essential features of the semiconductor detector technology, going through the history of its advancements, which have led to the currently most promising sensors based on CMOS logic structure, the Monolithic Active Pixel Sensors (MAPS). As we have seen in the previous chapter, the VTX program wants to make the most of the technologies that have already proven reliable in precision measurements, like the TJ-Monopix development line, with also fast readout and high radiation tolerance. We will briefly present it, mentioning the peculiarities of its prototypes, to better understand how they could fulfill the Belle II requirements.

1.1 Semiconductor detectors

The detection of elementary particles, nuclei and radiations occurs through their interactions with matter. In particular, charged particles are often detected by atom ionization or excitation of the sensitive detector layers along the path they take passing through. This detection method can be used in gases, liquids and semiconductors. We want to focus on detectors that use semiconductors as sensitive material.

All solid can be divided into three categories based on their electrical conductivity: conductors, semiconductors and insulators. In a solid state lattice, the constituent atoms have a dense periodic arrangement and for this reason, the energy of single atoms are split due to the influence of other atoms in the vicinity. The energy levels of some level groups lie energetically so dense (order of meV) that one speaks of *energy bands*, separated from each other by a *band gap*, which represent the distance in energy between them (E_G , energy gap). The electrical conduction properties of materials are determined by the two highest energy bands, which are the **valence band (VB)** and the **conduction band (CB)**. The energy levels within the same band are so dense that the transitions to unoccupied levels, if they are not completely filled, are easily possible. Therefore the electrical conduction properties depend on the band gap between the two levels and on the band occupation, as we can see in Figure 1.1.

In insulators the valence band electrons are strongly bonded to neighbouring atoms, they are not free and they do not contribute to the conduction. In fact the VB is entirely occupied, the CB instead, is empty. As a consequence of the strong interatomic bond, there are large energy gap between the VB and the CB (typically E_G of about 9 GeV). Thus current flow is practically impossible.

In semiconductors weaker bonds between neighbouring atoms result in a smaller energy gap with respect to the insulator (for example 1.12 eV in silicon). In this way electrons from VB can easily overcome the gap, moving on the CB by thermal excitations or by external electric fields. When an electron makes this transition, it leaves a hole in the VB, which could be filled in turn

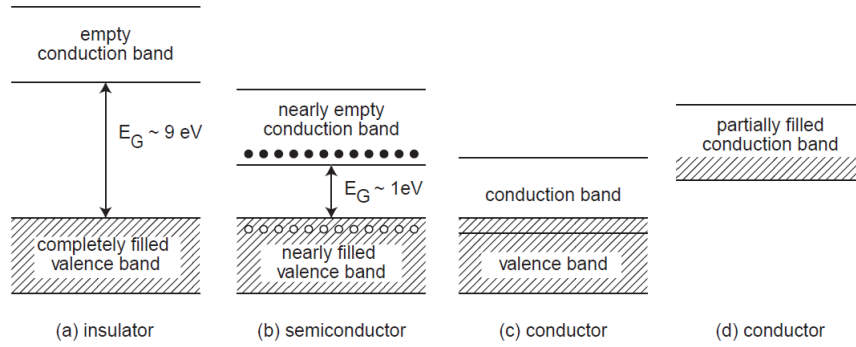


Figure 1.1: Schematic structure of the energy bands in insulators (a), semiconductors (b) and conductors (c,d).

by another electrons of the VB. If and electric field is applied, the free electrons in the CB and the holes in the VB start to move producing two different current flows, one negative and the other positive, respectively.

In conductors the conduction and valence band overlap or the conduction band is partially filled so transitions within the same band and between the two different bands are easy and current conductions requires minimal energy.

1.1.1 Movement of charge carriers and signal formation in semiconductors

Semiconductor materials are the only ones that allow the detection of charged particles by ionization of the sensitive matter (in conductors a current is always present, not only in case of particle or radiation crossing).

When a charged particle or a photon pass through the medium, they release a certain amount of energy mainly by ionization or absorbtion by semiconductor, respectively. Most part of this energy loss, in turn, causes the formation of positive and negative charges, which in this context, are defined charge carriers (the rest is absorbed by the lattice). In semiconductors these carrier are the hole electron pairs created by ionization, which start to move in opposite direction due to an electric field: the holes (positive) migrate towards the **anode** and the electrons (negative) towards the **catode**, which sense the signal induced by this movement. In fact, their drift induce an accumulation of charges on the electrode surfaces, and it is possible to record this charge induction as a charge, current or voltage signal. It is worth to notice that the generation of the signal is dependent on the movement of the carriers relative to the electrodes, and not when they actually arrive, that is the moment in which the signal stop.

The charge carrier density of semiconductors can be modified by doping the material with specific chemical elements, and this process causes a modification of their conduction properties. Undoped semiconductors are called *intrinsic semiconductors*.

Extrinsic semiconductors instead, are artificially doped with external impurities like:

- Pentavalent elements (P, As, Sb), called *donors*, added in a tetravalent material (Si, Ge) produce an axecss of conduction electron with respect to the holes (n doping, Figure 1.2 (a)).

- Trivalent atoms (B, Al, Ga), called *acceptors*, create an excess of holes (p doping, Figure 1.2 (b)).

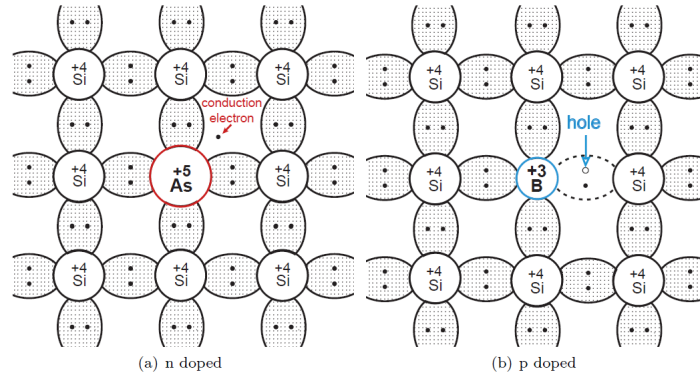


Figure 1.2: Schematic representation of atom bonding structure in n-doped and p-doped semiconductors.

1.1.2 The pn junctions as detector

The base material employed in semiconductor detectors is silicon, which is stable, abundant and it has a low band gap which allow to produce an adequate amount of charge, enough to be detected.

When a p-doped semiconductor get in contact with a n-doped material, a *pn junction* is formed. In particular, the p-doped part is the one where holes are the dominant charge carriers, called **majority carriers**; in the n-doped part of the crystal instead, the majority carriers are the electrons. The presence of these excesses of opposite charge in the two part of the junction, and as consequence the generation of a potential difference across the junction, causes a migration of the majority carriers from each part to the opposite one. At the boundary the charges recombine, and this process creates a zone which is free of charge carriers, called **depletion zone**. After the recombination the atoms of this depletion region are ionized and so it is no longer neutral, but features a *space-charge*: a positive one in the n-layer, and a negative in the p-layer. Moreover these space charge densities are opposite in sign, so they generate an intrinsic electrical field that stop the original diffusion.

[NOTE ON RECOMBINATION]

Moreover, the application of an external voltage V_{ext} between the two section of the junction, provokes a variation of the width of the depletion region, depending on the size and polarity of the applied voltage. It is possible to distinguish:

- *forward bias*, $V_{ext} > 0$: a positive external voltage applied to the p side with respect to the n side, causes a reduction of the depletion region ???
- *reverse bias*, $V_{ext} < 0$: if a negative voltage at the p side or positive at the n side relative to the respectively opposite side is applied, the depletion region gets wider.

Depleted region is a zone without free charge carriers (do not come from the signal), and with the presence of an external electric field (reverse bias), this is a fundamentals for semiconductor detectors.

The performance of the junction as a detector is determined above all by the boundary properties between p- and n- doped silicon. Boundaries of the same doping type, but with different concentration, also create a similar pn structure, like for example n^+n or p^+p . There are also Metal-semiconductor boundaries, used in metal contact with the outside and Metal-Oxide-Semiconductor interfaces (MOS) that we will see in more details in the following.

1.1.3 Complementary Metal-Oxide-Semiconductor (CMOS)

A MOS structure is a double interface made of three different media: an insulator (oxide) placed between the metal and the semiconductor, as shown in Figure 1.3.

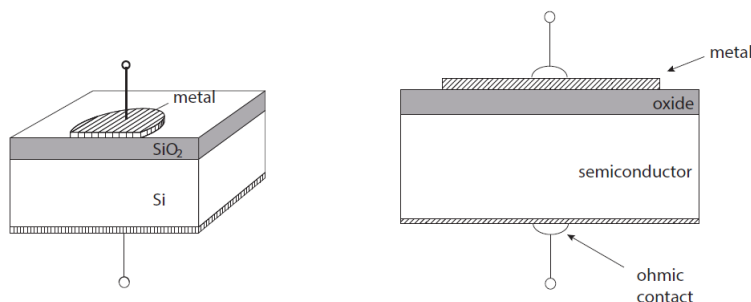


Figure 1.3: A perspective (on the left) and a cross-sectional illustration (on the right) of a MOS structure.

In recent transistor technology, the metal is almost entirely replaced by highly doped polysilicon, like n^{++} and p^{++} since these materials are more resistant to high temperature without reacting with the oxide (?). Despite this, the physics remains essentially the same. The MOS structure plays a very important role in chip electronics, including the readout of detectors, which employ a combination of NMOS and PMOS transistors, embedded in the substrate. This is at the base of the *Complementary* MOS (CMOS) electronics, which allows to develop more complex circuits. This technique consists in accommodate one of the two transistor type in a differently doped area, called *well*. For example, in a p-type substrate, a PMOS transistor are accommodate in n-wells, and vice versa with a n-type substrate.

1.2 Hybrid and monolithic pixel sensors

Nowadays the most important sensors used as tracking detector are the semiconductor detectors, especially with high rate and high radiation level. We have already seen that the particle passing through semiconductor, releases energy producing electron-hole pairs in the depletion region, which in turn, are separated by an external electric field. Moreover, the signal produced, depends on the number of pairs generated, the carriers velocity drifting towards the electrodes, and the electrode geometry. In particular, the drift velocity depends on the charge carriers mobility, which is a function of the electric field, and on the electric field applied (Drude model):

$$v_D = \mu(E)E \quad (1.1)$$

At high electric field values, the mobility starts to saturate. Typical values for silicon: electron and hole mobility are $\mu_n = 1450 \text{ cm}^2/Vs$, $\mu_p = 500 \text{ cm}^2/Vs$ and $v_{sat} \approx 10^7 \text{ cm/s}$. Spatially sensitive semiconductor detectors, like microstrip or pixel detector, are usually very thin (200 -

300 μm) with typical velocities of about 50 $\mu\text{m}/\text{ns}$. So the time needed to pass through the space charge region is of about 4-6 ns.

We can distinguish two different types of silicon detector:

- **single-sided:** sensors are processed only on one side of the silicon wafer. Only one-dimensional position information is possible to obtain. For two-dimensional information, two or more crossed layers of sensors could be superimposed, but in this way, also the material thickness increases, and as consequence the multiple scattering which generally worsens the precision measurements.
- **double-sided:** in this case the wafer is processed on both sides, and this procedure requires special precaution to protect the side already processed. This technology is more expensive. But this type of sensors could measure two orthogonal coordinates at the same time, with only one layer of sensitive material. In addition there is a correlation between the hits on the different sides of the sensor, since they are generated from the same energy release.

There are several types of semiconductor detector which are distinguished from their geometry, their micro-structure, their arrangement and other features. We want to see in more details, two among them: *hybrid* and *monolithic* pixel sensors, where the sensor and the readout could be separate entities or integrated in the same silicon crystal, respectively.

1.2.1 Hybrid pixel detector

Differently from *monolithic* sensors, *Hybrid* pixel detectors are composed by two different parts: a silicon layer structured in pixel cells, which represents the pixel sensor, and the readout chips with the same cell pattern, that process, digitize, store and transmit the hit data. At each pixel, they are connected by a conducting microconnection (called *bump bond*). In Figure 1.4 is shown an example of a detector module. There are different bonding techniques which allow to connect the two layers, like *bump-bonding*, *flip-chipping* and *3D integration*.

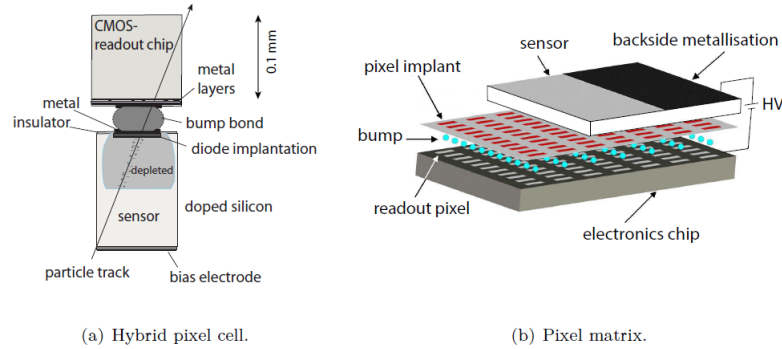


Figure 1.4: On the left (a), the structure of a single pixel cell, made by the sensor and the electronic readout. On the right (b), an exploiting representation of the entire hybrid pixel matrix arrangement.

In a few words, when a particle crosses the sensor, a signal is generated on the electrodes due to the drift of the charge carriers in the depleted region. This signal passes through the conductive bump in the readout chip, where it is amplified and discriminated.

One of the advantage of the pixel detectors with respect to the strip sensors, is the higher tolerance to radiation damage. The *leakage current* increases as the radiation doses become higher, and it depends on the volume of the sensors and it is distributed over all electrode. Thus, in pixel detectors this current is shared among more electrodes with respect to the strip detectors. So the leakage current per electrode is smaller. Moreover, as separate entities, sensor and readout could be independently optimize. Among the disadvantages instead, there are the cost and complexity of the implementation processes, but also large material thickness together with the necessity to add support and cooling structures, which worsen the track reconstruction and momentum resolution because of the multiple scattering. [NOTE ON LEAKAGE]

1.2.2 Monolithic pixel detector

We have seen that hybrid detector are made by two separate structures: the active sensor and the passive readout chip, connected by micro-connections. Since both of them are made of silicon, in principle, it could be possible to build them in a monolithic unit. In this way the amount of material decreases, enhancing the tracking performance and momentum resolution.

Developments of this sensors have tried to exploit industrially already available technologies, like CMOS technologies. They have to reach a large depletion zone in order to improve the signal-to-noise ratio, but also design electrode with small capacitance, to reduce the noise. High radiation tolerance is also required. [note on capacitance, influence power consumption]

An example of this type of sensor is the DEPFET pixel detector, which contains only one active transistor in every pixel. Monolithic Active Pixel Sensors (MAPS) employed CMOS technologies to include a readout circuit in their structure and we will see them in more details in section 1.3

Depleted p-channel field effect transistor (DEPFET)

In a DEPFET pixel detector, each pixel implements only one transistor. In Figure 1.5 is shown an example of a DEPFET pixel.

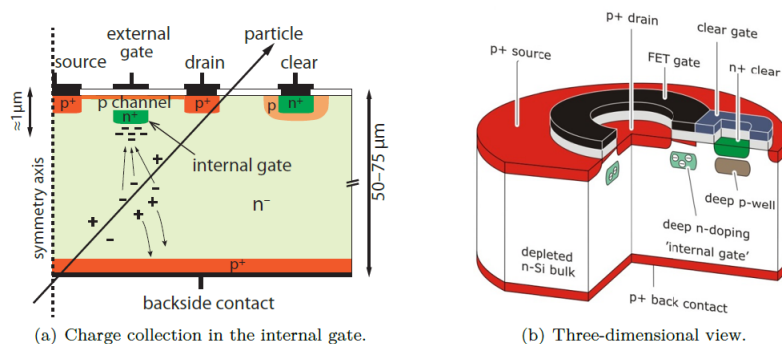


Figure 1.5: On the left (a) a cross section of a circular DEPFET pixel cell, where the charge collection is also sketched. On the right (b), a three-dimensional view of the same pixel cell.

The depletion region extends between the backside p^+ contact and the several p^+ regions near the transistor element (drain, source and a n^+ clear contact installed in a p region) and the n^- substrate. When a traversing particle releases energy, ionizing the medium, electrons drift towards the top surface, and the holes towards the backside due to the external potential.

The transistor is a p-channel MOSFET that produces a hole current from source to drain, controlled by the potential on the external gate. Moreover, there is also a deep n^+ implant placed under the transistor, a few micrometers away. It is the most positive point in the pixel structure and so it is a local minimum for the electrons. In fact this implant features an electron accumulation, which changes the potential making it an *internal gate*. Electrons collected on this electrode, influences with the external gate the current flow in the DEPFET transistor channel. After the measurement, they are removed applying a positive voltage on the *clear contact*. In order to not compete as a collection electrode for the electrons, this element is embedded in a p region (*deep p-well*).

With some variations in the pixel structure, this is the type of sensors that PXD is made of.

1.3 CMOS Monolithic Active Pixel Sensors technology

First prototypes of pixel detector, which employed the CMOS technology to fabricate both the sensor and the readout circuit in the same silicon die, date back to the early 1990s. Further developments have led to the *monolithic active pixel sensors* (MAPS) with an epitaxial[NOTE?] silicon layer for charge collection (at most diffusion?) and then to the Depleted MAPS (DMAPS), where the depleted region is extended throughout the volume. CMOS is the essential feature that have allowed to realize this delicate and complex detectors.

1.3.1 MAPS pixel detectors

This type of sensors have been exploited the CMOS technologies for optical application, where the structure have an epi-layer with high resistivity to detect the light, and the electronic circuitry on the top of it. In this case, not the entire area is sensitive to the charge production. The effectively active fraction of the pixel area is called **fill factor**. In Figure 1.6 is shown a schematic of their structure.

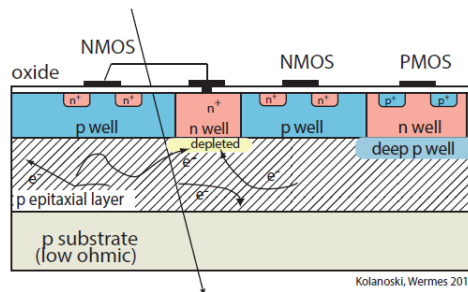


Figure 1.6: Schematic of a monolithic pixel detector (MAPS).

In MAPS pixel detector, charge collection is mostly achieved by diffusion, because the sensitive region is not fully depleted. The collection electrode is a n^+ contact in a n-well, embedded in a p-epitaxial layer (highly resistive?) put on the top of a p substrate (low ohmic). Other n-wells can be necessary, for example to host PMOS transistors, and for this reason they have to be shielded by deep p-well, to prevent them to become competitive for charge collection. These highly doped deep layers assume a negative potential with respect to the collection electrode and hence a repulsive effect. Due to the absence of a drift field in the epi-layer, with the exception of

the region immediately below the collection electrode, collection charge occurs mainly by diffusion and thus it is slow and incomplete. Typical values of the epi-layer thickness are within the range of 1 - 20 μm .

Maps detector can't be used in high rates experiments because they have charge collection time of the order of 100 ns, thus too slow and also a not very suitable radiation tolerance. But they have successfully employed for heavy ions collisions, like STAR experiment at RHIC (Relativistic Heavy Ion Collider) and the ALICE upgrade at the LHC[chip pALPIDE articolo 1]. [In fact they do not require complex bump-bonding processes and they could be produced in large volumes, so they result ideal for large dimension experiments.]

1.3.2 Depleted MAPS pixel detectors

In order to obtain fast and fully collection of released charge, it is necessary to drift the carriers toward the electrodes, by an external electric field. A fully depletion of the sensitive zone, enhance the charge collection, producing large signal (and thus a better signal-to-noise ratio). The depletion depth depends on the substrate resistivity and the bias voltage, according to the relation:

$$d \propto \sqrt{\rho V} \quad (1.2)$$

For this reason, new processing techniques have been employed to allow applying higher voltage or process high-ohmic substrate wafers. Both of them are used to increase the depletion region and so to provide large and fast signal.

We can distinguish two main variants of DMAPS pixel detector: with a *large* or *small* collection electrode, shown in Figure 1.7.

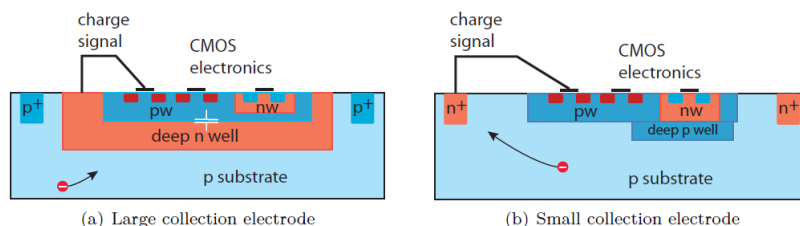


Figure 1.7: On the left (a) a schematic of the large electrode design. On the right (b) the small electrode design.

The *large collection electrode* DMAPS features a deep n-well which acting as electrode but also as shield for the entire CMOS electronics for the readout, which is embedded within it. This architecture improve the radiation tolerance because the reduced average drift distance of the charge carriers decreases the probability of trapping. At the same time though, large size of the electrode implicates higher values of capacitance (several hundred fF) which increases the noise and worsens the timing performance.

The *small collection electrode* variants has a small n-well collection node, distanced from the CMOS circuitry which is embedded in p-well and deep p-well layers (following the logic of the opposite doping?). In this design, low capacitance of about 5-20 fF can be obtained, improving noise and timing performance. Radiation tolerance instead, is more difficult to reach due to larger average distance travelled by the carriers. Smaller pixel dimensions are preferred for small electrode (to reduce the path), and therefore higher power density is accepted in exchange of

increased robustness against radiation.

[NOTE ON TRAPPING]

However a additional modification of the technology have allowed to further improve radiation tolerance. In Figure 1.8 is displayed an example.

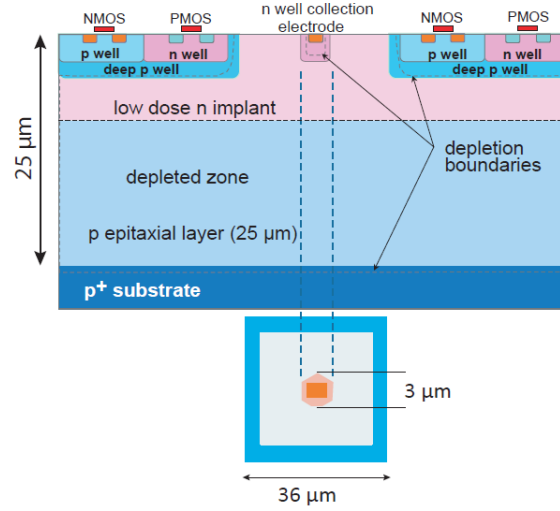


Figure 1.8: Small electrode design with the addition of a low n-doped layer.

The epi-layer is depleted from two pn junctions: the deep p-wells and the low dose n-implant, the n-implant and the p-epitaxial layer[CITE ARTICOLO 2]. This addition creates a potential minimum for electron collection underneath the deep p-well with a field direction towards the n collection well, thus strengthening collection of charges laterally[CITE]. The epi-layer is 25 μm thick and the collection electrode is on positive potential. [ESEMPIO DI SEGNALE CON CAPACITAE CARICA RILASCIATA.]

1.3.3 Silicon On Insulator (SOI) technology

Silicon on Insulator (SOI) technology represents another way to combine the sensitive region and the readout circuit in a single monolithic unit. In this architecture, the transistor is isolated by vertical trenches and is divided from the bulk by a SiO_2 layer, called *buried oxide* (BOX). An high resistivity bulk wafer allows to depleted the volum in the region below the BOX, in order to generate a large charge signal when a particle pass through the detector. The bulk and the CMOS electronics are connected by vertical connections, called *vias*.

In Figure 1.9 is displayed a monolithic SOI pixel, with a doped volume placed between the CMOS circuitry and the BOX. This variation prevents the capacitive coupling from the substrate into the electronics, through the BOX.

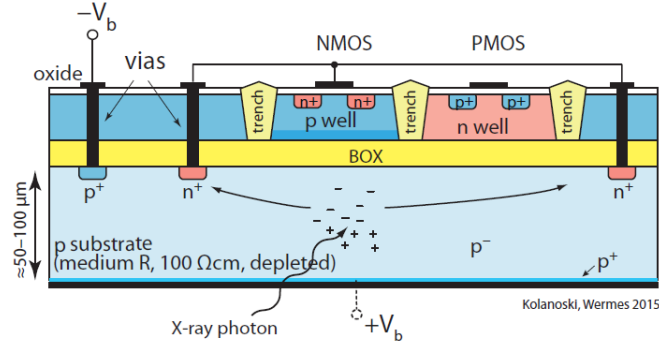


Figure 1.9: An example of a Monolithic SOI pixel.

1.4 History of Monopix developments

As we have try to show in the previous, in recent years, advances in CMOS technologies have led to the development of a new generation of monolithic pixel sensors (DMAPS) with fast readout and high radiation tolerance. For this reason these new devices become promising candidate for high-energy physics experiment with high rate and high radiation environment.

1.4.1 Developments of DMAP devices

Specifically two different lines of DMAPS development have been followed, distinguished by different pixel architectures, entrusted to two different implementation process technologies:

- **large fill factor** line: with large collection electrode and the electronics inside the charge collection well, these prototypes are indicate to experiments with high rate and high radiation conditions, because they could ensure a greater tolerance to huge doses of radiation. They have been fabricated in LFOUNDRY 150 nm design. [REFERENCE] In Figure 1.10 are shown some of these chip development.
- **small fill factor** line: small collection electrode and the electronics outside the charge collection well, these devices need a process modification to enhance the radiation hardness, but they are faster and due to less values of total capacitance, they implicate much less power consumption, with respect to the previous. These devices instead, are fabricated ina modified() TowerJazz 180 nm CMOS imaging process.

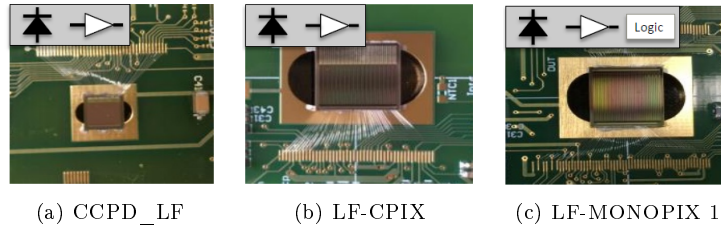


Figure 1.10: LFOUNDRY 150 nm development line.

1.4.2 TJ-Monopix line

In Figure 1.11 are displayed the major prototypes that have allowed to design the last iteration of this series, TJ-Monopix 2, whose characterization results will be shown in ??.



Figure 1.11: TowerJazz 180 nm development line.

The standard TJ 180 nm process has been employed to realize the ALPIDE (sigla) monolithic active pixel sensor, selected for the ALICE Inner Tracking System (ITS) upgrade [reference]. The chip proved to be suitable for the modest ALICE requirements, but the standard process do not ensure the full depletion volume, which is crucial to limit the signal degradation especially after irradiation. For this reason, the aforementioned process modification have been developed by CERN in collaboration with the foundry [cite and reference], that allows full depletion of sensitive layer. This new implementation has been tested in a dedicated chip called TJ-Investigator, and the obtained results have been demonstrated the effectiveness of the modified process.

Therefore two large scale demonstrator chips have been realized, called TJ-Monopix1 and TJ-Malta1, whose main difference lies in the different readout architecture. The TJ-Malta1 chip implemented an *asynchronous* readout architecture, which eliminate the Bunc Crossing ID (BCID, timestamp), in order to reduce the digital power consumption. For TJ-Monopix1 instead, a *column-drain* readout architecture was chosen, which will be described in the following. Both chips have been fully tested and irradiated to investigate their functionality and efficiency, which however has decreased from 97 % to 70 % after irradiation. The reason was address to the weak lateral field at the pixel edge, so the process has been further optimized in order to resolve this issue and another chip, called mini-Malta, was implemented with this variation to test its efficiency. Results show significant improvement, thus it was implemented in the original Tj-Monopix1 and TJ-Malta1 chips. The variation consist in two different structure of the pixel, displayed in Figure 1.12 called **Full deep p-well (FDPW)** and **Removed deep p-well (RDPW)**. As we can see, the deep p-well underneath the CMOS electronics is reduced at the pixel edge in case of RDPW structure. It can be seen the significant improvement of the electric lateral field, which results in turn in faster charge collection and so high efficiency even after irradiation.

Further optimization of the pixel size, which is critical to take full advantage of field shaping through process modifications and to improve charge collection, have been implemented in the last iteration of this development line: TJ-Monopix2, considered as starting point for the development of the OBELIX final chip, designed for the upgrade of the Belle II vertex detector.

Now we want to describe the readout architecture chosen for TJ-Monopix2, which will crucial in the following.

The Column-drain readout architecture(pag.42)

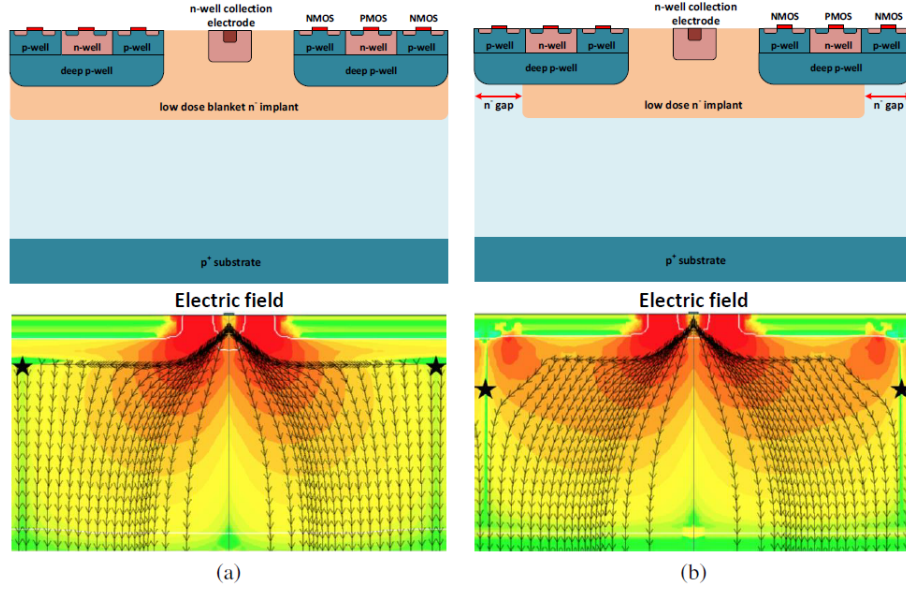


Figure 1.12: In the left, the Full deep p-well (FDPW) structure and its lateral electric field, compared with the Removed deep p-well (RDPW) variation. Both of them implemented the process modification with a low dose n implant.

The *column-drain* architecture implemented in TJ-Monopix ensures fast readout by encoding the analog charge information using the standard **Time Over Threshold (ToT)** technique. This procedure exploits two timing information: the **Leading Edge (LE)** which corresponds to the hit time of arrival (when the signal value goes beyond the threshold), and the **Trailing Edge (TE)** that is when the signal goes below the threshold value. From the difference between the TE and the LE, the ToT can be calculated. The *in-pixel* circuitry implemented a Random Memory Access (RAM) where to store the LE and TE timing info, a Read-Only Memory to store the pixel address and the control and arbitration logic, which we will see more about in the following. The readout is *column-based*, so all pixels of each double column share a common column-bus which could be accessed by one pixel at a time, with a defined priority logic. The column bus includes the BCID timestamp, the data (LE, TE, address) and the control signals. The *periphery* includes the End Of Column (EoC) block which deals with the transmission and readout of the column-bus signals, and the Digital Chip Bottom (DCB), that instead, processes the hit information. The readout could be triggered or full-readout. In TJ-Monopix line follows the second type, hit data is continuously transmitted to the DAQ. In case of triggered readout, hit data is stored in a trigger memory, and the information is transmitted only when the trigger signal arrives.

In Figure 1.14 is displayed an example of the readout of two hits. The readout sequence starts when the TE pulse arrived. A hit flag is set and it activates the **TOKEN** signal, which in turn is raised to warn that the pixel is available to be read out. This signal propagates across the double column with a priority logic until it arrives to a readout controller, which uses other two global signals, the **FREEZE** and **READ**, to control the readout progression. They are distributed to across the EoC blocks and local copies are transmitted only to the double column that has been hit and that has the higher priority (It is a different priority logic among each double column which goes from left to right across the matrix). The first ensures that new hits

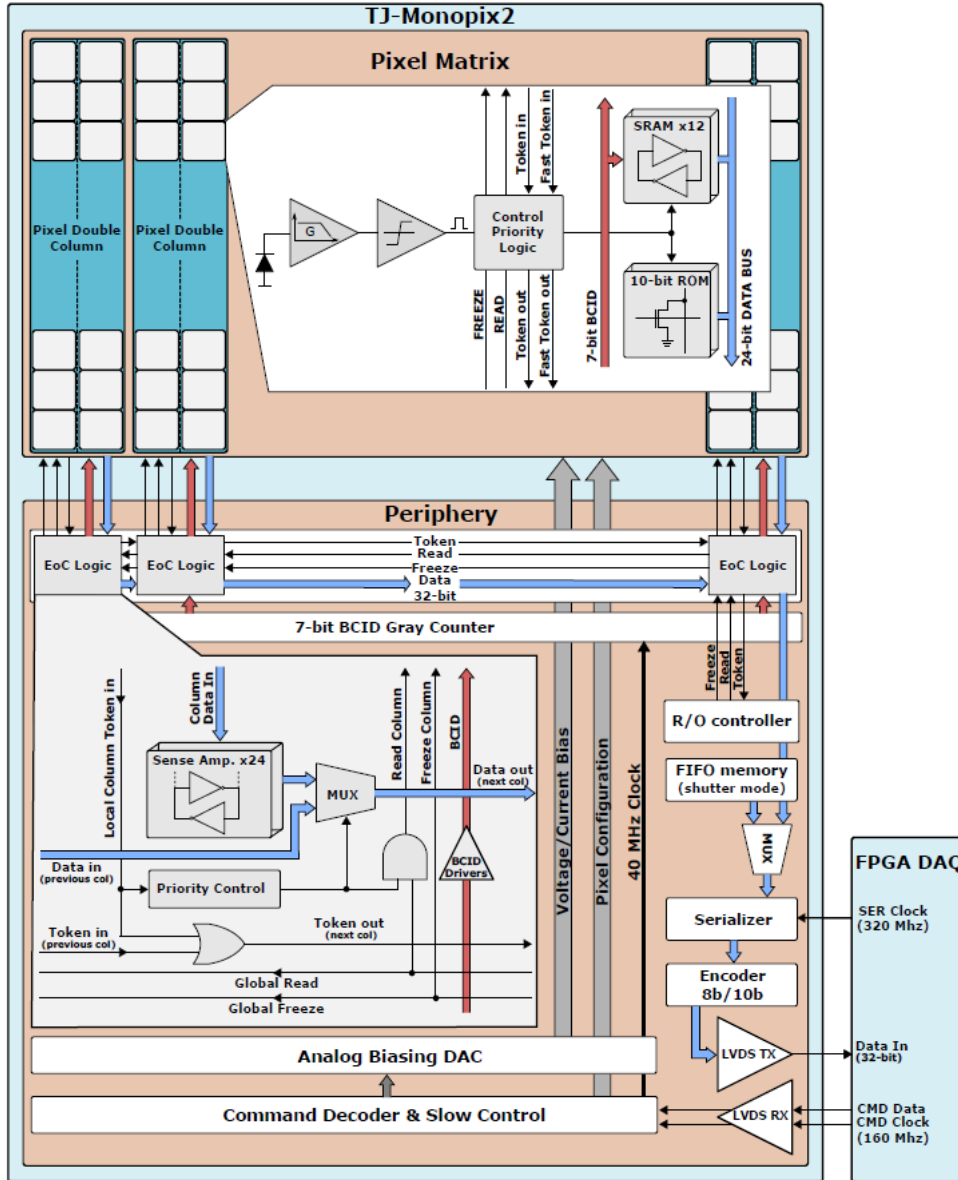


Figure 1.13: Architecture of TJ-Monopix 2.

do not interrupt the pixel priority logic setting other new hit flag, which means that they could not transmit new hit information. In this way the pixel priority in the readout sequence is well defined. The latter instead, allows to the pixel with the hit flag and highest priority to access the data bus and transmit the hit information to the periphery. A series of **READ** cycles allow all pixel in the sequence to be read out.

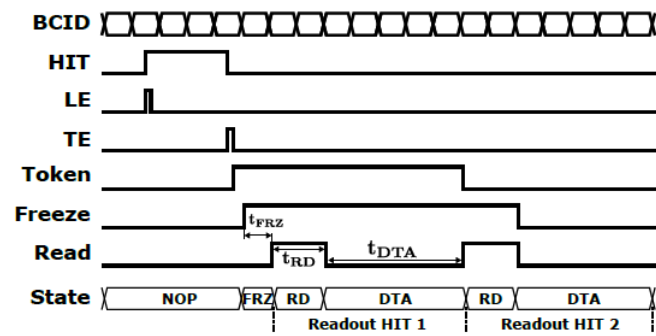


Figure 1.14: ?

2. Conclusions