Embedded System Interfacing

Lecture 16
EEPROM

IMT SCHOOL

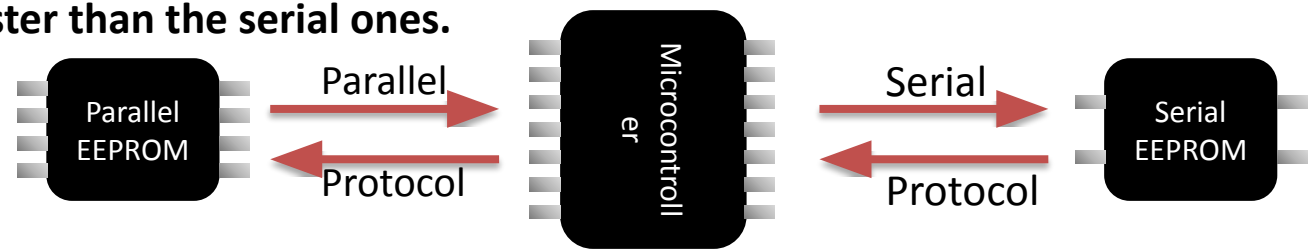
Introduction

Introduction

- **EEPROM as described in previous lectures, is abbreviation for Electrically Erasable Programmable Read Only Memory. It is a type of ROM that can be electrically erased and reprogrammed up to 1 Million cycle.**

The EEPROM can be internal inside the microcontroller, our it can be external to the microcontroller. External EEPROM is connected to the microcontroller through certain communication protocol and hence the microcontroller can make write or read operations.

The External EEPROM interface may be serial or parallel. Serial EEPROM is cheaper than the parallel one, while the parallel EEPROM are normally faster than the serial ones.



24C08 Serial EEPROM

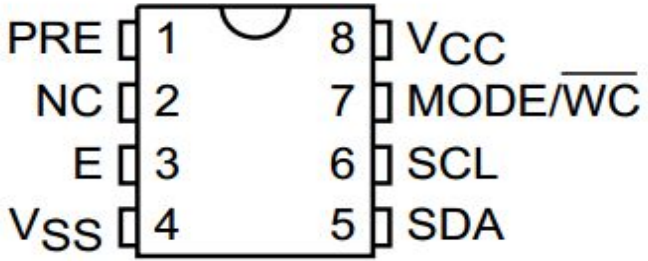
Specifications

- 1 MILLION ERASE/WRITE CYCLES with 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE 3V to 5.5V
- TWO WIRE SERIAL INTERFACE, FULLY I2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 8 BYTES)
- PAGE WRITE (up to 16 BYTES)
- AUTOMATIC ADDRESS INCREMENTING
- BYTE, RANDOM and SEQUENTIAL READ MODES

24C08 Serial EEPROM

Pin Description

PRE	Write Protect Enable
E	Chip Enable Input
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

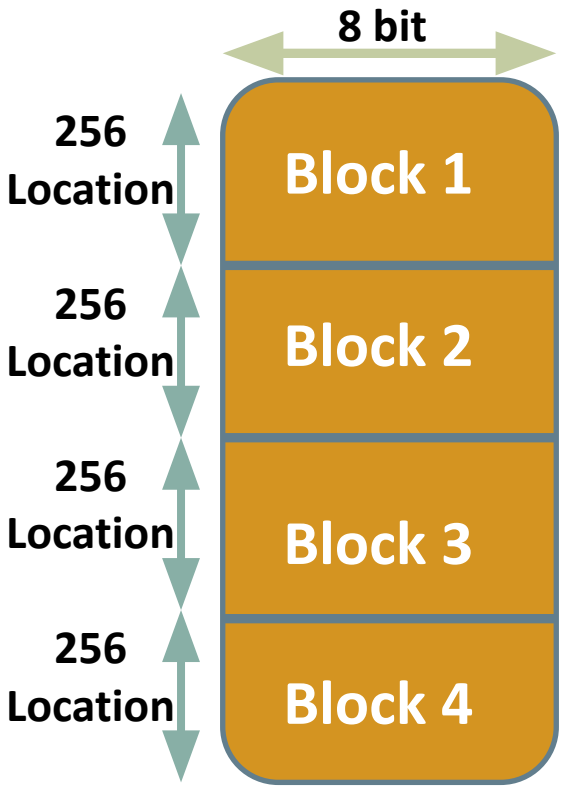


24C08 Serial EEPROM

Description

The 24C08 IC is 8 Kbit electrically erasable programmable memories (EEPROM), organized as 4 blocks of 256 x8 bits.

The memory carry a built-in 4 bit, unique device identification code (1010) corresponding to the I2C bus definition. This is used together with 1 chip enable input(E) so that up to 2 x 8K devices may be attached to the I2C bus and selected individually. The memories behave as a slave device in the I2C protocol with all memory operations synchronized by the serial clock.



24C08 Serial EEPROM

	Device Code				Chip Enable	Block Select		$\overline{RW}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E	A9	A8	$\overline{RW}$

Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010) + E bit Value (0 or 1) + Block Selection bits (A9,A8). Then one bit for read/write and terminated by an acknowledge bit.

Notes:

1- E pin can be connected to GND or Vcc, according to the connection you can write 1 or 0 in the chip address. For that reason, we can connect up to 2 chips from 24C08 at the same I2C bus.

2- The MSB 2 bits in the slave address determine the block to read or write.

24C08 Serial EEPROM

Write Operation:

1- Master Sends Start Condition.
2- Master Sends Slave address(1010+E+Block) + Write Operation.
3- Slave Sends Acknowledge.
4- Master Sends Byte address within the chosen block (0 To 255) To Write.
5- Slave Sends Acknowledge.
6- Master Send up to 8 byte, each followed by an acknowledge from the slave

Read Operation:

1- Master Sends Start Condition.
2- Master Sends Slave address(1010+E+Block) + Write Operation.
3- Slave Sends Acknowledge.
4- Master Sends Byte address within the chosen block (0 To 255) To read.
5- Slave Sends Acknowledge.
6- Master Sends Repeated Start Condition
7- Master Sends Slave address(1010+E+Block) + Read Operation.
8- Slave Sends Acknowledge.
9- Slave send up to 8 byte each followed by an acknowledge from the master

The End

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