MARCOS AUGUSTO FERREIRA

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EDUCATION

Illinois Institute of Technology **Graduated: May 2024**
Bachelor of Science, Computer Science (2020 - 2024) **Major GPA:** 3.96

TECHNICAL SKILLS

Languages: Verilog, System Verilog, C, Python, Java, Scala (Chisel)
Technologies: Vivado Lattice Diamond, UART, I2C, DSPs, Crossing Clock Domains, Git

PROFESSIONAL EXPERIENCE

BiV Lab - Northwestern University **August 2024 - Present**
Research Assistant *Chicago, IL*

- Working as an FPGA developer at the Bio Inspired Vision Lab headed by Emma Alexander (https://www.alexander.vision/)
- Developing low powered hardware convolution filter and bilinear interpolator (see projects) for our image processing techniques used in depth sensing cameras by using lattice semiconductors ultra low powered ECP5 FPGA
- Demonstrated our work in the Computer Vision and Pattern Recognition (CVPR) conference 2025 (to be published soon)

Qualcomm **May 2023 - August 2023**
Software Engineering Intern *San Diego, CA*

- Analyzed the behavior of the Neural Signal Processor on the Snapdragon chip under synthetic and real loads
- Developed Python scripts to automate chip/device configuration, benchmarking, and capturing and visualizing performance metrics

PROJECTS

Convolution Filter & Bilinear Interpolator
https://github.com/Marc103/Image-Processing-SV-RTL

- See a Convolution Filter and Bilinear Interpolator written and tested in System Verilog, using adjustable Fixed Point Arithmetic
- Stream processing pixel data for efficient usage of block ram

Debayering System Verilog Implementation
https://github.com/Marc103/OV7670-with-FPGA-and-Demosaicing

- Working on embedded digital image processing with FPGAs
- In particular, demosaicing bayer pattern
- Setup I2C to communicate with the camera being used (OV7670)

LC-3 ISA CPU Verilog Implementation
https://github.com/Marc103/LC-3-Verilog-Implementation

- Implemented a CPU that follows the Little Computer 3 (LC-3) instruction set architecture from scratch in Verilog
- Performed simulation tests in Vivado Design Suite for QA
- Used the LC-3 ISA CPU implementation to program a Xilinx FPGA
- Leveraged UART as the communication protocol to send and receive data to a terminal emulator
- Reading and writing to dual port video buffer RAM