MARCOS AUGUSTO FERREIRA

(312) 818-0709 mferreira103301@gmail.com https://www.linkedin.com/in/marc10 https://marc103.github.io/

EDUCATION

Illinois Institute of Technology **Expected: May 2024**

Bachelor of Science, Computer Science (2020 - 2024) **Major GPA:** 3.96

Relevant Coursework: Data Structures & Algorithms, Introduction to Algorithms, Computer Organization & Assembly, Systems Programming, Database Organization, Programming Paradigms/Patterns, Programming Languages & Translators, Operating Systems, Data Mining, Software Engineering, Digital Systems, Virtual Machines

TECHNICAL SKILLS

Languages: Verilog, System Verilog, C, Python, Java, Javascript, HTML/CSS, SQL,
Technologies: Vivado, UART, I2C, DSPs, BRAM, LS Diamond, Node.js, React, PostgreSQL, Flask, Conda, Git

PROFESSIONAL EXPERIENCE

BiV Lab - Northwestern University **August 2024 - Present**

Research Assistant *Chicago, IL*

- Working as an FPGA developer at the Bio Inspired Vision Lab headed by Emma Alexander (https://www.alexander.vision/)
- Developing low powered hardware convolution networks for our image processing techniques used in depth sensing cameras by using lattice semiconductors ultra low powered ECP5 FPGA

Qualcomm **May 2023 - August 2023**

Software Engineering Intern *San Diego, CA*

- Analyzed the behavior of the Neural Signal Processor on the Snapdragon chip under synthetic and real loads
- Developed Python scripts to automate chip/device configuration, benchmarking, and capturing and visualizing performance metrics
- Planned to employ linear regression techniques to optimize performance under specific power and thermal constraints

PROJECTS

LC-3 ISA CPU Verilog Implementation https://github.com/Marc103/LC-3-Verilog-Implementation

- Implemented a CPU that follows the Little Computer 3 (LC-3) instruction set architecture from scratch in Verilog
- Performed simulation tests in Vivado Design Suite for QA
- Used the LC-3 ISA CPU implementation to program a Xilinx FPGA
- Leveraged UART as the communication protocol to send and receive data to a terminal emulator

Debayering System Verilog Implementation
https://github.com/Marc103/OV7670-with-FPGA-and-Demosaicing

- Working on embedded digital image processing with FPGAs
- In particular, demosaicing bayer pattern
- Setup I2C to communicate with the camera being used (OV7670)
- Reading and writing to dual port video buffer RAM