Miniproject 1

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https://github.com/MarcEftimie/VLSI.git
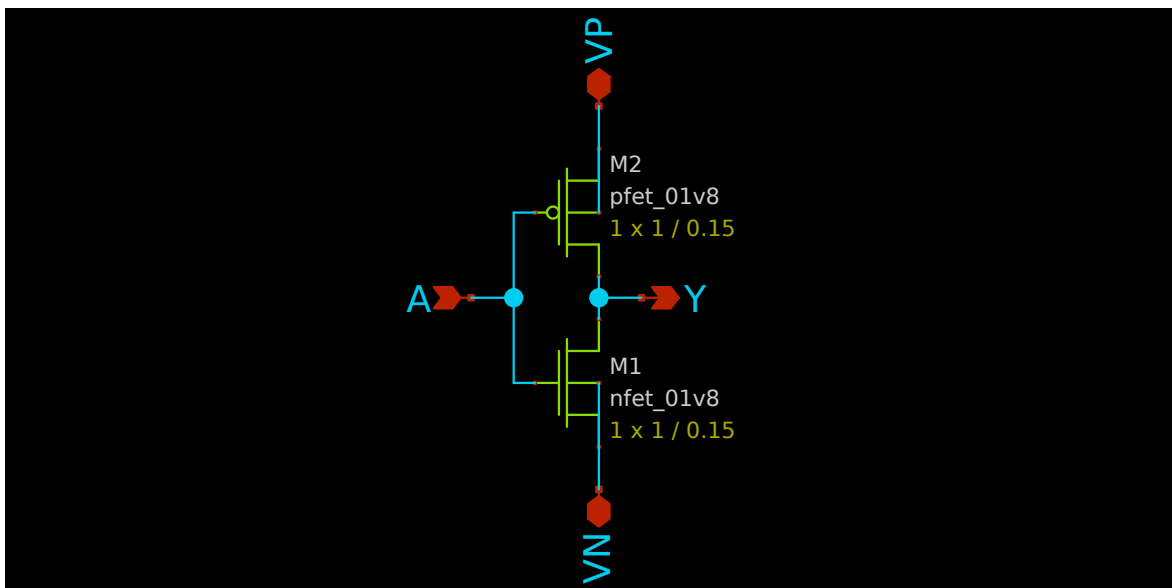
1 Schematics

1.1 Inverter

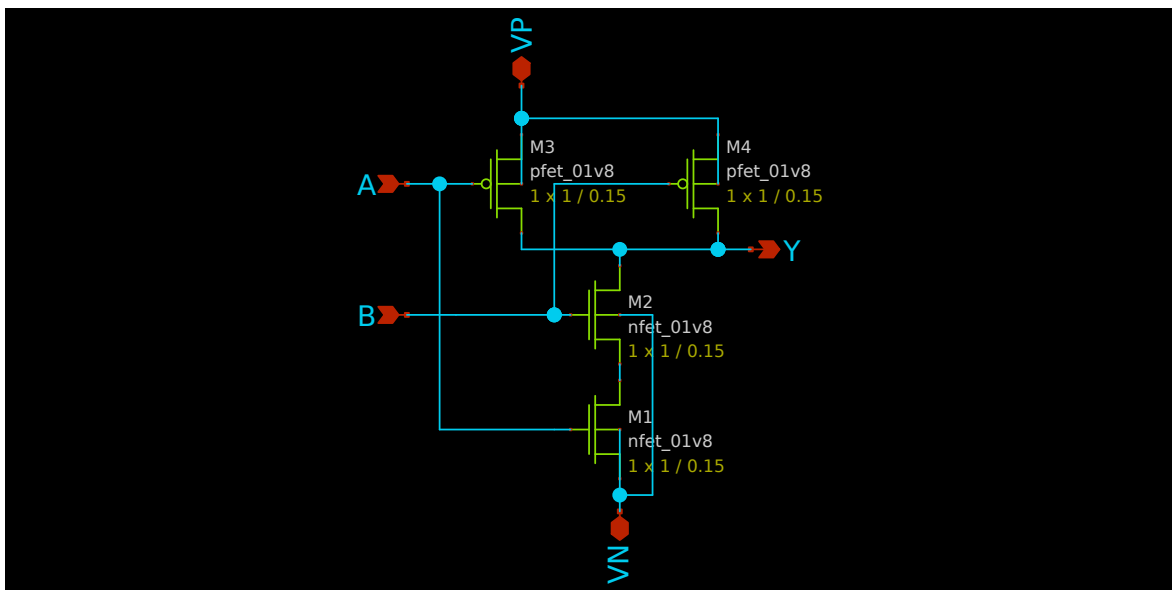Figure 1: Inverts the signal connected to port A.

1.2 NAND

Figure 2: Computed the NAND operation on the signals connected to ports A and B.
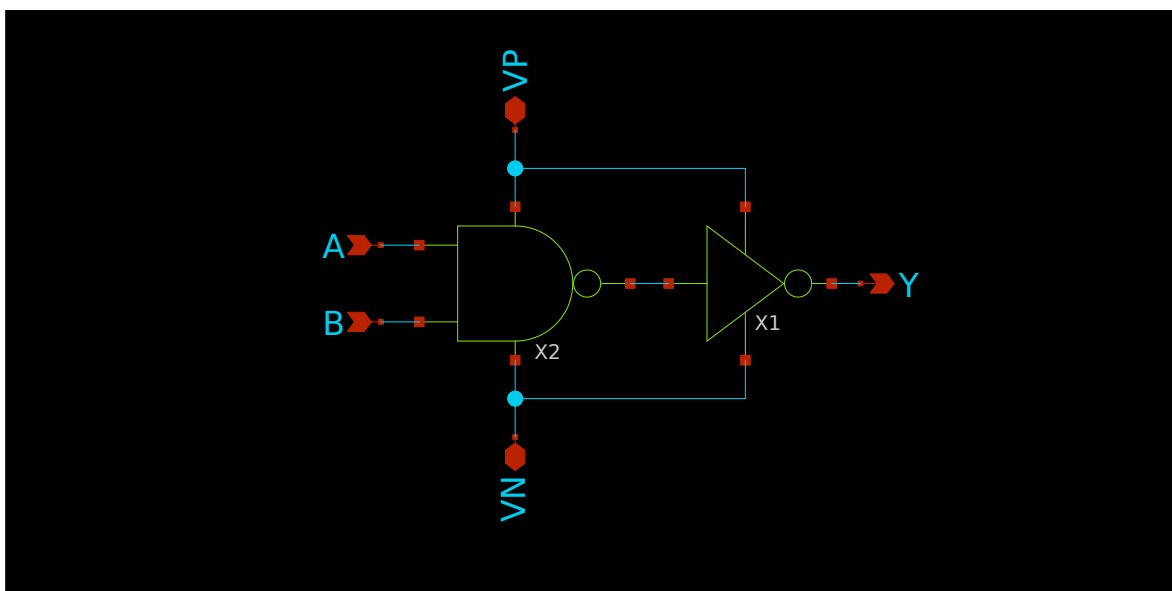
1.3 AND

Figure 3: AND logic is obtained by inverting the output of a NAND gate.

1.4 AND Test Harness

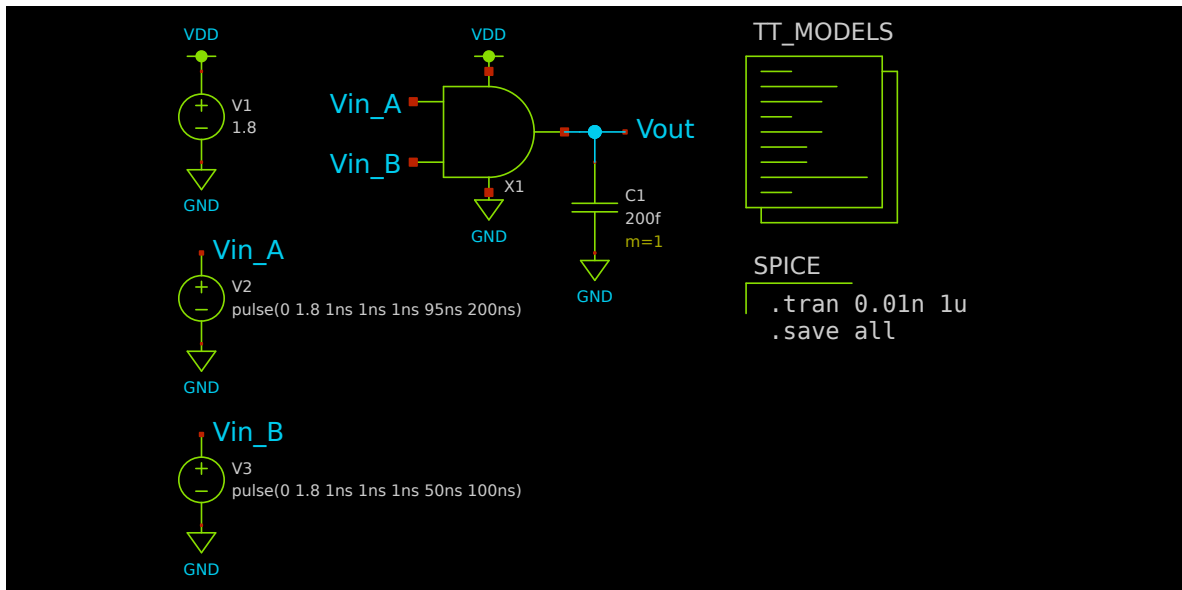Figure 4: Test harness of the AND gate. Voltage pulses are setup to test all possible inputs for A and B.

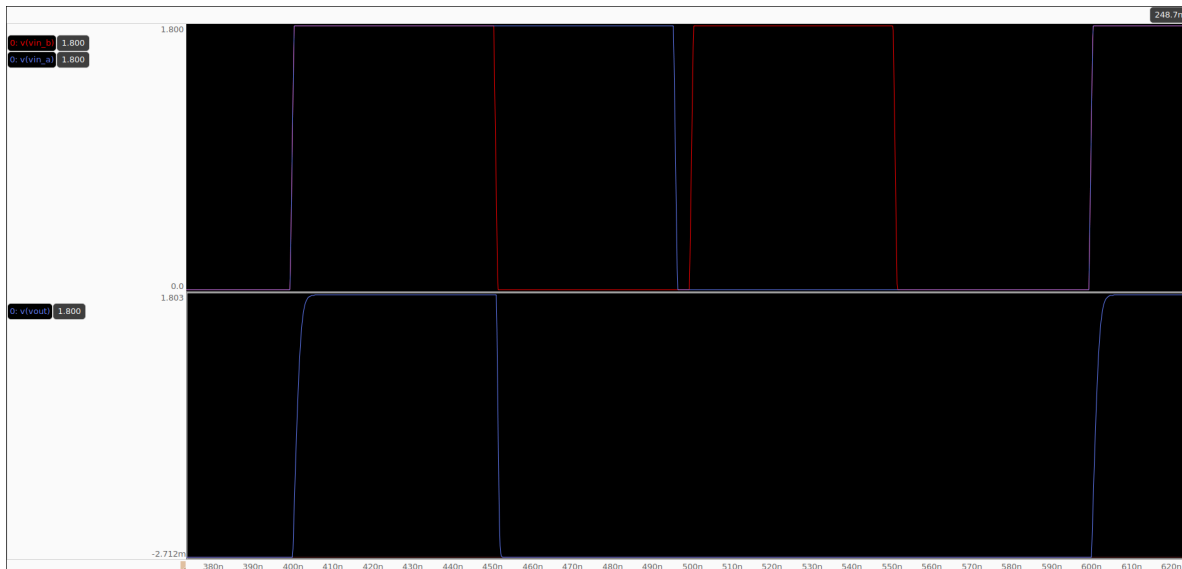# 2 Transient Plots

2.1 AND Transient

Figure 5: The top pain shows the inputs of the AND gate A (blue) and B (red). All permutations of the inputs are tested (00, 01, 10, 11). The bottom pain shows the output of the AND gate Y (blue). The output is high when A and B are high and low at all other times.

3 Layouts

3.1 AND Layout
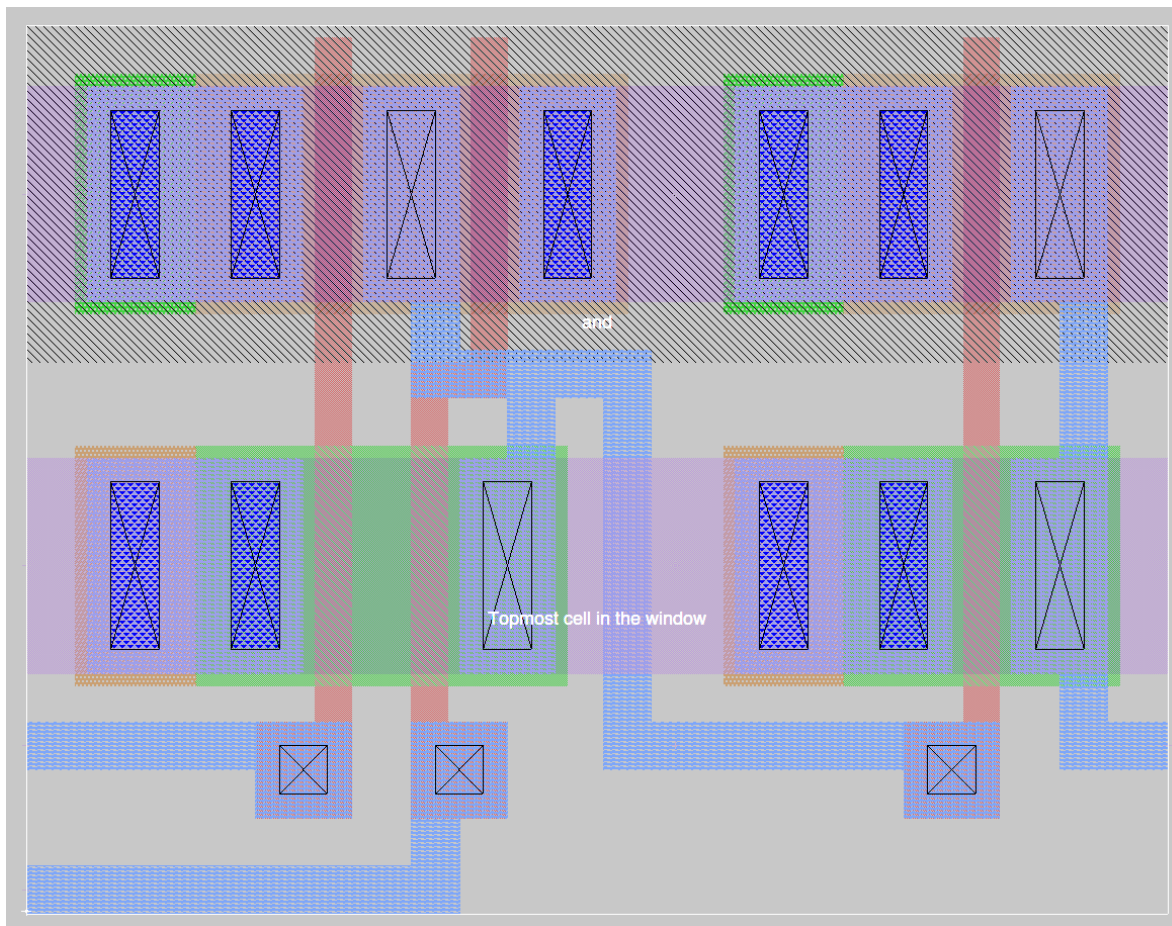
Figure 6: NAND gate (left) is abutted to an inverter (right) to create a AND gate.

4 Layout Vs Schematic

4.1 LVS Comparison Output

Listing 1: Command output

```
Circuit 1 cell sky130_fd_pr__pfet_01v8 and Circuit 2 cell
    sky130_fd_pr__pfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__pfet_01v8 and sky130_fd_pr__pfet_01v8 are
    equivalent.

Circuit 1 cell sky130_fd_pr__nfet_01v8 and Circuit 2 cell
    sky130_fd_pr__nfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__nfet_01v8 and sky130_fd_pr__nfet_01v8 are
    equivalent.

Subcircuit summary:
```

```
Circuit 1: inverter                      |Circuit 2: inverter
-----------------------------------------|----------------------------------------|--------

sky130_fd_pr__pfet_01v8 (1)              |sky130_fd_pr__pfet_01v8 (1)
sky130_fd_pr__nfet_01v8 (1)              |sky130_fd_pr__nfet_01v8 (1)
Number of devices: 2                     |Number of devices: 2
Number of nets: 4                        |Number of nets: 4
-----------------------------------------|----------------------------------------|--------

Netlists match uniquely.

Subcircuit pins:
Circuit 1: inverter                      |Circuit 2: inverter
-----------------------------------------|----------------------------------------|--------

Y                                        |Y
A                                        |A
VP                                       |VP
VN                                       |VN
-----------------------------------------|----------------------------------------|--------

Cell pin lists are equivalent.
Device classes inverter and inverter are equivalent.

Subcircuit summary:
Circuit 1: nand                          |Circuit 2: nand
-----------------------------------------|----------------------------------------|--------

sky130_fd_pr__pfet_01v8 (2)              |sky130_fd_pr__pfet_01v8 (2)
sky130_fd_pr__nfet_01v8 (2)              |sky130_fd_pr__nfet_01v8 (2)
Number of devices: 4                     |Number of devices: 4
Number of nets: 6                        |Number of nets: 6
-----------------------------------------|----------------------------------------|--------

Netlists match uniquely.

Subcircuit pins:
Circuit 1: nand                          |Circuit 2: nand
-----------------------------------------|----------------------------------------|--------

VP                                       |VP
B                                        |B
A                                        |A
VN                                       |VN
Y                                        |Y
-----------------------------------------|----------------------------------------|--------

Cell pin lists are equivalent.
Device classes nand and nand are equivalent.

Subcircuit summary:
Circuit 1: and.spice                     |Circuit 2: and_xschem.spice
-----------------------------------------|----------------------------------------|--------

inverter (1)                             |inverter (1)
nand (1)                                 |nand (1)
Number of devices: 2                     |Number of devices: 2
Number of nets: 6                        |Number of nets: 6
-----------------------------------------|----------------------------------------|--------

Netlists match uniquely.
Cells have no pins;  pin matching not needed.
```

```
63  Device classes and.spice and and_xschem.spice are equivalent.
64
65  Final result: Circuits match uniquely.
66  .
```