Miniproject 2

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https://github.com/MarcEftimie/VLSI.git

1 Schematics

1.1 CRSL D Flip Flop

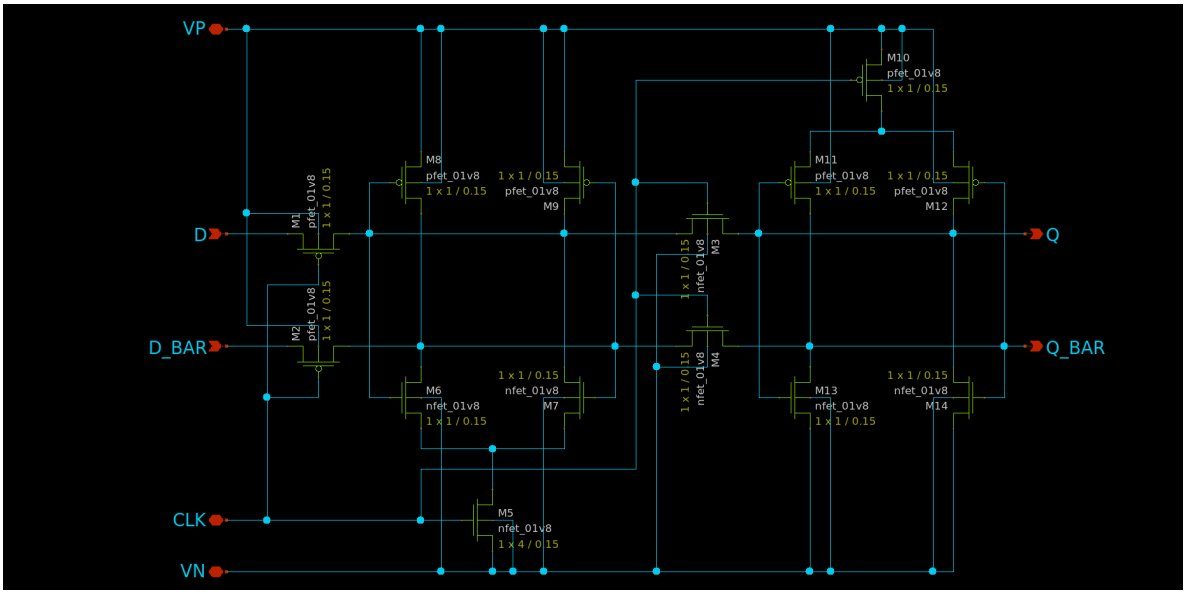

Figure 1: A 14 transistor complementary set-reset logic D flip flop.

1.2 4 Bit Shift Register

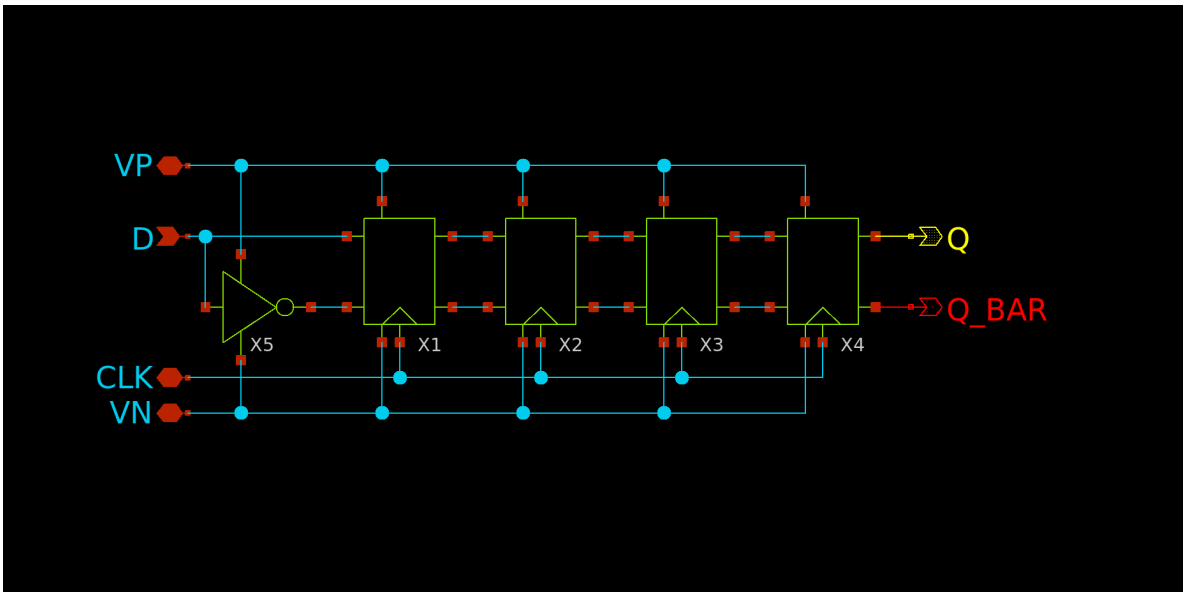

Figure 2: A 4 bit shift register comprised of 4 CRSL D flip flops connected in a chain like structure. The input D is delayed by 4 clock cycles by the time it reaches Q. An inverted input D-BAR is provided by an inverter inverting the D input.

1.3 4 Bit Shift Register Test Harness

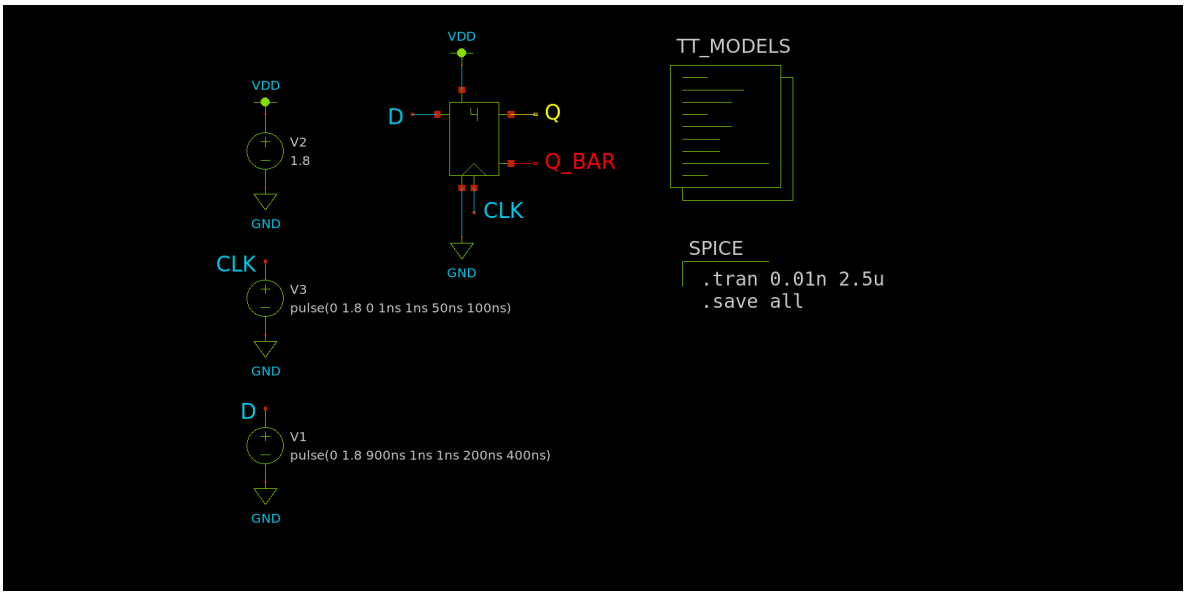

Figure 3: Test harness of the 4 bit shift register. A 10 MHz clock signal is generated using a voltage pulse. The input D is held low for 900 ns to give the shift register time to empty out the initial unknown state of the shift register. After the 900 ns period, D changes from high to low with a period of 200 ns.

2 Transient Plots

2.1 4 Bit Shift Register Transient

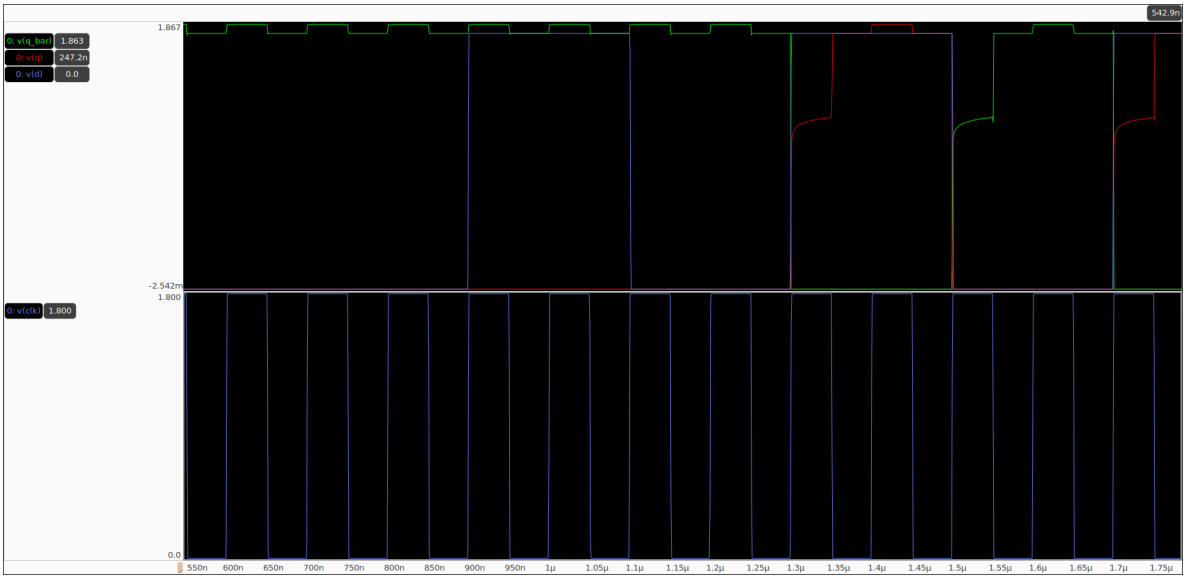

Figure 4: The top pain shows the input signal D, the output signal Q, and the inverted output signal Q-BAR. The simulation starts by holding the input low for 900 ns to clear the initial unknown state of the register. During this period we see that Q is low along with Q-BAR being high which is expected. Once D goes high, Q goes high 4 clock cycles later which is expected in a 4 bit shift register. When D goes low, again, it takes 4 clock cycles for the output to go low.

3 Layouts

3.1 CRSL D Flip Flop Layout

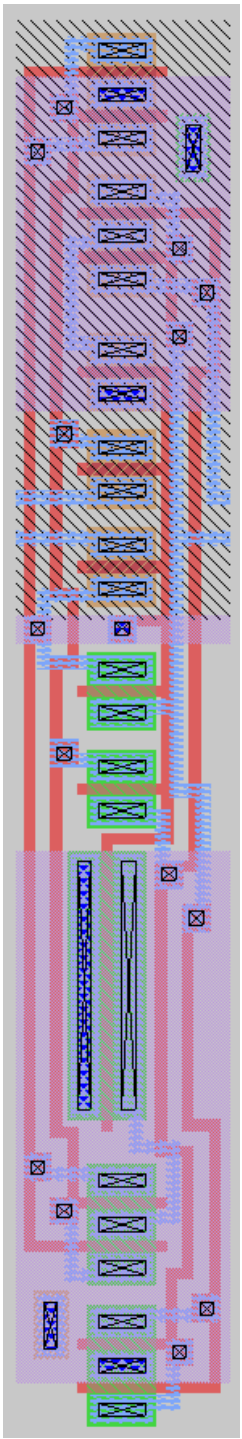

Figure 5: CRSL D Flip Flop layout with a width of 3.15 microns and a height of 20.9 microns

3.2 4 Bit Shift Register Layout

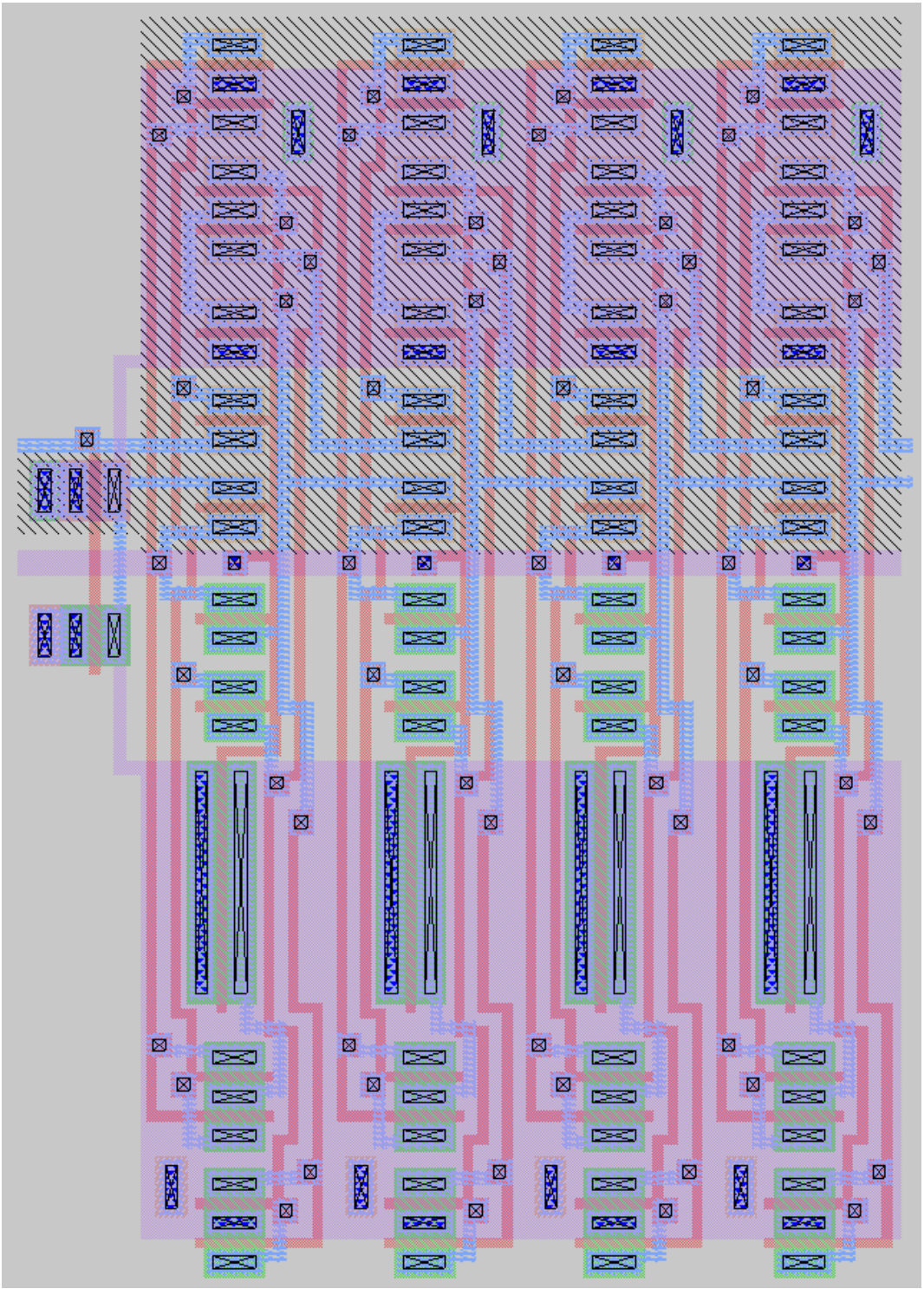

Figure 6: 4 Bit Shift Register composed of abutted CRSL D Flip Flops with a width of 14.7 microns and a height of 20.9 microns. The flip flops share common power and clock lines as well as feed inputs and outputs into each other without extra wiring in the top level layout. An inverter is attachted to the front of the shift register to provide the D-BAR signal.

4 Layout Vs Schematic

4.1 LVS Comparison Output

Listing 1: Command output

```
Circuit 1 cell sky130_fd_pr__pfet_01v8 and Circuit 2 cell
    sky130_fd_pr__pfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__pfet_01v8 and sky130_fd_pr__pfet_01v8 are
    equivalent.

Circuit 1 cell sky130_fd_pr__nfet_01v8 and Circuit 2 cell
    sky130_fd_pr__nfet_01v8 are black boxes.
Equate elements:  no current cell.
Device classes sky130_fd_pr__nfet_01v8 and sky130_fd_pr__nfet_01v8 are
    equivalent.

Subcircuit summary:
Circuit 1: crsl_d_flip_flop                |Circuit 2: crsl_d_flip_flop
-------------------------------------------|-------------------------------------------

sky130_fd_pr__pfet_01v8 (7)                |sky130_fd_pr__pfet_01v8 (7)
sky130_fd_pr__nfet_01v8 (7)                |sky130_fd_pr__nfet_01v8 (7)
Number of devices: 14                      |Number of devices: 14
Number of nets: 11                         |Number of nets: 11
-------------------------------------------------------------------------------------

Resolving symmetries by property value.
Resolving symmetries by pin name.
Netlists match uniquely.

Subcircuit pins:
Circuit 1: crsl_d_flip_flop                |Circuit 2: crsl_d_flip_flop
-------------------------------------------|-------------------------------------------

D                                          |D
D_BAR                                      |D_BAR
Q                                          |Q
Q_BAR                                      |Q_BAR
CLK                                        |CLK
VP                                         |VP
VN                                         |VN
-------------------------------------------------------------------------------------

Cell pin lists are equivalent.
Device classes crsl_d_flip_flop and crsl_d_flip_flop are equivalent.

Subcircuit summary:
Circuit 1: inverter                        |Circuit 2: inverter
-------------------------------------------|-------------------------------------------

sky130_fd_pr__nfet_01v8 (1)                |sky130_fd_pr__nfet_01v8 (1)
sky130_fd_pr__pfet_01v8 (1)                |sky130_fd_pr__pfet_01v8 (1)
Number of devices: 2                       |Number of devices: 2
Number of nets: 4                          |Number of nets: 4
-------------------------------------------------------------------------------------

Netlists match uniquely.

Subcircuit pins:
Circuit 1: inverter                        |Circuit 2: inverter
```

```
-----------------------------------------|-------------------------------------|--------

Y                                        |Y
A                                        |A
VP                                       |VP
VN                                       |VN
-------------------------------------------------------------------------------------

Cell pin lists are equivalent.
Device classes inverter and inverter are equivalent.

Subcircuit summary:
Circuit 1: 4_bit_shift_register.spice    |Circuit 2: 4
    _bit_shift_register_xschem.spi
-----------------------------------------|-------------------------------------

crsl_d_flip_flop (4)                     |crsl_d_flip_flop (4)
inverter (1)                             |inverter (1)
Number of devices: 5                     |Number of devices: 5
Number of nets: 13                       |Number of nets: 13
-------------------------------------------------------------------------------------

Netlists match uniquely.
Cells have no pins;  pin matching not needed.
Device classes 4_bit_shift_register.spice and 4_bit_shift_register_xschem.
    spice are equivalent.

Final result: Circuits match uniquely.
```