Miniproject 3

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October 16, 2023

1 Github

https://github.com/MarcEftimie/VLSI.git

2 Circuit Analysis

2.1

V_1 is the non inverting input to the circuit while V_2 is the inverting input. If V_1 increases then V_{gs} of $M1$ will increase therefore increasing I_1. Since $I_1 + I_2 = I_B$, I_2 will have to decrease to balance the increase in I_1. The current going through the left side of the folded cascode configuration ($M5$ and $M9$) is equal to $I_b - I_1$ by KCL. The current going through the right side of the folded cascode configuration ($M6$ and $M10$) is equal to $I_b - I_2$ by KCL. $I_b - I_1$ is mirrored from $M9$ to $M10$. Therefore, $M6$ is pushing current into the node at V_{out} while $M10$ is pulling current out of the node at V_{out}. This pushing and pulling is equal to $I_{out} = (I_b - I_2) - (I_b - I_1)$. If $I_1 > I_2$ when V_1 increases while V_2 remains constant, then the current I_{out} will become positive. The voltage at this node will therefore increase due to the parasitic capacitance at this node $I_{out} = \frac{dv}{dt}C$. Since the voltage at this node increases when V_1 increases, V_1 is the non inverting terminal. When V_2 increases, the voltage at this node drops, making it the inverting terminal.

2.2

In order for the differential pair to function properly, the bias transistor Mb must remain in saturation. Using a model for a simple source follower, the relationship between V_{out} and V_{in} is $V_{out} = k(V_{in} - V_b)$ where V_{out} is the drain of Mb, V_b is the gate of Mb, and V_{in} is our input. Since Mb must remain in saturation and its drain is equal to V_{out}, $V_{out} \geq V_{DSSAT}$. Replacing V_{out} with the equation above gives us that $V_{in} \geq V_b + \frac{V_{DSSAT}}{k}$.

2.3

$I_{out} = I_1 - I_2$

2.4

In the worst case where $M1$ is pulling I_b and $M2$ is pulling zero current, in order to satisfy the I_b that needs to go through Mb, $M3$ needs to at least supply I_b. The same is true for $M4$ in the reverse case where $M2$ is pulling I_b and $M1$ is pulling zero current. Both $M1$ and $M2$ need to therefore supply at least Ib. Any extra current will run through the folded cascode configuration and will be dissipated as waste energy.

2.5

See bias generator in schematics section.

3 Schematics

3.1 Bias Voltage Generator

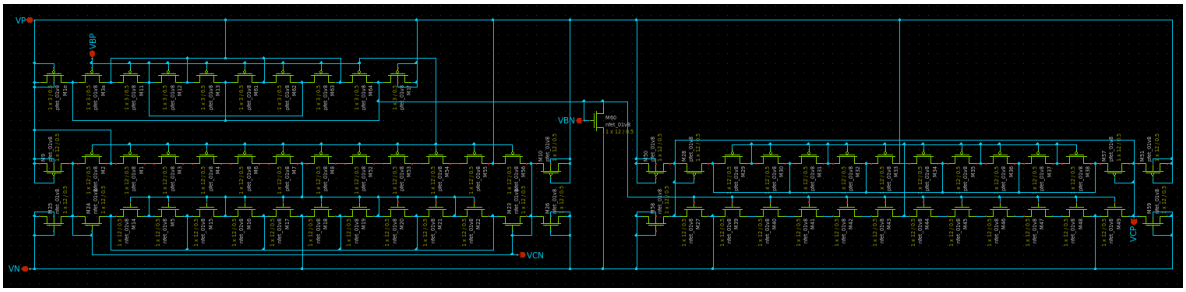


Figure 1: Layout driven schematic of bias voltage generator that generates gate voltages for cascode MOSFETS in the folded cascode differential amplifier circuit. Also produces bias gate voltages for bias current MOSFETS in the folded cascode differential amplifier circuit. Takes VBP as an input to drive current mirrors.

3.2 Folded Cascode Differential Amplifier

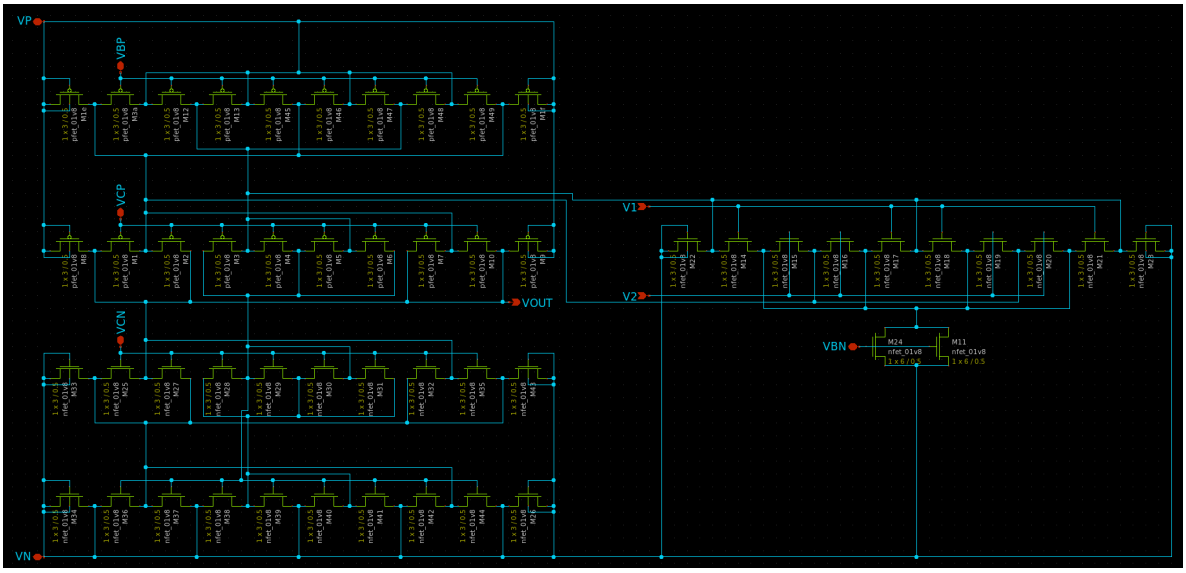


Figure 2: Layout driven schematic of a differential pair with an folded cascode MOSFET configuration to help improve performance of the circuit. Takes four bias voltages, VCP and VCN for cascode MOSFETS and VBP and VBN for bias current MOSFETS.

3.3 Differential Amplifier

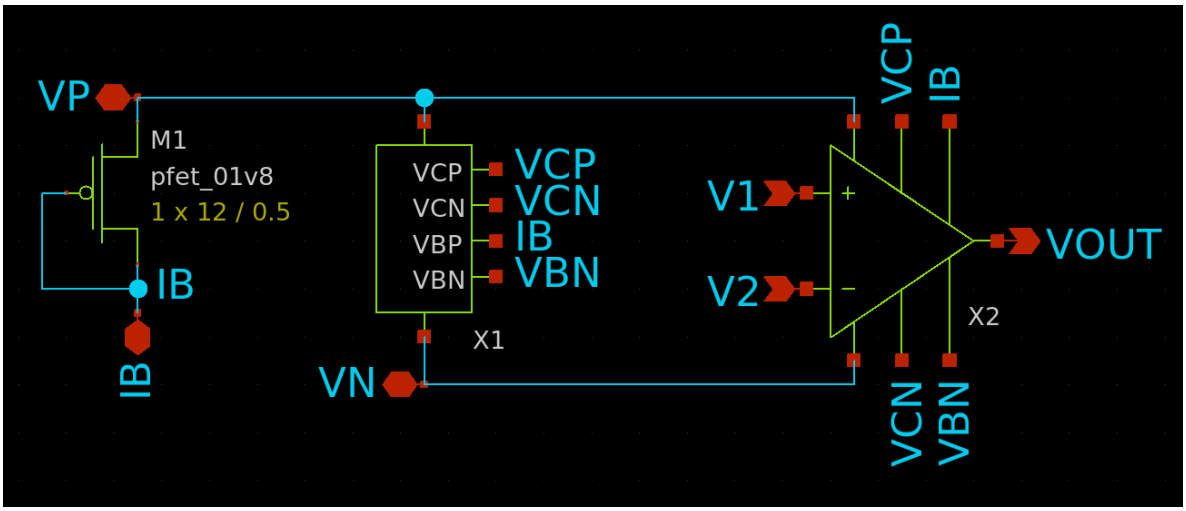


Figure 3: Complete circuit of differential amplifier with a diode connected transistor to produce VBP from an input current IB

4 Simulations

4.1 Voltage Transfer Characteristics

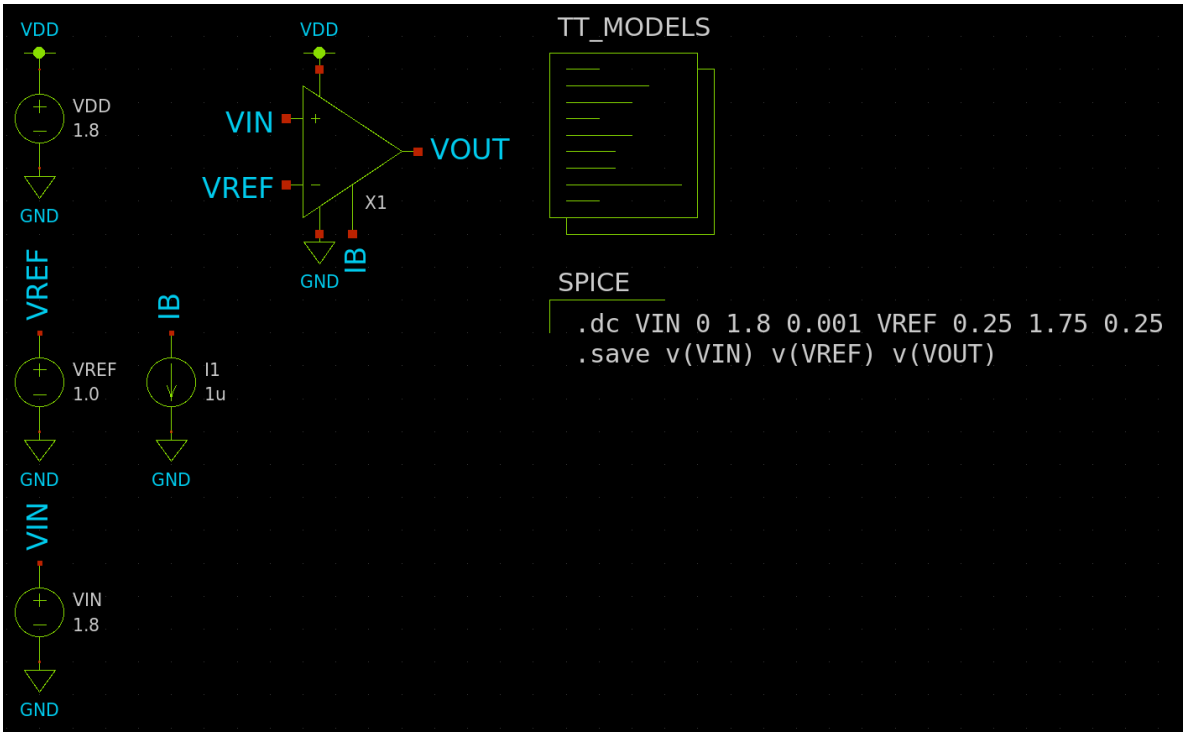


Figure 4: VTC test harness

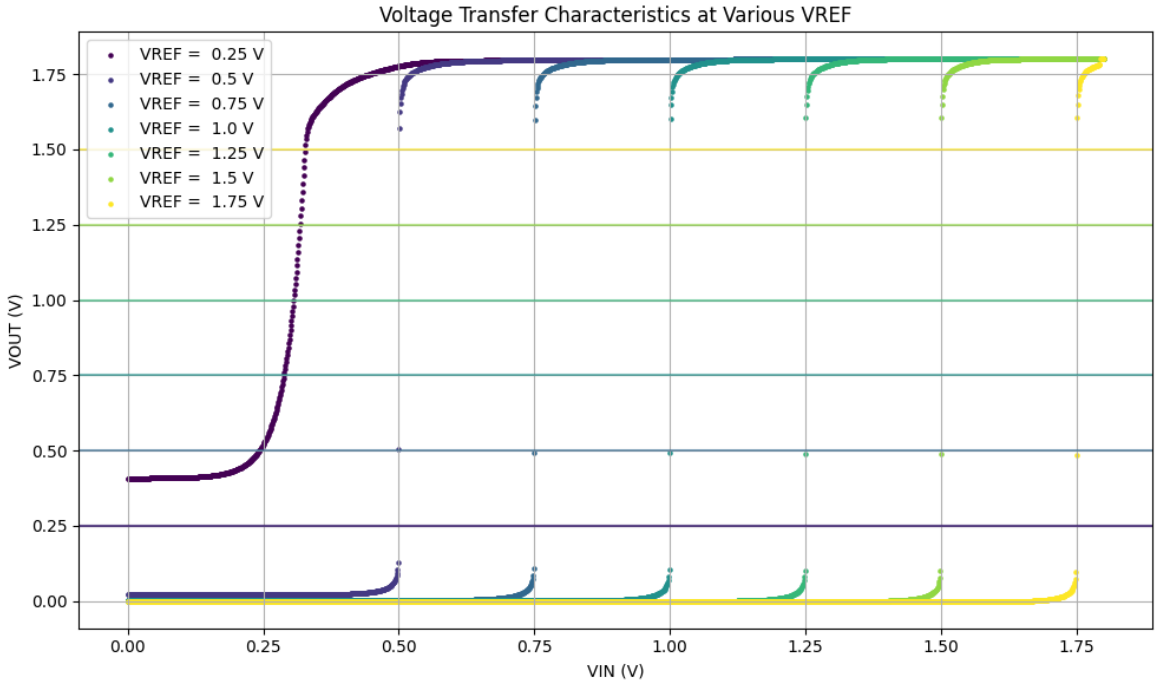


Figure 5: VTC of the differential amplifier at seven different values of $VREF$. The DC gain of the circuit at the steep part of each slope is around 1100.

4.2 Voltage-to-Current Transfer Characteristics

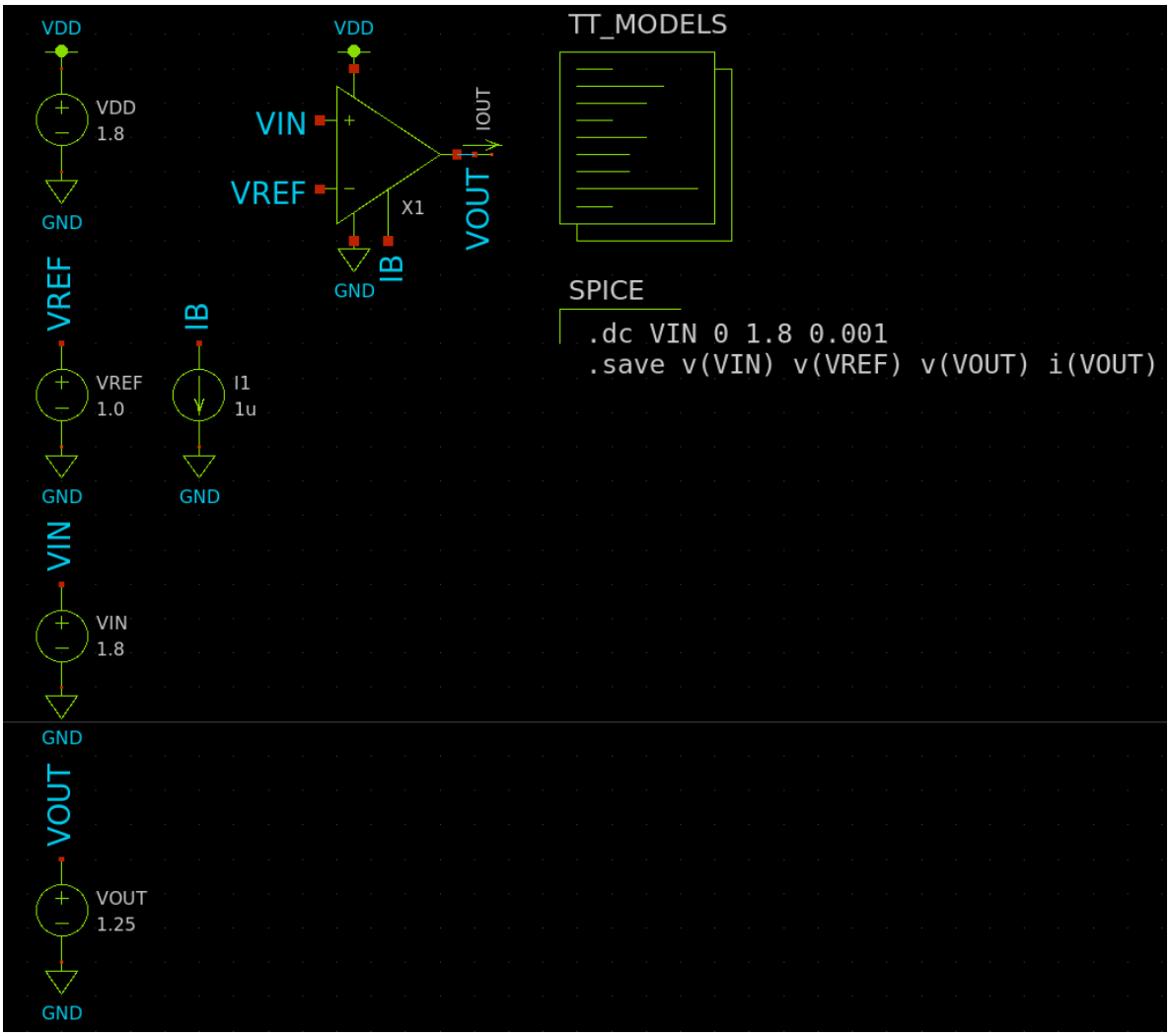


Figure 6: Voltage-to-Current test harness schematic

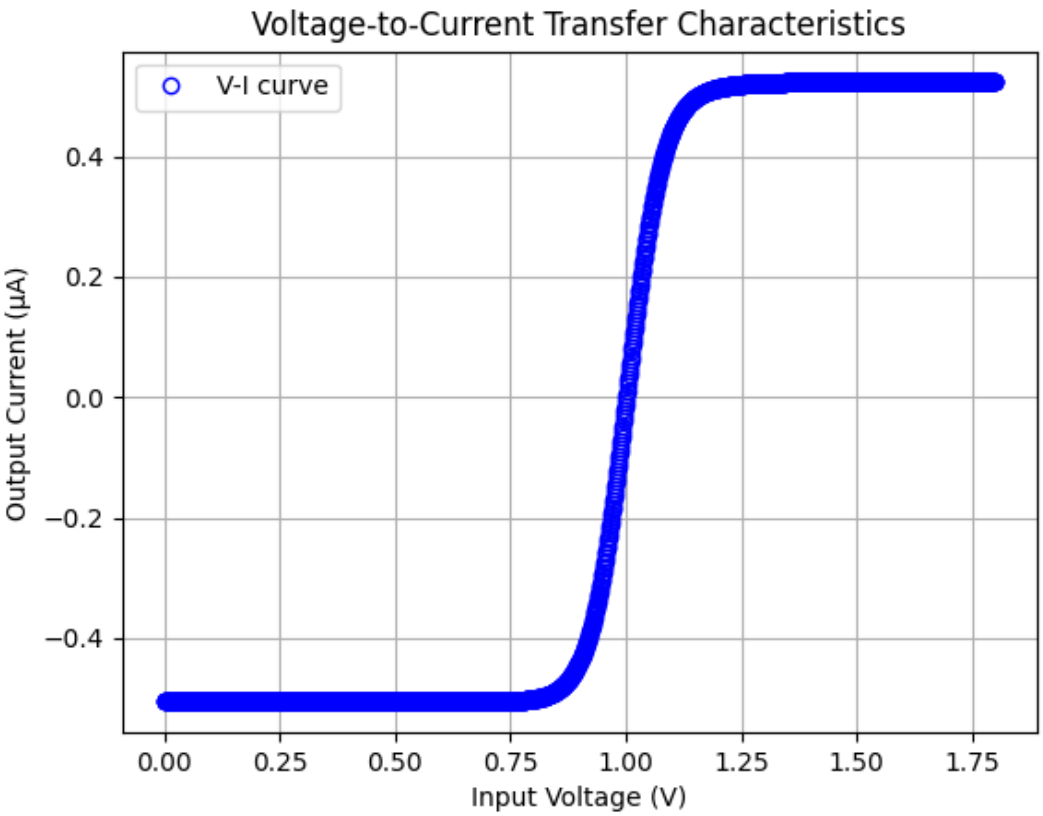


Figure 7: Voltage-to-Current characteristics of the differential amplifier at $V_{ref} = 1V$. The incremental transconductance gain of the circuit at the steep part of the slope is $6.49 \cdot 10^{-6}$ Siemens. The limiting values of the output current are $-0.51\mu A$ and $0.51\mu A$

4.3 Loopgain

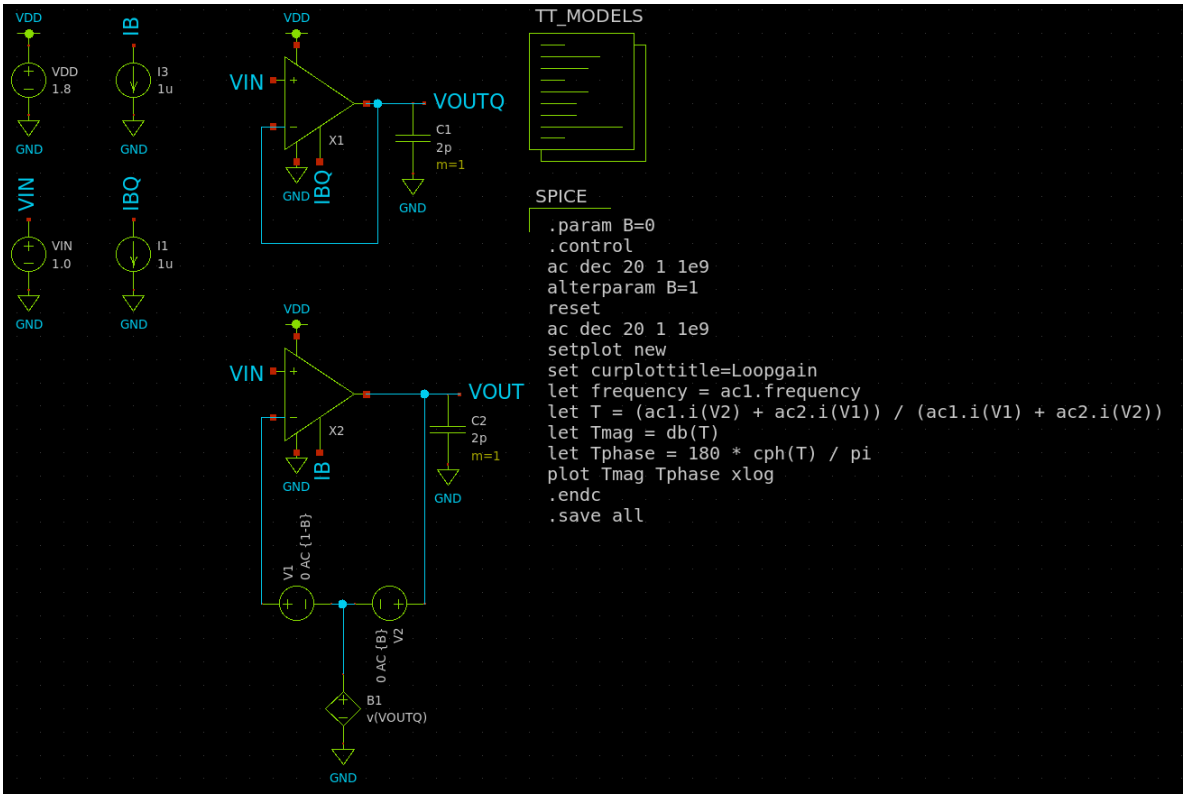


Figure 8: Loopgain test harness schematic

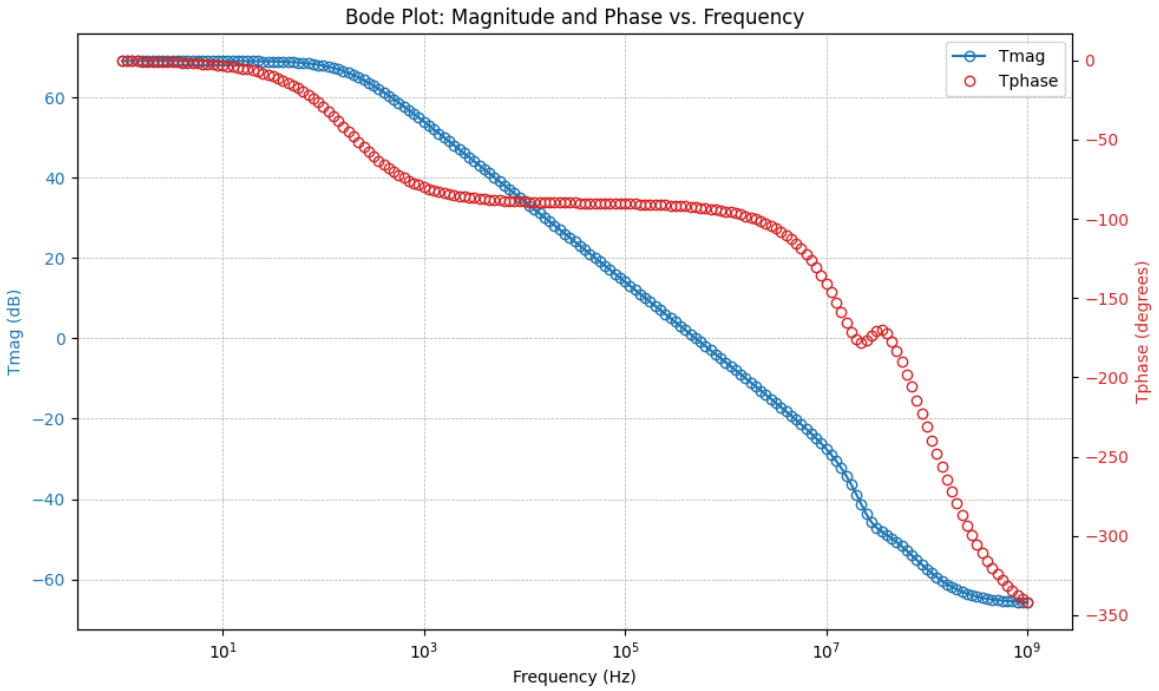


Figure 9: Loopgain characteristics of the differential amplifier. The low-frequency gain is $69dB$ (2818 dc gain) which is more than two times as great than the 1100 dc gain gathered earlier. The unity-gain crossover frequency is 523 KHz. The expected unity-gain crossover frequency with this test harness setup is equal to $\frac{g_m}{2\pi C}$. With a g_m of $6.49 \cdot 10^{-6}$ Siemens and a C of $2pF$ we should expect a unity-gain crossover frequency of $5.16 \cdot 10^5$

which is close to the measured value.

4.4 Unity-Gain Follower Frequency Response

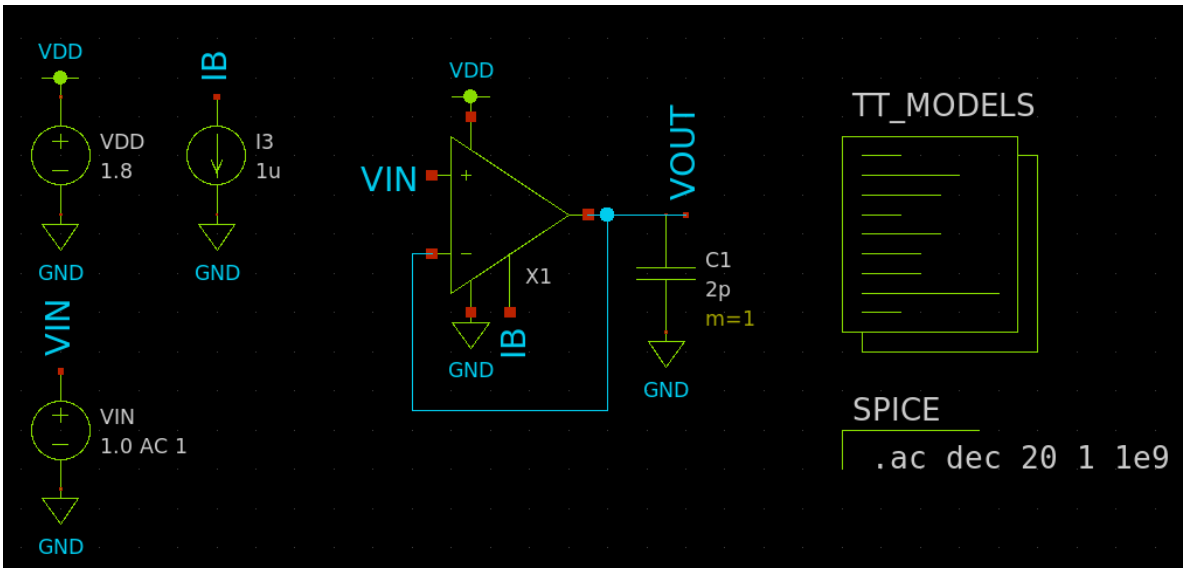


Figure 10: Unity-Gain Follower test harness schematic

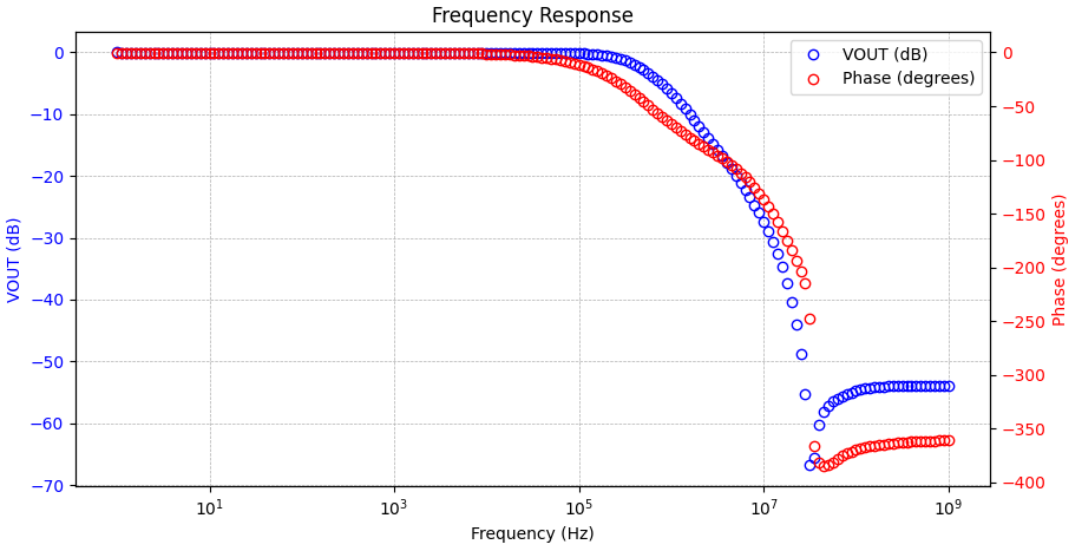


Figure 11: Unity-Gain Follower Frequency Response of the differential amplifier. The corner frequency is around the measured unity-gain crossover frequency at 524 kHz.

5 Layouts

5.1 Bias Voltage Generator

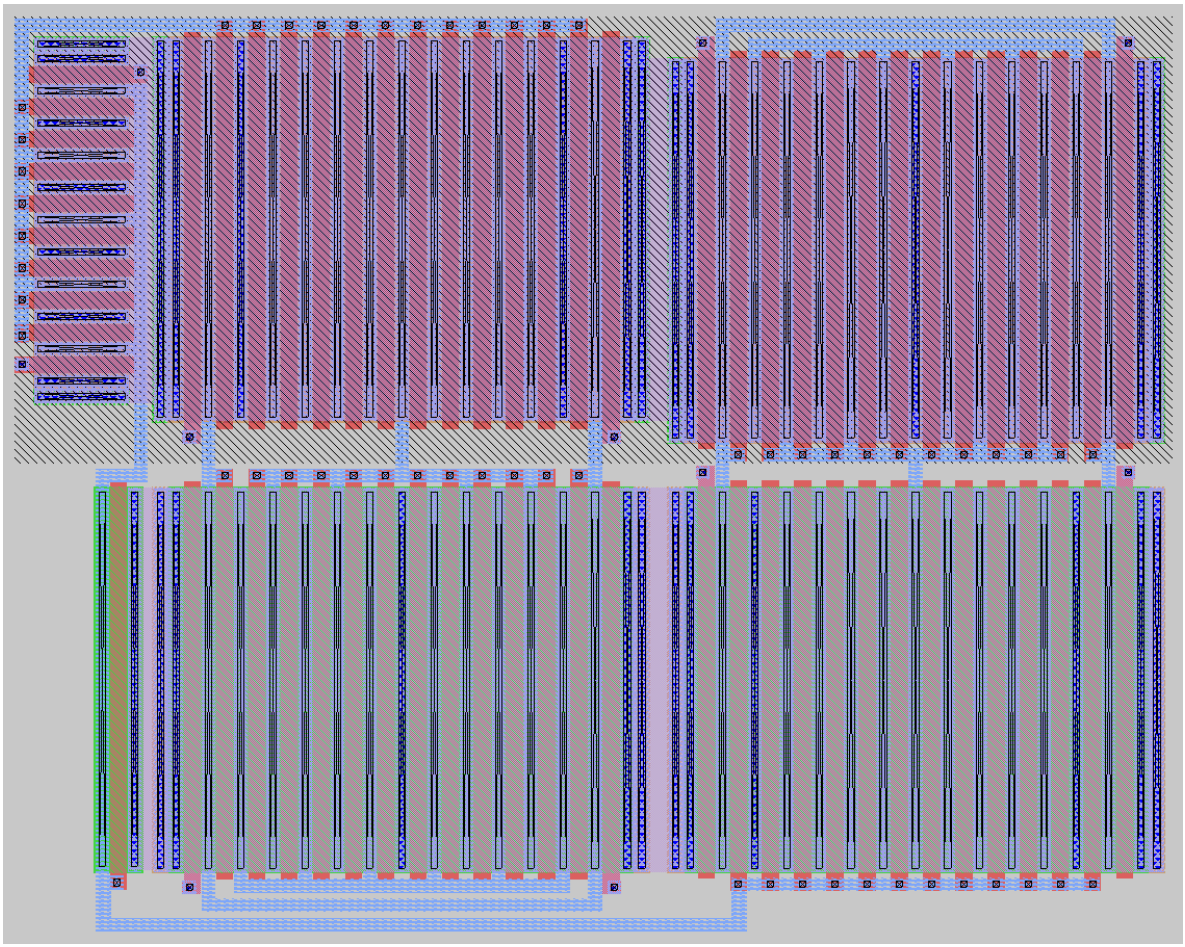


Figure 12: Layout driven schematic of bias voltage generator that generates gate voltages for cascode MOSFETS in the folded cascode differential amplifier circuit. Also produces bias gate voltages for bias current MOSFETS in the folded cascode differential amplifier circuit. Takes VBP as an input to drive current mirrors.

5.2 Folded Cascode Differential Amplifier

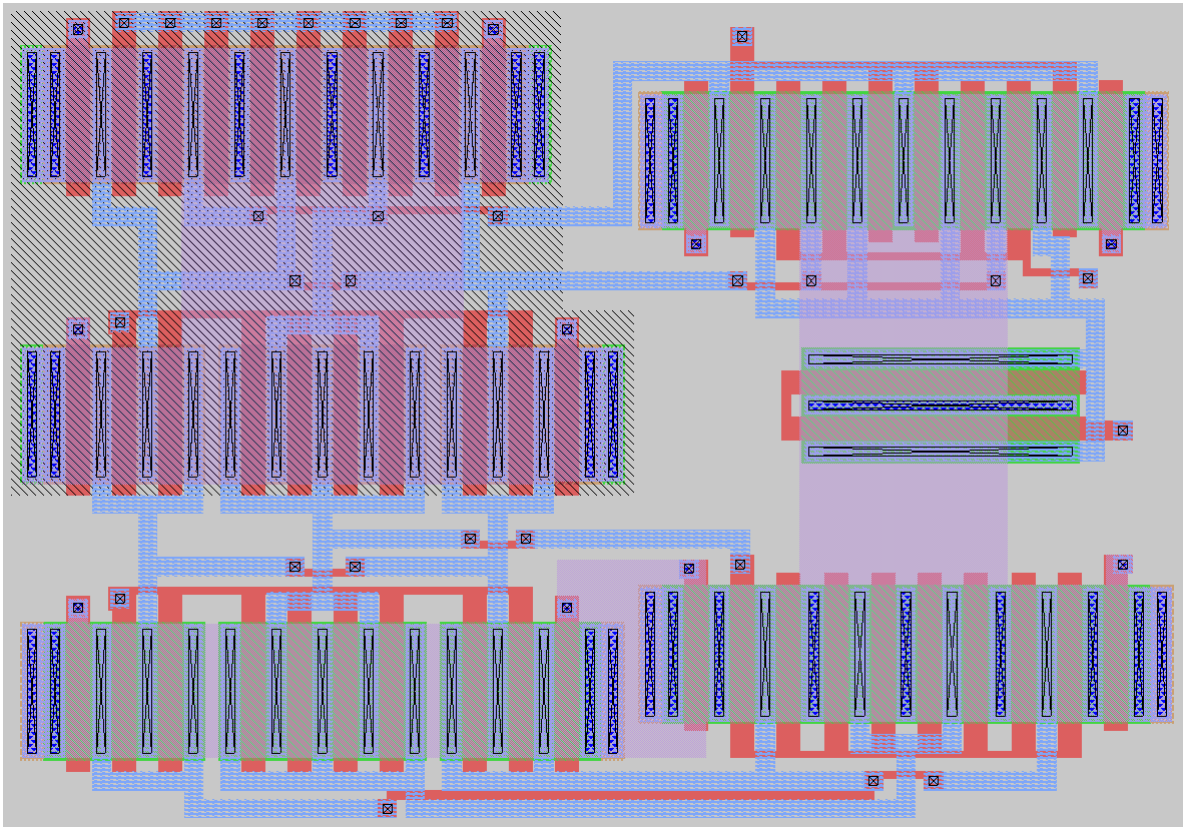
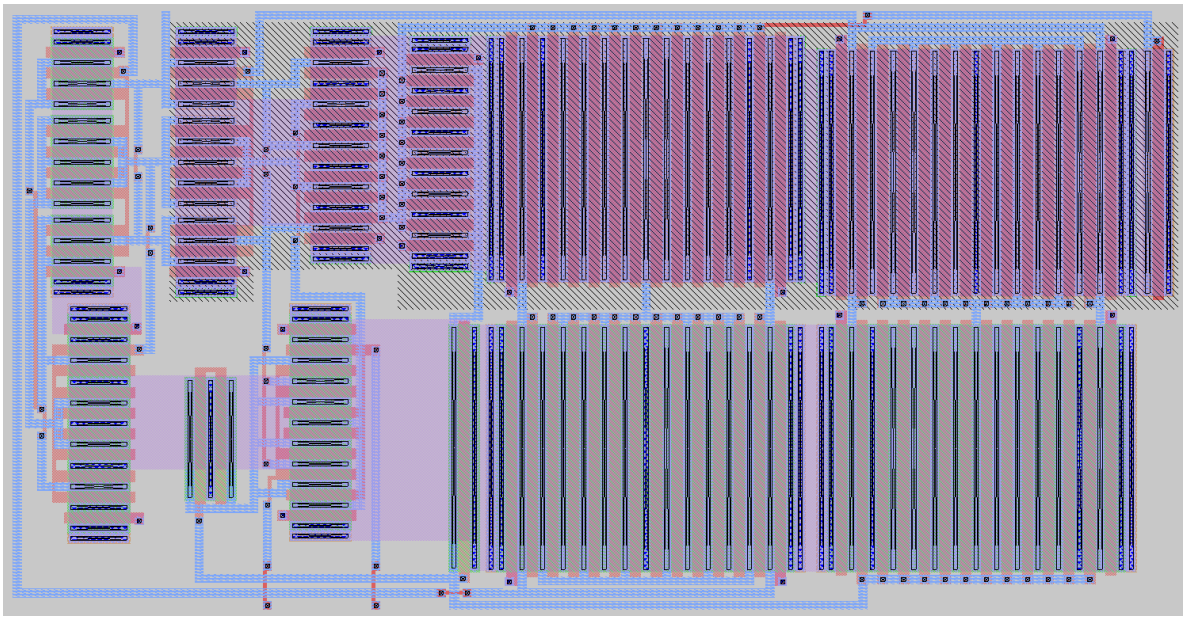


Figure 13: Layout driven schematic of a differential pair with an folded cascode MOSFET configuration to help improve performance of the circuit. Takes four bias voltages, VCP and VCN for cascode MOSFETS and VBP and VBN for bias current MOSFETS.

5.3 Differential Amplifier



6 LVS

6.1 LVS Comparison Output

Listing 1: Command output

```
1
2  Circuit 1 cell sky130_fd_pr__pfet_01v8 and Circuit 2 cell
       sky130_fd_pr__pfet_01v8 are black boxes.
3  Equate elements:  no current cell.
4  Device classes sky130_fd_pr__pfet_01v8 and sky130_fd_pr__pfet_01v8 are
       equivalent.
5
6  Circuit 1 cell sky130_fd_pr__nfet_01v8 and Circuit 2 cell
       sky130_fd_pr__nfet_01v8 are black boxes.
7  Equate elements:  no current cell.
8  Device classes sky130_fd_pr__nfet_01v8 and sky130_fd_pr__nfet_01v8 are
       equivalent.
9
10 Class bias_generator (0):  Merged 31 parallel devices.
11 Class bias_generator (1):  Merged 31 parallel devices.
12 Subcircuit summary:
13 Circuit 1: bias_generator                  |Circuit 2: bias_generator
14 -------------------------------------------|-------------------------------------------

15 sky130_fd_pr__pfet_01v8 (38->19)           |sky130_fd_pr__pfet_01v8 (38->19)
16 sky130_fd_pr__nfet_01v8 (29->17)           |sky130_fd_pr__nfet_01v8 (29->17)
17 Number of devices: 36                      |Number of devices: 36
18 Number of nets: 26                         |Number of nets: 26
19 ------------------------------------------------------------------------------------------

20 Resolving symmetries by property value.
21 Resolving symmetries by pin name.
22 Netlists match with 18 symmetries.
23
24 Subcircuit pins:
25 Circuit 1: bias_generator                  |Circuit 2: bias_generator
26 -------------------------------------------|-------------------------------------------

27 VBN                                        |VBN
28 VBP                                        |VBP
29 VN                                         |VN
30 VP                                         |VP
31 VCN                                        |VCN
32 VCP                                        |VCP
33 ------------------------------------------------------------------------------------------

34 Cell pin lists are equivalent.
35 Device classes bias_generator and bias_generator are equivalent.
36
37 Class folded_cascode_differential_amplifier (0):  Merged 36 parallel devices.
38 Class folded_cascode_differential_amplifier (1):  Merged 36 parallel devices.
39 Subcircuit summary:
40 Circuit 1: folded_cascode_differential_amp |Circuit 2:
       folded_cascode_differential_amp
41 -------------------------------------------|-------------------------------------------

42 sky130_fd_pr__pfet_01v8 (20->6)            |sky130_fd_pr__pfet_01v8 (20->6)
43 sky130_fd_pr__nfet_01v8 (32->10)           |sky130_fd_pr__nfet_01v8 (32->10)
44 Number of devices: 16                      |Number of devices: 16
45 Number of nets: 15                         |Number of nets: 15
```

```
---------------------------------------------------------------------------------------

Netlists match uniquely.

Subcircuit pins:
Circuit 1: folded_cascode_differential_amp |Circuit 2:
    folded_cascode_differential_amp
-------------------------------------------|-------------------------------------------

VBN                                        |VBN
V2                                         |V2
V1                                         |V1
VN                                         |VN
VOUT                                       |VOUT
VP                                         |VP
VCP                                        |VCP
VCN                                        |VCN
VBP                                        |VBP
---------------------------------------------------------------------------------------

Cell pin lists are equivalent.
Device classes folded_cascode_differential_amplifier and
    folded_cascode_differential_amplifier are equivalent.

Subcircuit summary:
Circuit 1: differential_amplifier.spice    |Circuit 2:
    top_differential_amplifier.spic
-------------------------------------------|-------------------------------------------

bias_generator (1)                         |bias_generator (1)
folded_cascode_differential_amplifier (1)  |
    folded_cascode_differential_amplifier (1)
sky130_fd_pr__pfet_01v8 (1)                |sky130_fd_pr__pfet_01v8 (1)
Number of devices: 3                       |Number of devices: 3
Number of nets: 9                          |Number of nets: 9
---------------------------------------------------------------------------------------

Netlists match uniquely.
Cells have no pins;  pin matching not needed.
Device classes differential_amplifier.spice and top_differential_amplifier.
    spice are equivalent.

Final result: Circuits match uniquely.
.
```