Lecture 1 - Introduction

ET3233 - Digital Systems Design

Geeth Karunarathne

Module Outline

1. Hardware Description Languages
2. RTL Based System Design
3. RISC Architecture
4. Processor Design
5. Memory Design
6. Design of an ALU
7. Asynchronous Sequential System Design

Digital Logic

1 and 0

Boolean Algebra - Axioms

(A1)	$X = 0$ If $X \neq 1$	(A1')	$X = 1$ If $X \neq 0$
(A2)	If $X = 0$, then $X' = 1$	(A2')	If $X = 1$, then $X' = 0$
(A3)	$0 \cdot 0 = 0$	(A3')	$1 + 1 = 1$
(A4)	$1 \cdot 1 = 1$	(A4')	$0 + 0 = 0$
(A5)	$0 \cdot 1 = 1 \cdot 0 = 0$	(A5')	$1 + 0 = 0 + 1 = 1$

Single Variable Theorems

(T1)	$X + 0 = X$	(T1')	$X \cdot 1 = X$	(Identities)
(T2)	$X + 1 = 1$	(T2')	$X \cdot 0 = 0$	(Null elements)
(T3)	$X + X = X$	(T3')	$X \cdot X = X$	(Idempotency)
(T4)	$(X')' = X$			(Involution)
(T5)	$X + X' = 1$	(T5')	$X \cdot X' = 0$	(Complements)

*All the above theorems involves Boolean rules related to a single variable "X", hence called single variable theorems.

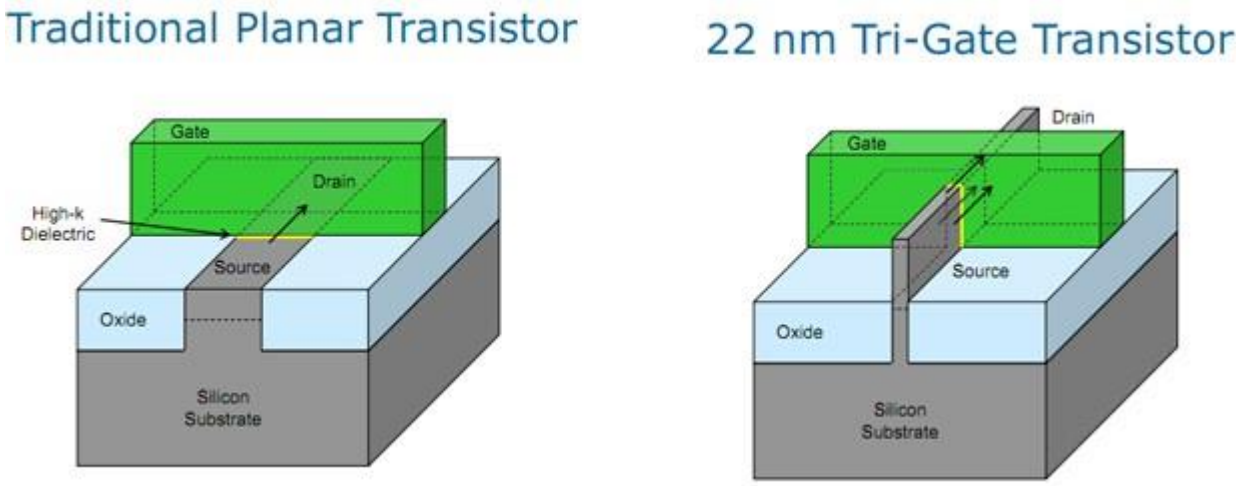
Multiple Variable Theorems

(T6)	$X + Y = Y + X$	(T6′)	$X \cdot Y = Y \cdot X$	(Commutativity)
(T7)	$(X + Y) + Z = X + (Y + Z)$	(T7′)	$(X \cdot Y) \cdot Z = X \cdot (Y \cdot Z)$	(Associativity)
(T8)	$X \cdot Y + X \cdot Z = X \cdot (Y + Z)$	(T8′)	$(X + Y) \cdot (X + Z) = X + Y \cdot Z$	(Distributivity)
(T9)	$X + X \cdot Y = X$	(T9′)	$X \cdot (X + Y) = X$	(Covering)
(T10)	$X \cdot Y + X \cdot Y' = X$	(T10′)	$(X + Y) \cdot (X + Y') = X$	(Combining)
(T11)	$X \cdot Y + X' \cdot Z + Y \cdot Z = X \cdot Y + X' \cdot Z$	(T11′)	$(X + Y) \cdot (X' + Z) \cdot (Y + Z) = (X + Y) \cdot (X' + Z)$	(Consensus)

* Above theorems involves Boolean rules related to two or three variables, hence called multiple variable theorems.

Transistor Fabrication

- Transistor fabrication in silicon chips

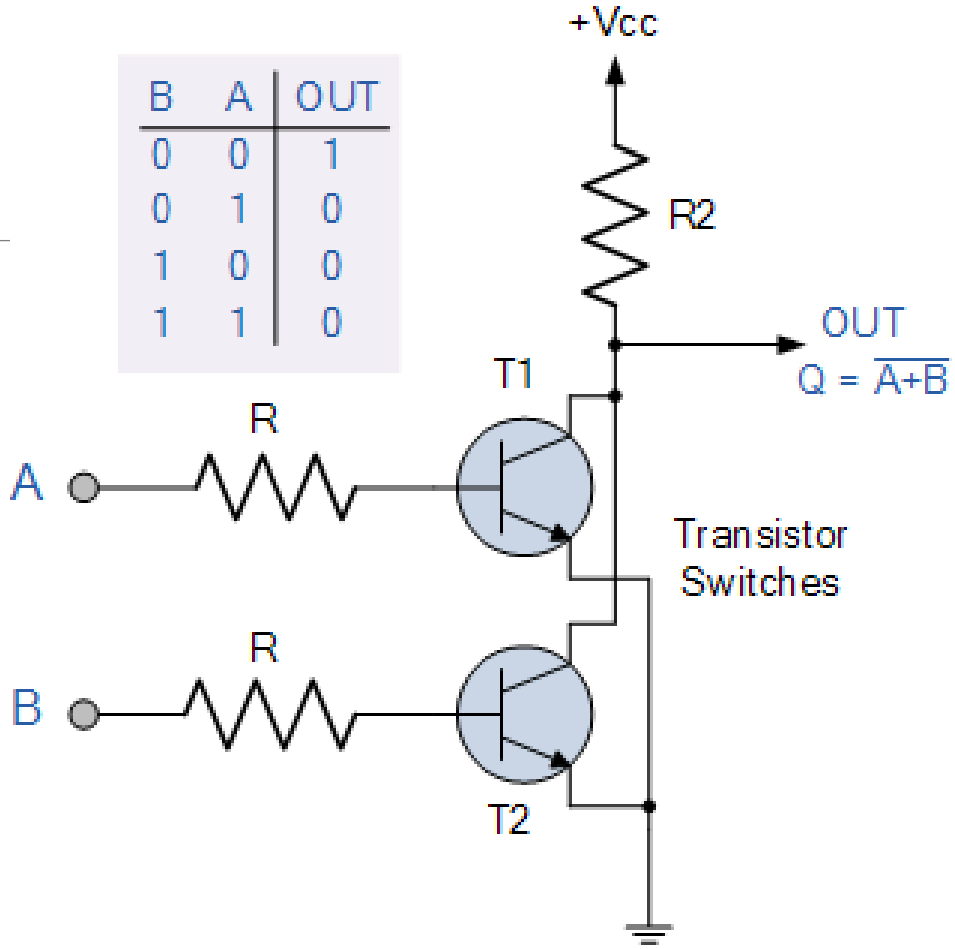



infineon
How are microchips made?
From sand to semiconductors

Transistor as a Switch

B	A	OUT
0	0	1
0	1	0
1	0	0
1	1	0

- NOR gate implementation using transistors.



Logic Circuit Design

Combinational Logic

Output is only a function of the current inputs.

They are stateless.

Sequential Logic

The output of Sequential logic circuits depends on BOTH current inputs and previous inputs.

Sequential Logic circuits have memory due to this property.

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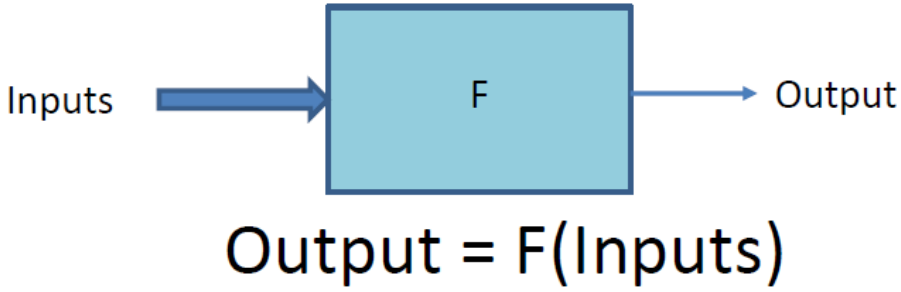
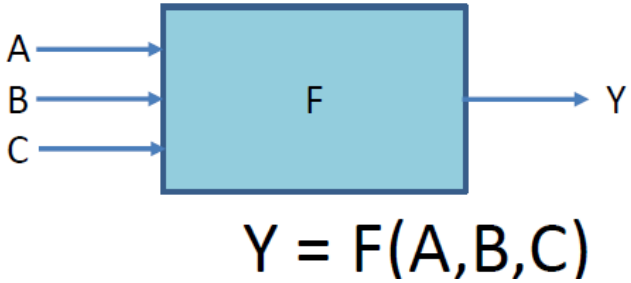
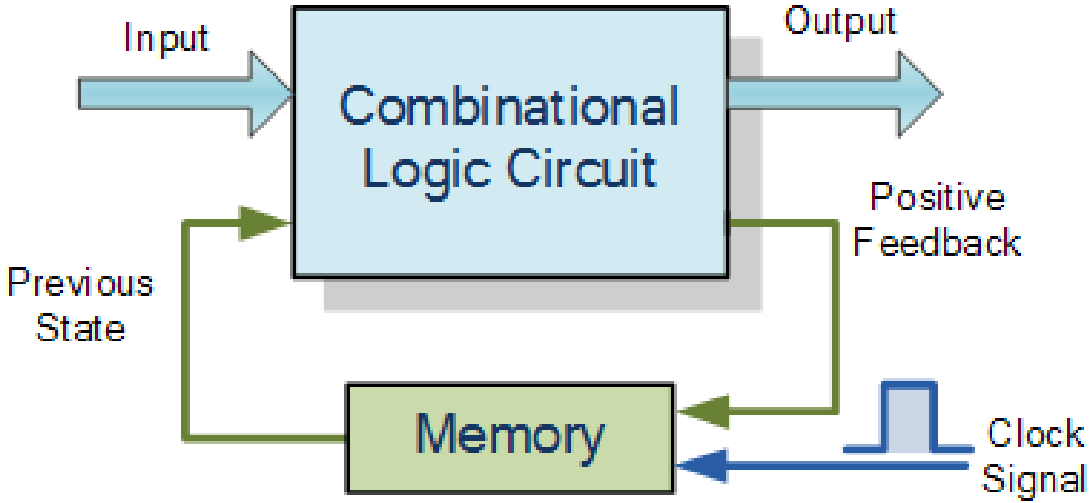




Logic Circuit Design



Sequential Logic

The output of Sequential logic circuits depends on BOTH current inputs and previous inputs.

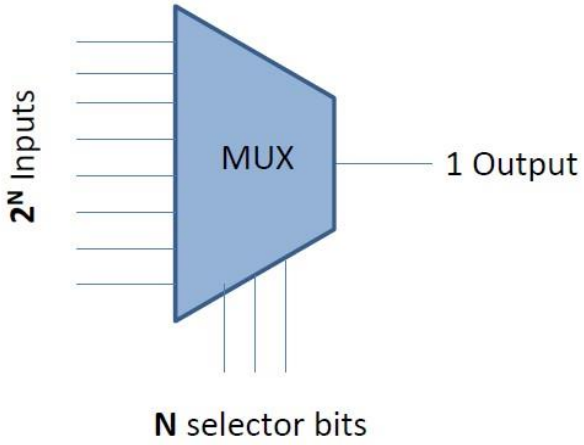
Sequential Logic circuits have memory due to this property.

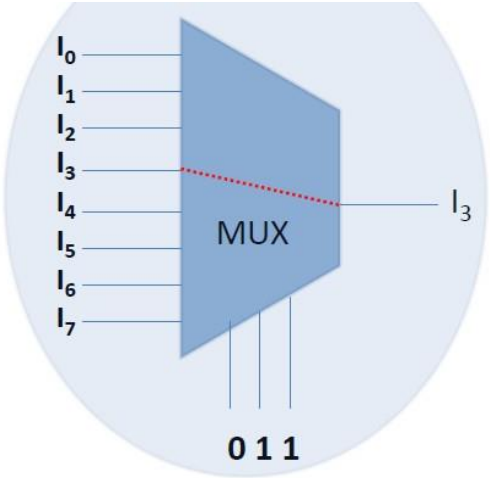
Combinational Logic Examples

- Enabling Circuits
- Encoder
- Decoder
- Multiplexer
- Demultiplexer
- Comparator
- Adder/ Subtractor

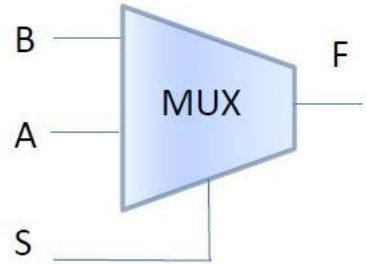
Multiplexer (MUX)

- Combinational circuit that selects binary data from one of many input lines to the output line.
- Multiplexer is also known as Data Selector.





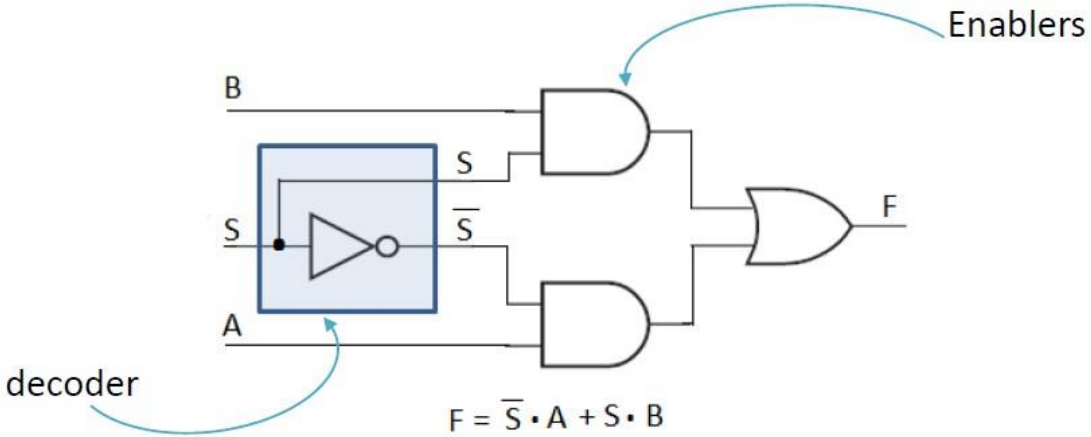
2 to 1 Multiplexer



Truth Table

S	F
0	A
1	B

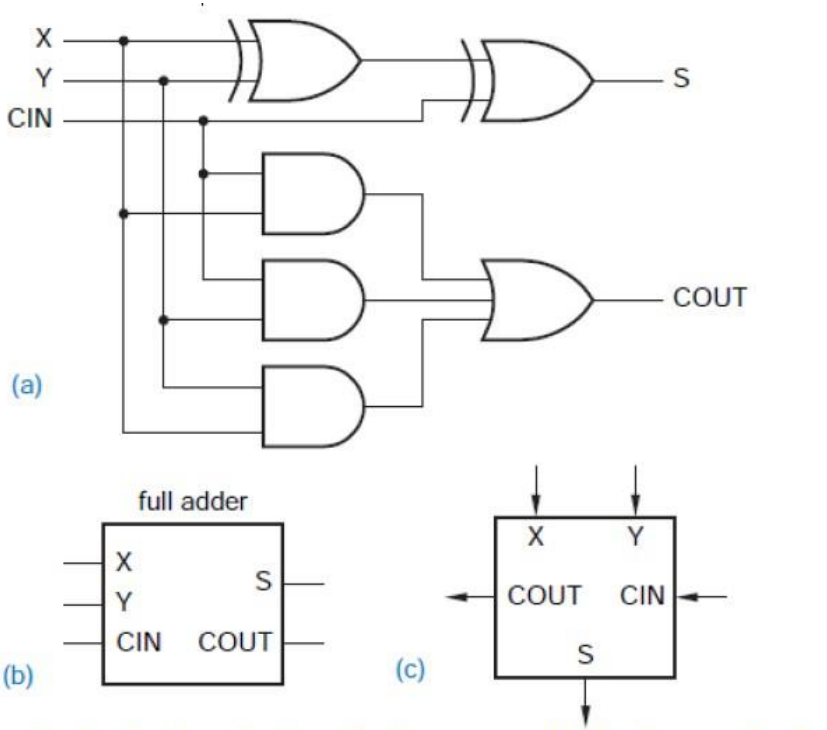
Abbreviated Truth Table
Inputs A,B listed in output column



Full Adder

Truth Table

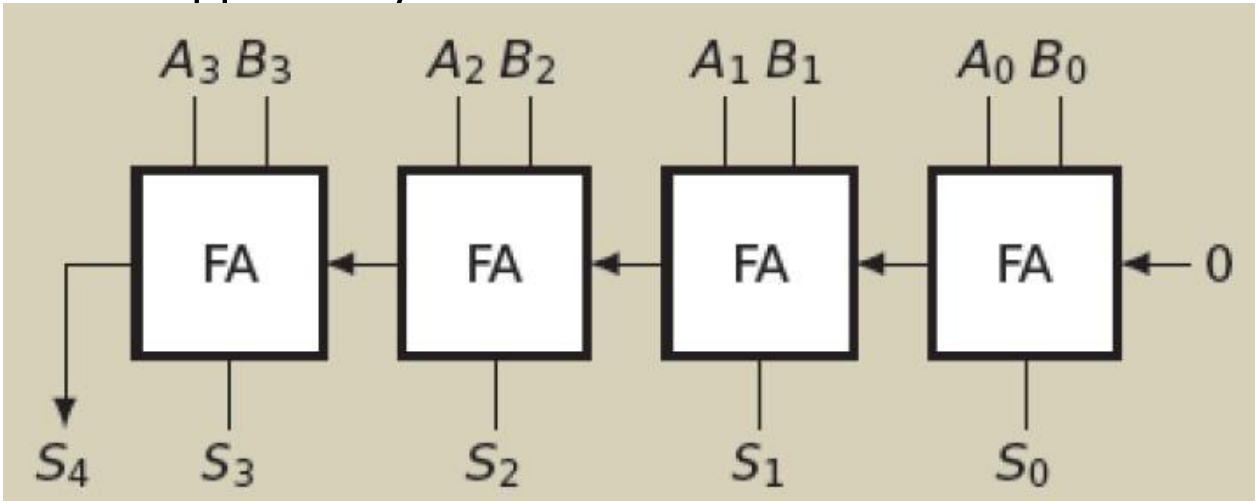
C_{IN}	X	Y	C_{OUT}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



Full adder: (a) gate level circuit diagram; (b) logic symbol; (c) alternate logic symbol suitable for cascading.

Ripple Carry Adder

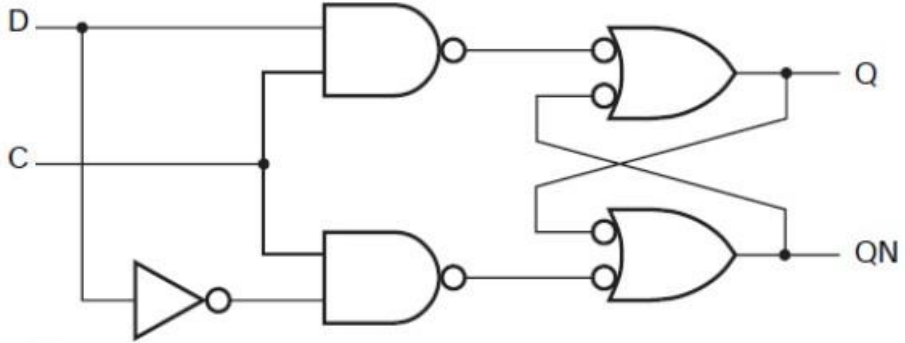
- Several full adders could be cascaded to make a ripple carry adder.
  - Four Bit Ripple Carry Adder



Sequential Logic Examples

- Latches
- Flip Flops
- Counters
- Registers

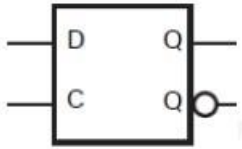
Latches - D Latch



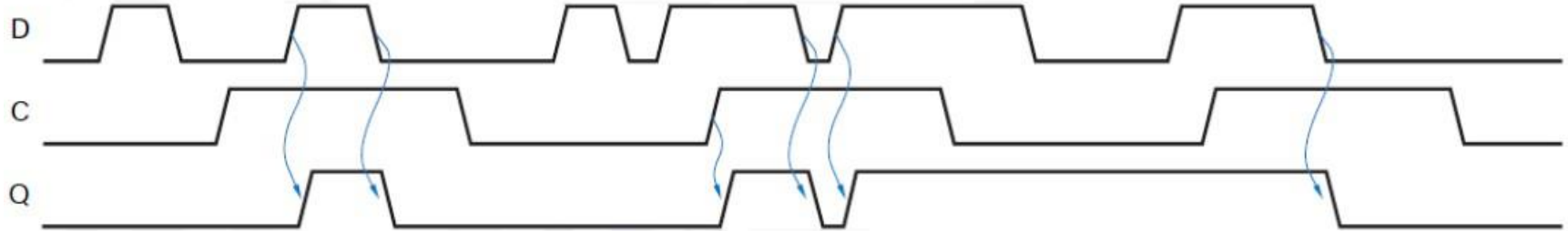
(a) circuit design using NAND gates

C	D	Q	QN
1	0	0	1
1	1	1	0
0	x	last Q	last QN

(b) function table



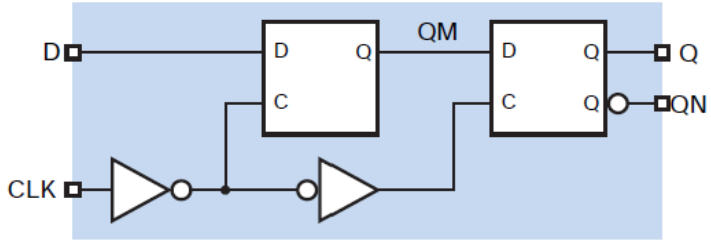
(c) logic symbol



Functional behavior of a D latch for various inputs.

Flip Flops - D Flip Flop

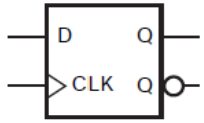
Positive-edge-triggered D flip-flop:



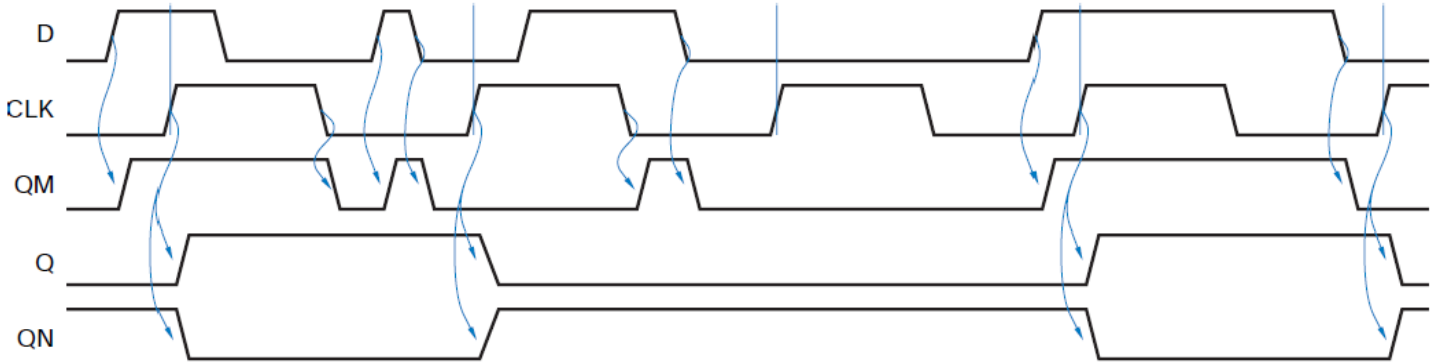
(a) circuit design using D latches

D	CLK	Q	QN
0	↑	0	1
1	↑	1	0
x	0	last Q	last QN
x	1	last Q	last QN

(b) function table

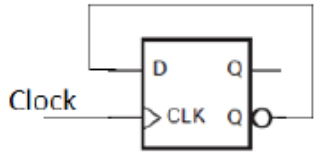


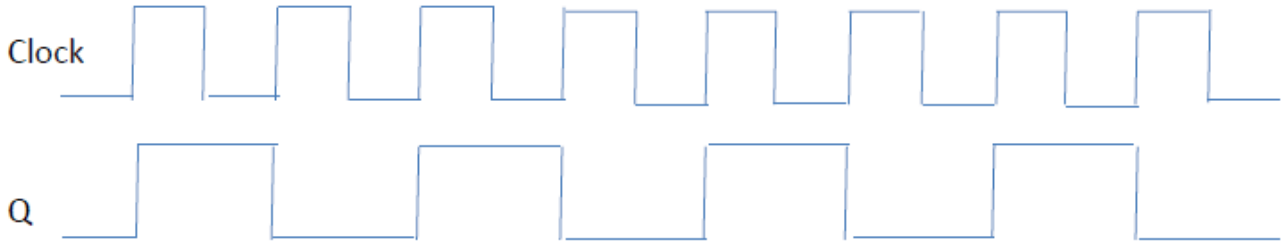
(c) logic symbol



Divide by 2 Counter

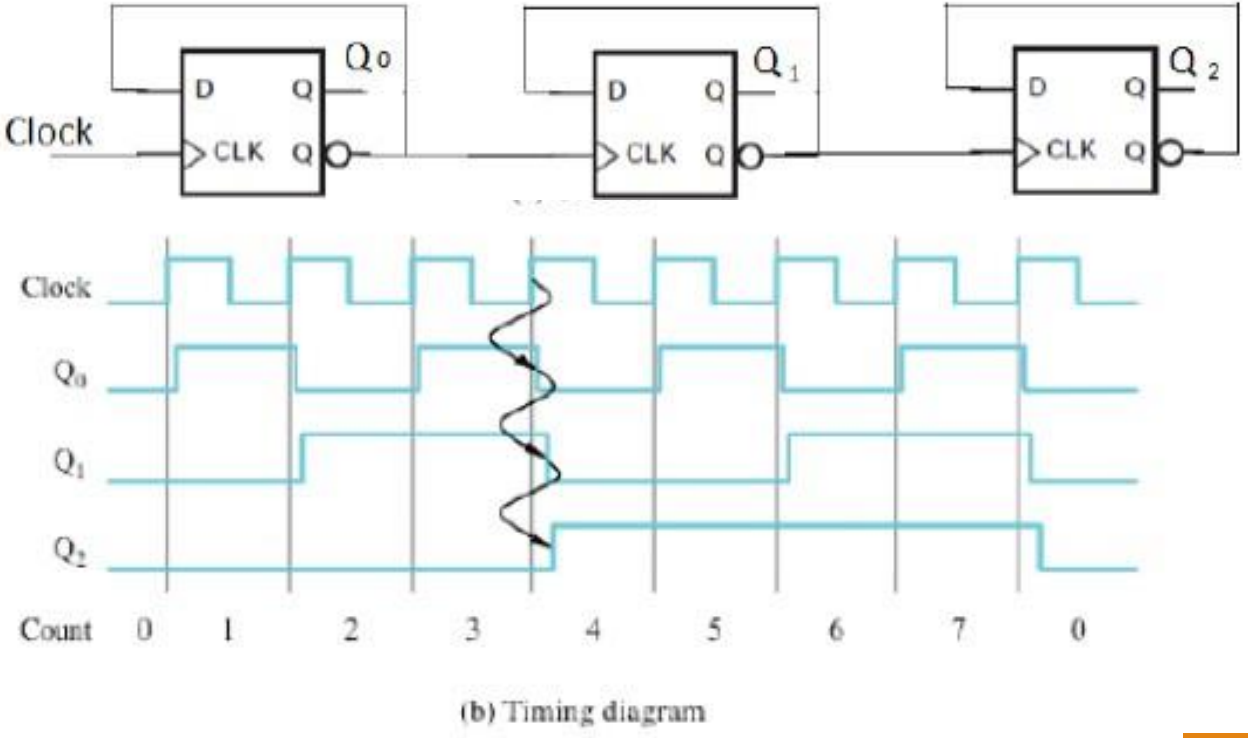
- The divide by two counter is the simplest counter which can only count up to 1 before it resets.
- This counter could also be used as a frequency divider which divide the input frequency by 2.





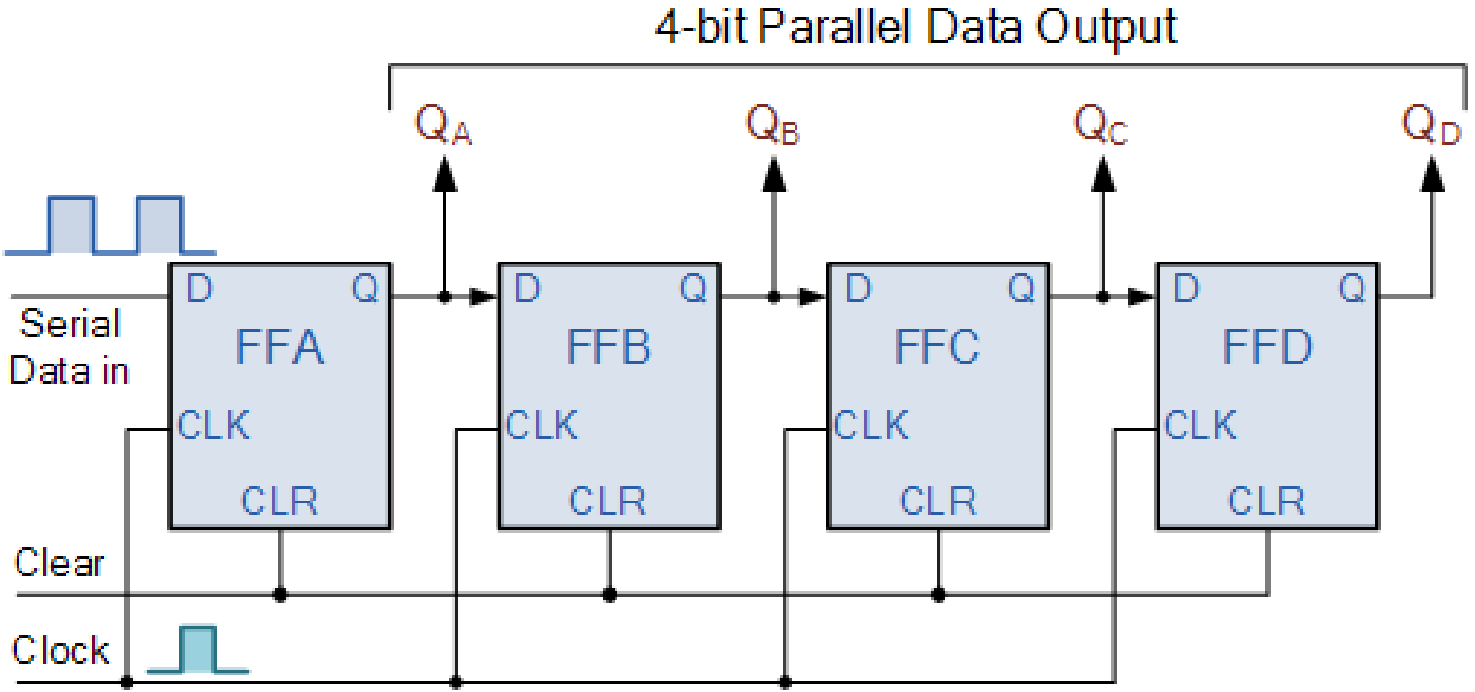
3-bit Ripple Counter

- A **n**-bit ripple counter could count up to a maximum of $\mathbf{2^n - 1}$.
- The 3-bit ripple counter can count up to 7.



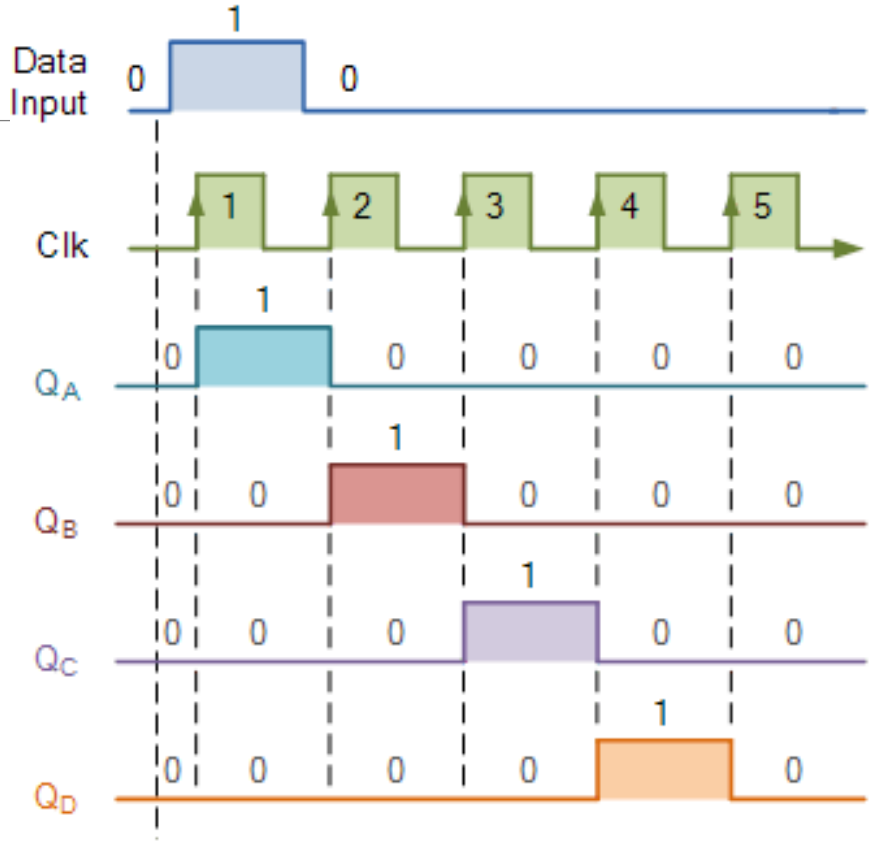
(b) Timing diagram

Serial-in to Parallel-out (SIPO) Shift Register



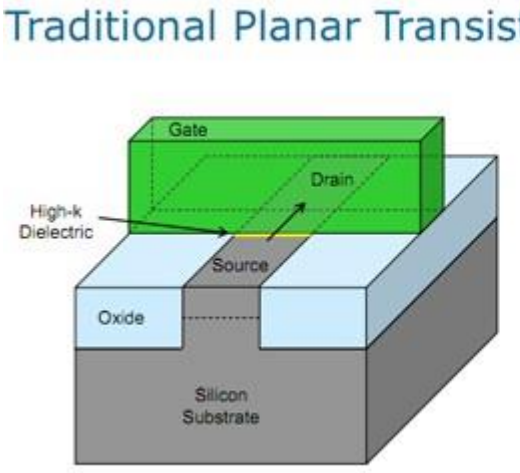
Serial-in to Parallel-out (SIPO) Shift Register ctd..

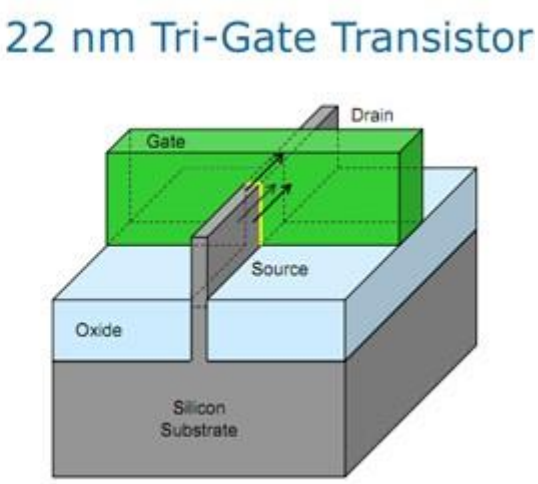
Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0



Recall: Transistor Fabrication

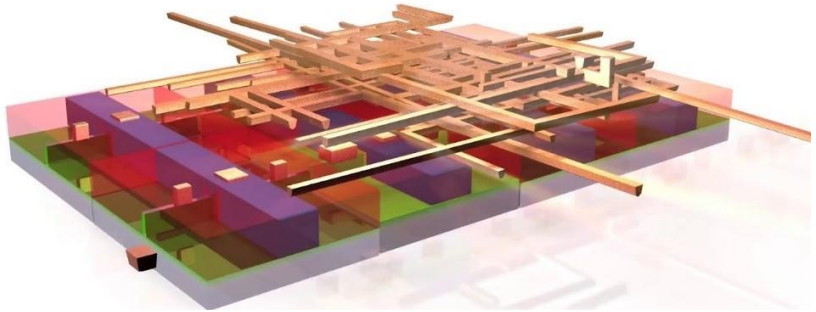
- Transistor fabrication in silicon chips





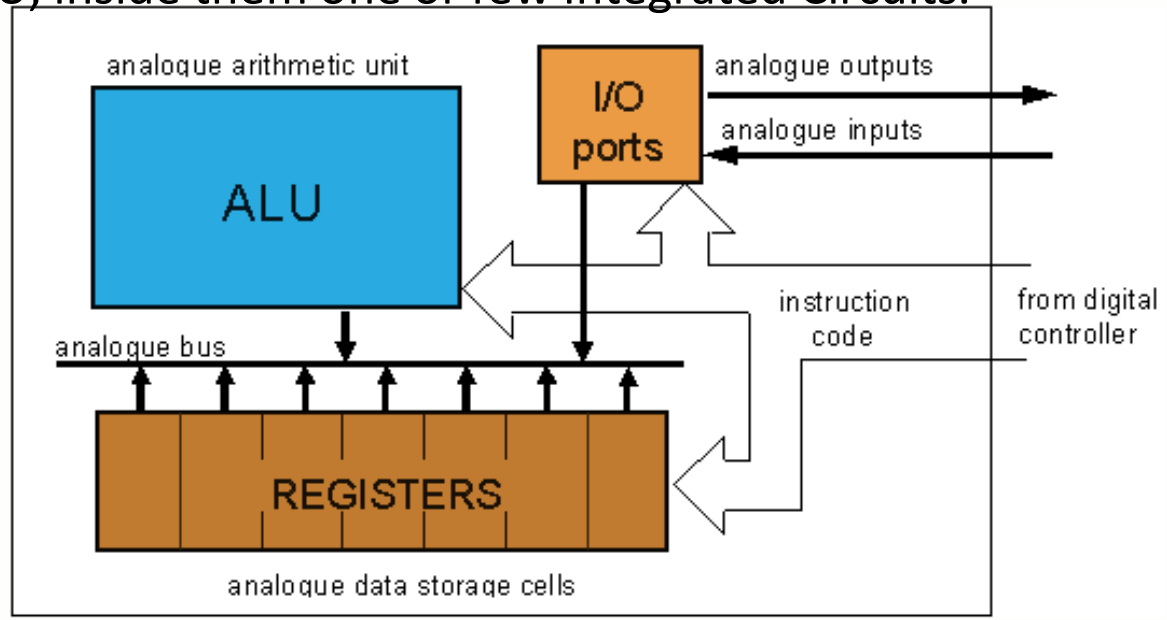
Transistor Implementation of Logic Circuits

- Transistors could be used to create simple circuits which implement logic gates.
- Logic gates are connected together to build simple logic circuits which will perform specific tasks such as:
  - Multiplexers
  - Decoders
  - Flip flops
  - Counters
  - Registers

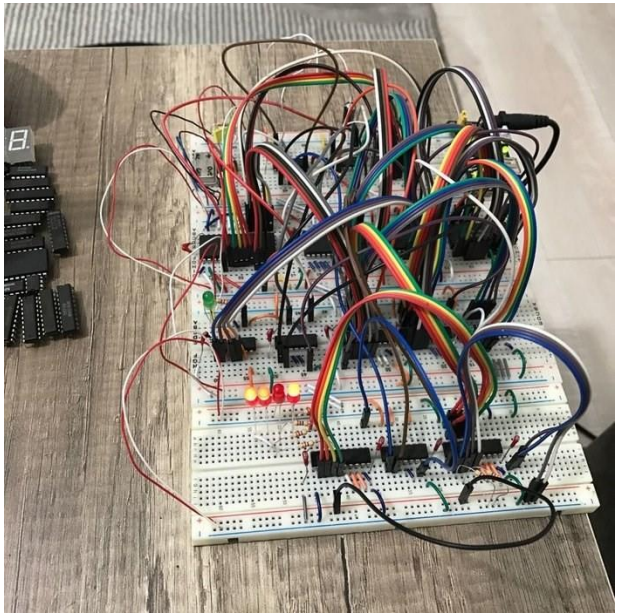


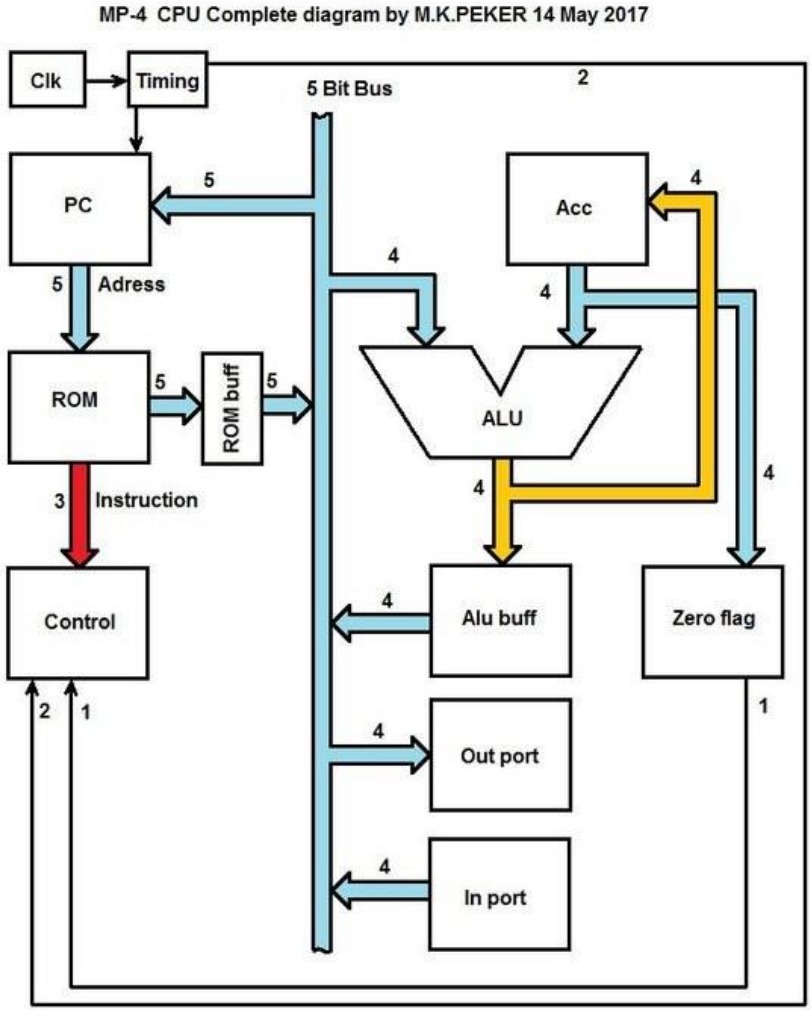
Microprocessor

- Microprocessor has only a CPU, inside them one or few Integrated Circuits.
  - It does not have RAM, ROM and other peripherals.
  - Microprocessors are not made for specific task but they are required where tasks are complex and tricky



4-bit CPU

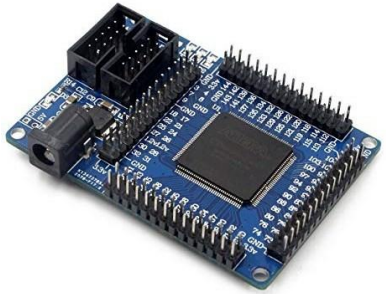


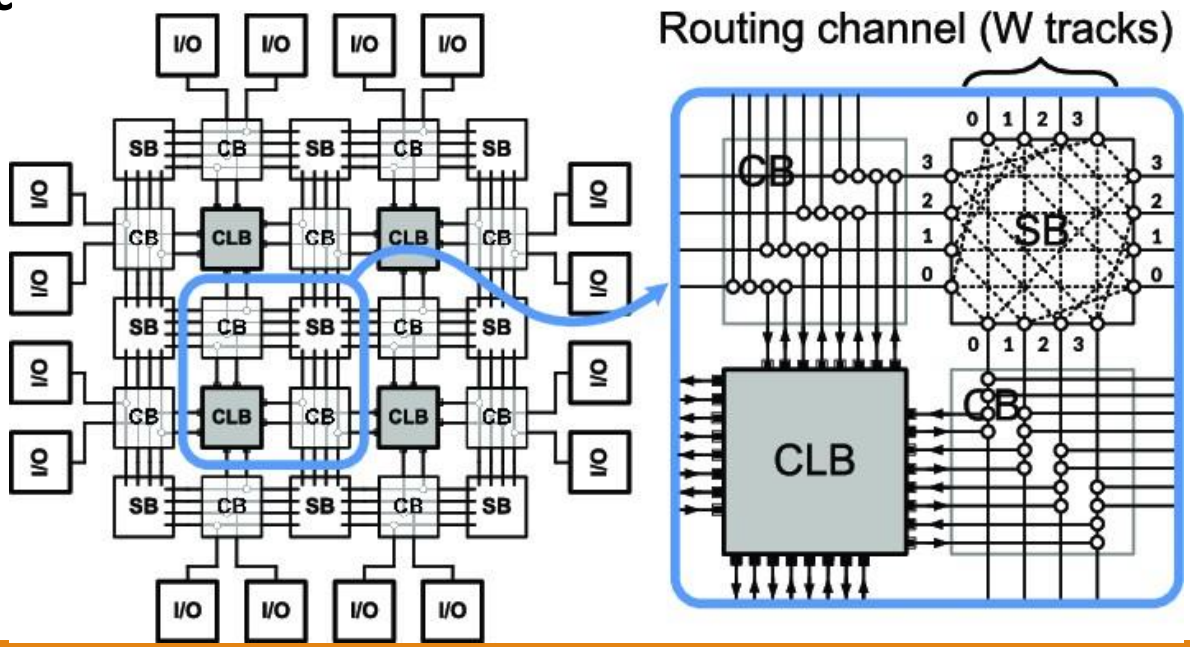

MP-4 CPU Complete diagram by M.K.PEKER 14 May 2017
Clk
Timing
5 Bit Bus
2
PC
5
Acc
4
5
Adress
4
4
ROM
5
ROM buff
5
ALU
3
Instruction
4
4
Control
Alu buff
4
Zero flag
2
1
1
Out port
4
In port
4

Processor Manufacturing

FPGA

- An FPGA is an **array of logic gates,** and this array can be **configured in the field**.
- It consists of a set of **C**onfigurable **L**ogic **B**locks and **S**witching **B**locks.





Thank You!