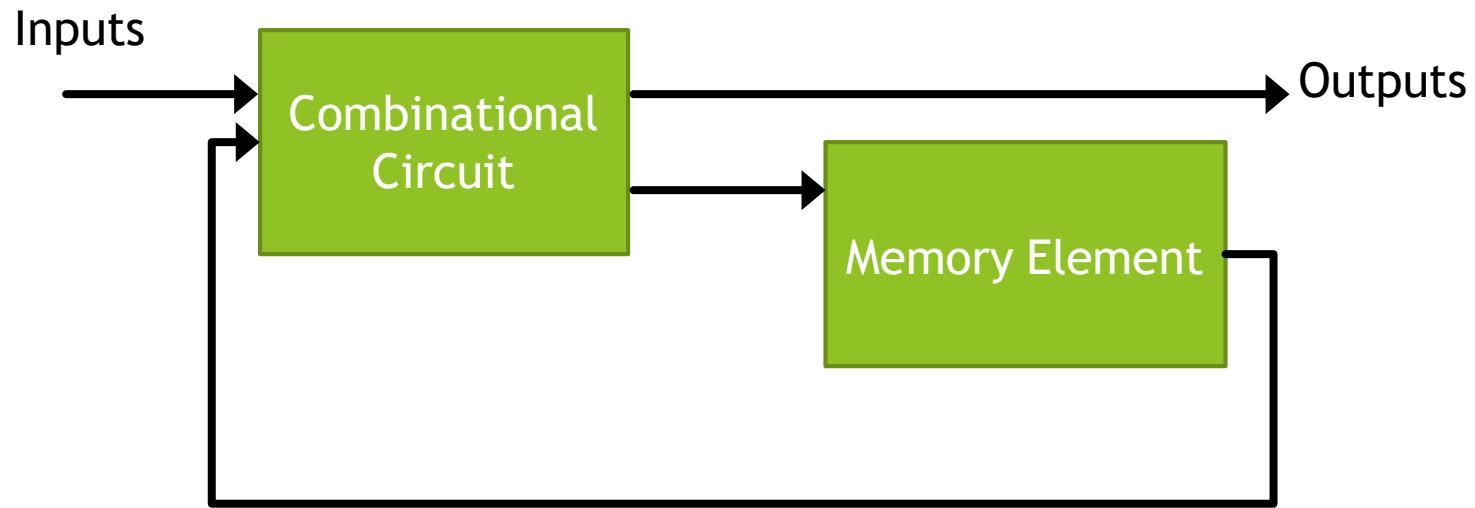


EE1212- Electronic System I

Synchronous Sequential Logic

Lecture 3
Capt Geeth Karunarathne

Sequential Circuits



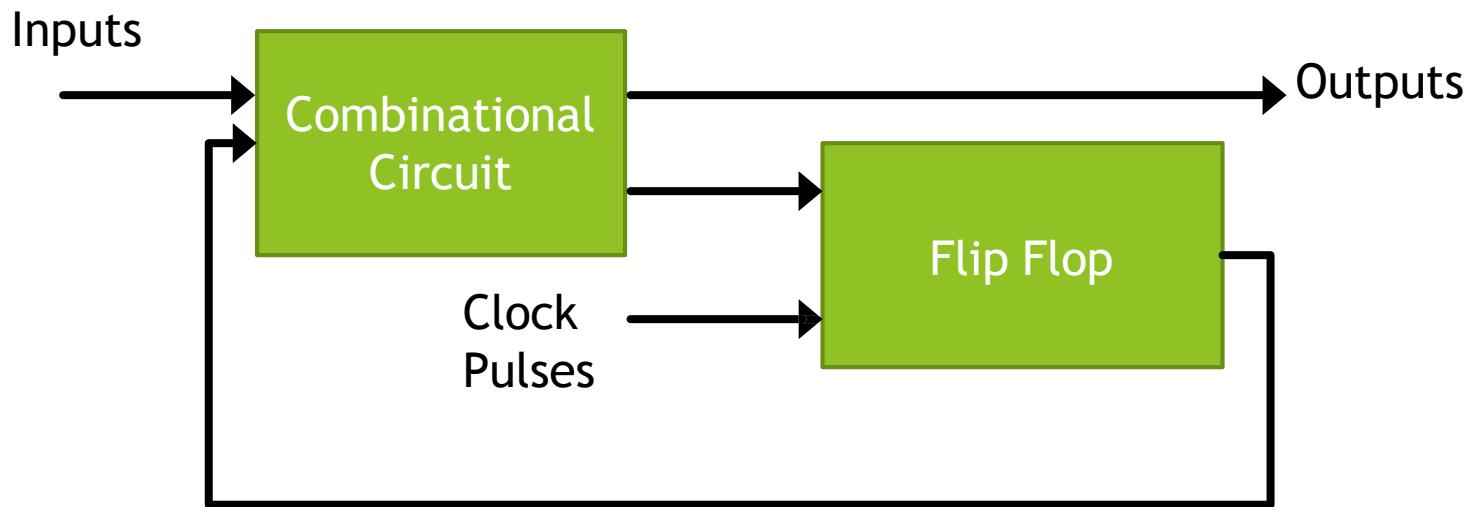
Sequential Circuits

- ▶ Sequential circuits consists of a combinational circuit with storage element (connected with a feedback path).
- ▶ Storage elements stores binary information.
- ▶ Inputs together with the present state of storage element determines the binary value of output.
- ▶ Two main types of sequential circuits:
 - Synchronous sequential circuit - Clock generator is used.
 - Asynchronous sequential circuit.

Flip Flop

- ▶ The storage elements used in clocked sequential circuits are called flip-flops.
- ▶ A binary storage device.

Synchronous Clocked Sequential Circuit

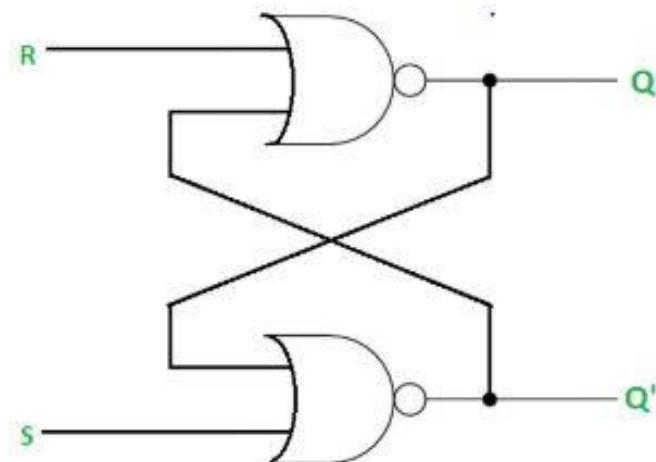


Latches

- ▶ Basic type of Flip-Flop
- ▶ Useful to design Asynchronous circuits.

SR Latch - with NOR gates

- ▶ When Q output is ‘1’ and Q' is ‘0’, it is said to be in *set* state.
- ▶ When Q output is ‘0’ and Q' is ‘1’, it is said to be in *reset* state.
- ▶ Under Normal conditions, both inputs remain 0 unless the state has to be changed.
- ▶ S input must go back to 0 before any other changes to avoid occurrence of undefined state.



SR Latch - with NOR gates

Function Table

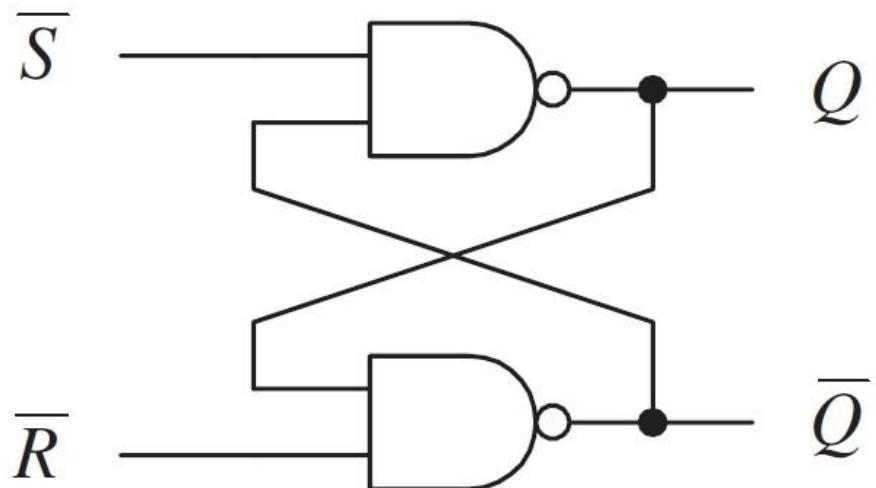
S	R	Q	Q'
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0

← After S=1, R=0

← After S=0, R=1

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	x

SR Latch - with NAND gates (S'-R' Latch)



SR Latch - with NAND gates (S'-R' Latch)

Function Table

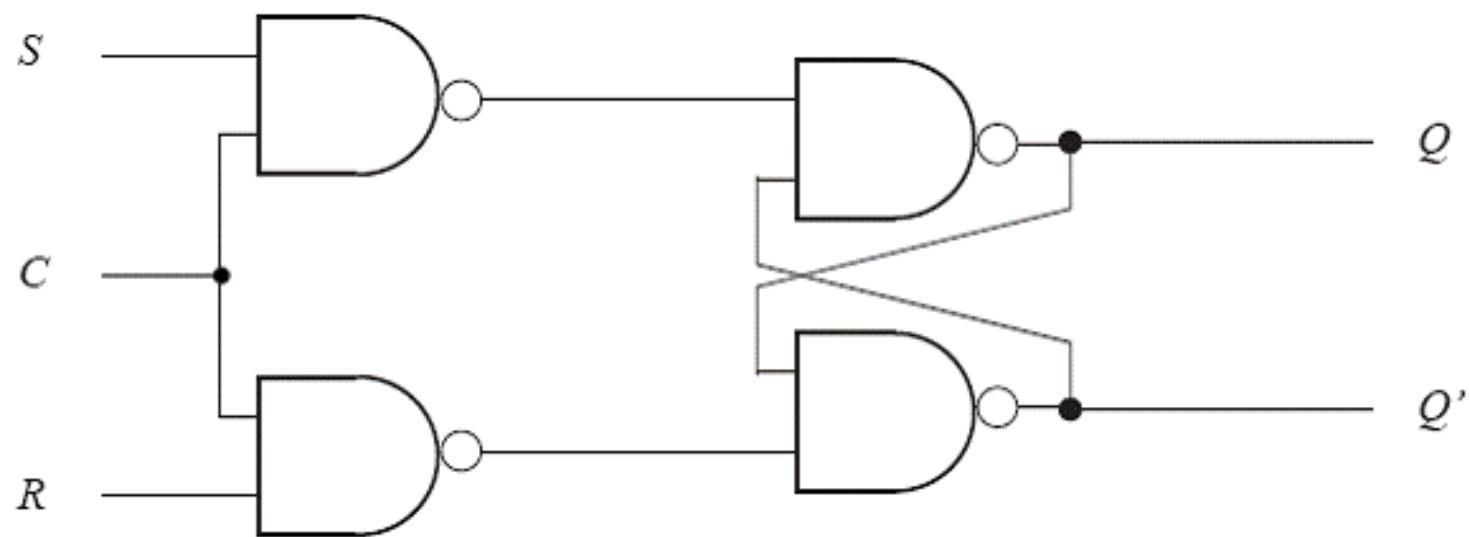
S	R	Q	Q'
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1

← After S=1, R=0

← After S=0, R=1

S	R	Q _{n+1}
1	1	Q _n
0	1	1
1	0	0
0	0	x

SR Latch - with NAND gates and control input

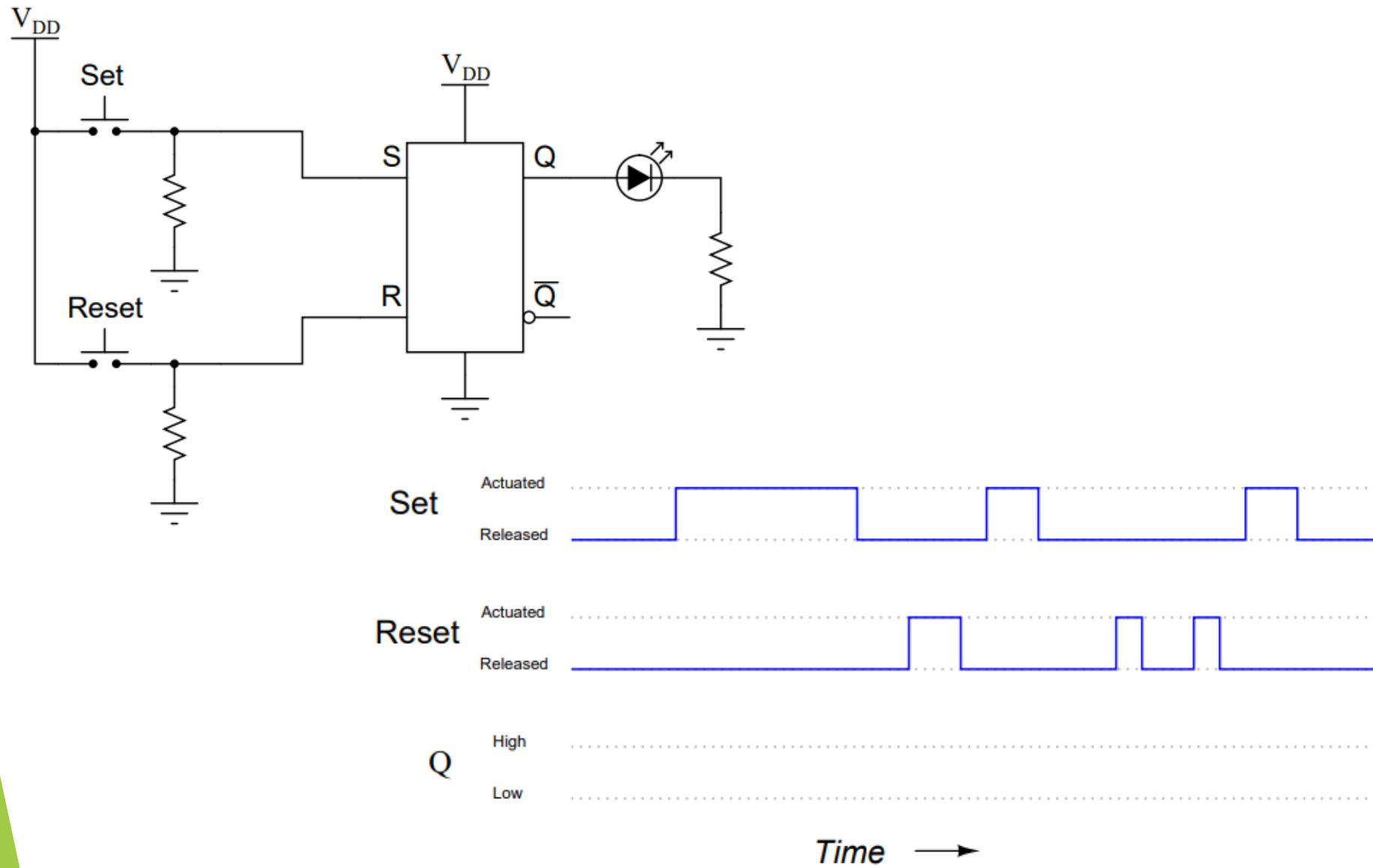


SR Latch - with NAND gates and control input

- ▶ Control input determines when the state of latch can be changed.
- ▶ The output of the NAND gates stay at unchanged state level when control is given 0.
- ▶ When Control is ‘1’, information from SR inputs is allowed to affect the SR latch.

C	S	R	Q_{n+1}
0	x	x	Q_n
1	0	0	Q_n
1	0	1	$Q_{n+1} = 0$; Reset state
1	1	0	$Q_{n+1} = 1$; Set state
1	1	1	Indeterminate

Complete the timing diagram, showing the state of the Q output over time as the Set and Reset switches are actuated. Assume that Q begins in the low state on power-up

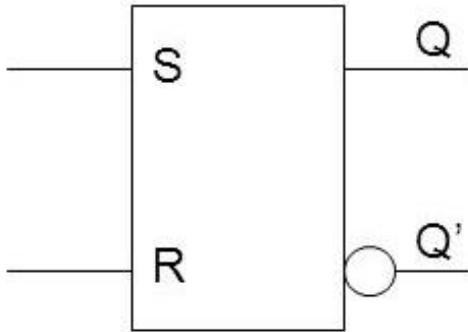


D Latch

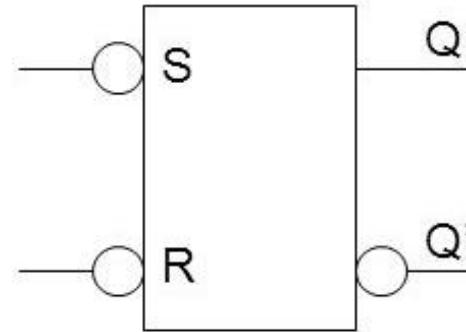
- ▶ Eliminates the undesirable condition of the indeterminate state in the SR Latch
- ▶ Latch has only 2 inputs. D (Data) & C (Control)

C	D	Q_{n+1}
0	x	Q_n
1	0	$Q_{n+1} = 0$; Reset state
1	1	$Q_{n+1} = 1$; Set state

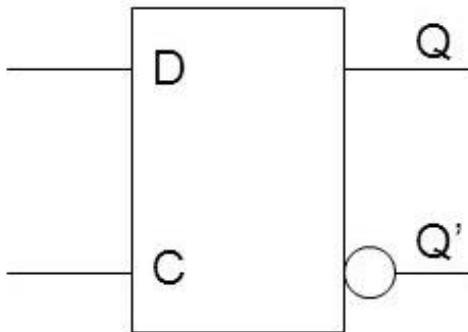
Graphic Symbols for Latches



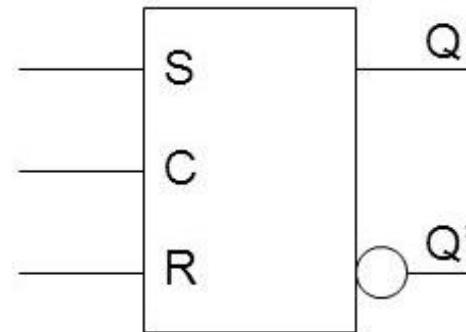
SR Latch



S'R' Latch



D Latch



SR Latch with Control

Flip Flops

- ▶ Flip Flop circuits are constructed in such a way as to make them properly when they are part of a sequential circuit that employs a common clock.
- ▶ Disadvantage of latch is, it responds to the level of a clock pulse.
- ▶ A Flip Flop is triggered only during a signal transition.
- ▶ Two types of transitions
 - Positive edge transition
 - Negative edge transition

J-K Flip Flop

- ▶ Three operations
 1. Set it to one ('1')
 2. Reset it to zero ('0')
 3. Complement it's output.

Characteristic Table of J-K Flip Flop

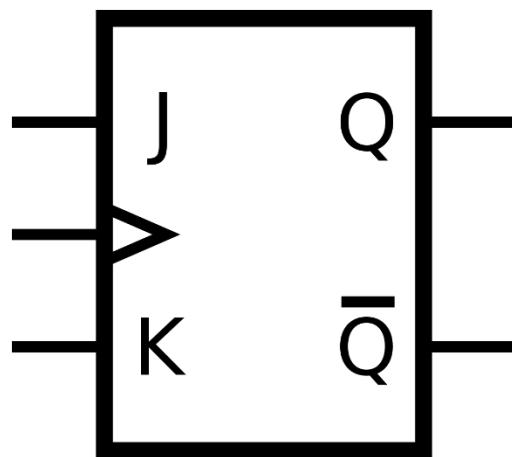
J	K	Q_{n+1}	
0	0	Q_n	No Change
0	1	0	Reset
1	0	1	Set
1	1	Q_n'	Complement

J-K Flip Flop

- ▶ Characteristic Equation

$$Q_{n+1} = JQ_n' + K'Q_n$$

- ▶ Graphical Symbol

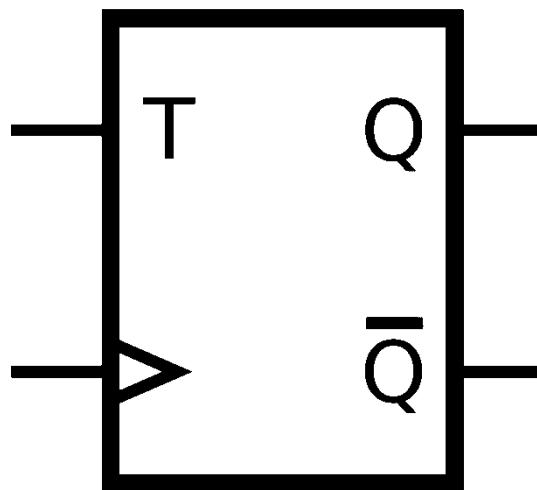


T Flip Flop

- ▶ Characteristic Equation

$$Q_{n+1} = T Q_n' + T' Q_n$$

- ▶ Graphical Symbol



- ▶ Characteristic Table of J-K Flip Flop

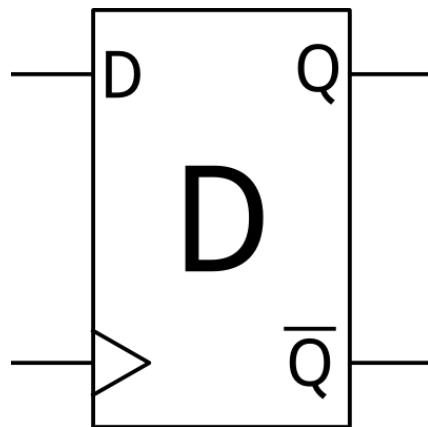
T	Q_{n+1}	
0	Q_n	No Change
1	Q_n'	Complement

D Flip Flop

- ▶ Characteristic Equation

$$Q_{n+1} = D$$

- ▶ Graphical Symbol



- ▶ Characteristic Table of J-K Flip Flop

D	Q_{n+1}	
0	0	Reset
1	1	Set