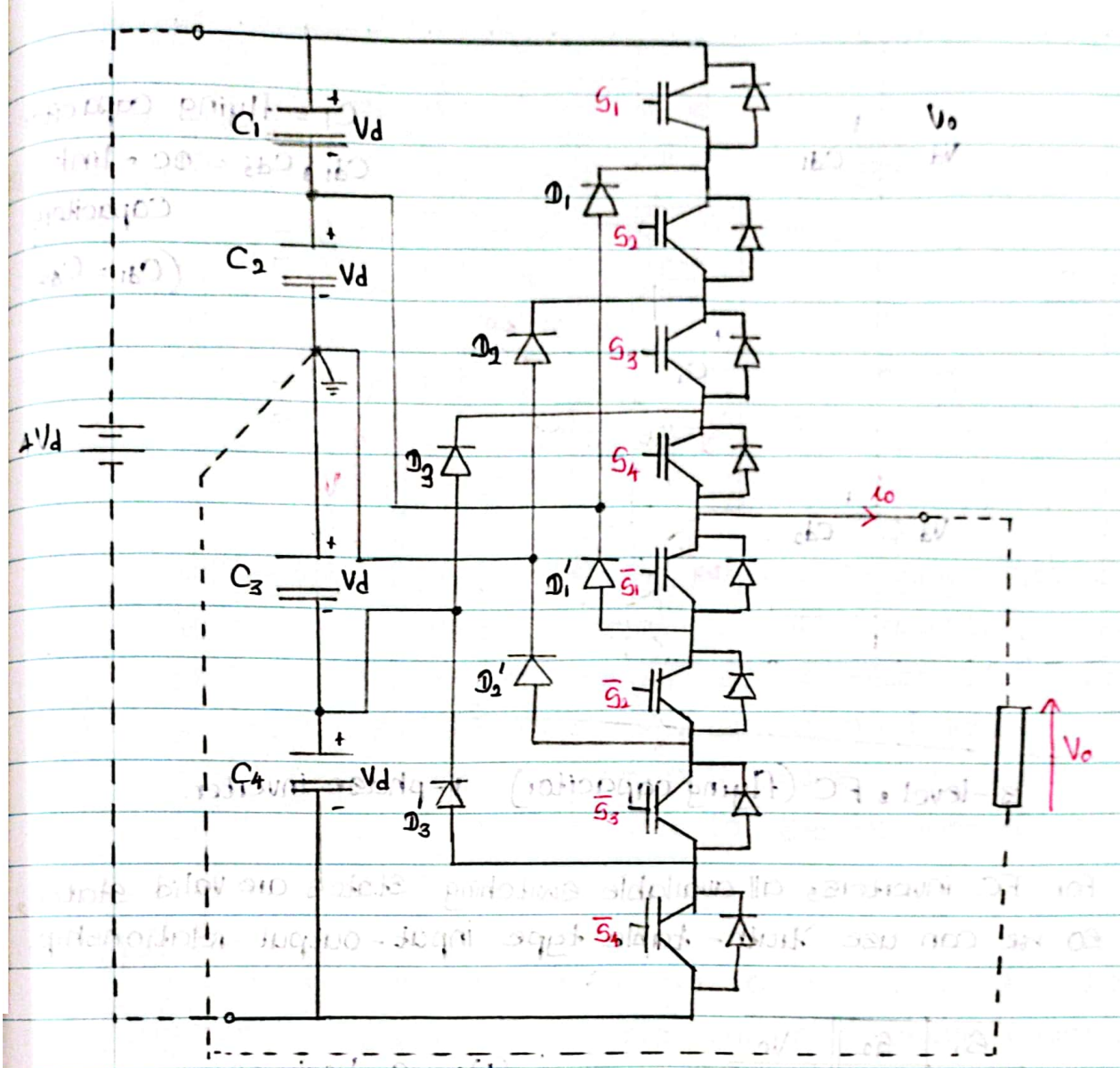


5-level, diode ~~clamped~~ Clamped 1-phase inverter.

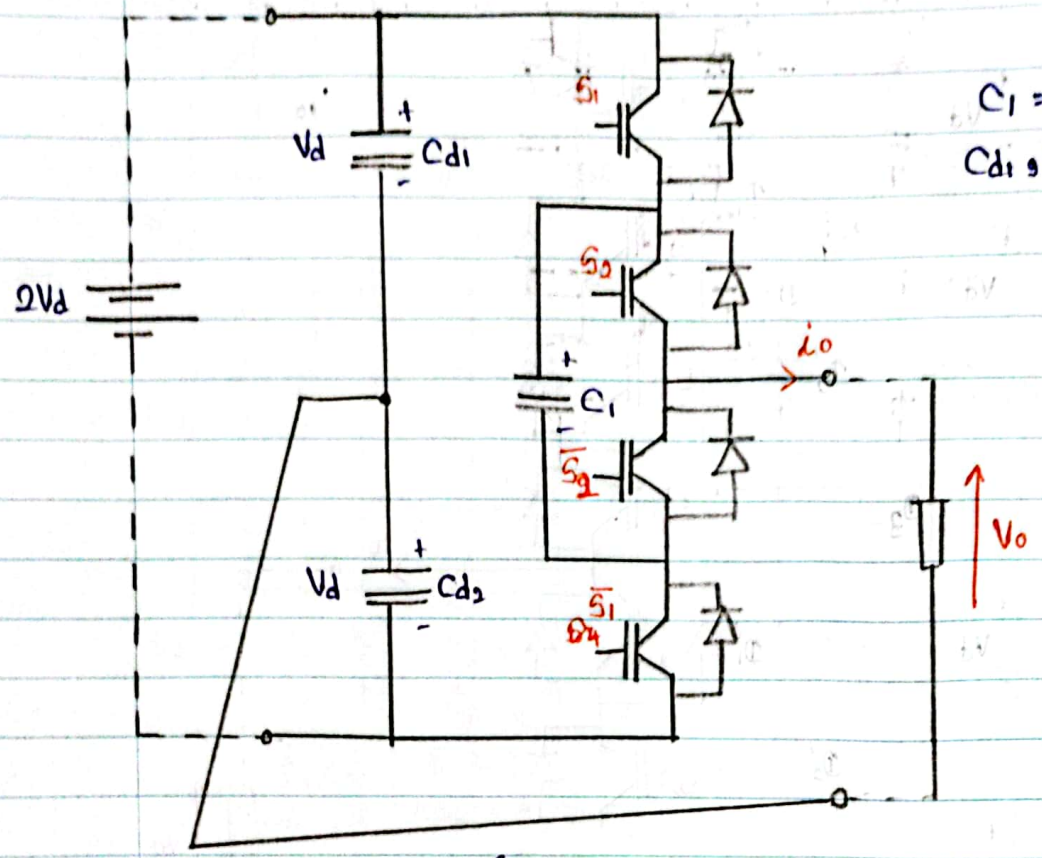
Output voltage V_o has the same waveform given for the 5 level CHB inverter.

23/07/2024

(iii) Flying Capacitor inverter:

This inverter too does not need different isolated DC ~~series~~ sources at the input but a single DC source with a capacitor divider. (i.e same as in diode clamped inverter.)

This inverter uses "capacitors", instead of clamping diodes to produce output voltage states, which we call "flying capacitor". Each flying capacitor is pre-charged to the voltage equal to one step of V_o.



3-level FC (flying capacitor) 1-phase inverter.

For FC inverters, all available switching states are valid states, so we can use truth-table type input-output relationship.

S_1	S_2	V_o
0	0	$-V_d$
0	1	0
1	0	0
1	1	$+V_d$

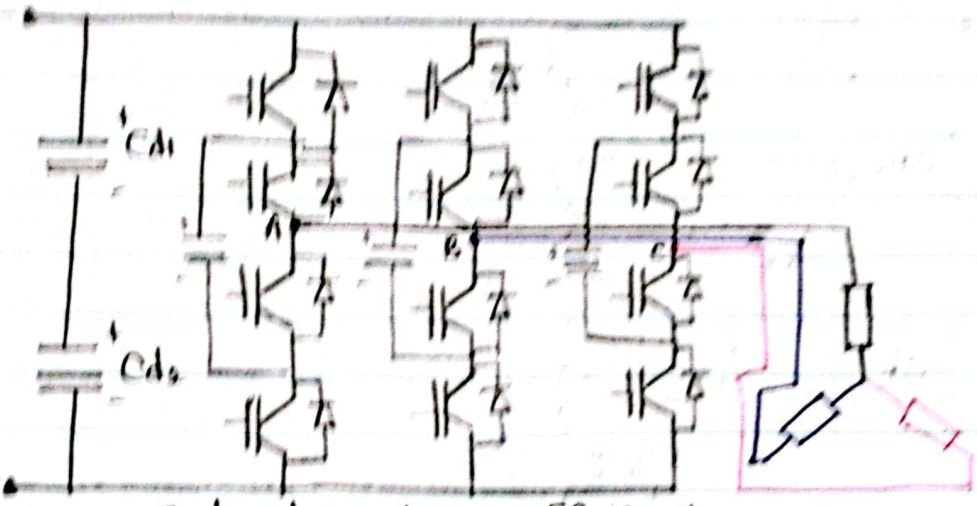
i_o (+)ve C_1 discharge
i_o (-)ve C_1 charge.

i_o (+)ve C_1 charge.
i_o (-)ve C_1 discharge.

- We have 2 alternative switching states to obtain $V_o = 0$, and this is called as having a "switching state redundant" we use these redundancy to regulate the voltage across the flying capacitor at its pre-charged of V_d.

i_o is positive and

For example, if $V_{c1} < V_d$ the $V_o = 0$ will be obtain using $S_1 S_2 = 10$, or if $V_{c1} > V_d$ using $S_1 S_2 = 01$.



3-level 3-phase FC inverter.

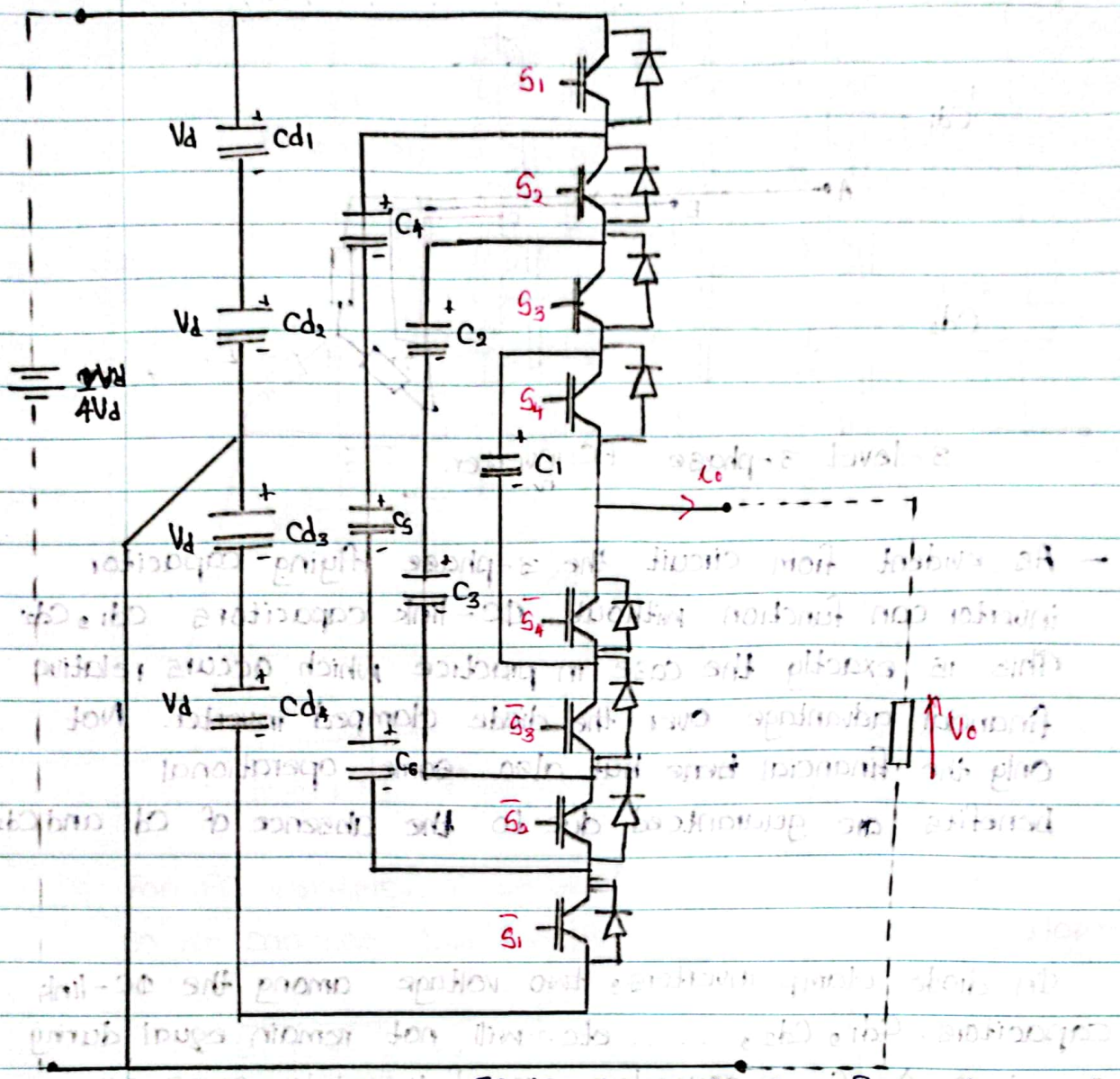
- As evident from circuit the 3-phase flying capacitor inverter can function without DC-link capacitors C_{d1}, C_{d2} this is exactly the case in practice which occurs relative financial advantage over the diode clamped inverter. Not only the financial benefits but also some operational benefits are guaranteed due to the absence of C_{d1} and C_{d2}.

Note

In diode clamp inverters, two voltage among the DC-link capacitors. C_{d1}, C_{d2}, ... etc. will not remain equal during operation. Some capacitors exceed V_d while some others fall below but total voltage of all cd's remain fixed.

In practice we need the seperate and dedicated circuit called "DC link voltage balancing circuit" regulate voltage across each Cd at V_d irrespective of the load current.

Such circuits operates independently with the ~~interference~~ normal operation of the inverter.



5-level, 1-phase FC inverter. $C_1 - C_6$ = Flying Capacitor

$C_{d_1} - C_{d_4}$ = DC-link Capacitor.

S_1	S_2	S_3	S_4	V_o
0	0	0	0	$-2V_d$
0	0	0	1	$-V_d$
0	0	1	0	$-V_d$
0	0	1	1	0
0	1	0	0	$-V_d$
0	1	0	1	0
0	1	1	0	0
0	1	1	1	V_d
1	0	0	0	$-V_d$
1	0	0	1	0
1	0	1	0	0
1	0	1	1	V_d
1	1	0	0	0
1	1	0	1	V_d
1	1	1	0	V_d
1	1	1	1	$2V_d$

$(\Sigma$ (1's) $- 2$.

- Each flying capacitor $C_1 \sim C_6$ is pre-charged to voltage V_d.
- No. of different V_o states are;

$2V_d \rightarrow 1$

$V_d \rightarrow 4$

$0 \rightarrow 6$ } possess redundancy.

$-V_d \rightarrow 4$

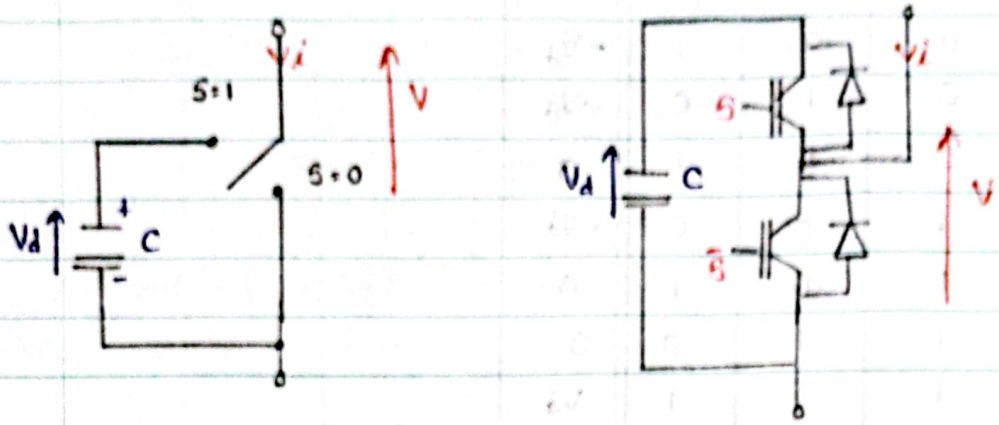
$-2V_d \rightarrow 1$

$\Sigma = 16$ //

$(a+b)^4 = a^4 + 4a^3b + 6a^2b^2 + 4ab^3 + b^4$

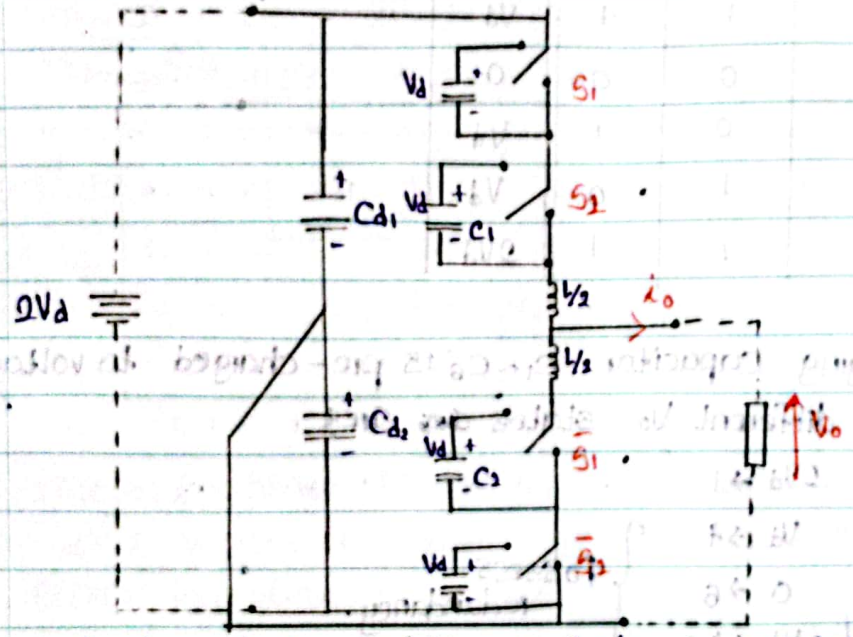
- Redundant switching states are selectively and adaptively use to regulate the voltage across each flying capacitor at its pre-charged value of V_d, during the operation.

(iv) Modular Multi-level inverter



Basic switching cell of an MMI.

S	V
1	Vd
0	0



3-level, 1 phase modular multi-level inverter.

All switching combinations are valid.

S_1	S_2	V_o
0	0	Vd
0	1	0
1	0	0
1	1	-Vd

At any time a two no.s of capacitors are connected in series on the full leg, thus satisfying the KVL.
A center tap inductor is used of the middle to absorb transient voltages during switchovers, and thereby to minimise current spikes rushing through the leg.

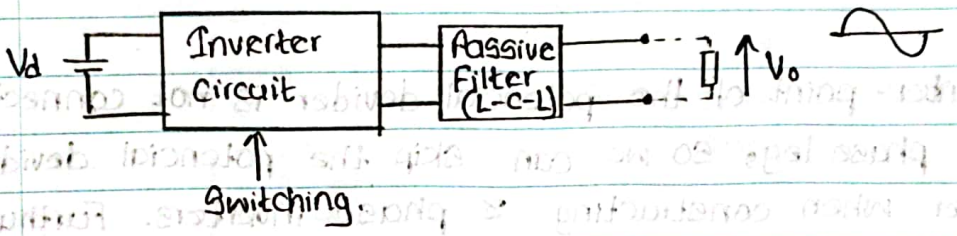
The 5-level inverter has the same structure but 4 cells in the upper half and 4 cells in the lower half.

The center-point of the potencial devider is not connected to the phase leg, so we can skip the potencial devider altogether when constructing 3 phase inverters. Furthurmore, regulating of voltage across capacitors in individual cells is straight forward, without having to execute complex algorithms.

Pulse Width Modulated (PWM) Inverters.

(a) Introduction:

PWM inverters use the same power circuit as ~~the~~ that used by square-wave inverters but different switching schemes. These inverters produce "pulsed-output voltage waveform" that can be easily filtered to ~~obtain~~ seperate the sinusoidal fundamental component.



We have quite a few no. of different switching schemes, called PWM schemes:

(i) Square-wave PWM.
(ii) Sinusoidal PWM.
(iii) Regular sampled PWM.
(iv) Harmonic Elimination PWM.
(v) Distortion Minimization PWM.
(vi) Voltage vector PWM.
(vii) Current control PWM etc.

Each scheme, except for voltage PWM has the 1 phase and 3 phase options. The voltage vector PWM has 3 phase option only.

All discussions follow will be based on 2-level PWM only.

All PWM inverters, except for square-wave PWM, produce a Vo with a significantly lesser amount of lower order harmon All PWM inverters offer voltage controlability within the inverter control.

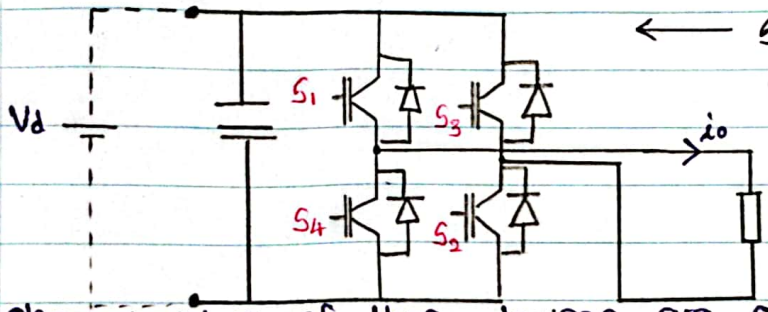
Date: ...../...../.....

b) Square - wave PWM.

Square wave PWM offers voltage controlabirty but not harmonic reduction. So, we do not filter V_o, in view of seperating the fundamental with a square wave PWM inverter.

- Note that whenever the term "square wave" becomes part of the name, the inverter does not give harmonic reduction in V_o.

(i) Single - phase inverter.



← Switching devices, i.e IGBTs and diodes in this circuit are designed to operate at higher switching frequencies, for example 25kHz. Switching times and reverse recovery ~~are~~ characteristics of these devices are critically looked of in the design

We have 2 alternative switching schemes to obtain square wave PWM.

(i) Bipolar switching schemes.
(ii) Unipolar switching schemes.