GENERAL SIR JOHN KOTELAWALA DEFENCE UNIVERSITY

Faculty of Engineering

Department of Electrical, Electronic and Telecommunication Engineering

BSc Engineering Degree

Semester 7 Examination – 2024 July

Intake 38 – ET

DIGITAL SYSTEMS DESIGN

(ET4173)

Time allowed: 3 hours 26 July 2024

ADDITIONAL MATERIAL PROVIDED

Nil

INSTRUCTIONS TO CANDIDATES

This paper contains 5 questions on 5 pages

Answer ALL questions.

This is a closed book examination.

This examination accounts for 70% of the module assessment. The marks assigned for each question and parts thereof are indicated in square brackets.

If you have any doubt as to the interpretation of the wordings of a question, make your own decision, but clearly state it on the script.

Assume reasonable values for any data not given in or provided with the question paper, clearly make such assumptions made in the script.

All examinations are conducted under the rules and regulations of the KDU.

DETAILS OF ASSESSMENT

Learning Outcome (LO)	Questions that assess LO	Marks allocated (Total 70%)
LO1	Q1	14
LO2	Q2	14
LO3	Q3	7
LO4	Q3	7
LO5	Q4	14
LO6	-	-
LO7	Q5	14

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Question 01

a. Discuss the advantages of Verilog HDL compared to VHDL. [4 marks]

b. Explain the Role of Libraries in VHDL and How They Enhance Code Modularity and Reusability. [4 marks]

a. Illustrate and Describe the Basic Structure of a VHDL Entity and Architecture: [4 marks]

c. Write the VHDL example code for full adder. [8 marks]

Question 02

a. Discuss the specialty of three-state gates and illustrate four such gates available in Verilog HDL with their keywords. [3 marks]

b. Explain the importance of using nonblocking statements in sequential RTL. [4 marks]

c. Discuss the different coding styles in verilog and in which ways these styles impact the synthesis of sequential circuits. [5 marks]

d. Write the RTL verilog code for 4-bit binary up-down counter shown in Figure Q.2. [8 marks
Note: for up counting, set *sel* to 1, and for down counting, set *sel* to 0.

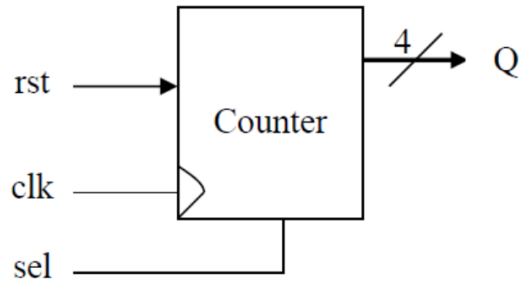

Figure Q.2

Question 03

a. Explain data dependency or stalling in processors, and describe the techniques used to mitigate these issues. [4 marks]

b. Illustrate and differentiate the three instruction formats available in a 32-bit MIPS processor. [5 marks]

c. Discuss the advantages of pipelining and its impact on performance. [3 marks]

d. Design a slice ALU circuit that has the following functions as shown in Table Q.3. All the required components of the circuit are given in Figure Q.3, including three 2-to-1 multiplexers, one inverter, one OR gate, two XOR gates and one 1- bit full adder. You need to draw the slice circuit and complete the connections on your answer sheet [8 marks]

Table Q.3

ALU mode m_1 m_2	**Function**
00	A XOR B
01	-A
10	A+B
11	A-B

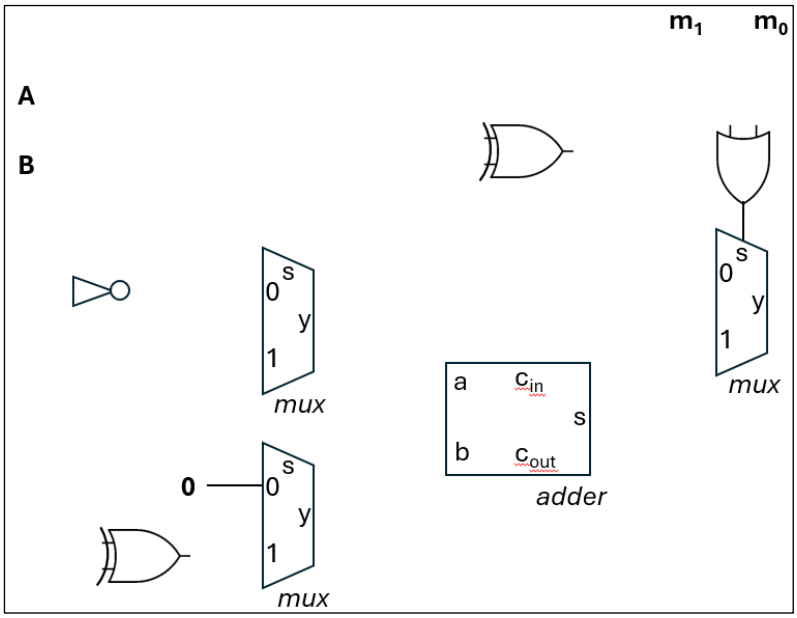

Fig Q.3

Question 04

a. Discuss the usage of ROM and state the different types of ROM. [5 marks]

b. State the characteristics used to measure memory performance. [5 marks]

c. Define *'cache miss'* and outline the key considerations in cache design. [5 marks]

d. A direct-mapped cache has a total size of 16 KB and a block size of 32 bytes.

i. Calculate the number of blocks in the cache. [2 marks]

ii. Given a 32-bit memory address, determine the number of bits used for the tag, index, and block offset. [3 marks]

Question 05

a. Discuss the algorithm used for state reduction when designing a asynchronous sequential circuit. [4 marks]

b. Design an asynchronous sequential circuit that has two inputs X_2 and X_1 and one output Z. When $X_1 = 0$, the output Z is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0.

i. Draw the state diagram and derive primitive flow table for the circuit. Show that it can be reduced to the table shown in the Fig Q.5a. [8 marks]

ii. Complete the design of the circuit and implement ths using NOR gate SR latch. The excitation table of NOR gate SR latch is given in Fig Q.5b. [8 marks]

Present state	Next state, Output Z for X_2X_1 Inputs			
	00	01	11	10
S_0	(S_0), 0	(S_0), 0	S_2, –	S_1, 0
S_1	S_0, 0	S_2, –	(S_1), 0	(S_1), 0
S_2	S_0, –	(S_2), 1	(S_2), 1	S_1, –

Fig Q.5a

Q(n)	Q(n+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Fig Q 5b

- End of the Question Paper –