GENERAL SIR JOHN KOTELAWALA DEFENCE UNIVERSITY
Faculty of Engineering
Department of Electrical, Electronic and Telecommunication Engineering

B.Sc. Engineering Degree
Semester 6 Examination – October 2021
(Intake 36 - EE/ET/MC)

EE 3213 – POWER ELECTRONICS AND APPLICATIONS I

Time allowed: 3 Hours 18 October 2021

INSTRUCTIONS TO CANDIDATES:

This paper contains 6 questions on 5 pages.
Answer any FIVE Questions only.
This is a closed book examination.

This examination accounts for 70% of the module assessment. The total maximum mark attainable is 100. The marks assigned for each question & sections thereof are indicated in square brackets.

If you have any doubt as to the interpretation of the wording of a question, make your own decision, but clearly state it on the script.

All Examinations are conducted under the rules & regulations of the University

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Question 1

a) Three-phase, full-bridge AC to DC diode-converter delivers 20 kW of power to an inductive load at a mean DC voltage of 540 V, with approximately constant DC current in the load. Frequency of input three-phase AC supply is 50 Hz and you may ignore the internal impedance of the AC supply. Assume ideal diodes.
Determine,

(i) RMS value of line-line voltage of AC supply. [03]
(ii) RMS value of the fundamental component of input line-current. [03]
(iii) Magnitude and frequency of the lowest order harmonic of input line current. [04]

b) In another application, a three-phase, dual-series-bridge diode-converter is used to deliver inductive 20 kW at mean DC voltage 540 V, in which the two bridges are supplied by two outputs of a *Dd*0*y*1 three-phase transformer having line-voltage ratio 1:1:1. Supply frequency is 50 Hz and you may ignore the internal impedances of the supply and the transformer. Determine

(i) RMS value of line-line voltage of AC supply. [03]
(ii) RMS value of the fundamental component of line-current at transformer input. [03]
(iii) Magnitude and frequency of the lowest order harmonics of line current at transformer input. [04]

Question 2

a) A three phase, full-bridge AC to DC thyristor-converter is operating on 400 V, 50 Hz, three phase AC supply. It delivers 10 kW of power to an inductive load at 420 V DC (mean). Supply side inductance is 3 mH per phase. You may assume that the output current is constant and ripple free.
Calculate,
(i) Delay (firing) angle. [04]
(ii) Conduction overlap angle. [04]
(iii) RMS value of the fundamental component of input line current. [04]

b) For the converter in (a) above, sketch the following waveforms indicating appropriate values.
(i) Output voltage. [03]
(ii) One of the line-line voltage waveforms at the converter input (PCC) showing deep and shallow notches. [03]

Describe briefly how the depths of voltage notches at the PCC in (ii) above are modified in practice to comply with utility standards. [02]

Question 3

a) Three-phase, voltage source inverter is operated with Sinusoidal PWM control, with carrier-ratio 51, depth of modulation 0.8 and reference frequency 50 Hz. Input DC voltage to the inverter is 750 V.

(i) Determine the RMS value of the fundamental component of output voltage. [04]
(ii) What is the lowest order significant harmonic present in the output voltage? [02]
(iii) What is the switching frequency? [02]

b) Another three-phase, voltage source inverter is operated with Regular sampled PWM control, with carrier-ratio 51, depth of modulation 0.8 and reference frequency 50 Hz. Sampling is done at consecutive positive peak of the triangular carrier, and the 0^{th} sampling instant is chosen a quarter carrier-cycle before the positive-going zero-crossing of the sinusoidal reference signal. Calculate the timing of switching signals S_a, S_b & S_c over the sampling-period following the 12^{th} sampling instant. [12]

Question 4

a) Sketch the waveform of phase-voltage at the output of a three-phase voltage source inverter (VSI), operated with six-step (square wave) control. Take DC input-voltage as V_d. Indicate appropriate values in the waveforms. [04]

b) The inverter in (a) above serves a balanced, three-phase, star-connected load with each phase having 15 Ω resistance in series with 75 mH inductance. Input DC voltage is 600 V and switching cycle time is 20 ms.

(i) Determine the RMS value of the fundamental component of load current. [04]
(ii) Calculate and sketch the waveform of load current in phase-*a*. [08]

c) Sketch the waveform of input current at the DC supply in (b) above, indicating values. [04]

Question 5

a) A single-phase VSI with input DC voltage V_d is delivering an output current $I_m \sin(\omega t)$ using hysteresis current control within a tolerance band ΔH. The load comprises a resistance R and inductance L in series. Derive expressions for the switching frequencies near the zero-crossing and near the peak of the output current. [10]

b) Three-phase voltage source inverter is to be operated with Distortion Minimization PWM to minimize net distortion due to harmonics up to 25th order in output voltage, and to set the magnitude of the fundamental component of output voltage to 78% of its maximum. Number of switching points per quarter-cycle of switching signal is chosen as 6.
Write down mathematical expressions in terms of switching-angles for the following components of the minimization model.

(i) Function to be minimized. [06]
(ii) Constraint function. [04]

Question 6

a) Show that the voltage vector $\overline{V}$ for a balanced, three-phase, sinusoidal voltages of angular frequency ω and line-voltage V_L (RMS) is rotating at constant angular frequency ω, with a constant magnitude $\frac{\sqrt{6}V_L}{2}$. [04]

b) A three-phase voltage source inverter is operated with Voltage Vector PWM at constant sampling frequency 10 kHz. The inverter delivers 50 Hz (fundamental) output with variable voltage. Input voltage to the inverter is 600 V DC.

(i) What is the greatest value of line-voltage fundamental (RMS) obtainable at the output with vector control? [04]

(ii) If the 0^{th} sampling instant is chosen to coincide with the positive-peak of the desired phase-a voltage, calculate the timing for switching signals S_a, S_b & S_c over the sampling-interval after the 75^{th} sampling instant, when the desired line-voltage fundamental is 400 V rms. [12]

End of Question Paper