GENERAL SIR JOHN KOTELAWALA DEFENCE UNIVERSITY

Faculty of Engineering

Department of Electrical, Electronic and Telecommunication Engineering

BSc Engineering Degree

Semester 5 End Semester Examination – June/July 2020

(Intake 35 - ET)

ET4082 – SEMICONDUCTOR AND SOLID STATE DEVICES

Time allowed: 2 hours 23rd June, 2020

INSTRUCTIONS TO CANDIDATES

This paper contains 4 questions on 4 pages

Answer all FOUR questions

This is a closed book examination

This examination accounts for **70%** of the module assessment. A total maximum mark obtainable is 100. The marks assigned for each question and parts thereof are indicated in square brackets

If you have any doubt as to the interpretation of the wordings of a question, make your own decision, but clearly state it on the script

Assume reasonable values for any data not given in or provided with the question paper, clearly make such assumptions made in the script

All examinations are conducted under the rules and regulations of the KDU

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Important Equations

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$

$$k'_n = \mu_n C_{OX}$$

$$i_D = \frac{1}{2} k'_n \frac{W}{L} V^2_{OV}$$

$$r_{DS} = \frac{1}{k'_n \frac{W}{L} V_{OV}}$$

QUESTION 1

Solid materials are important in fabrication of electronics components. They are classified in to three types, depending on their atomic structures.

(a) Explain the atomic structure of three basic types of solid materials [06]

(b) Explain the difference between intrinsic and extrinsic semiconductors [04]

(c) Explain how could doping increased the conductivity using ***Band Structure*** of semiconductor [07]

(d) Explain the Fermi Level arrangement and of forward biased **p-n** Junction [08]

QUESTION 2

(a) Calculate the total charge stored in the channel of an NMOS transistor having C_{OX} = 12 fF/μm^2, L = 0.15 μm, and W = 1.5 μm, and operated at V_{OV} = 0.5V and V_{DS} = 0V. [07]

(b) A circuit designer intending to operate a MOSFET in saturation region by considering the effect of changing the device dimensions and operating voltages on the drain current. Explain, what factor does change, in each of the following cases.

i. The channel length is doubled.

ii. The channel width is doubled. [10]

(c) A process technology which $L_{min} = 0.18\mu m$ (0.18-μm fabrication process) is specified to have $t_{ox} = 4nm$, $\mu_n = 450cm^2/V.s$, and $V_t = 0.5V$.($\varepsilon_{OX} = 3.45 \times 10^{-11}\ F/m$)

i. For a MOSFET with minimum length fabricated in aforementioned process, find the required value of W so that the device exhibits a channel resistance r_{DS} of $1k\Omega$ at $V_{GS} = 1V$. [08]

QUESTION 3

The Semiconductor manufacturing is a major industry in the world. The semiconductor manufacturing process consists of main four steps.

(a) Explain briefly, the main steps in silicon manufacturing [08]

(b) Explain the Czochralaki Process of silicon manufacturing [07]

(c) Discuss the main steps of Photolithography [05]

(d) Discuss the advantage of using 5X reticle [05]

QUESTION 4

The Oxidation is a key step in Silicon Manufacturing Process.

(a) Explain the dry oxidation process [05]

(b) Discuss advantages and disadvantages of wet oxide used in oxidation of silicon. [06]

(c) Describe the process of wet chemical etching. [07]

(d) Compare the advantage of "*ion implantation*" for improving performance of MOS transistors [07]

END OF THE QUESTION PAPER