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Faculty of Engineering
Department of Electrical, Electronic and Telecommunication Engineering

BSc Engineering Degree
Semester 4 Examination – Nov/Dec 2018
(Intake 32 - ET)

ET2203 – SEMICONDUCTOR AND SOLID STATE DEVICES

Time allowed: 3 hours 07th November, 2018

INSTRUCTIONS TO CANDIDATES

This paper contains 4 questions on 5 pages

Answer all **FOUR** questions

This is a closed book examination

This examination accounts for 70% of the module assessment. A total maximum mark obtainable is 100. The marks assigned for each question and parts thereof are indicated in square brackets

If you have any doubt as to the interpretation of the wordings of a question, make your own decision, but clearly state it on the script

Assume reasonable values for any data not given in or provided with the question paper, clearly make such assumptions made in the script

All examinations are conducted under the rules and regulations of the KDU

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$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$

$$k'_n = \mu_n C_{OX}$$

$$i_D = \frac{1}{2} k'_n \frac{W}{L} V^2_{OV}$$

$$r_{DS} = \frac{1}{k'_n \frac{W}{L} V_{OV}}$$

Question 1

Crystalline materials are solids with an atomic structure based on a regular repeated pattern

(a) Name types that solid materials could classify, and explain the atomic structure of each type. [05]

(b) Explain the relation of Fermi Level and Band Structure for n-type semiconductor [07]

(c) Diagram in Figure Q1.1 is band diagram of a p-n junction

$V = 0$

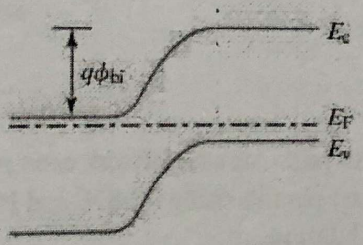

Figure Q1.1

(d) Draw Band diagram for

a. A **forward biased** p-n Junction

b. A **reversed biased** p-n Junction [08]

(e) Explain, what represent the constant Fermi level along the p-n junction. [05]

Question 2

(a) Calculate the total charge stored in the channel of an NMOS transistor having C_{ox} = 6 fF/μm², L = 0.25 μm, and W = 2.5 μm, and operated at V_{OV} = 0.5V and V_{DS} = 0V. [05]

(b) An NMOS transistor that is operated with a small v_{DS} is found to exhibit a resistance r_{DS}. By what factor r_{DS} will change in each of the following situations?

a. V_{OV} is doubled. [03]
b. The device is replaced with another, fabricated in the same technology but with double the width. [03]
c. The device is replaced with another, fabricated in the same technology but with both the width and length doubled. [03]
d. The device is replaced with another, fabricated in a more advanced technology for which the oxide thickness is halved and similarly for W and L (assume μ_n remains unchanged). [05]

(c) An n-channel MOS device in a technology for which oxide thickness is 20 nm, minimum channel length is 1 μm, $k_n' = 100\ \mu A/V^2$ and V_t = 0.8 V operates in the triode region, with small v_{DS} and with the gate–source voltage in the range 0V to +5 V. What device width is needed to ensure that the minimum available resistance is 1 kΩ? [06]

Question 3

(a) Explain the operation of pull – down Network constructed of NMOS transistors [05]
(b) Construct following gate circuits using NMOS and PMOS transistors
   a. Two-input NAND gate
   b. Two-input XOR gate
   c. Two-input NOR gate

(c) [12]

A CMOS inverter for which $k_n = 10k_p = 100\ \mu A/V^2$ and V_t = 0.5 V is connected as shown in Figure Q3.1to a sinusoidal signal source having a Thévenin equivalent voltage of 0.1-V peak amplitude and resistance of 100 kΩ. What signal voltage appears at node A,

a. With v_I = +1.5 V?
b. With v_I = −1.5 V?

[08]

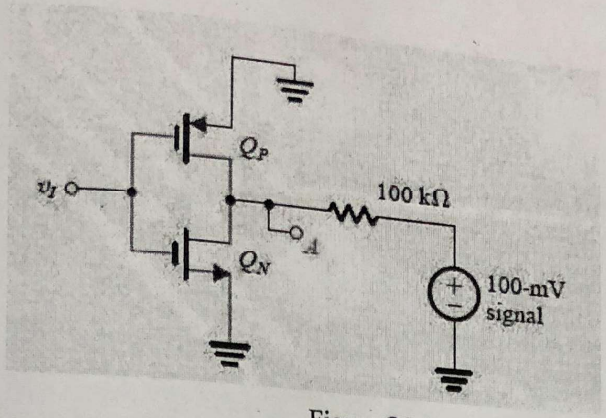

Figure Q3.1

Question 4

The semiconductor manufacturing process consist of main four steps

(a) Explain the main steps in silicon manufacturing [08]

(b) What is Photolithography [05]

(c) What is Photo mask and explain the arrangement of a projection exposure method. [06]

(d) Write short note on two topics listed below

a. Ion Implantation

b. Local Oxidation

[06]

End of question paper