EE1212-

Electronic System I

Lecture 2 - Combinational Logic

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Magnitude Comparator

- Output should provide whether two numbers are greater than, less than, or equal.
- The circuit for comparing two n-bit numbers has 2^n inputs and 3 outputs and 2^{2n} entries in the truth table.
- Consider two numbers

  $A = A_3A_2A_1A_0$

  $B = B_3B_2B_1B_0$

Condition for two numbers to be same?

Magnitude Comparator

Let $x_i = A_i B_i + A'_i B'_i$

- A = B

$$(x_3\ x_2\ x_1\ x_0) = 1$$

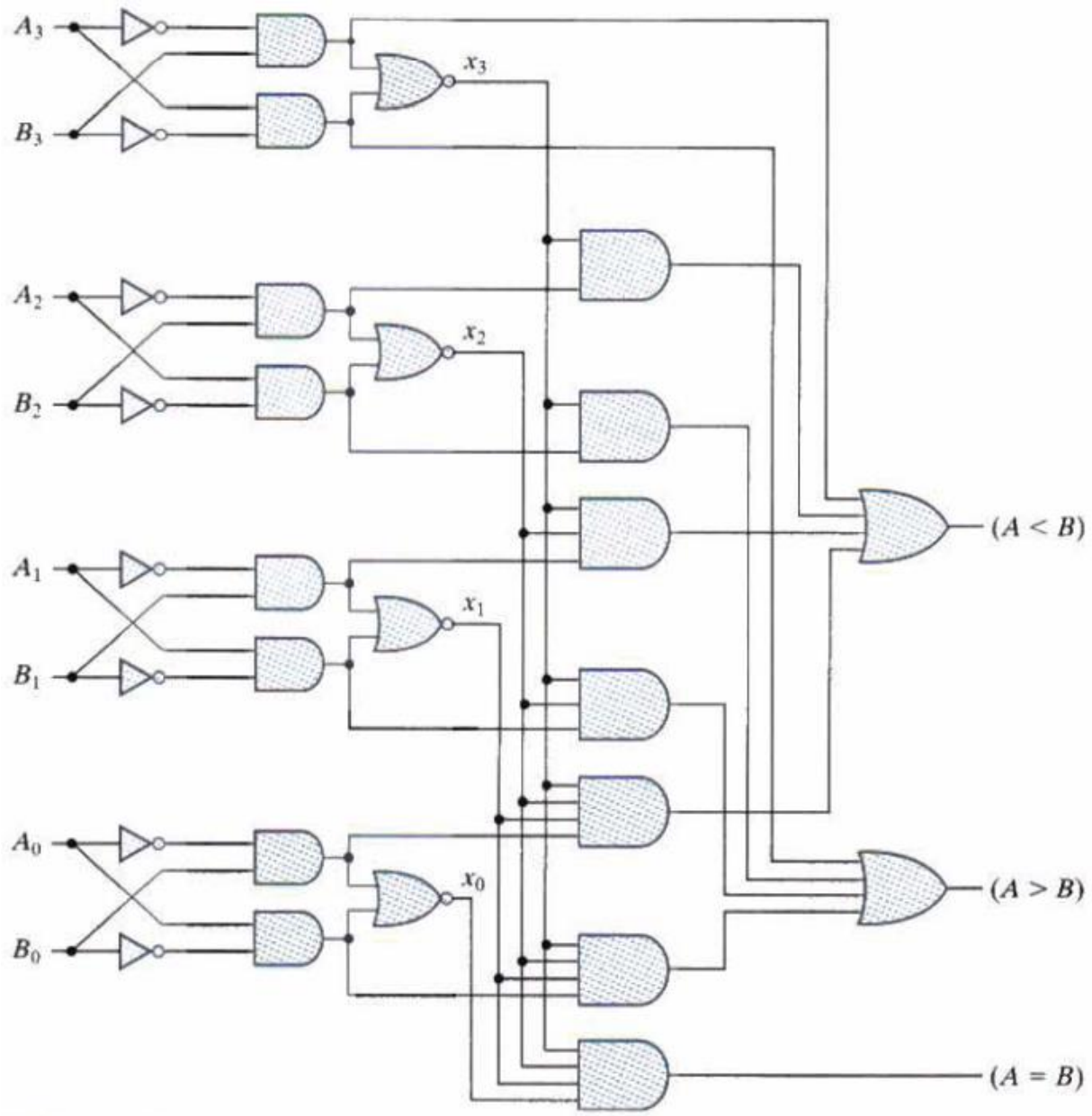
- A > B

$$A_3 B'_3 + x_3 A_2 B'_2 + x_3 x_2 A_1 B'_1 + x_3 x_2 x_1 A_0 B'_0 = 1$$

- A < B

$$A_3' B_3 + x_3 A_2' B_2 + x_3 x_2 A_1' B_1 + x_3 x_2 x_1 A_0' B_0 = 1$$

4-bit Magnitude Comparator



Decoders

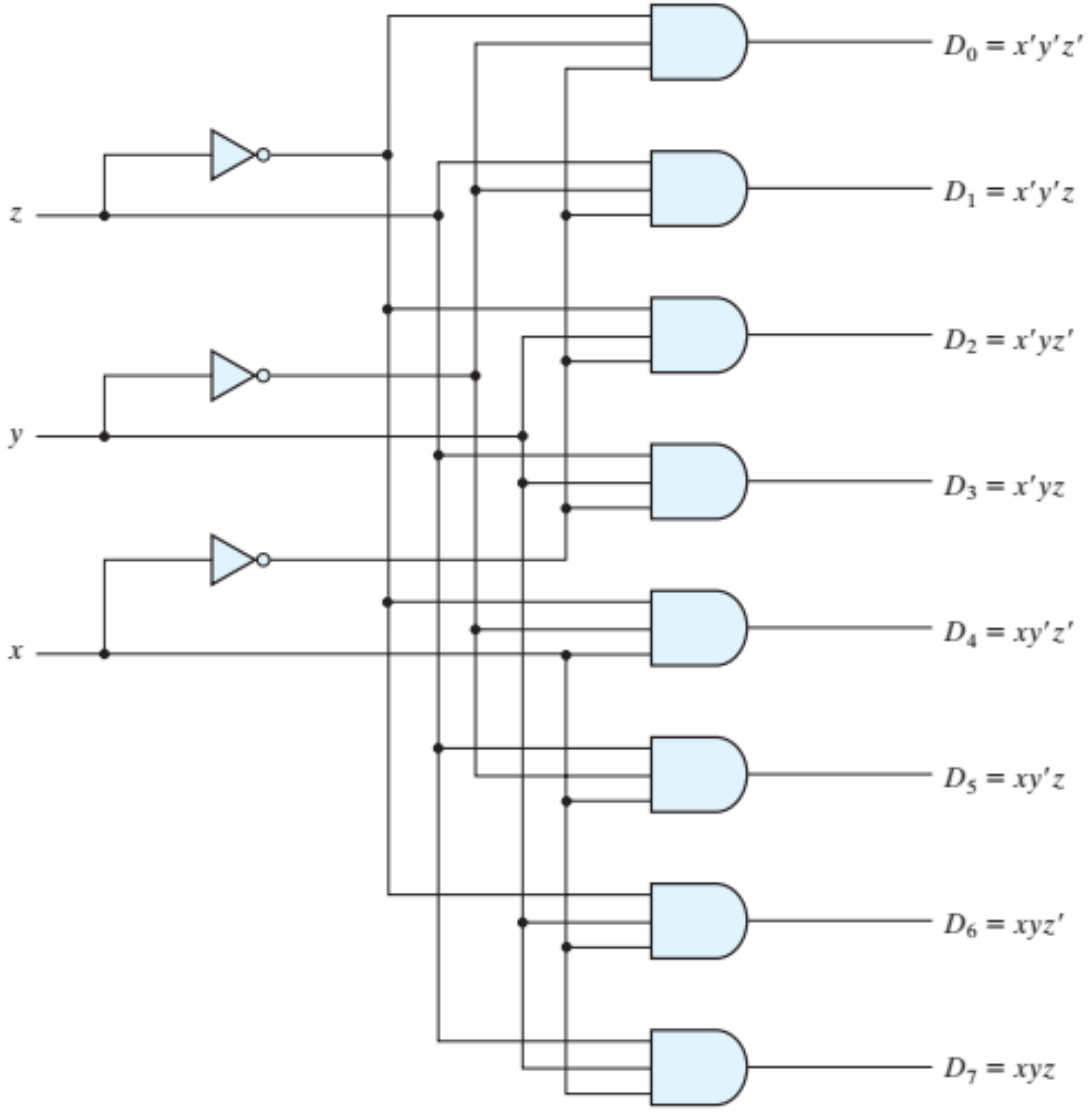
- A binary code of n bits is capable of representing upto 2^n distinct elements of coded information.
- A decoder is a combinational circuit that converts binary information from n inputs to a maximum of 2^n unique output lines.
- Example:
    - 3-to-8 line decoder circuit. Three inputs are decoded into eight outputs.
- Application:
    - Code conversion (Binary to Octal conversion).

Truth Table of a Three-to-Eight-Line Decoder

Inputs			Outputs							
x	y	z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Output of 2 bit Decoder

- If the input lines are A & B,
- $m_0 = \bar{A}\bar{B}$
- $m_1 = \bar{A}B$
- $m_2 = A\bar{B}$
- $m_3 = AB$



3 bit Decoder

Combinational Logic Implementation

- A decoder provides 2^n minterm of n input variables.
- Since any Boolean function can be expressed in sum of minterms, decoder can be used to generate sum of min terms and OR gate can be used to obtain the summation of minterms.

Combinational Logic Implementation

- Example

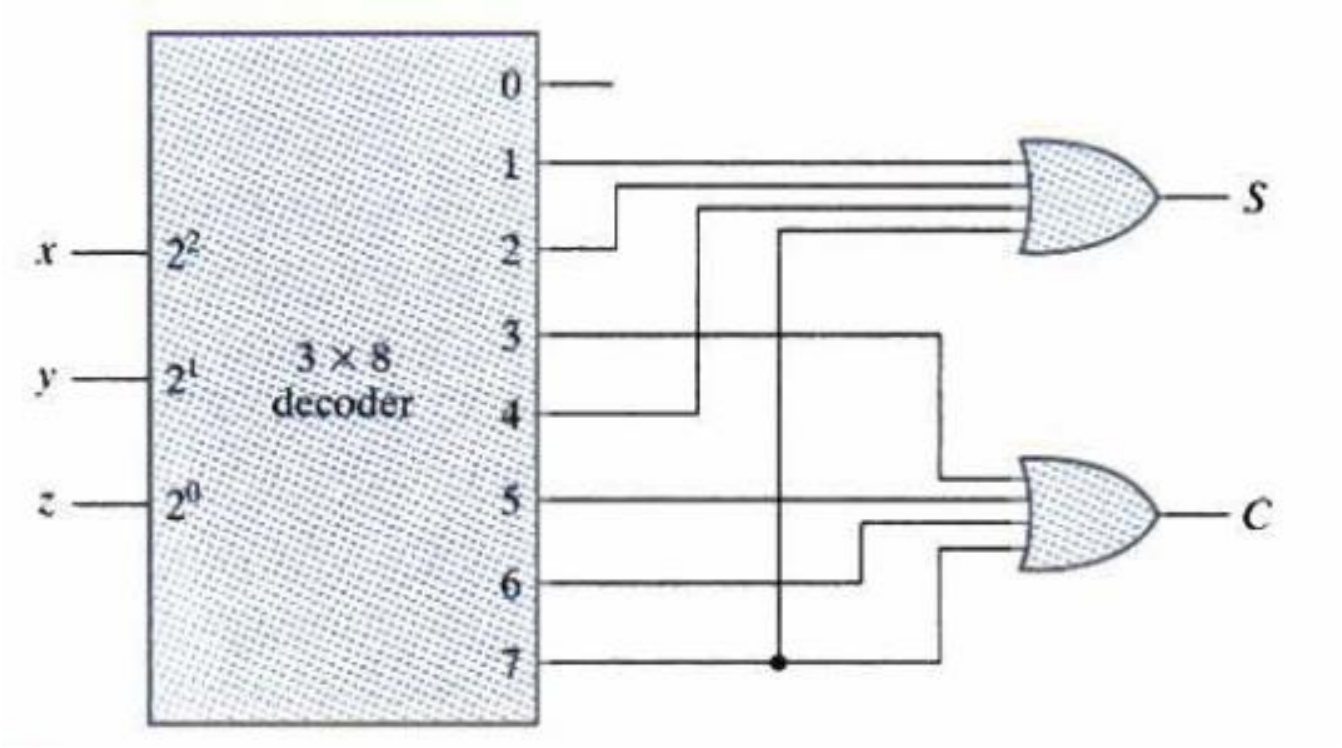
x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$S(x, y, z) = \sum(1,2,4,7)$$

$$C(x, y, z) = \sum(3,5,6,7)$$

Combinational Logic Implementation

- Example



Encoders

- An encoder is a digital circuit that performs the inverse operation of decoder.
- Example of encoder is octal-to-binary encoder.

Truth Table of an Octal-to-Binary Encoder

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	x	y	z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Encoders

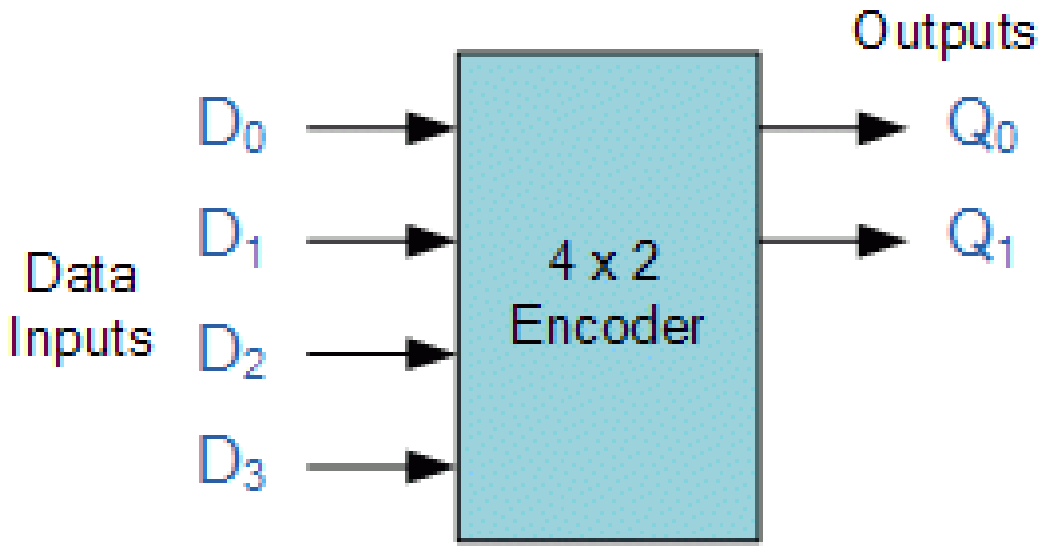
Truth Table of an Octal-to-Binary Encoder

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	x	y	z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

$$x = D4 + D5 + D6 + D7$$
$$y = D2 + D3 + D6 + D7$$
$$z = D1 + D3 + D5 + D7$$

- The encoder can be implemented by three OR gates

4 to 2 Encoder



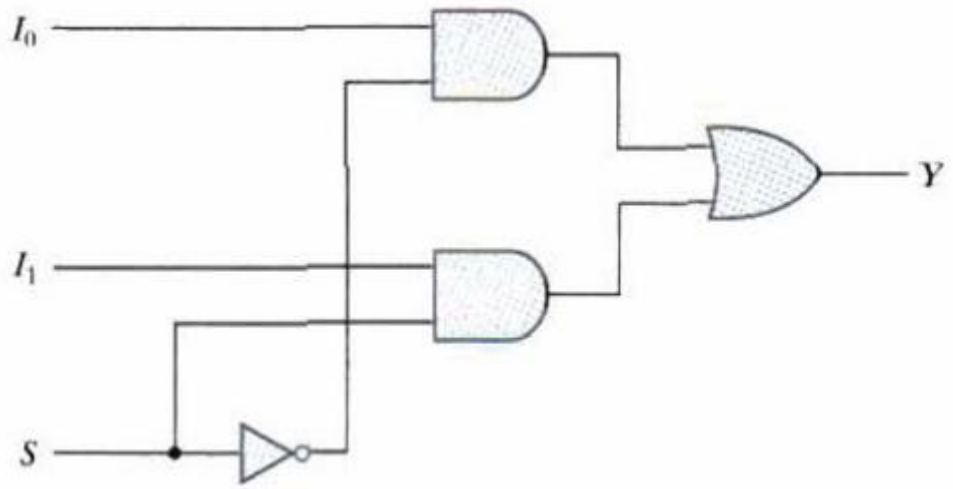
Multiplexers

- A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line.
- The selection of a particular input line is controlled by a set of selection lines.
- There are 2^n input lines and n selection lines whose bit combinations determine which input to be selected

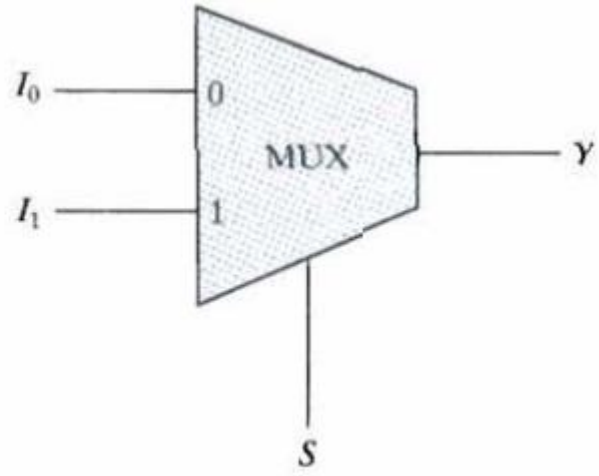
2-to-1 line Multiplexer

- Example:
- A 2-to-1 line multiplexer.

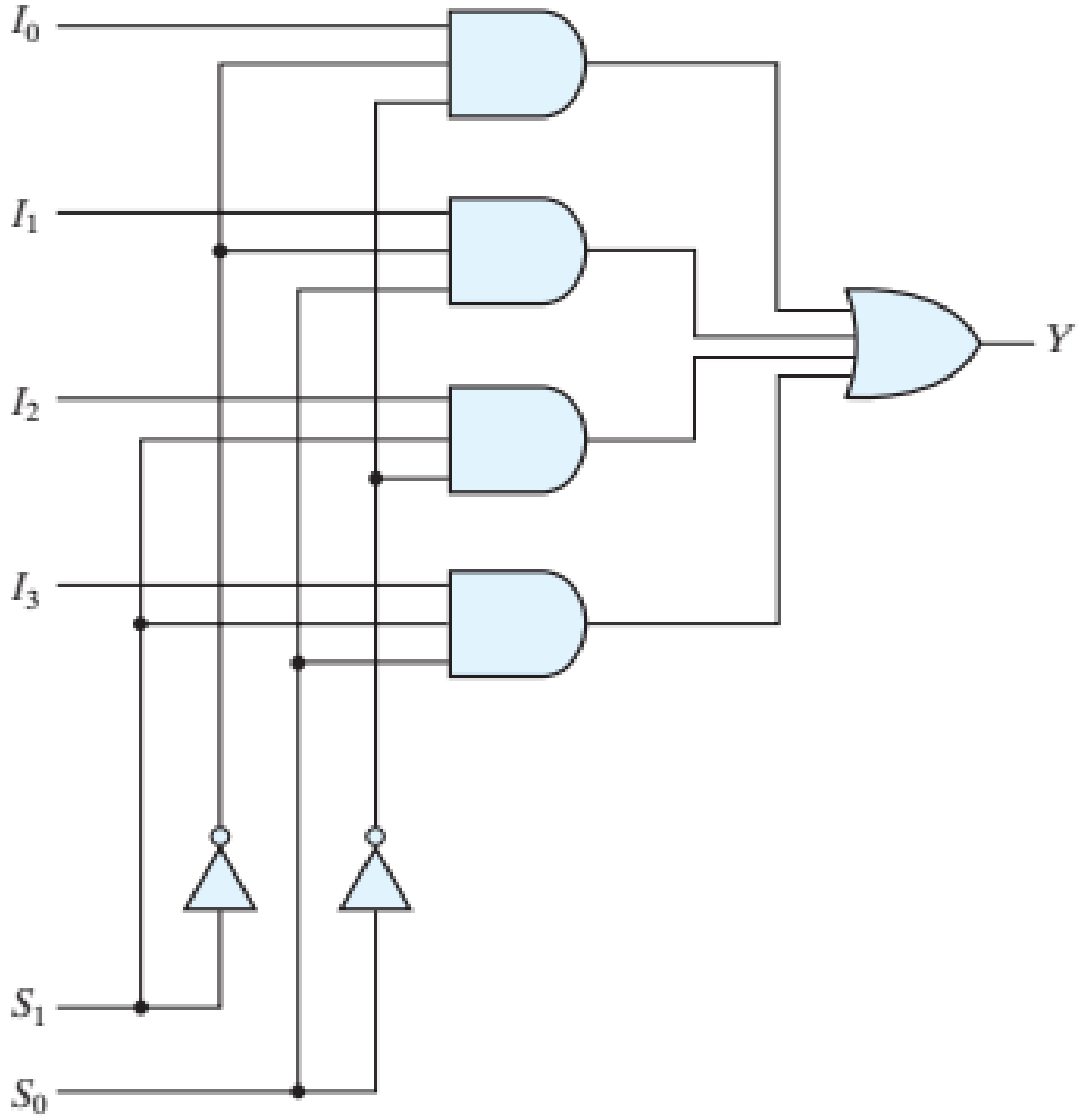
When S = 0, the upper AND gate is enabled and when S=1, the lower AND gate is enabled.



(a) Logic diagram



(b) Block diagram



(a) Logic diagram

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

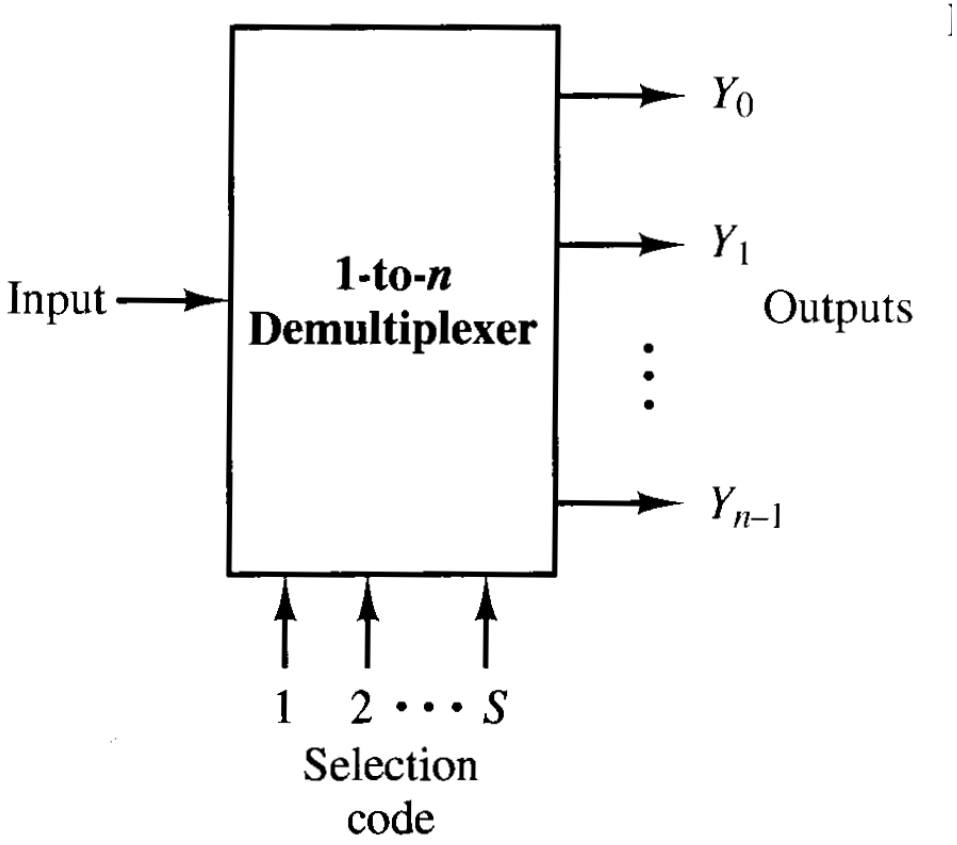
(b) Function table

Four-to-one-line multiplexer

Demultiplexer

- Demultiplexer is a circuit that receives information from a single line and direct it to one of 2^n possible output line.
- The selection of a specified output is controlled by the bit combination of n selection lines.

Functional diagram of demultiplexer



1-4 Demultiplexer