GENERAL SIR JOHN KOTELAWALA DEFENCE UNIVERSITY

Faculty of Engineering

Department of Electrical, Electronic and Telecommunication Engineering

B.Sc. Engineering Degree

Semester 6 Examination – January 2021

(Intake 35 - EE/ET/MC)

EE 3223 – POWER ELECTRONICS AND APPLICATIONS I

Time allowed: 3 Hours 02 February 2021

INSTRUCTIONS TO CANDIDATES:

This paper contains 6 questions on 5 pages.
Answer any FIVE Questions only.
This is a closed book examination.

This examination accounts for 80% of the module assessment. The total maximum mark attainable is 100. The marks assigned for each question & sections thereof are indicated in square brackets.

If you have any doubt as to the interpretation of the wording of a question, make your own decision, but clearly state it on the script.

All Examinations are conducted under the rules & regulations of the University

Question 1

a) (i) Describe briefly the strengths and weaknesses of the thyristor as a power switching device. [03]

(ii) Why is the IGBT popular in most of the present day power switching applications? [03]

(iii) How do you compare IGBT with Power MOSFET? [03]

b) An IGBT in a certain converter is required to switch inductive load current of 20A at 10 kHz with a maximum switching duty factor of 0.9. Converter voltage is 500V DC. The following data are available for the IGBT in this application:

Conduction voltage drop	=	1.8 V
Turn on transient time	=	0.2 μs
Turn off transient time	=	0.8 μs
Junction-to-Case thermal resistance	=	0.4 °C/W
Case-to-sink contact thermal resistance	=	0.1 °C/W
Ambient temperature	=	35 °C
Specified maximum junction temperature	=	135°C

(i) Determine the thermal resistance of the required heat sink. [08]

(ii) What is the Case temperature of the IGBT for the heat sink in (i) above? [03]

Question 2

a) Figure Q2 shows a linear DC power supply based on a single-phase bridge-rectifier with capacitor filter.

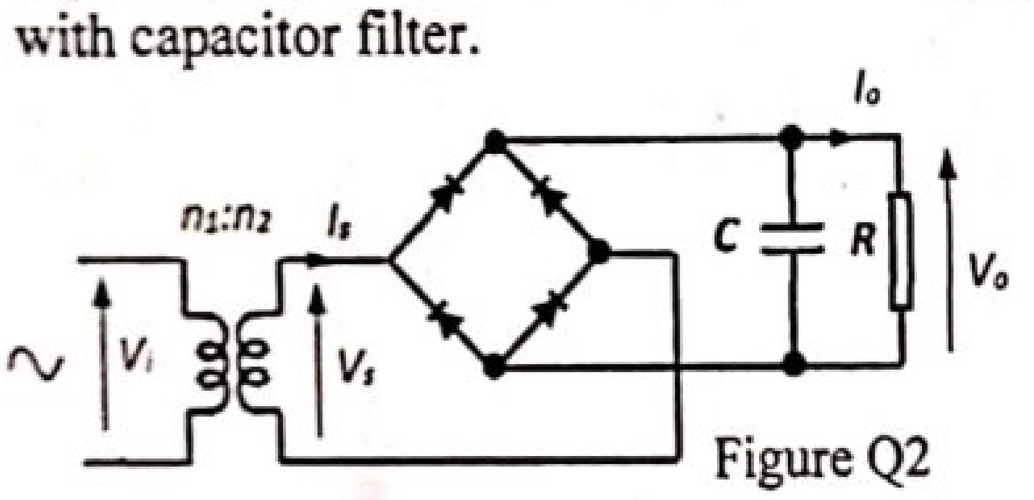
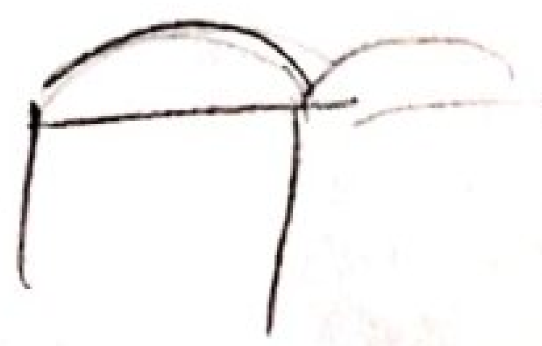


Figure Q2

$R = 15\ \Omega$
$C = 6000\ \mu F$
$n_1{:}n_2 = 18{:}1$
$V_i = 230$ V (rms)
$f = 50$ Hz
$V_D = 0.7V$ (diode conduction voltage drop)



Estimate,

(i) Mean value of output voltage V_o. [04] 15.79

(ii) Peak-peak ripple in output voltage. [02] ~~45.572~~ 3.158V

(iii) Peak value of diode current. [04] 19.014

b) A three phase full-bridge diode-converter is operating on 400 V, 50 Hz, three phase AC supply. It delivers 6 kW of power to an inductive load. Assume that the output current is continuous and having negligible ripple.

Determine,

(i) Mean value of output DC voltage. [04] 541.59

(ii) Peak-peak ripple in output voltage [02] 75.78

(iii) RMS value of the fundamental component of line current at the input. [04]

Question 3

a) A three phase full-bridge thyristor converter is operating on 400 V, 50 Hz, three phase AC supply. It delivers 9 kW of power to an inductive load at 380 V DC (mean). Supply side inductance is 3 mH per phase. You may assume that the output current is continuous and ripple free.

Calculate,

(i) Delay (firing) angle. 46.68° [04]

(ii) Conduction overlap angle. 7.006° [04]

(iii) RMS value of the fundamental component of input line current. [04]

18.426A

b) For the converter in (a) above, sketch the following waveforms indicating appropriate values.

(i) Output voltage. [04]

(ii) One of the line-line voltage waveforms at the converter input (PCC). [04]

Question 4

a) Unipolar, sinusoidal PWM control with carrier-ratio 54, depth of modulation 0.8 and reference frequency 50 Hz is applied on a single-phase VSI, which is fed at 300 V DC input.

(i) Sketch the arrangement of the PWM modulator. [03]

(ii) Determine the RMS value of the fundamental component of output voltage. [03]

-3 (iii) What is the lowest order significant harmonic present in the output voltage? [03] 107th

(iv) What is the switching frequency? 2700 Hz [02]

b) Regular sampled PWM control is applied on a three-phase VSI with a depth of modulation 0.65, carrier ratio 75, and reference frequency 50 Hz. Calculate the timing of switching signals S_a, S_b & S_c over the sampling-period following the 40[th] sampling instant. Take the 0[th] sampling point to coincide with a positive-going zero-crossing of phase-A reference signal. [09]

Question 5

a) A single-phase VSI with input DC voltage V_d is delivering an output current $I_m \sin(\omega t)$ using hysteresis current control within a tolerance band ΔH. The load comprises a resistance R and inductance L in series. Derive expressions for the maximum and the minimum switching frequencies during one cycle of output current. Assume the maximum and the minimum switching frequencies to occur at the zero-crossing and the peak, respectively, of the reference current. [10]

b) Voltage vector PWM is applied on a three-phase VSI at a sampling frequency 5 kHz, to deliver 50 Hz fundamental output voltage. Input voltage to the inverter is 750 V DC. Determine the timing for switching signals S_a, S_b & S_c over the sampling interval when the sampled values of desired voltages V_a, V_b & V_c for three phases are −400 V 250 V and 150 V respectively. [10]

Question 6

a) Three-phase VSI shown in Figure Q6(a) is controlled using sinusoidal PWM to deliver a specified combination of real-power (P) and reactive-power (Q) to the grid. Three-phase reference signals for the PWM modulator are derived through vector control and Figure Q6(b) shows inverter voltage vector $\overline{V}_I$, inverter current vector $\overline{I}$ and the grid-voltage vector $\overline{V}_G$. Synchronously rotating d-axis is chosen to coincide with the direction of $\overline{V}_G$ and the d & q components of different vectors are as shown in the Figure.

(i) State magnitude V_{gd} of the grid-voltage vector in terms of the grid line-voltage RMS value V_L. [02]

$\frac{\sqrt{6}\,V_L}{2}$

(ii) Give the set values $(I_d)_{SET}$ and $(I_q)_{SET}$ in terms of P, Q and V_L. [04]

(iii) Show that,

$$V_{id} = L\frac{dI_d}{dt} - \omega L I_q + V_{gd}$$
$$V_{iq} = L\frac{dI_q}{dt} + \omega L I_d$$

Where, ω is angular frequency of grid voltage and L is inductance per phase of the interconnection. [07]

b) Draw a block diagram to show how the three-phase reference signals for the sinusoidal PWM modulator are generated using the inputs of $(I_d)_{SET}$, $(I_q)_{SET}$ and feedback grid voltages v_{ga}, v_{gb} and v_{gc}. [07]

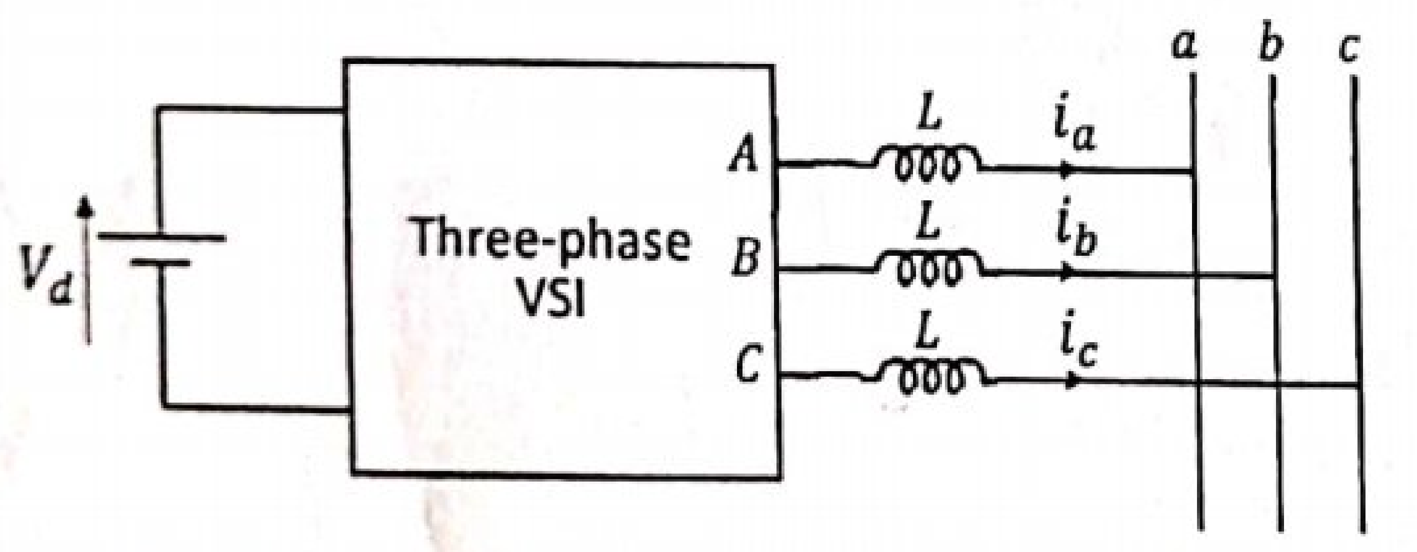


Fig. Q6(a)

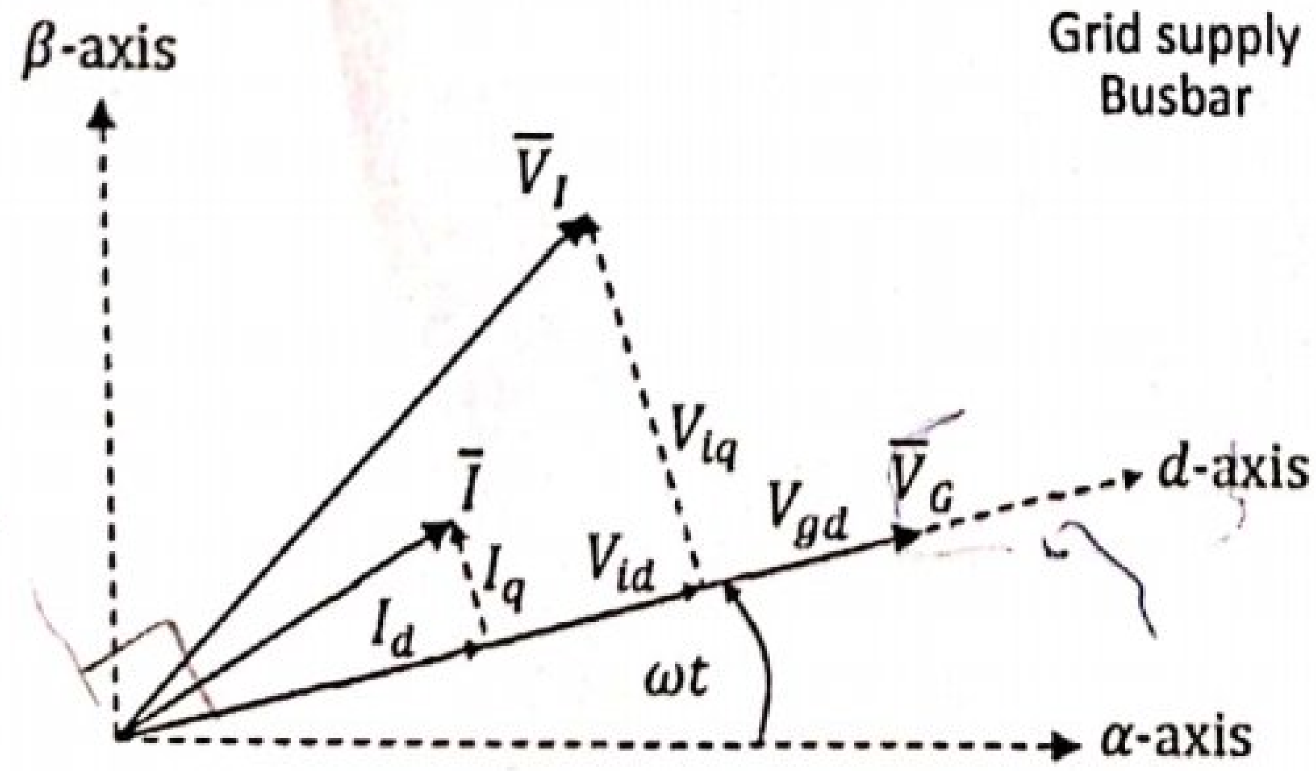


Fig. Q6(b)

9
5
14

$\frac{86 \times 80}{100} =$

68.8
15
83.8 %

End of Question Paper