



GENERAL SIR JOHN KOTELAWALA DEFENCE UNIVERSITY
Faculty of Engineering
Department of Electrical, Electronic and Telecommunication Engineering

BSc Engineering Degree
Semester 4 Examination – November 2017
(Intake 33 - ET)

ET4082 – SEMICONDUCTOR AND SOLID STATE DEVICES

Time allowed: 2 hours

30th November, 2017

INSTRUCTIONS TO CANDIDATES

This paper contains 4 questions on 5 pages

Answer all **FOUR** questions

This is a closed book examination

This examination accounts for 70% of the module assessment. A total maximum mark obtainable is 100. The marks assigned for each question and parts thereof are indicated in square brackets

If you have any doubt as to the interpretation of the wordings of a question, make your own decision, but clearly state it on the script

Assume reasonable values for any data not given in or provided with the question paper, clearly make such assumptions made in the script

All examinations are conducted under the rules and regulations of the KDU

This Page is Intentionally Left Blank

Useful Formulas

$$C_{OX} = \frac{\epsilon_{OX}}{t_{OX}}$$

$$k'_n = \mu_n C_{OX}$$

$$i_D = \frac{1}{2} k'_n \frac{W}{L} V_{OV}^2$$

$$r_{DS} = \frac{1}{k'_n \frac{W}{L} (V_{GS} - V_t)}$$

$$V_{IL} = V_t + \frac{V_{DD} - V_t}{\sqrt{r(r+1)}}$$

$$V_{OL} = (V_{DD} - V_t) \left[1 - \sqrt{1 - \frac{1}{r}} \right]$$

Question 1

Solids materials are classified in to three types atomic structure.

- a. Explain the atomic structures of crystalline and polycrystalline types. [04]
- b. Using the band theory, explain the difference in conductivity of semiconductors and conductors [06]
- c. Explain how to increase conductivity by doping [07]
- d. Explain the Fermi Level arrangement and Band Structure of forward biased p-n Junction [08]

Question 2

- a. A circuit designer intending to operate a MOSFET in saturation region by considering the effect of changing the device dimensions and operating voltages on the drain current. Explain, what factor does change, in each of the following cases.
 - i. The channel length is doubled.
 - ii. The channel width is doubled.
 - iii. The overdrive voltage is doubled. [15]

- b. A process technology which $L_{min} = 0.18\mu m$ (0.18- μm fabrication process) is specified to have $t_{ox} = 4nm$, $\mu_n = 450cm^2/V.s$, and $V_t = 0.5V$. ($\epsilon_{ox} = 3.45 \times 10^{-11} F/m$)
- Find the value of the process transconductance parameter (K'). [04]
 - For a MOSFET with minimum length fabricated in this process, find the required value of W so that the device exhibits a channel resistance r_{DS} of $1k\Omega$ at $V_{GS} = 1V$. [06]

Question 3

- Explain the operation of pull – up Network constructed using of PMOS transistors [04]
- Explain the operation of circuit diagram in Figure Q3.1. [06]

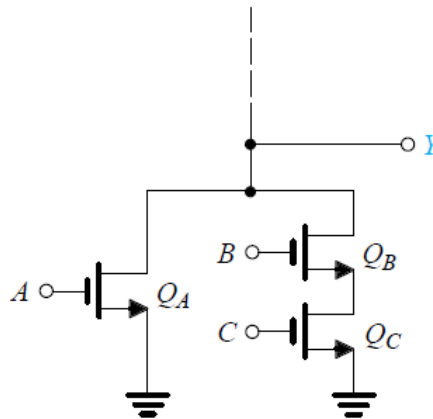


Figure Q3.1

- Consider a pseudo-NMOS inverter fabricated in a 0.25- μm CMOS technology for which $\mu_n C_{ox} = 115\mu A/V^2$, $\mu_p C_{ox} = 30\mu A/V^2$, $V_{tn} = -V_{tp} = 0.5V$ and $V_{DD} = 25V$. Let the (W/L) ratio of Q_N be $(0.375\mu m/0.25\mu m)$ and $r = 9$. Find
 - V_{OH}, V_{OL}, V_{IL} [15]

Question 4

The silicon manufacturing process is one of main step in semiconductor manufacturing.

- a. Explain the process of wafer manufacturing. [04]
- b. Explain the main steps in photolithography. [05]
- c. Discuss advantages and disadvantages of dry oxide used in oxidation of silicon. [05]
- d. Explain the process of wet chemical etching. [05]
- e. Compare the advantage of “*ion implantation*” for improving performance of MOS transistors. [06]

End of question paper