GENERAL SIR JOHN KOTELAWALA DEFENCE UNIVERSITY

Faculty of Engineering

Department of Electrical, Electronic and Telecommunication Engineering

BSc Engineering Degree

Semester 2 Examination – November/December 2022

(Intake 39 – EE/ ET)

EE1212 - ELECTRONIC SYSTEMS I

Time allowed: 2 hours 02nd December 2022

ADDITIONAL MATERIAL PROVIDED

Nil

INSTRUCTIONS TO CANDIDATES

This paper contains 4 questions on 6 pages.

Answer ALL questions.

This is a closed book examination.

This examination accounts for 70% of the module assessment. A total maximum mark obtainable is 100. The marks assigned for each questions and parts thereof are indicated in brackets.

If you have any doubt as to the interpretation of the wordings of a question, make your own decision, but clearly state it on the script.

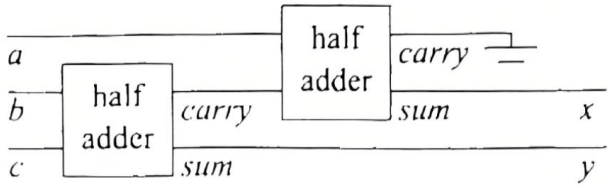
Assume any reasonable values for any data not given in or provided with the question paper, clearly make such assumptions made in the script.

All examinations are conducted under the rules and regulations of the KDU.

Question 01

a) (i) Derive two truth tables illustrating the outputs of a half-adder, one table for the *sum* output and the other for the *carry* output. (2 marks)

(ii) Determine the outputs x and y of the circuit in Figure Q1.1and fill in the truth table at right. Ignore rows not included in the table. (4 marks)



a	b	c	x	y
0	1	1		
1	0	1		
1	1	0		
1	1	1		

Figure Q1.1

b) Answer the following questions based on encoders and decoders;

(i) Determine the number of inputs and outputs needed to encode all decimal digits in binary? (2 marks)

(ii) Determine the number of inputs needed to encode only odd decimal digits? (1 mark)

(iii) State the number of inputs and outputs a BCD-to-Decimal decoder have? (2 marks)

(iv) If a decoder has 6 inputs, determine the number of outputs is it expected to have? (1 mark)

(v) Given that the input of such a decoder in (iv) is 101011, What will be the decoded decimal number? (2 marks)

c) Design a combinational logic circuit that can add 2 binary numbers with 2 bits each (5 marks)

d) Implement the three-variable Boolean function $F(A,B,C) = \bar{A}.C + A.\bar{B}.C + A.B.\bar{C}$ using (6 marks)

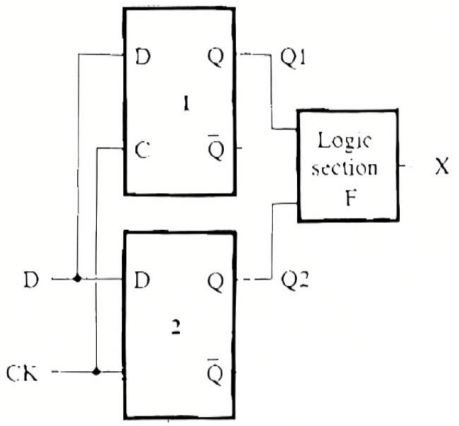
(i) 8-to-1 multiplexer

(ii) 4-to-1 multiplexer

Question 02

a) Explain the difference between a combinational logic circuit and a sequential logic circuit. (4 marks)

b) Complete the timing diagram - signals Q1 and Q2 in Figure Q2.1 and determine the logic function F and suggest how it can be implemented. (10 marks)



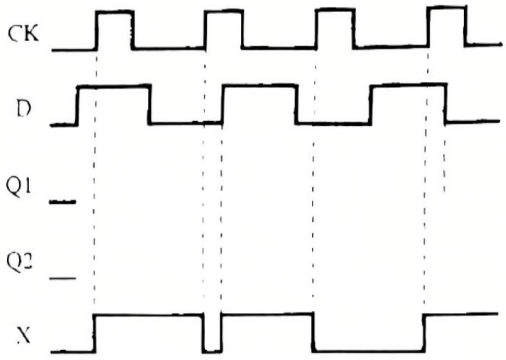


Figure Q2.1

c) With the help of a schematic arrangement, explain how a J-K flip-flop can be used as a

(i) D flip-flop (3 marks)

(ii) T flip-flop (3 marks)

d) Briefly describe the operational aspects of bistable, monostable and astable multivibrators. Which multivibrator closely resembles a flip-flop? (5 marks)

Question 03

a) Consider the logic circuit of the counter shown in Figure Q3.1 and answer followings;

(i) Determine the logic equations for the inputs of each flip-flop. (5 marks)

(ii) Determine the timing diagram for the counter assuming that all the flip-fops are initially reset to 0. (5 marks)

(iii) Determine the state diagram for the counter. (3 marks)

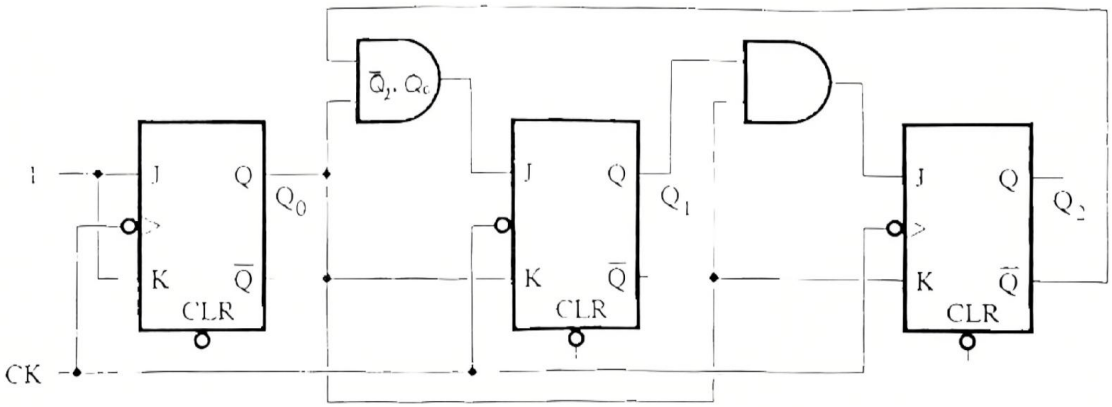


Figure Q3.1

(iv) Following is a truth table of a three-input, four-output, combinational circuit. Implement the circuit using a PAL and mark the fuse map in the diagram. (12 marks)

Inputs			*Outputs*			
X	*Y*	*Z*	*A*	*B*	*C*	*D*
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

Question 04

(a) (i) Identify the diode logic, represented in Figure Q4.1 and draw truth tables for positive logic and negative logic. (3 marks)

(ii) Define the logic gate type for each truth table, by considering logic states. (2 marks)

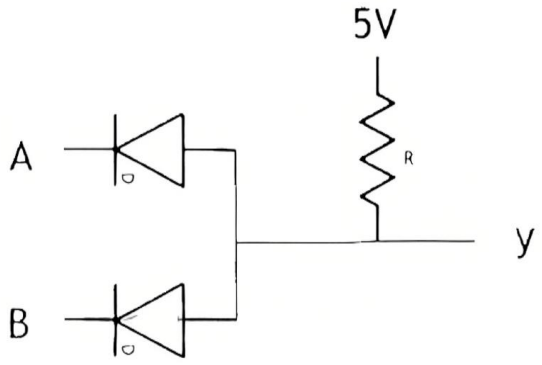


Figure Q4.1

(b) Describe the characteristics and advantages of CMOS logic. (4 marks)

(c) Categorize the type of oscillators and explain the advantages of Crystal Oscillators. (4 marks)

(d) A 1 pF capacitor is available. Choose the inductor values in a Hartley oscillator so that f = 1 MHz and m_v = 0.2. (m_v is feedback fraction which is equals to L1/L2) (4 marks)

f) State the topologies of Feedback Amplifiers (4 marks)

g) The open-loop gain of an amplifier is A=50, and the feedback factor is β = 50. If the open- loop gain A changes by -20% and the feedback factor β changes by +15%, determine the closed- loop gain A_f. (4 marks)

End of the Question Paper