Register Transfer Level (RTL) Design

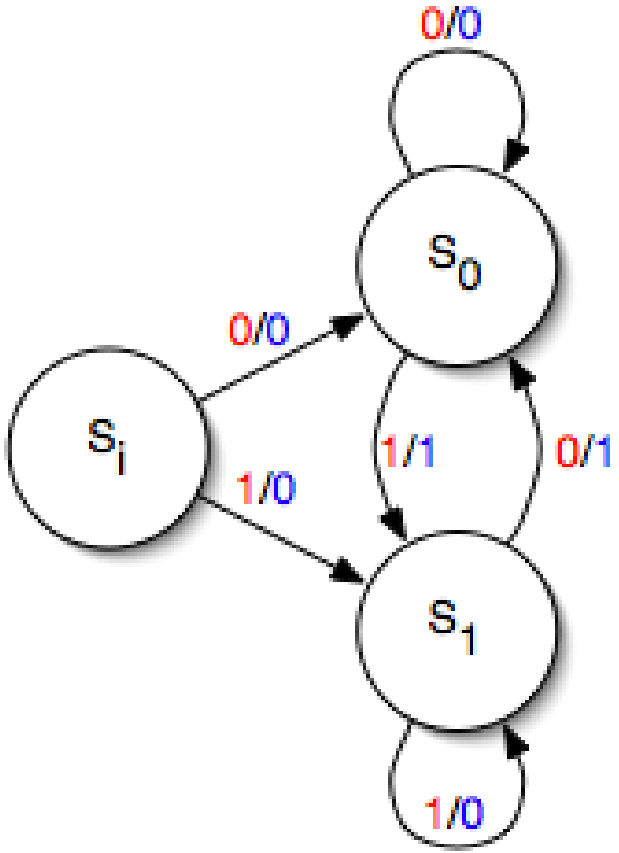
Lecture Outline

1. Finite State Machines
2. Datapath-Controller Architecture
3. Datapath Design
4. Behavioral Synthesis
5. Design Constrains in RTL
6. Controller Design

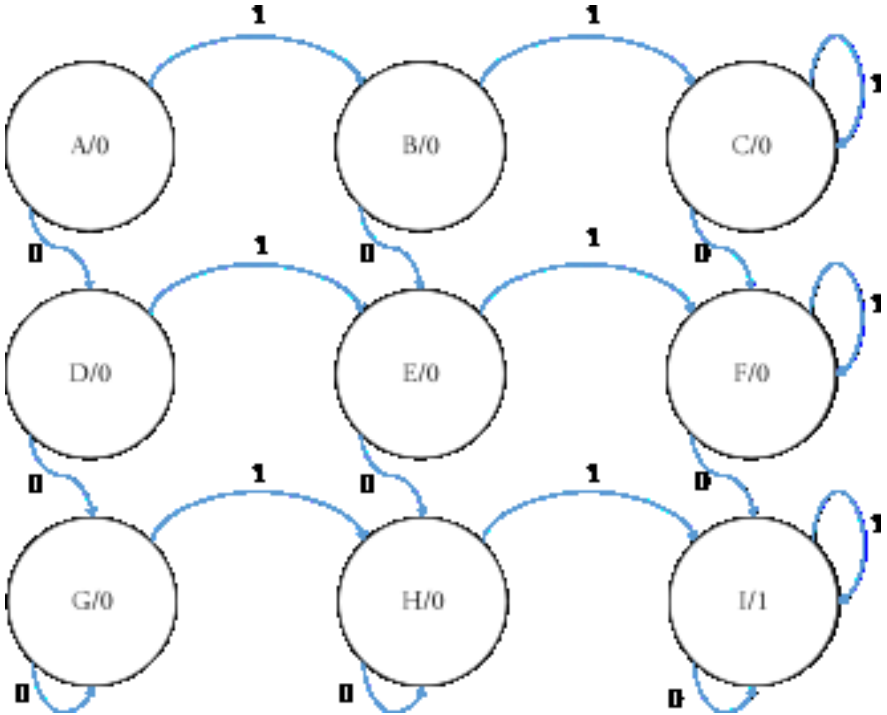
Finite State Machines

- Moore Machine
  - Moore machine is an FSM whose outputs depend on only the present state.
- Mealy Machine
  - A Mealy Machine is an FSM whose output depends on the present state as well as the present input.

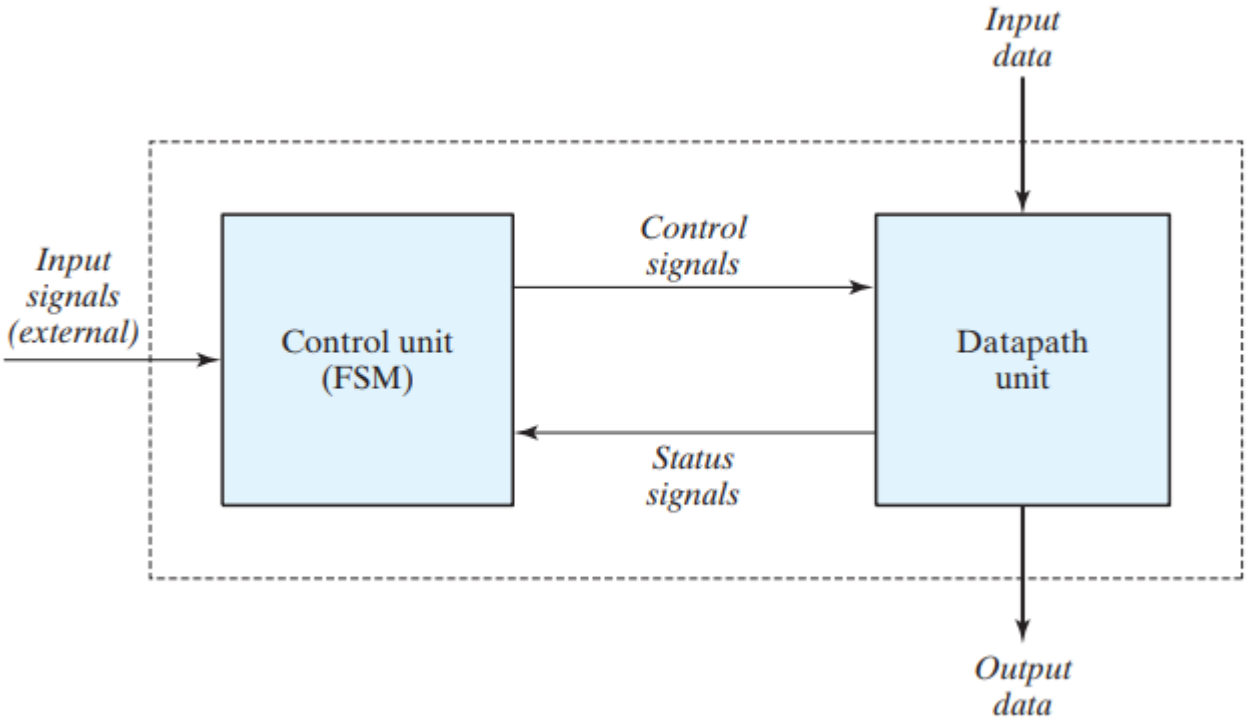
Mealy Machine



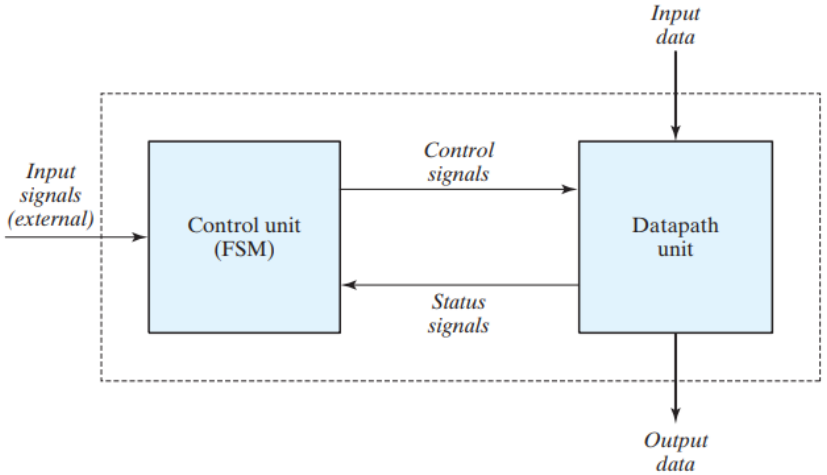
Moore Machine



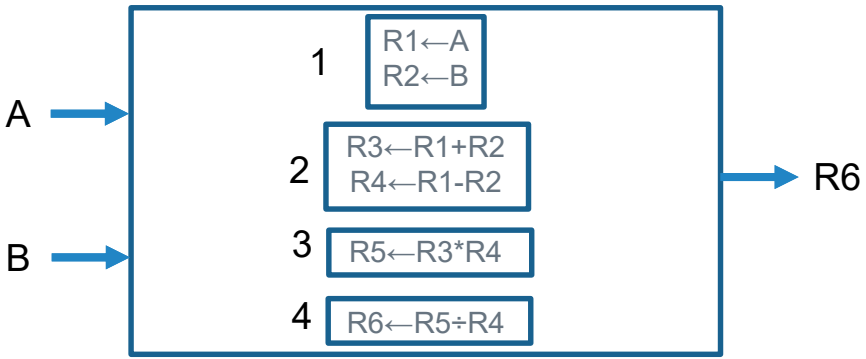
Datapath-Controller Architecture

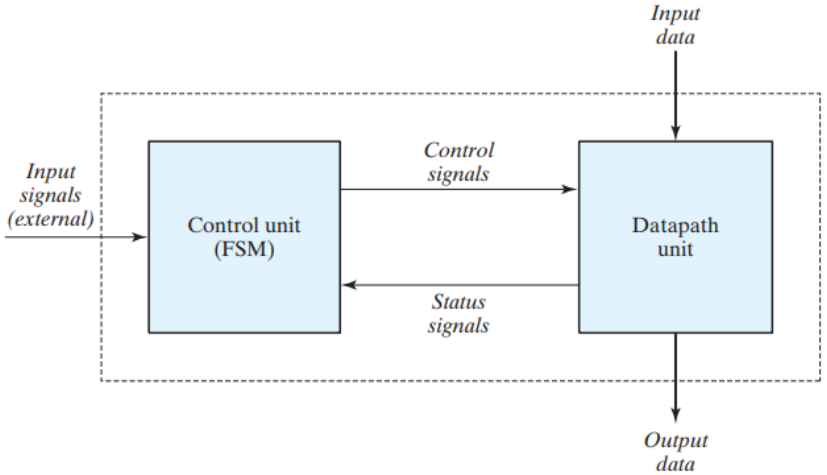


Datapath-Controller Architecture

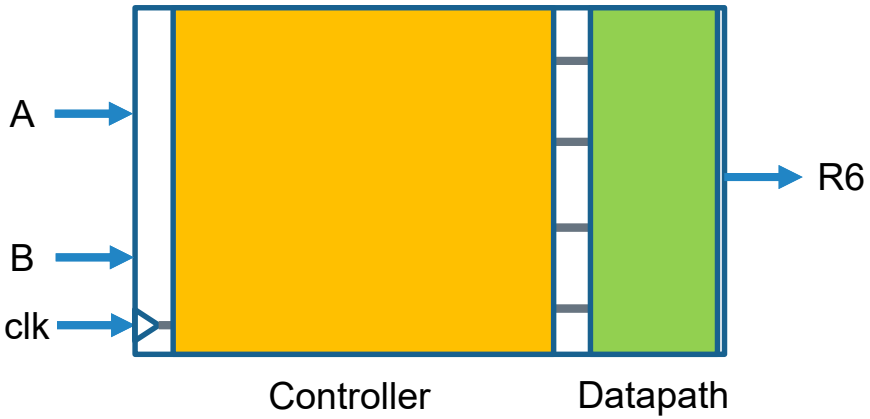


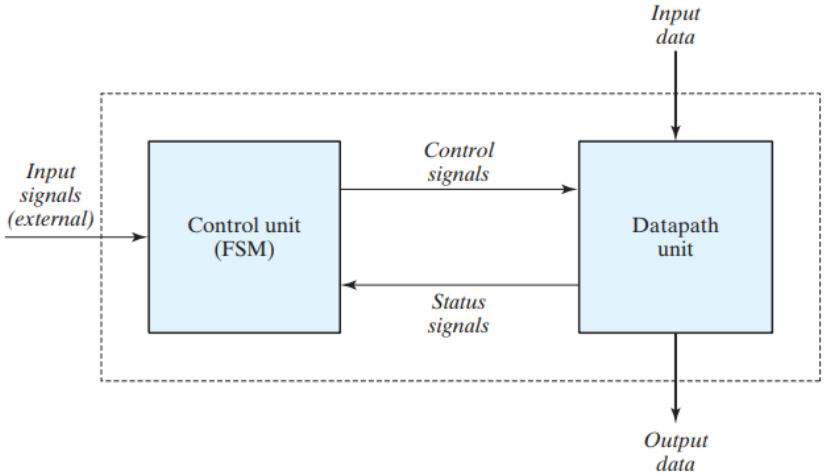
Datapath-Controller Architecture





Datapath-Controller Architecture



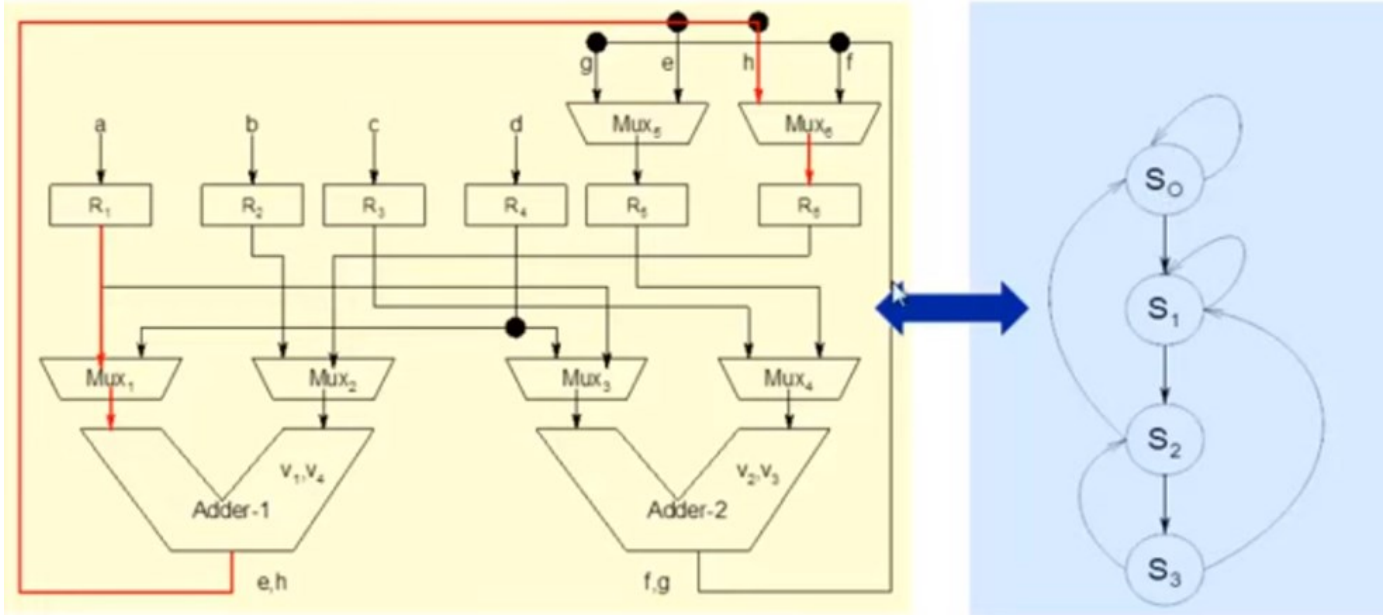


- Operations are typically carried out in a single clock cycle.

Datapath

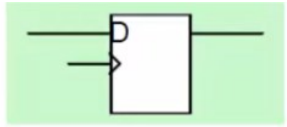
- A digital system is represented at the register transfer level (RTL) when it is specified by the following three components:
  - Storage Units (Registers)
  - Functional Units (Adders, Multipliers, …)
  - Interconnect Units (Mux, Bus, …)

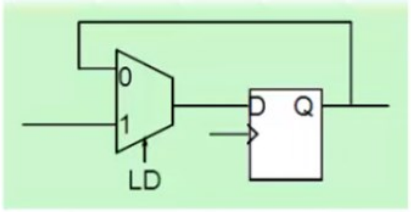
Datapath Example

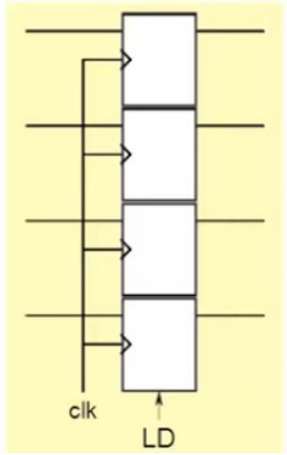


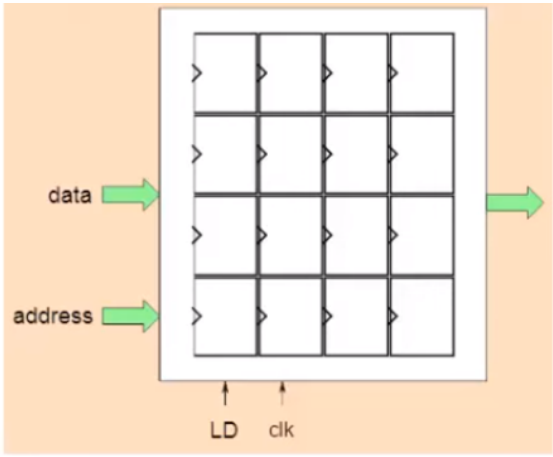
Storage Units (Registers)

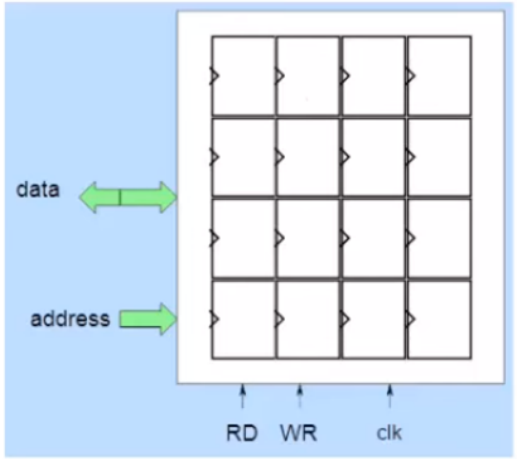
- The set of registers in the system.











Functional Units

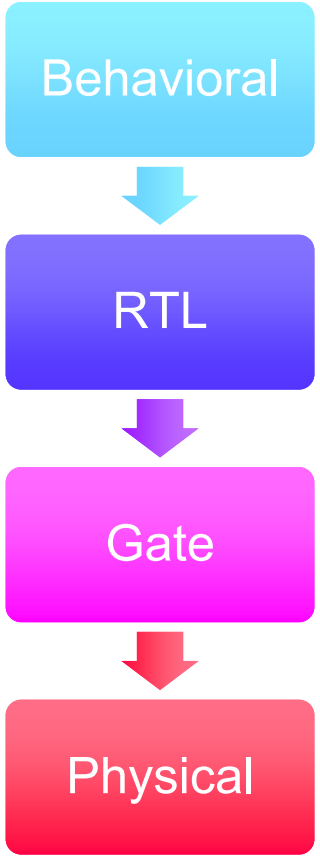
- The operations that are performed on the data stored in the registers.
- Arithmetic circuits such as adders etc.
- Could be any other combinational circuit which may serve a predefined function.

Interconnect Units

- The control that supervises the sequence of operations in the system.
- Multiplexers that controls data flow.
- A bus is a set of connections which carries data.

Levels of Abstraction in Digital Design

- Behavioral synthesis defines the RTL description.
- RTL synthesis defines the gate level design.
- Gate level designs are converted into physical systems. (Transistor Circuits)



Behavioral Synthesis

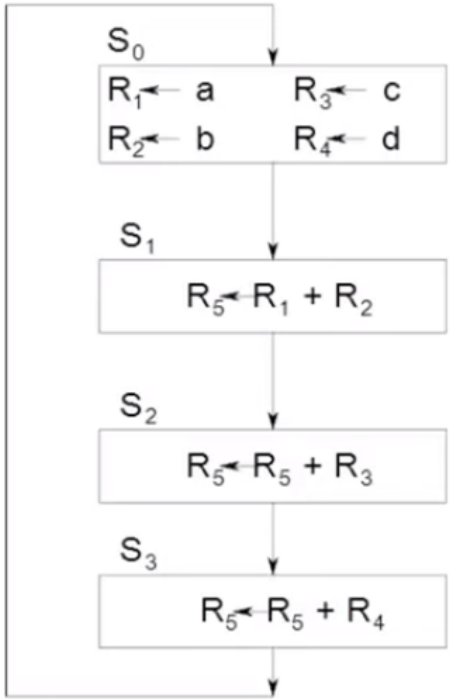
- Behavioral description is a high-level abstraction of the design.
- The process of converting a behavioral description to an RTL description involves in developing an **Algorithmic State Machine (ASM) Chart**.
- The ASM chart denotes the clock cycle by clock cycle implementation of the system.

Algorithmic State Machine (ASM) Chart

- Example

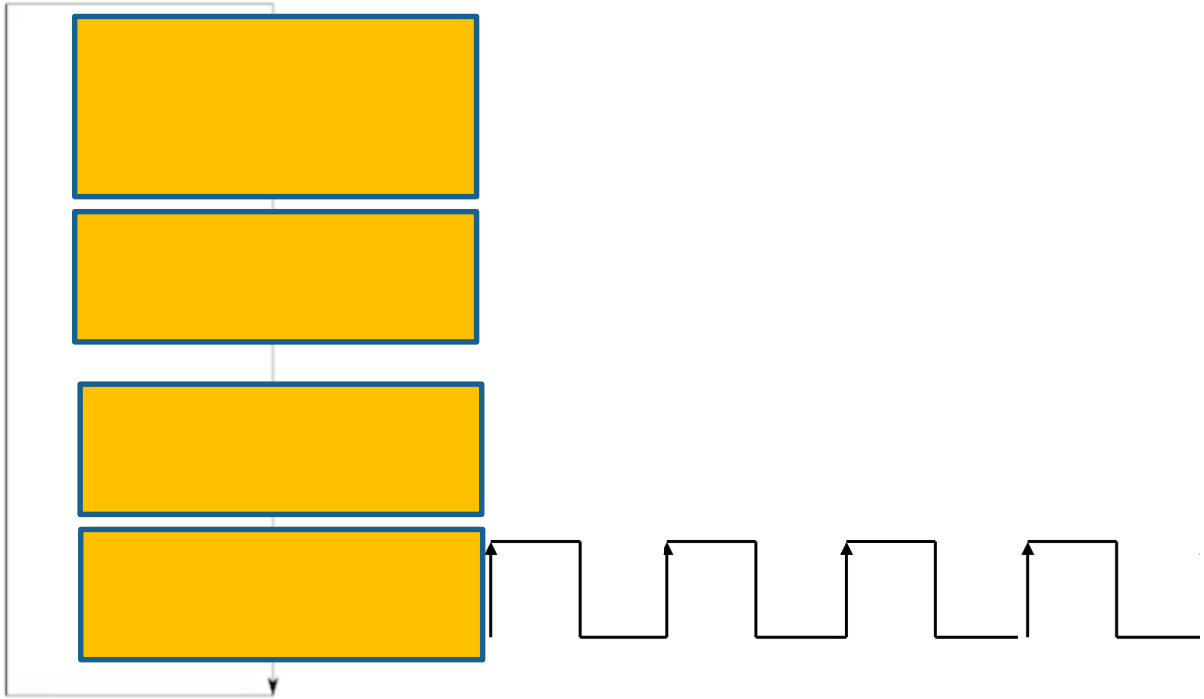
```
WHILE{   } Loop
            Read a,b,c,d
          y = a + b + c + d
           END WHILE

a,b,c,d are 4-bit numbers.
```

Behavioral Description



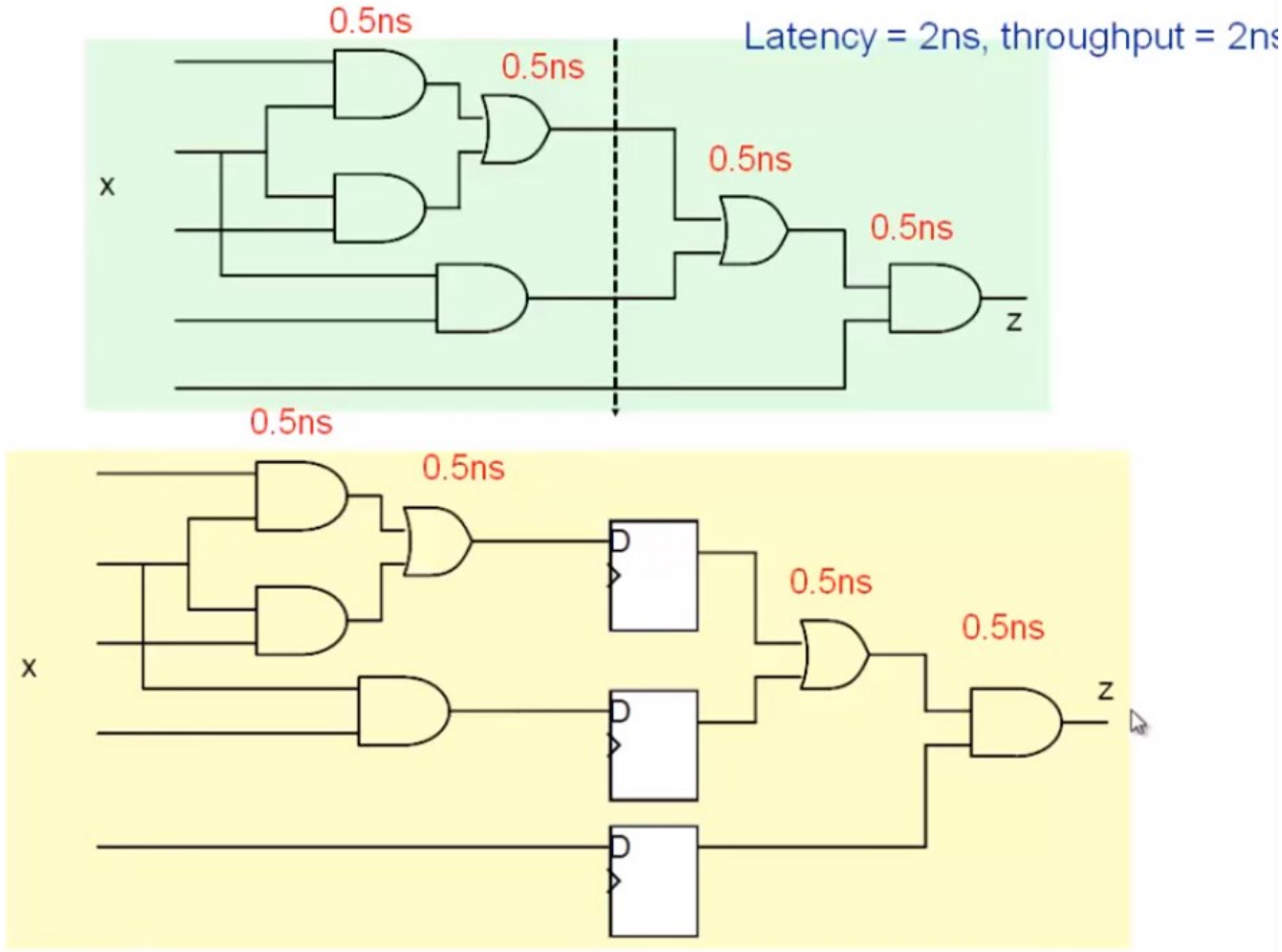
ASM Chart

Algorithmic State Machine (ASM) Chart



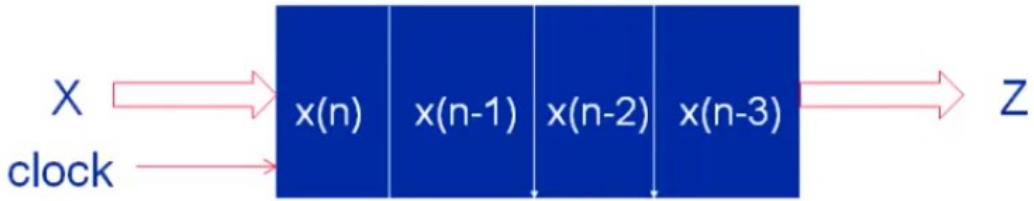
Design Constrains in RTL

- Latency
  - The delay between the time input is read and the time the corresponding output is produced.
- Throughput
  - The rate at which the input could be read and processed.

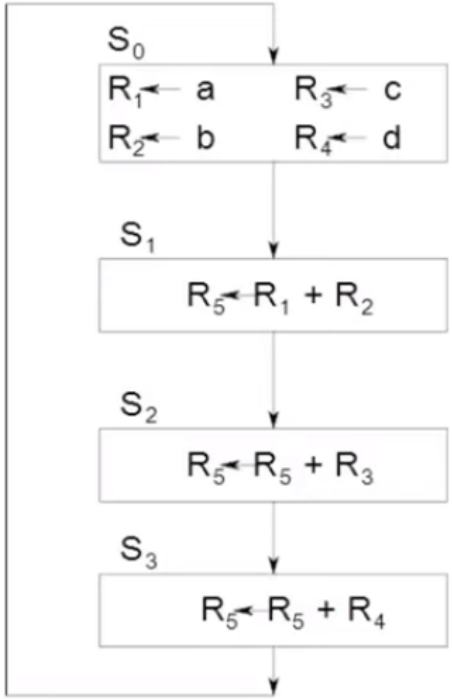

0.5ns
0.5ns
Latency = 2ns, throughput = 2ns
0.5ns
x
0.5ns
z
0.5ns
0.5ns
0.5ns
x
0.5ns
z

Pipelined Processing

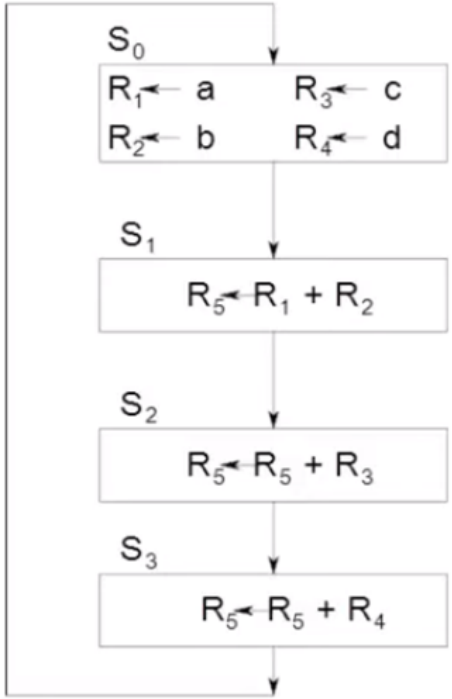
- The system is broken down into several stages which could operate simultaneously to achieve better throughput.

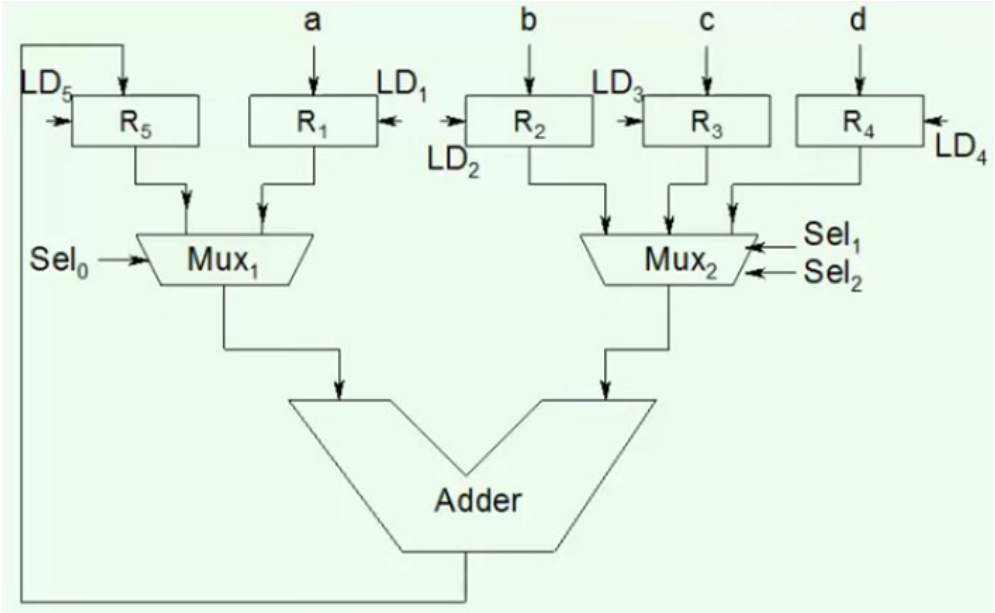


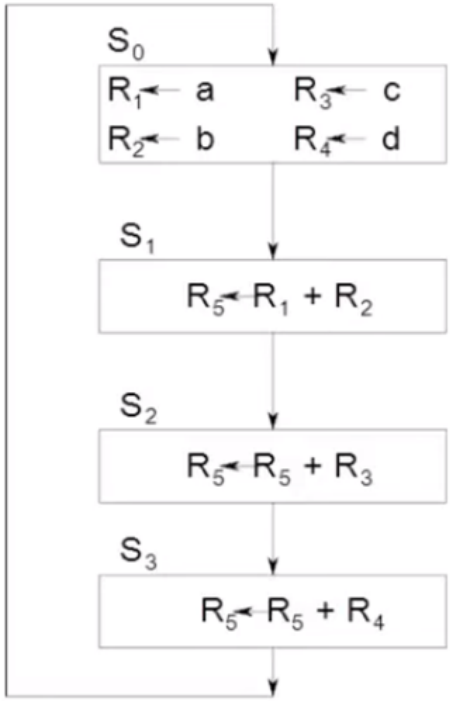
Datapath Design

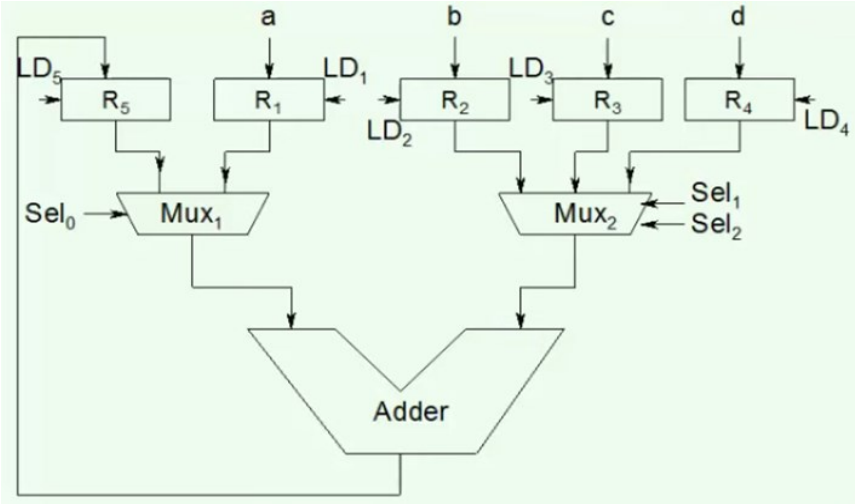


Datapath Design



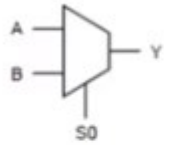



S0
R1 ← a
R3 ← c
R2 ← b
R4 ← d
S1
R5 ← R1 + R2
S2
R5 ← R5 + R3
S3
R5 ← R5 + R4


a
b
c
d
LD5
LD1
LD3
LD2
LD4
R5
R1
R2
R3
R4
Sel0
Mux1
Mux2
Sel1
Sel2
Adder

Latency Throughput Tradeoff

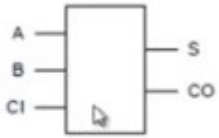
Logic Symbol



Cell Size

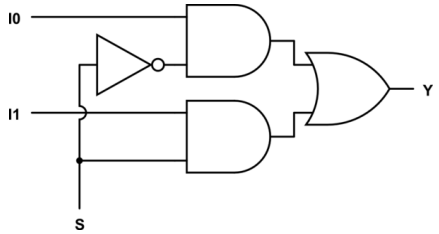
Drive Strength	Height (μm)	Width (μm)
MX2XL	5.0	5.3
MX2X1	5.0	5.3
MX2X2	5.0	5.9
MX2X4	5.04	6.60

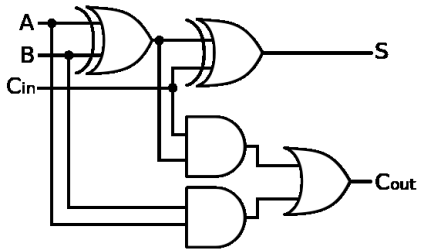
Logic Symbol



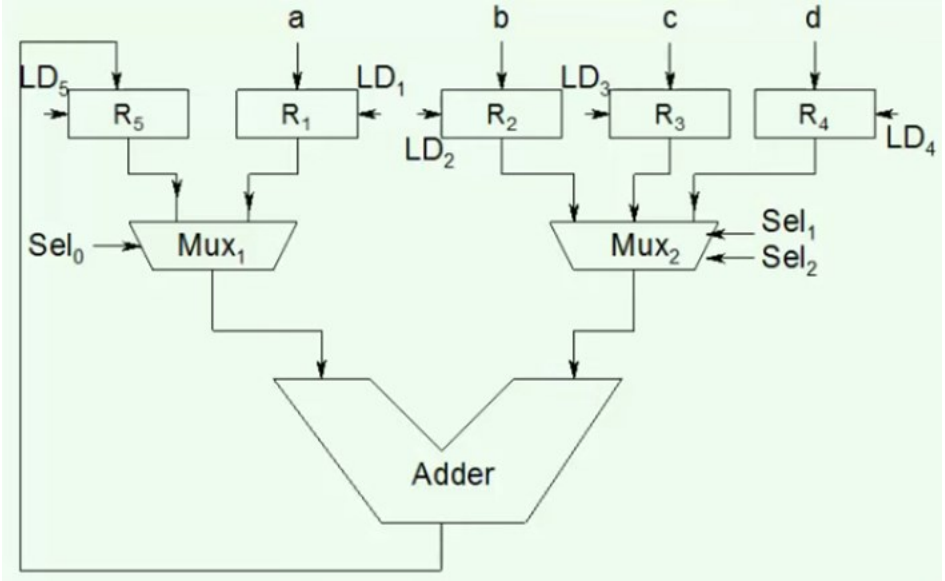
Cell Size

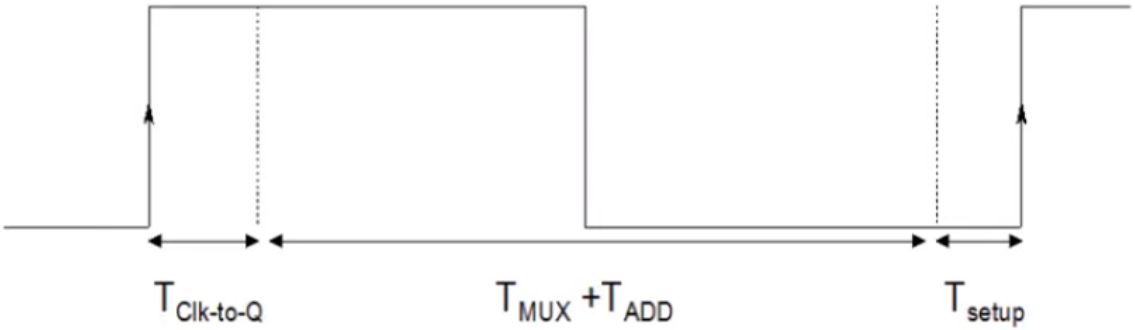
Drive Strength	Height (μm)	Width (μm)
ADDFXL	5.0	13.9
ADDFX1	5.0	13.9
ADDFX2	5.0	13.9
ADDFX4	5.0	15.2





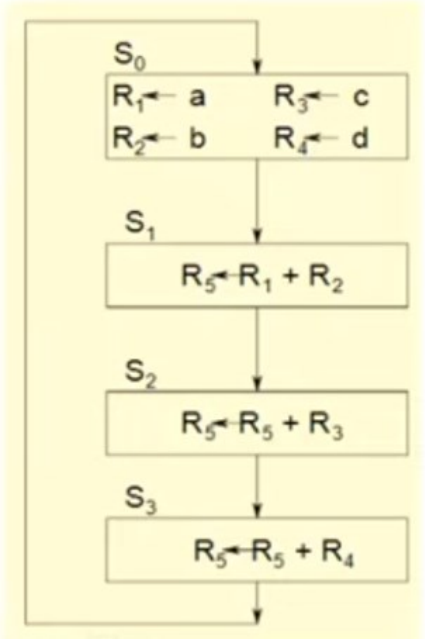
Latency Calculation

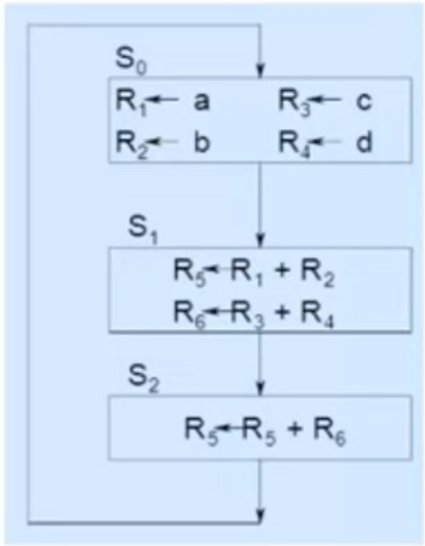


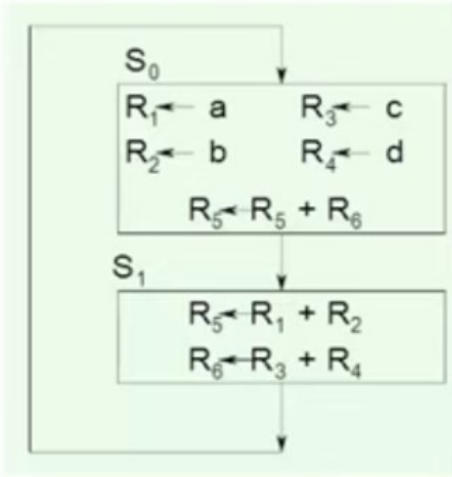


$$T_{Clock} = T_{clk\text{-}to\text{-}Q} + T_{Mux} + T_{ADD} + T_{setup}$$

Throughput Optimization

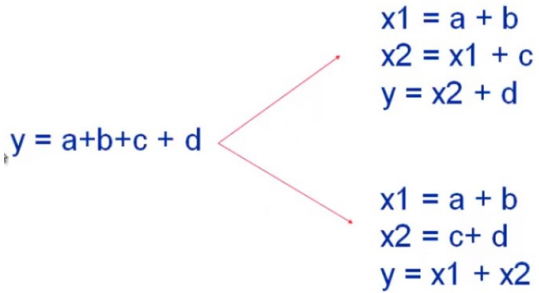


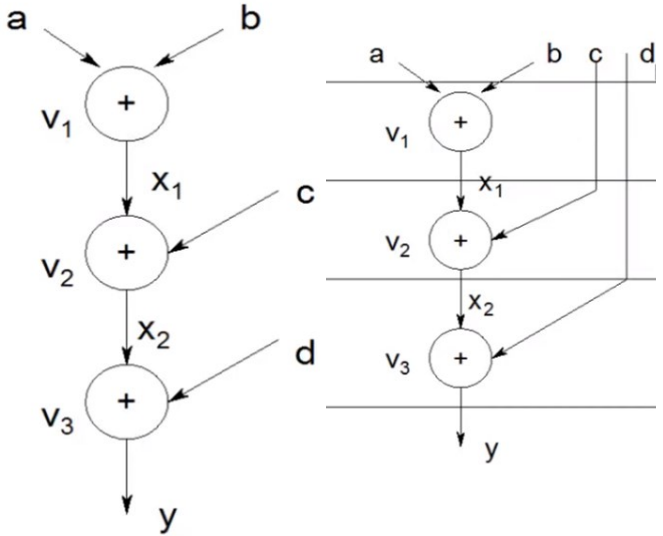




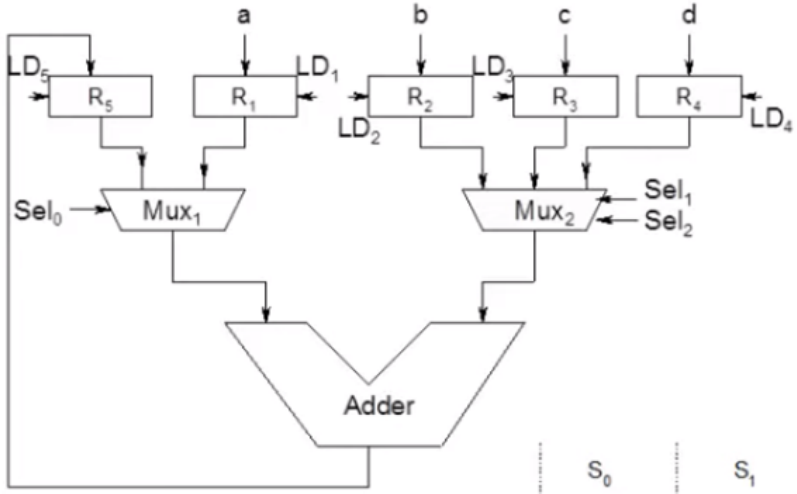
RTL Design Summary

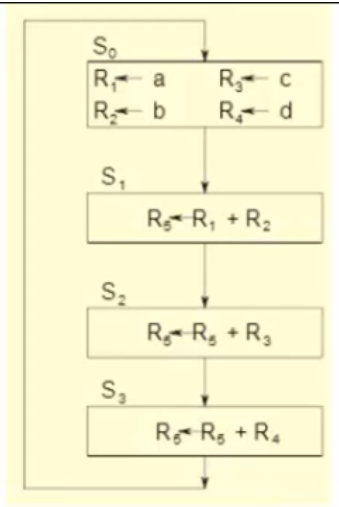
- Break down the problem into single clock cycle instructions.
- Create a data flow graph (DFG).
- Decide the clock cycle in which the operation will be carried out.

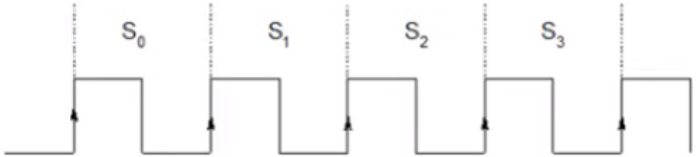




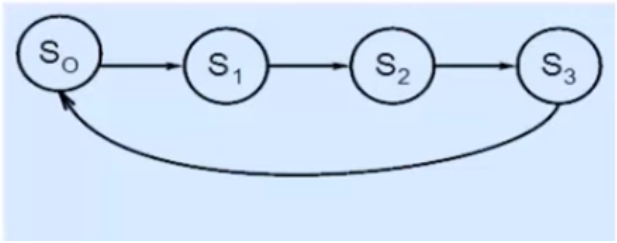
Controller : Moore machine







P. State	N. State	$LD_{1-5}Sel_{0-2}$
S_0	S_1	11110XXX
S_1	S_2	00001100
S_2	S_3	00001001
S_3	S_0	00001010



Thank You...!