GENERAL SIR JOHN KOTELAWALA DEFENCE UNIVERSITY

Faculty of Engineering

Department of Electrical, Electronic and Telecommunication Engineering

BSc Engineering Degree

Semester 6 Examination – 2024 September

Intake 39 – ET

DIGITAL SYSTEMS DESIGN

(ET2233)

Time allowed: 3 hours 18th September 2024

ADDITIONAL MATERIAL PROVIDED

Nil

INSTRUCTIONS TO CANDIDATES

This paper contains 5 questions on 5 pages

Answer ALL questions.

This is a closed book examination.

This examination accounts for 60% of the module assessment. The marks assigned for each question and parts thereof are indicated in square brackets.

If you have any doubt as to the interpretation of the wordings of a question, make your own decision, but clearly state it on the script.

Assume reasonable values for any data not given in or provided with the question paper, clearly make such assumptions made in the script.

All examinations are conducted under the rules and regulations of the KDU.

DETAILS OF ASSESSMENT

Learning Outcome (LO)	Questions that assess LO	Marks allocated (Total 70%)
LO1	Q1	10
LO2	Q2	10
LO3	Q3	12.5
LO4	Q4	12.5
LO5	Q5	15

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Question 01

a. Explain the following modules in a VHDL programme with a suitable example. [4 marks]

i. Library
ii. Entity
iii. Architecture

b. Write a Verilog code for a 2-bit comparator. [3 marks]

c. Discuss the different coding styles available in verilog. [3 marks]

Question 02

a. Explain the importance of using nonblocking statements in sequential RTL. [3 marks]

b. You are provided with the following Verilog code for a 4-bit counter with an enable and synchronous reset:

```
module counter (
  input clk,          // Clock input
  input reset,        // Synchronous reset
  input enable,       // Enable counting
  output reg [3:0] count  // 4-bit counter output
);
  always @(posedge clk) begin
    if (reset) begin
      count <= 4'b0000;  // Reset count to 0
    end else if (enable) begin
      count <= count + 1;  // Increment count if enable is high
    end
  end
endmodule
```

i. Draw the RTL diagram of the 4-bit counter based on the provided Verilog code. [3 marks]

ii. Modify the Verilog code to add a down-counting mode controlled by an input signal *mode*. If *mode* is 0, the counter should increment, and if *mode* is 1, the counter should decrement.Write the modified Verilog code and briefly describe your changes. [4 marks]

Question 03

a. Distinguish the difference between the super pipelining and superscalar pipelining. [3 marks]

b. Construct the data path and draw a detailed diagram for a single-cycle MIPS processor that supports the following functionality: • Store word instruction • Load word instruction • PC increment For each of the instructions and the PC increment functionality, explain clearly how the instruction memory, the register file, the ALU, and the data memory interacts. Clearly motivate your answers. [5.5 marks]

c. Compare the performance of a single-cycle processor and a multi-cycle processor. The delay times for the instruction stages are as follows:

- Instruction memory access time = 500 ps
- Data memory access time = 500 ps
- Instruction Decode and Register read = 200 ps
- Register write = 200 ps
- ALU delay = 100 ps

IF ALU
ID
EXE lw

Ignore the other delays in the multiplexers, wires, etc. Assume a program has the following instruction mix: 40% ALU, 5% load, 5% store, 30% branch, and 20% jump.

i. Compute the delay for each instruction class and the clock cycle for the single cycle processor. [2 marks]

ii. Compute the clock cycle and the average CPI (Cycles per Instruction) for the multi-cycle processor. [2 marks]

Question 04

a. Explain the internal construction and the R/W operation of static cell. [3 marks]

b. Discuss advantages and disadvantages of cache replacement policies.. FIFO least recently [3 marks]

c. A two-way set-associative cache has lines of 16 bytes and a total size of 8 kbytes. The 64-Mbyte main memory is byte addressable. Show the format of main memory addresses. [4 marks]

d. Construct a 128Kx16 RAM using 64Kx8 chips. [2.5 marks]

Question 05

a. Discuss the algorithm used for state reduction when designing a asynchronous sequential circuit. [2 marks]

b. It is necessary to design a negative-edge-triggered T flip-flop. The circuit has two inputs, T (toggle) and C (clock) , and one output, Q.The output state is complemented if T = 1 and the clock C changes from 1 to 0 (negative-edge triggering). Otherwise, under any other input condition, the output Q remains unchanged .Although this circuit can be used as a flip-flop in clocked sequential circuits, the internal design of the flip-flop (as is the case with all other flip-flops) is an asynchronous problem.

i. Draw the state diagram and derive primitive flow table for the circuit. Show that it can be reduced to the table shown in the Fig Q.5a. [7 marks]

ii. Complete the design of the circuit and implement ths using NOR gate SR latch. The excitation table of NOR gate SR latch is given in Fig Q.5b. [6 marks]

	TC 00	01	11	10
a	d , -	(a) , 0	(a) , 0	(b) , -
b	(b) , 1	(b) , 1	c , -	(b) , 1
c	b , -	(c) , 1	(c) , 1	d , -
d	(d) , 0	(d) , 0	a , -	(d) , 0

Fig Q.5a

Q(n)	Q(n+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Fig Q.5b

- End of the Question Paper –