JFET Biasing

LECTURE 10

DR. SK WIJAYASEKARA

Introduction

For the JFET, the relationship between input and output quantities is nonlinear due to the squared term in Shockley's equation.

Nonlinear functions results in curves as obtained for transfer characteristic of a JFET.

Graphical approach will be used to examine the dc analysis for FET because it is most popularly used rather than mathematical approach

The input of BJT and FET controlling variables are the current and the voltage levels respectively

Introduction

Common FET Biasing Circuits

- JFET
  - Fixed – Bias
  - Self-Bias
  - Voltage-Divider Bias

General Relationships

For all FETs:

$$I_G \approx 0A$$

$$I_D = I_S$$

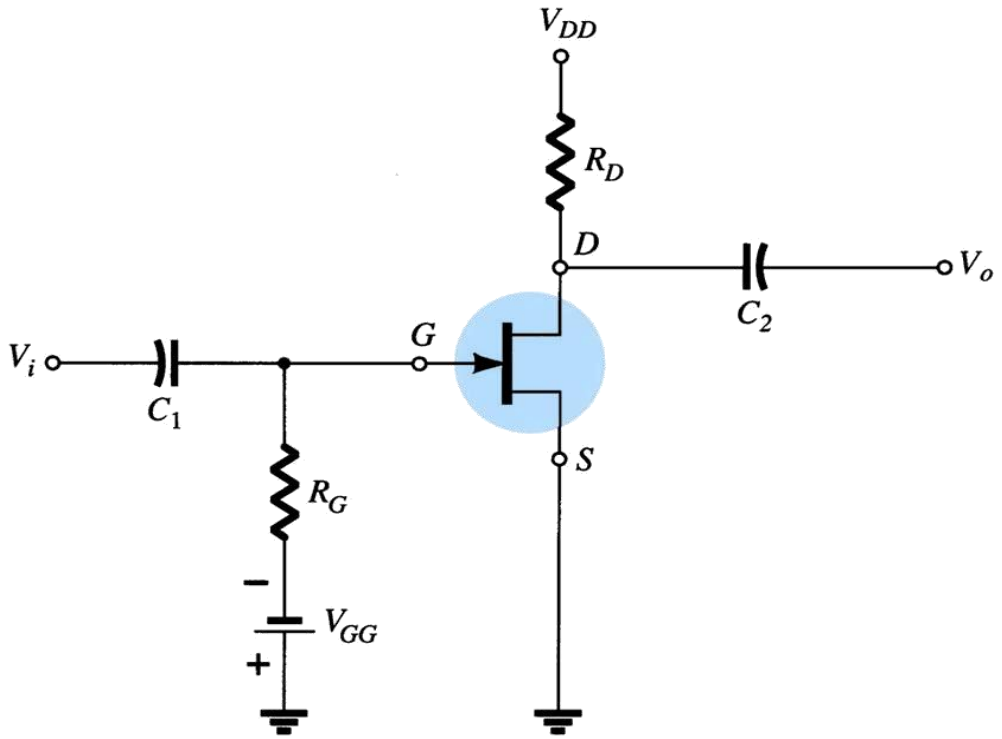
For JFETs

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Fixed-Bias Configuration

The configuration includes the ac levels V_i and V_o and the coupling capacitors.

The resistor is present to ensure that V_i appears at the input to the FET amplifier for the AC analysis.

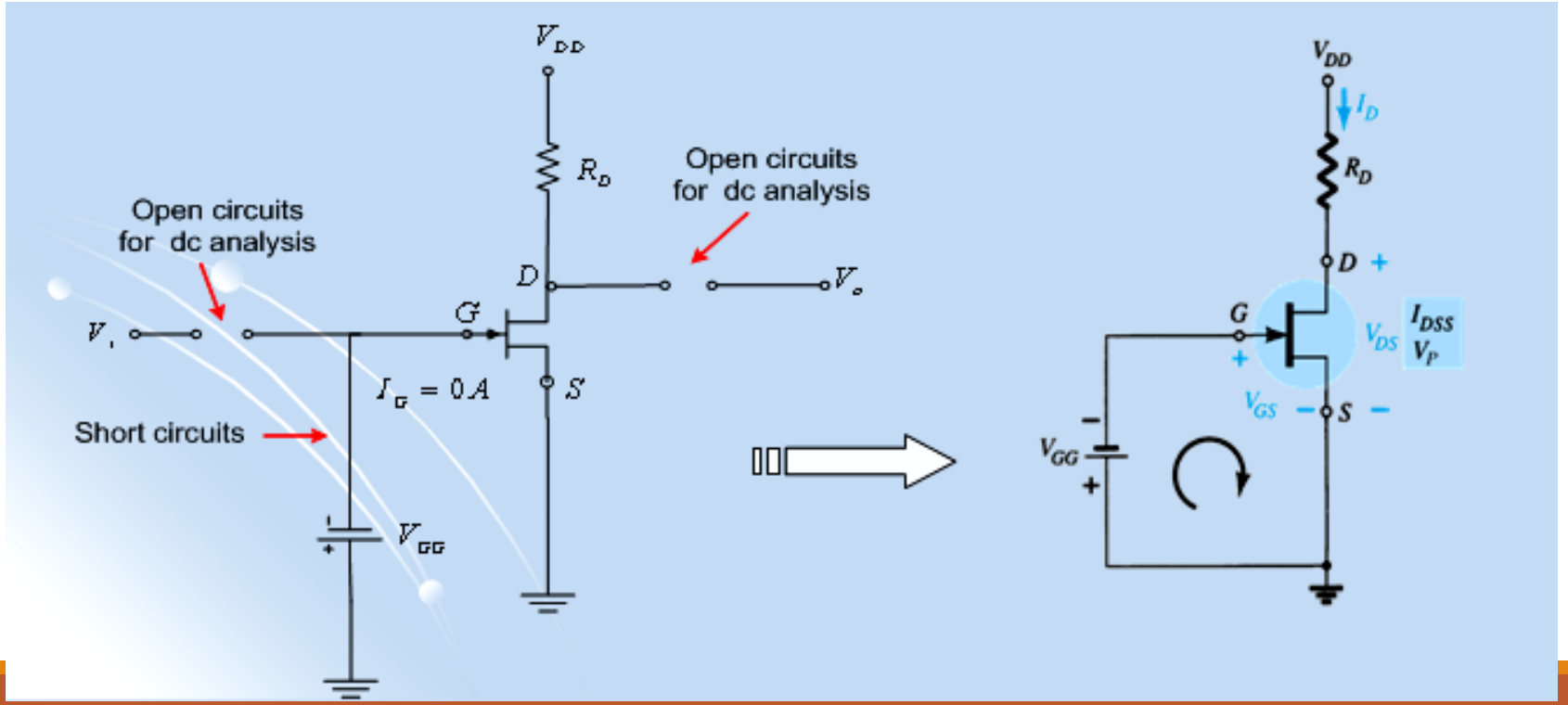


Fixed-Bias Configuration

For the DC analysis,

- Capacitors are open circuits
- and $I_G \cong 0A$ $V_{RG} = I_G R_G = (0A)R_G = 0V$

The zero-volt drop across R_G permits replacing R_G by a short-circuit



Fixed-Bias Configuration

Investigating the input loop

I_G=0A, therefore

$V_{RG}=I_G R_G=0V$

Applying KVL for the input loop,

$-V_{GG}-V_{GS}=0$

$V_{GG}= -V_{GS}$

It is called *fixed-bias configuration* due to V_{GG} is a fixed power supply so V_{GS} is fixed

The resulting current,

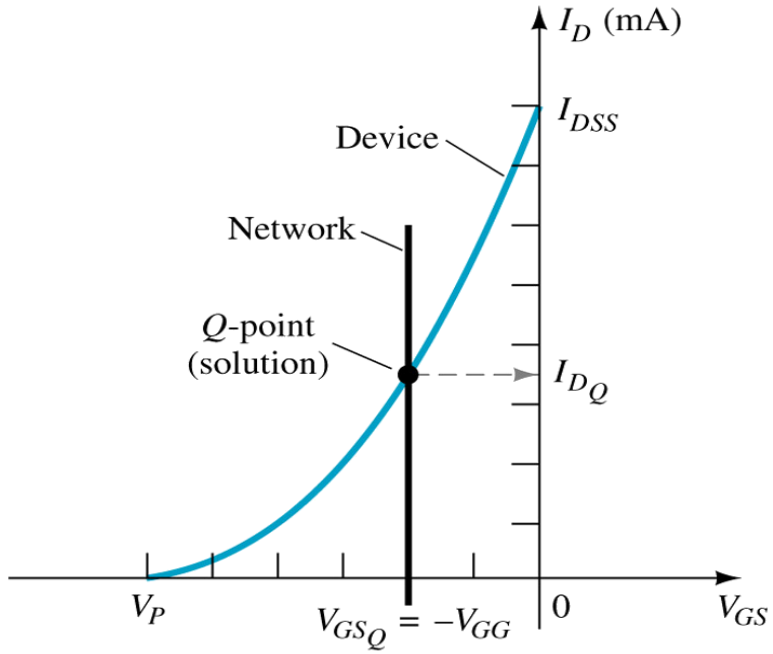
$$I_D = I_{DSS}(1-\frac{V_{GS}}{V_P})^2$$

Investigating the graphical approach.

Using below tables, we

can draw the graph

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
0.5	$I_{DSS}/4$
V_P	0mA



The fixed level of V_{GS} has been superimposed as a vertical line at

$$V_{GS} = -V_{GG}$$

At any point on the vertical line, the level of V_G is $-V_{GG}$--- the level of I_D must simply be determined on this vertical line.

The point where the two curves intersect is the common solution to the configuration – commonly referrers to as the **quiescent** or operating point.

The quiescent level of I_D is determined by drawing a horizontal line from the Q-point to the vertical I_D axis.

Output loop

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_S = 0V$$

$$V_{DS} = V_D - V_S$$

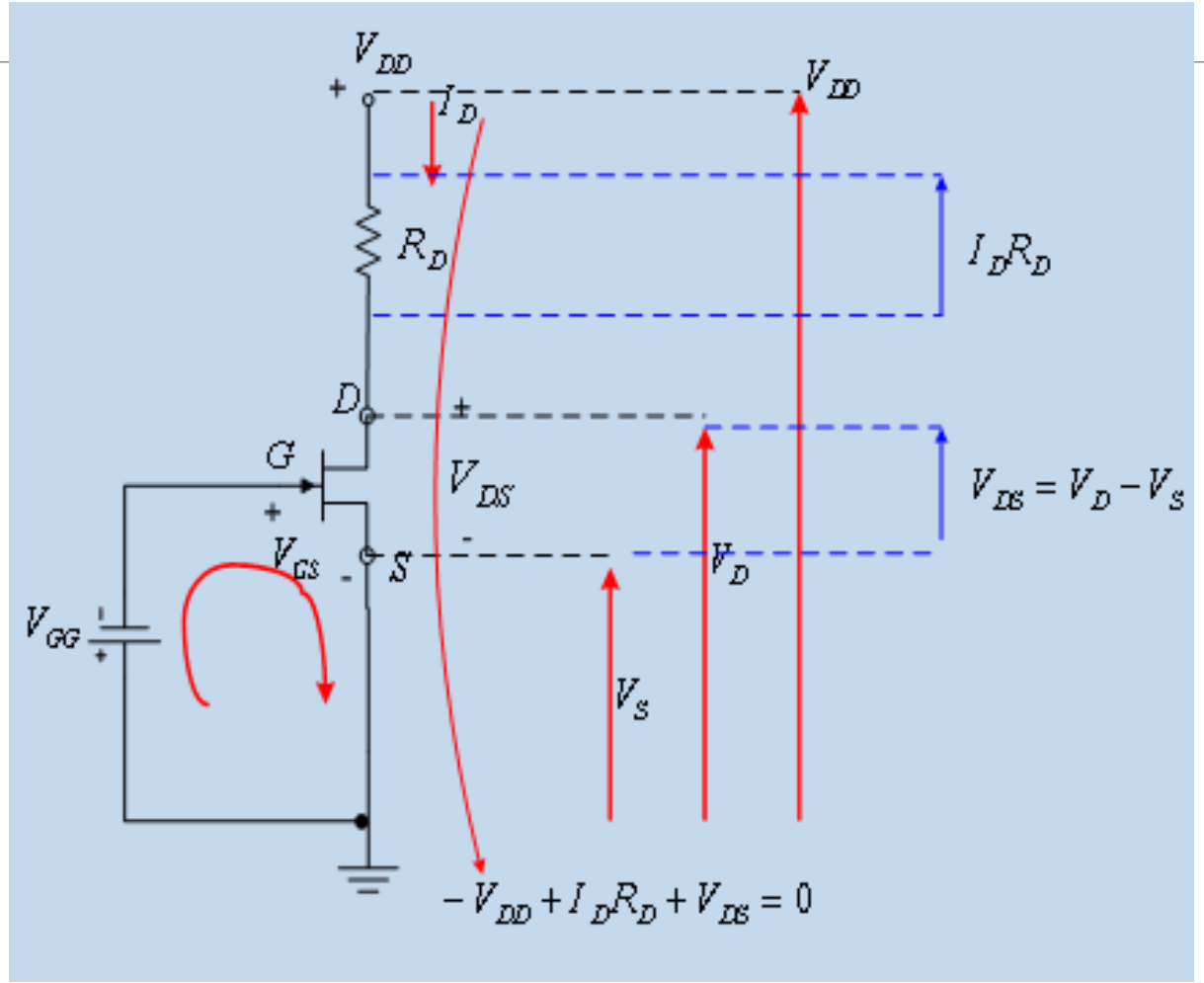
$$V_D = V_{DS} + V_S \qquad V_S = 0$$

$$V_D = V_{DS}$$

$$V_{GS} = V_G - V_S$$

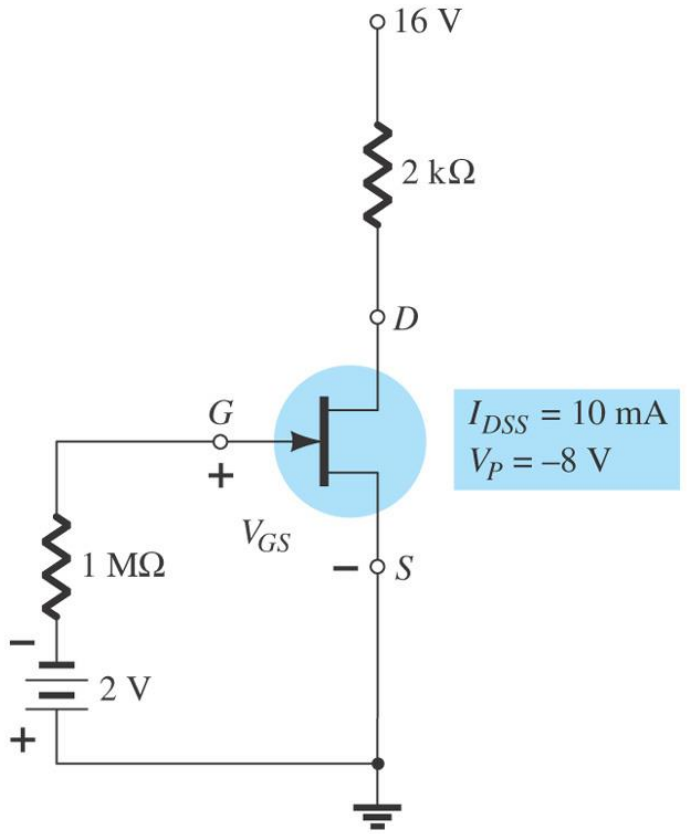
$$V_G = V_{GS} + V_S \qquad V_S = 0$$

$$V_G = V_{GS}$$



Example

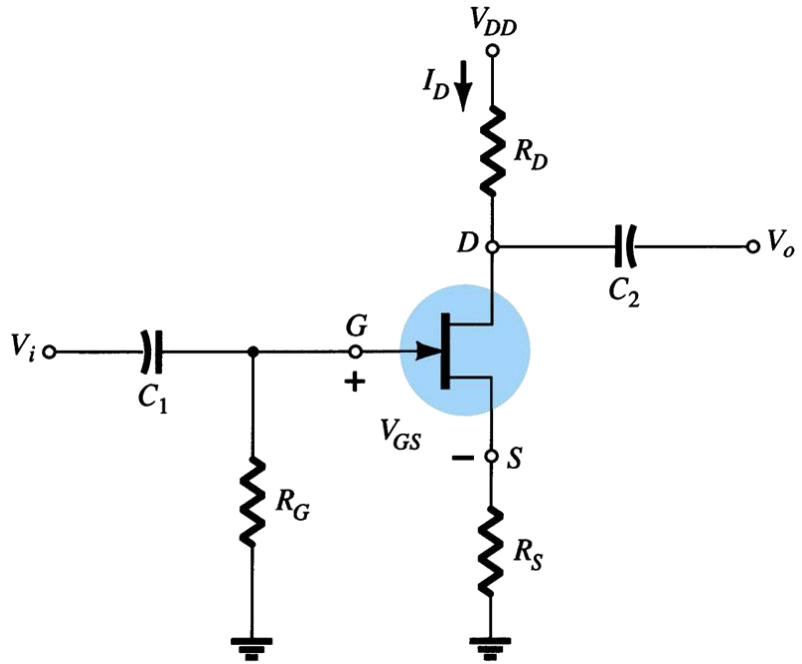
Determine V_{GS}, I_D, V_{DS}, V_D, V_G, V_S

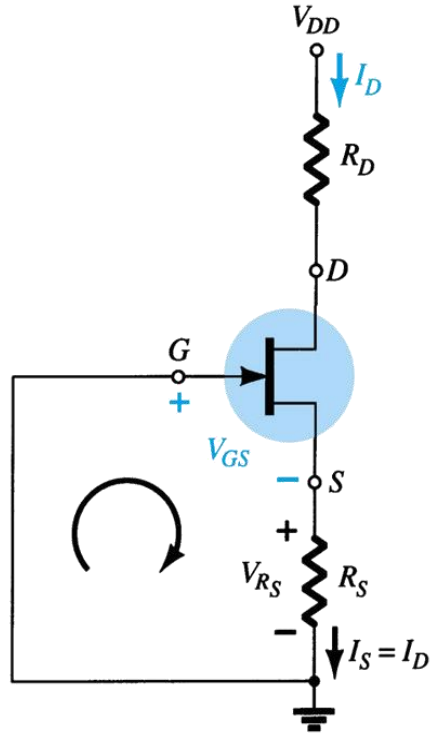


Self Bias Configuration

The self-bias configuration eliminates the need for two dc supplies.

The controlling V_{GS} is now determined by the voltage across the resistor R_S





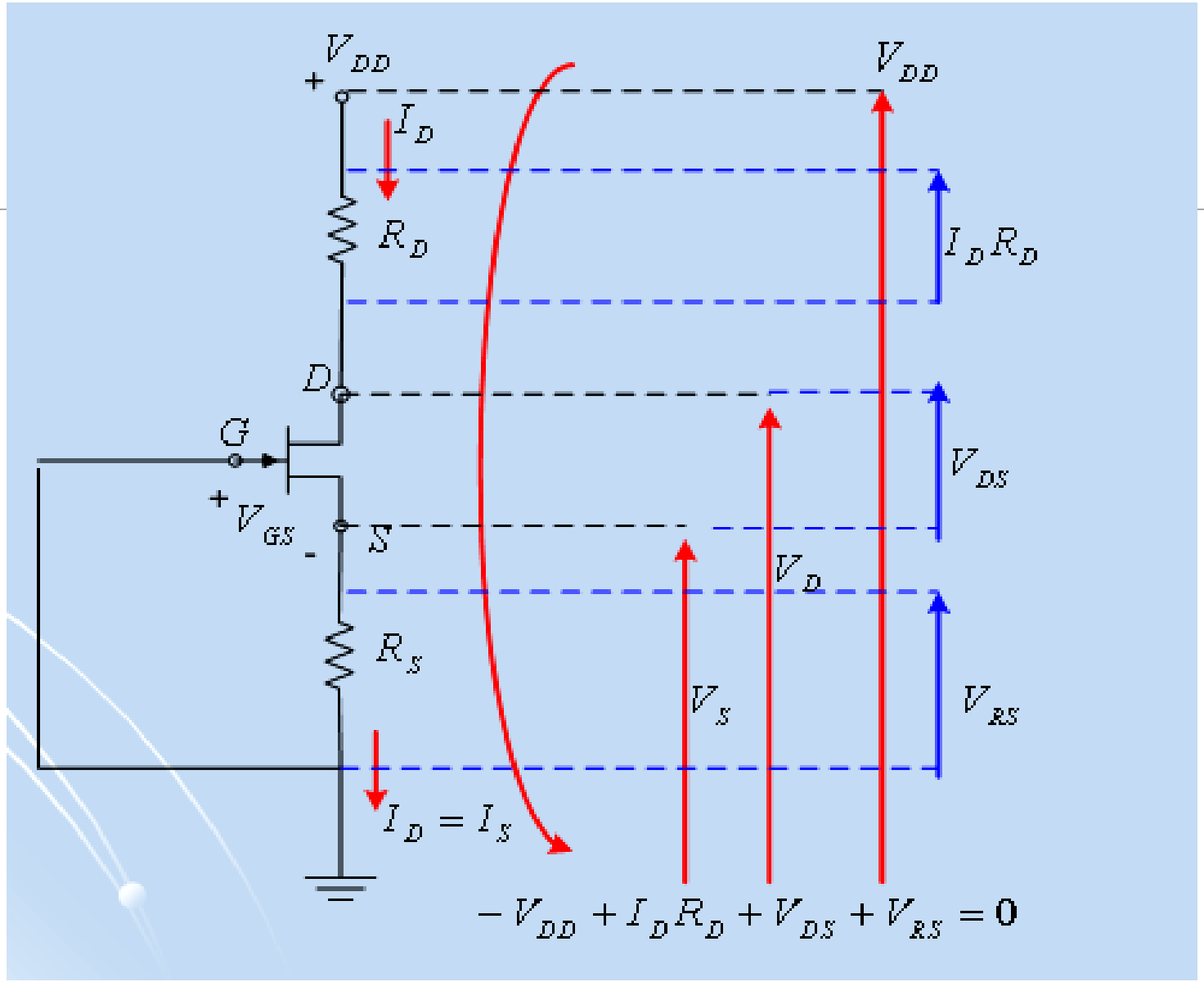
For the indicated input loop:

$$V_{GS} = -I_D R_S$$

Mathematical approach:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$


V_{DD}
I_D
R_D
D
G
V_{GS}
S
R_S
$I_D = I_S$
V_{DD}
$I_D R_D$
V_{DS}
V_D
V_S
V_{RS}
$-V_{DD} + I_D R_D + V_{DS} + V_{RS} = 0$

For output loop

- Apply KVL of output loop
- Use $I_D = I_S$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$V_S = I_D R_S$$

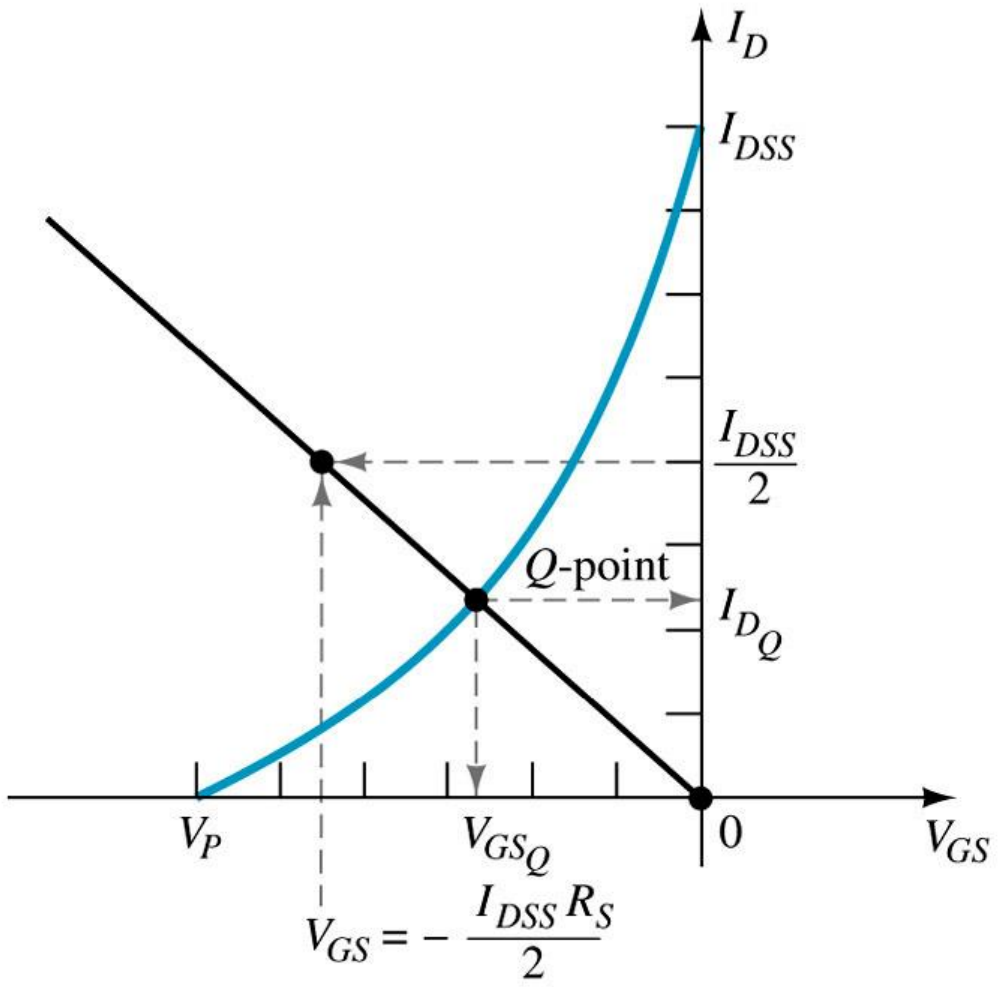
$$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$$

- Graphical approach
  - Draw the device transfer characteristic
  - Draw the network load line
    - Use $V_{GS} = -I_D R_S$ to draw straight line.
    - First point, $I_D = 0,\ V_{GS} = 0$
    - Second point, any point from $I_D = 0$ to $I_D = I_{DSS}$. Choose

$$I_D = \frac{I_{DSS}}{2} \text{ then}$$

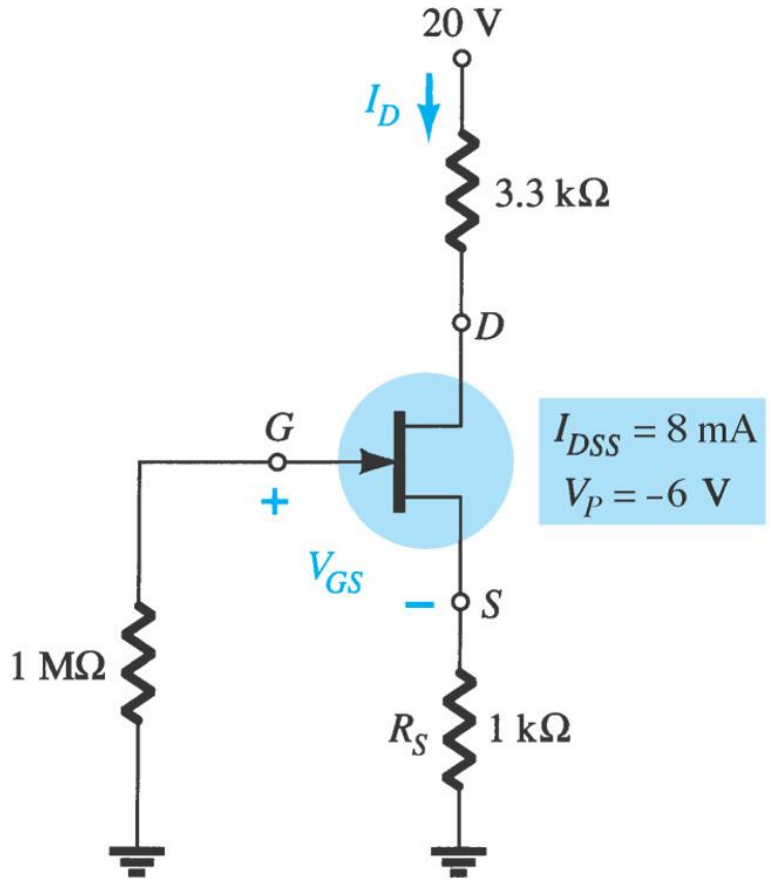
$$V_{GS} = -\frac{I_{DSS} R_S}{2}$$

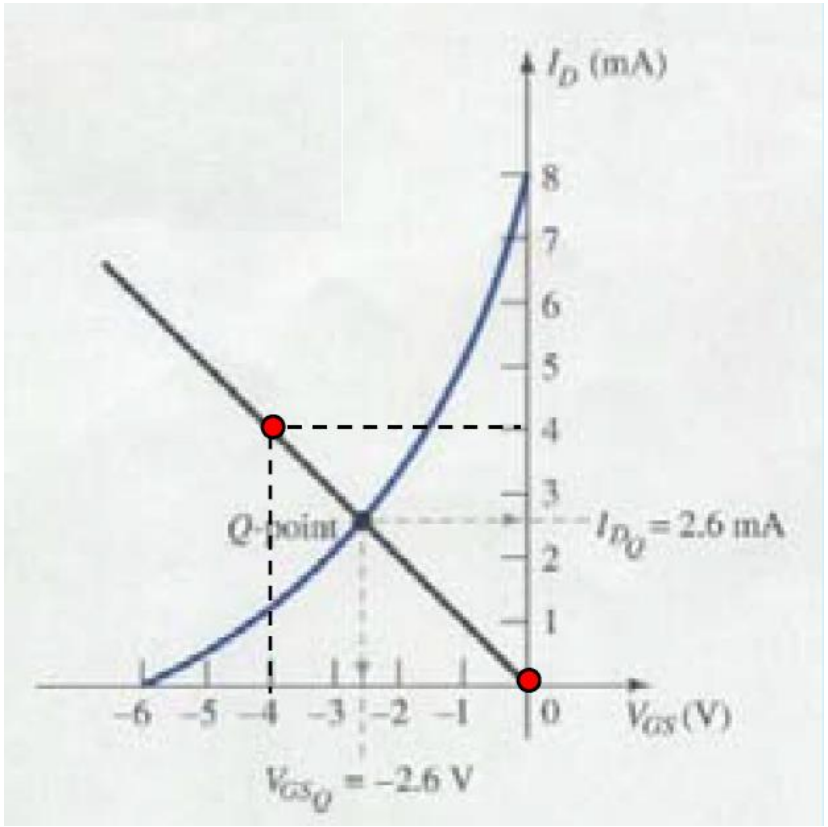
  - the quiescent point obtained at the intersection of the straight line plot and the device characteristic curve.
  - The quiescent value for I_D and V_{GS} can then be determined and used to find the other quantities of interest.


I_D
I_{DSS}
$\frac{I_{DSS}}{2}$
Q-point
I_{D_Q}
V_P
V_{GS_Q}
0
V_{GS}
$V_{GS} = -\frac{I_{DSS} R_S}{2}$

Example

Determine V_{GS}, I_D,V_{DS},V_S,V_G and V_D.

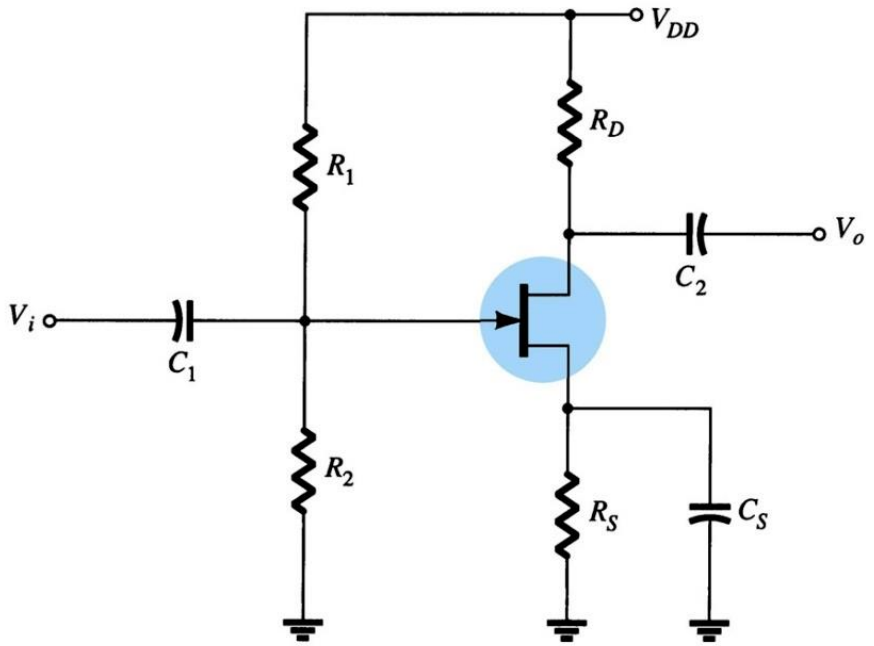


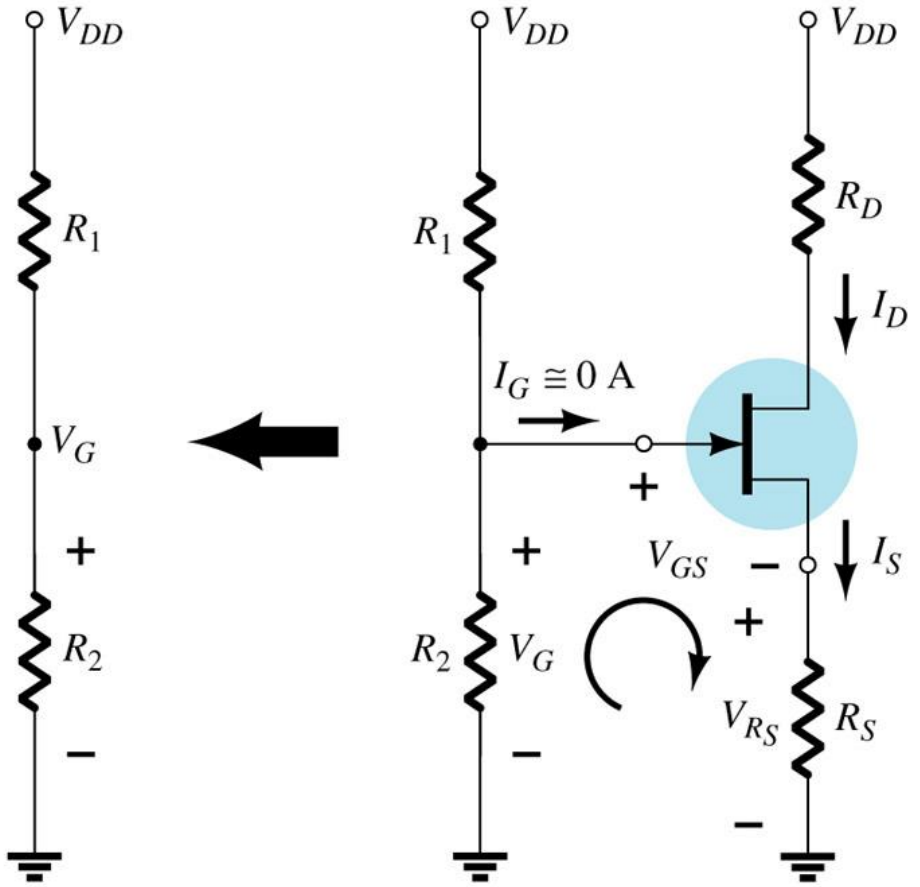


Voltage-Divider Bias

The arrangement is the same as BJT but the DC analysis is different

In BJT, I_B provide link to input and output circuit, in FET V_{GS} does the same





Voltage-Divider Bias

The source V_{DD} was separated into two equivalent sources to permit a further separation of the input and output regions of the network.

I_G = 0A ,Kirchoff's current law requires that I_{R1}= I_{R2} and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G.

Voltage-Divider Bias

V_G can be found using the voltage divider rule :

$$\mathbf{V_G = \frac{R_2 V_{DD}}{R_1 + R_2}}$$

Using Kirchoff's Law on the input loop:

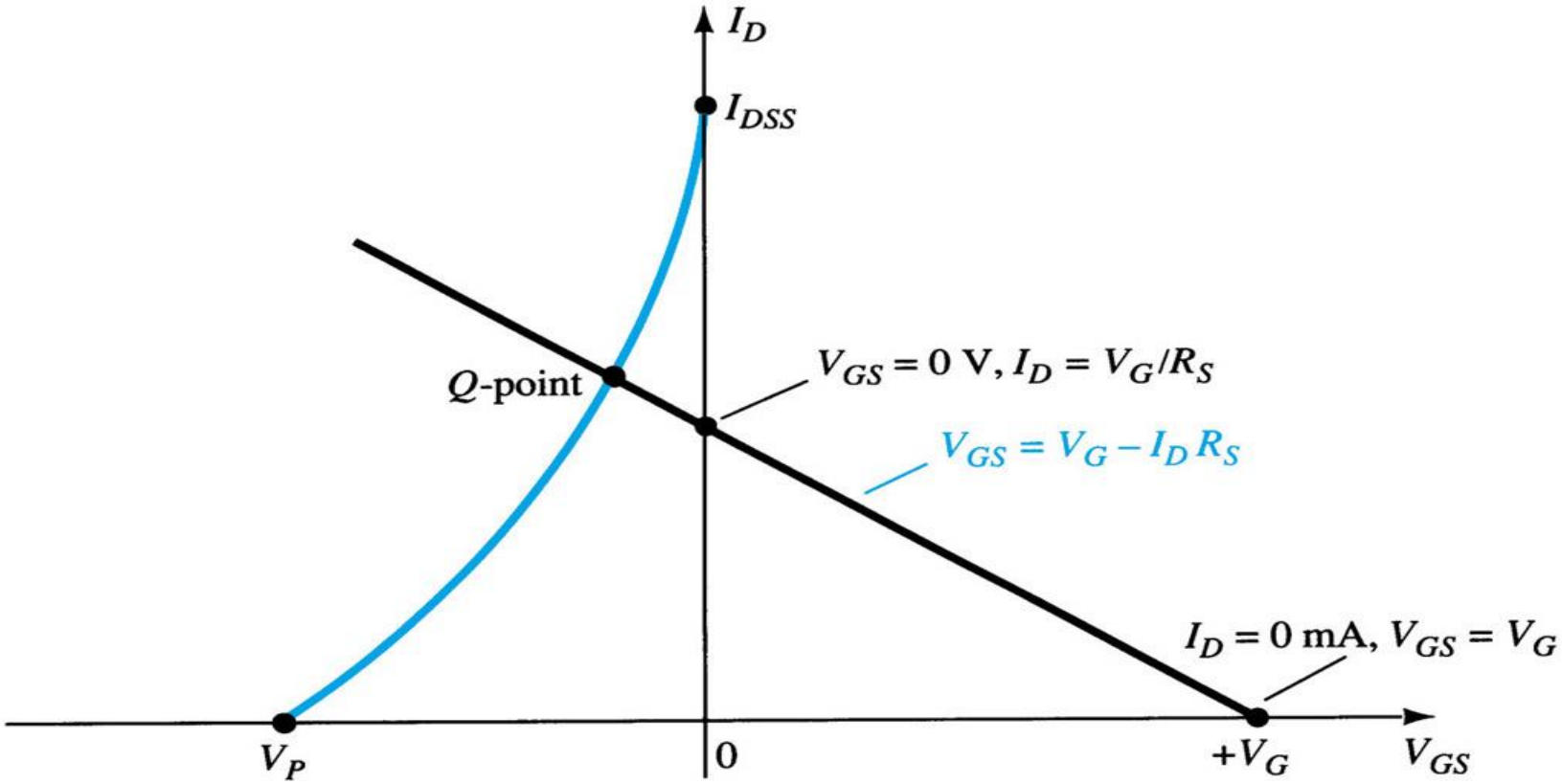
Rearranging and using ID =IS:

$$V_G - V_{GS} - V_{RS} = 0$$

$$V_{GS} = V_G - I_D R_S$$

Again the Q point needs to be established by plotting a line that intersects the transfer curve.

Procedures for plotting



1. Plot the line: By plotting two points: $V_{GS} = V_G$, $I_D = 0$ and $V_{GS} = 0$, $I_D = V_G/R_S$
2. Plot the transfer curve by plotting I_{DSS}, V_P and calculated values of I_D.
3. Where the line intersects the transfer curve is the Q point for the circuit.

Once the quiescent values of I_{DQ} and V_{GSQ} are determined, the remaining network analysis can be found.

$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

$$V_{DS} = V_{DD} - I_D(R_D + I_D R_S)$$

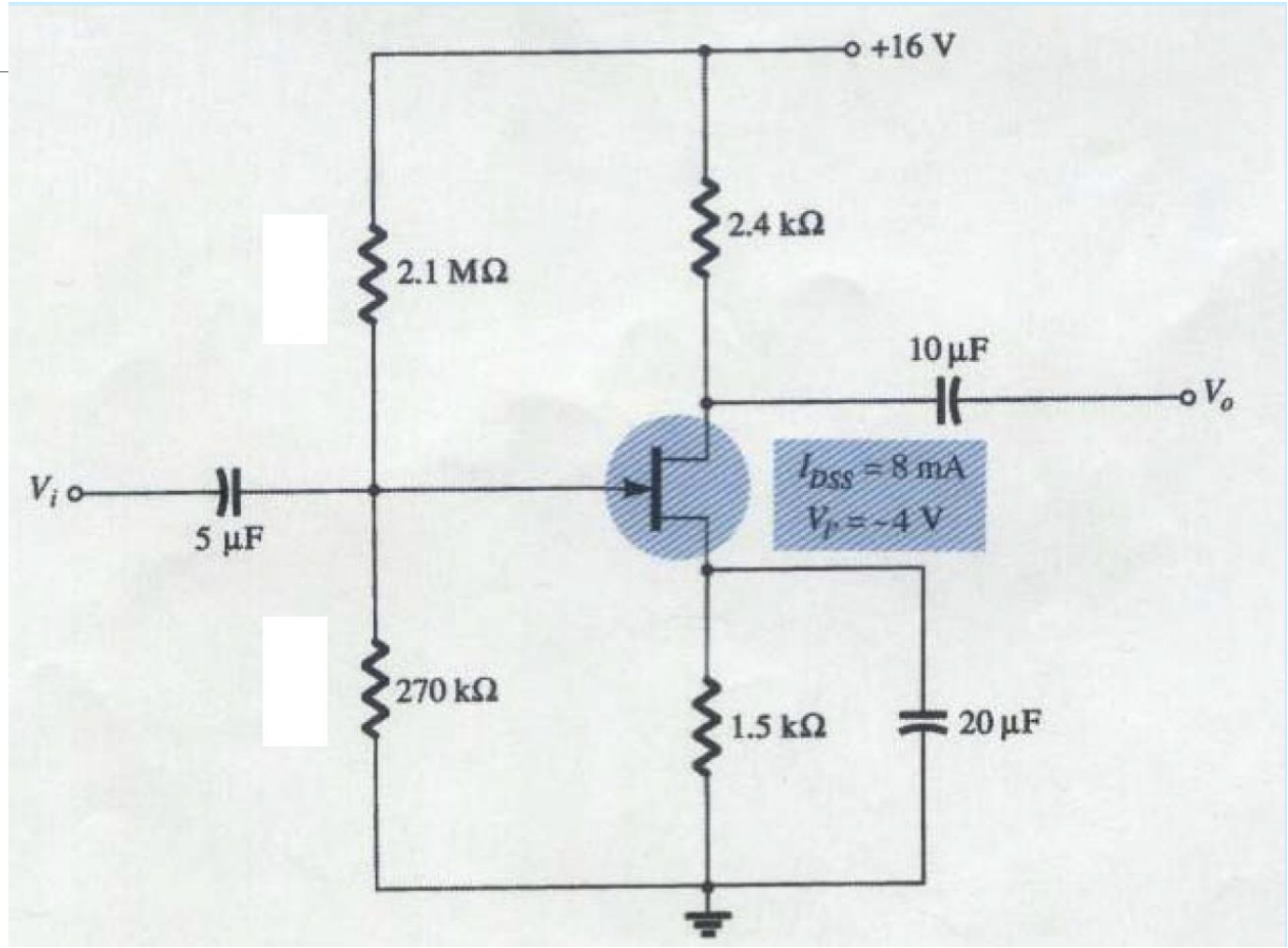
Output loop:

$$V_D = V_{DD} - I_D R_D$$

$$V_S = I_D R_S$$

Example

V_{DS} = 9v and determine V_G, I_D,V_{GS},V_S.



Thank You