GENERAL SIR JOHN KOTELAWALA DEFENCE UNIVERSITY
Faculty of Engineering
Department of Electrical, Electronic and Telecommunication Engineering

B.Sc. Engineering Degree
Semester 6 Examination – September 2024
(Intake 39 - EE/ET/MC)

EE 3213 – POWER ELECTRONICS AND APPLICATIONS I

Time allowed: 3 Hours 30 September 2024

INSTRUCTIONS TO CANDIDATES:

This paper contains 5 questions on 6 pages.
Answer All Questions.
This is a closed book examination.

This examination accounts for 70% of the module assessment. The total maximum mark attainable is 100. The marks assigned for each question & sections thereof are indicated in square brackets.

If you have any doubt as to the interpretation of the wording of a question, make your own decision, but clearly state it on the script.

All Examinations are conducted under the rules & regulations of the University

DETAILS OF ASSESSMENT:

This module has 4 LOs, assessed at the end-semester examination
Table below shows LO assessment details

Learning Outcome (LO)	Questions that assess LO	Marks allocated (Total 70%)
LO1	Q1	13
LO2	Q2	17
LO3	Q3, Q4	25
LO4	Q5	15

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Question 1

a) Explain briefly how the Voltage Utilization of a sinusoidal PWM voltage source inverter can be improved by modifying the three sinusoidal reference signals of its modulator. [03]

Adding 3rd harmonic

b) Explain briefly why it is necessary to increase the carrier-ratio when delivering low-frequency output voltage by a PWM voltage source inverter operated with constant V to f control. [03]

c) Explain why the sequential control is preferred over the concurrent control for 3-Phase dual-series-bridge thyristor converter for delivering a given combination of output power and voltage. [04]

d) Explain why the distortion minimization PWM is generally preferred over the harmonic elimination PWM in practice. [03]

Question 2

a) Three-phase, full-bridge AC to DC diode-converter is operating on 400 V, 50 Hz three-phase AC supply. The converter delivers 15 A constant current to an inductive load. You may ignore the internal impedance of the AC supply. Assume ideal diodes. Determine,

(i) Mean value of the output DC voltage. $3\sqrt{2}V_{ph}/\pi$ [02]
(ii) Peak-peak ripple in the output DC voltage. $\sqrt{2}V_L - \sqrt{2}V_L \cos 30$ [02]
(iii) RMS value of the fundamental component of AC side line-current. [02]

$\sqrt{6}I_d/\pi$

b) A three-phase voltage source inverter is operated with Voltage Vector PWM at constant sampling frequency 10 kHz. The inverter delivers variable frequency and variable voltage output. Input voltage to the inverter is 750 V DC.

(i) What is the greatest value of line-voltage fundamental (RMS) obtainable at the output with vector control? [02]

(ii) The inverter is set to deliver line-line fundamental output voltage of 400 V (rms) of 50Hz. If the 0th sampling instant is chosen to coincide with the positive-peak of the desired phase-a voltage, calculate the timing for switching signals S_a, S_b & S_c over the sampling-interval after the 75th sampling instant. [09]

$k = 75$

$\frac{1}{2pf_s}\left(1 + m(\sin 2\pi k - 0.25)\right)$

$V_0 = \frac{3\sqrt{2}}{\pi} \times 560 \times$

Question 3

a) In order to protect from shoot-through faults, inverters are designed with a blanking-time t_B for switchover between the upper and the lower IGBTs in each leg. Input DC voltage to the inverter is V_d. If the inverter is operated with square-wave-PWM at carrier frequency f_C, show that the step-change in the rms value of fundamental line-line voltage at the output, when over-modulation is used to transfer the control to the square-wave (six-step) control will be given by,

$m = 1 - 2f_C t_B$

$$(\Delta V_{Line})_{rms} = \frac{2\sqrt{6}V_d f_C t_B}{\pi}$$

[05]

b) A single-phase VSI with input DC voltage V_d is delivering an output current $I_m \sin(\omega t)$ using hysteresis current control within a tolerance band ΔH. The load has a resistance R in series with an inductance L.
Derive expressions for the switching frequency,

(i) Near the zero-crossing of the output current. [05]
(ii) Near the peak of the output current waveform. [05]

Question 4

A single-phase, full-bridge thyristor converter operating at delay angle α, delivers constant DC current I_o to an inductive load. Input sinusoidal AC source has rms voltage V_{ph}, frequency f, and internal inductance L_s.
Show that the mean output voltage $(V_o)_{mean}$ and the conduction overlap angle u are given by,

$$(V_o)_{mean} = \left(\frac{2\sqrt{2}V_{ph}\cos\alpha}{\pi}\right) - 4fL_sI_o$$

$\Delta V_o/2$

[05]

$$u = -\alpha + \cos^{-1}\left(\cos\alpha - \frac{4\pi f L_s I_o}{\sqrt{2}V_{ph}}\right)$$

[05]

$\frac{A}{\pi}$ $\left(\cos\left(\alpha + \pi/4\right) - \cos\left(\alpha - \pi/4\right)\right)$

$\cos\alpha\cos\pi/4 \mp \sin\alpha\sin\alpha/4 \; \mp \; \cos\alpha\cos\pi/4 \mp \sin\alpha\sin\pi/4$

$\frac{1}{\sqrt{2}}\cos\alpha - \frac{\sin\alpha}{\sqrt{2}} - \frac{\cos\alpha}{\sqrt{2}} + \frac{\sin\alpha}{\sqrt{2}}$

Question 5

a) Figure Q5 shows a linear DC power supply based on a single-phase bridge-rectifier with capacitor filter.

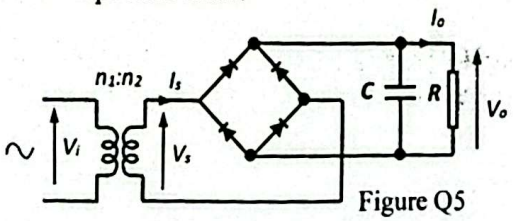

Figure Q5

$V_i = 230$ V (rms)
$f = 50$ Hz
$V_D = 0.7$V (diode conduction voltage drop)

$V_S - 2V_D = V_P$

$V_o = V_P - \frac{I_o}{4fC}$ $\quad I_P = \omega C\sqrt{2\omega V_m} + I_o$

The power supply needs to deliver output up to 900 mA at nearly 14 V, with peak-peak ripple not exceeding 1.5 V. Design suitable values for,

(i) Filter capacitance C. [03]
(ii) Transformer turn-ratio $n_1 : n_2$. [03]
(iii) Pulse current rating for each diode. [03]

b) Construct the power circuits for the following multilevel inverters.

(i) Three-phase, 5-level, cascaded H-bridge inverter. [02]

(ii) Single-phase, 5-level modular multilevel inverter. [02]

Construct the phase-voltage waveform for a 5-level, 3-Phase inverter corresponding to balanced 3-phase square-wave control. [02]

End of Question Paper