GENERAL SIR JOHN KOTELAWALA DEFENCE UNIVERSITY

Faculty of Engineering

Department of Electrical, Electronic and Telecommunication Engineering

BSc Engineering Degree

Semester 7 Examination – 2023 August

Intake 37 – ET

DIGITAL SYSTEMS DESIGN

(ET4173)

Time allowed: 3 hours 11 August 2023

ADDITIONAL MATERIAL PROVIDED

Data Path Diagram required to Question 3 part c is given in a separate sheet.

INSTRUCTIONS TO CANDIDATES

This paper contains 5 questions on 5 pages

Answer ALL questions.

This is a closed book examination

This examination accounts for 70% of the module assessment. The marks assigned for each question and parts thereof are indicated in square brackets

If you have any doubt as to the interpretation of the wordings of a question, make your own decision, but clearly state it on the script

Assume reasonable values for any data not given in or provided with the question paper, clearly make such assumptions made in the script

All examinations are conducted under the rules and regulations of the KDU

DETAILS OF ASSESSMENT

Learning Outcome (LO)	Questions that assess LO	Marks allocated (Total 70%)
LO1	Q1	14
LO2	Q2	14
LO3	Q3	7
LO4	Q3	7
LO5	Q4	14
LO6	-	-
LO7	Q5	14

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Question 01

a. Compare VHDL with Verilog. [6 marks]

c. List down the Operator Classes available in VHDL with examples. [6 marks]

d. Write VHDL code for 2x1Multiplexer. [8 marks]

Question 02

a. List the levels of Abstraction in Digital Design. [4 marks]

b. State the types of modelling in Verilog. [4 marks]

c. Briefly explain the type of components in digital system represented at the register tranfer level (RTL). [6 marks]

d. Write the Verilog RTL to implement the circuit shown in Fig Q 2. [6 marks]

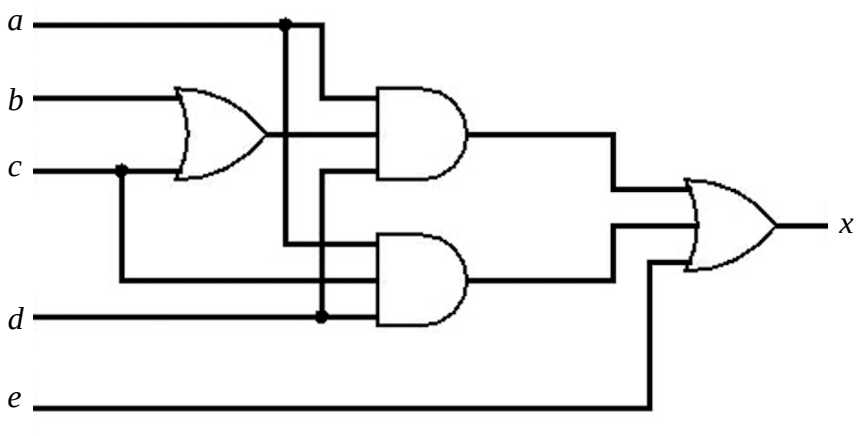

Fig Q 2

Question 03

a. State the 5 stages of the instruction pipeline of RISC processor. [5 marks]

b. Consider the following sequence of instructions being processed on the pipelined 5-stage RISC processor.

Add R4, R2, R3
Store R5, #100(R4)
Load R6, #200(R4)
Subtract R7, R5, R6

i. Identify all the data dependencies in the above instruction sequence. [3 marks]

ii. Assume that the pipeline does not use operand forwarding. Also assume that the only sources of pipeline stalls are the data hazards. Draw a diagram that represents instruction flow through the pipeline during each clock cycle. Calculate the time taken for the instruction sequence to complete. [6 marks]

c. It is required to implement a new *I-type* MIPS instruction *getpc $rt* which sets register *$rt* to the PC value of this instruction. Make changes to the given datapath in Fig Q 3 to implement the *getpc* instruction. Indicate the value of all control signals, including any new control signals. You will be given a separate paper with this diagram to make any modifications, and it should be attached to your answer script [6 marks]

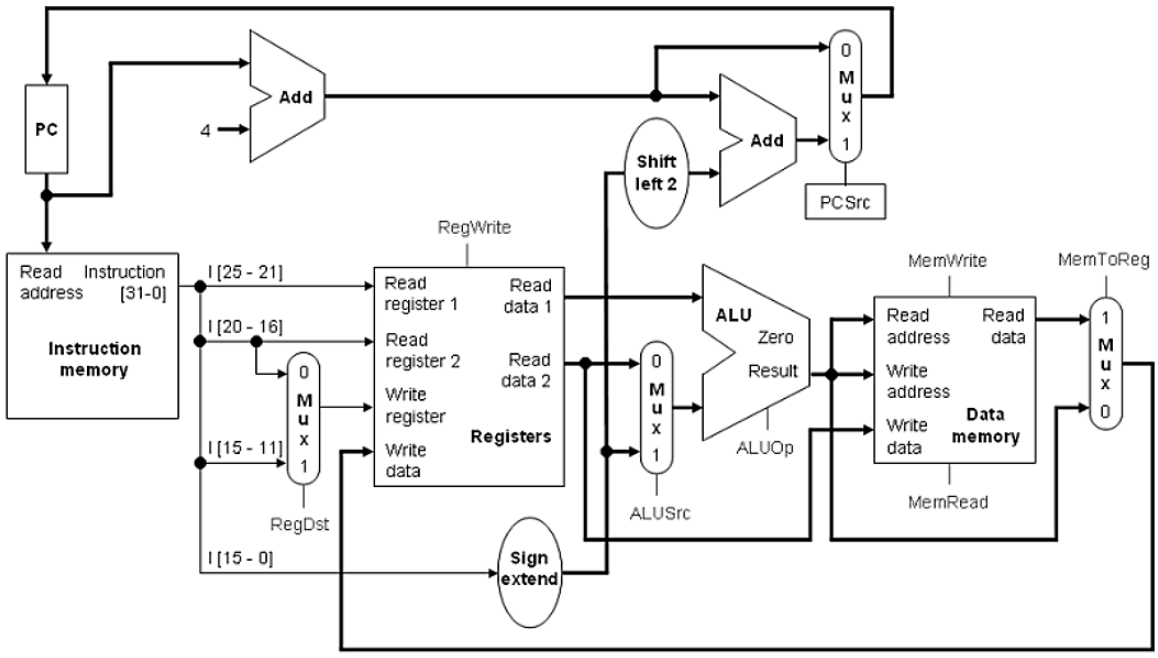

Fig Q 3

Question 04

a. Briefly explain the sequence of events in Read and Write operations between CPU and Main Memory interface. [6 marks]

b. Give four comprisons between SRAM and DRAM. [4 marks]

c. Construct an 8Kx32 RAM using 8Kx8 RAM chips. [5 marks]

d. A processor has a direct mapped cache has following specifications. How many blocks are in this cache? [5 marks]

- Data words are 8 bits long (i.e. 1 byte).
- Data addresses are to the word.
- A physical address is 20 bits long.
- The tag is 11 bits.
- Each block holds 16 bytes of data.

Question 05

a. Compare Synchronous & Asynchronous sequential circuits. [4 marks]

b. Design an asynchronous sequential circuit with inputs x_1 and x_2 and one output z. Initially and at any time if both the inputs are 0, output is equal to 0. When x_1 or x_2 becomes 1, z becomes 1. When second input also becomes 1, output changes to 0. The output stays at 0 until circuit goes back to initial state.

i. Obtain a primitive flow table for the circuit and show that it can be reduced to the table shown in the Fig Q.5a. [8 marks]

ii. Complete the design of the circuit and implement ths using NOR gate SR latch. The excitation table of NOR gate SR latch is given in Fig Q.5b. [8 marks]

	x_1x_2 = 00	01	11	10
a	ⓐ, 0	ⓐ, 1	b , -	ⓐ, 1
b	a , -	ⓑ, 0	ⓑ, 0	ⓑ, 0

Fig Q.5a

Q(n)	Q(n+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Fig Q 5b

- End of the Question Paper –