GENERAL SIR JOHN KOTELAWALA DEFENCE UNIVERSITY
Faculty of Engineering
Department of Electrical, Electronic and Telecommunication Engineering

BSc Engineering Degree
End Semester Examination – July 2022
Semester 1 - Intake 39 (2nd Batch)

ET1102 – BASIC ELECTRONICS

Time allowed: 2 hours 12th July 2022

ADDITIONAL MATERIÁL PROVIDED

Nil

INSTRUCTIONS TO CANDIDATES

- This paper contains 5 questions and answer **all** the questions on answer booklets.
- This paper contains 7 pages with the cover page.
- This is a closed book examination.
- Those sitting for this examination will be allowed to use a non-programmable calculator.
- This examination accounts for 70% of the module assessment. A total maximum mark obtainable is 100. The marks assigned for each questions and parts thereof are indicated in square brackets.
- If you have any doubt as to the interpretation of the wordings of the question, make your own decision, but clearly state it on the script.
- Assume any reasonable values for any data not given in or provided with the question paper, clearly make such assumptions made in the script.
- All examinations are conducted under the rules and regulations of the KDU.

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Question 01

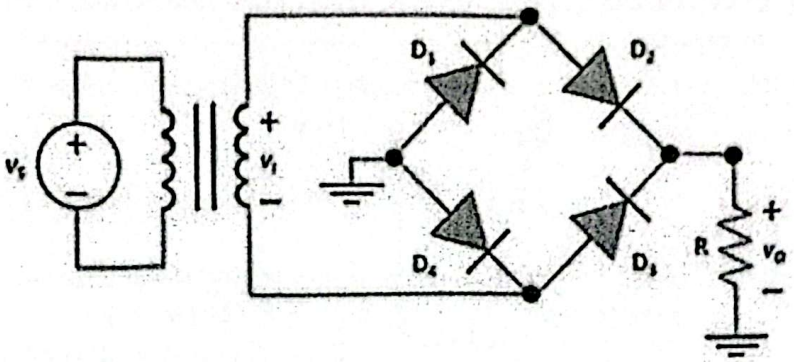

Figure Q1.1

1) A Typical full-wave bridge rectifier circuit is shown in Figure Q1.1 with four silicon diodes. The input voltage (v_I) to the rectifier is a sinewave with 25V amplitude.

   a. Sketch and clearly label v_O output for positive and negative half-cycle of v_I.

   b. Draw the current path for positive and negative half-cycle of v_I.

[10 marks]

2) The output resistance, R is now replaced with a **Zener diode** with the Zener voltage of 5V as shown in Figure Q1.2. Sketch and clearly label v_O output for positive and negative half-cycle of v_I. [10 marks]

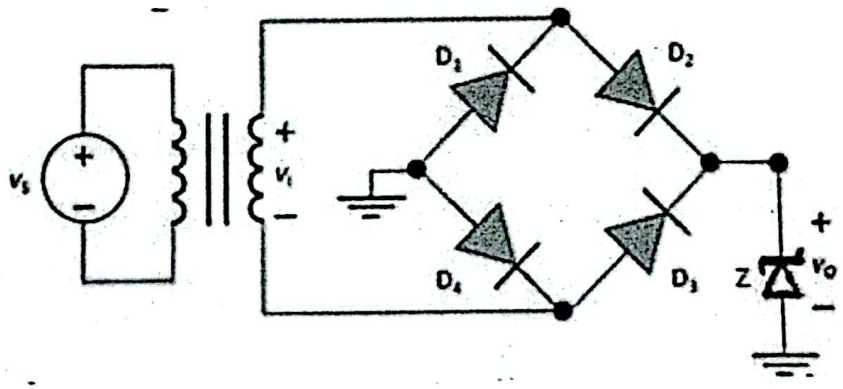

Figure Q1.2

Question 02

1) Briefly explain the usual operating region of transistors when they are used in digital circuits. [5 marks]

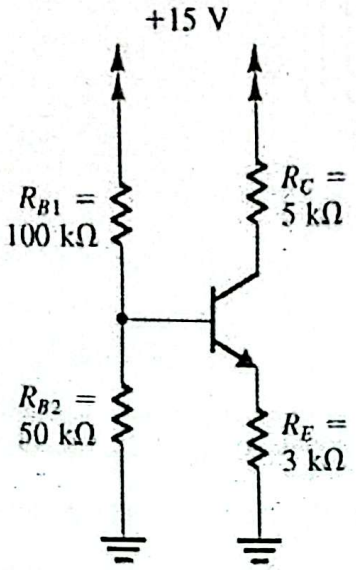

Figure Q2.1

2) Calculate the values of V_E, V_B, V_C, I_B, I_C, V_E for Figure Q2.1. [15 marks]

Question 03 [20 marks]

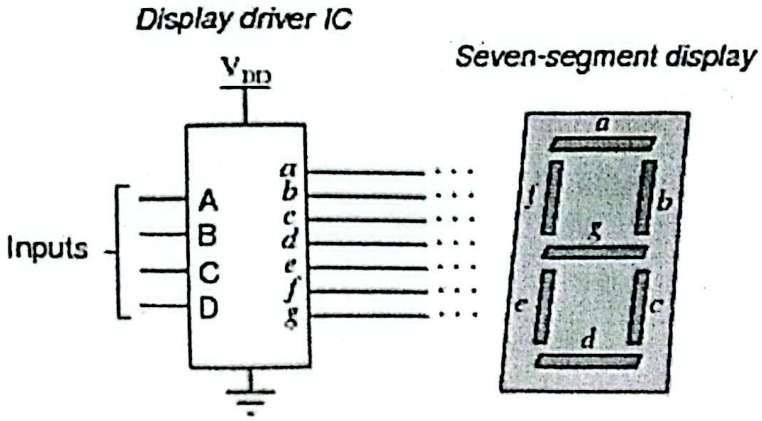

Figure Q3.1

As shown in Figure Q3.1, you are going to design a BCD to 7-Segment Display Decoder to convert four binary numbers (ABCD) to decimal numbers in a 7-segment display. 7 LED segments carries "a", "b", "c", "d", "e", "f" and "g pins where each of the pins will illuminate the specific segment only. The input, output and display are demonstrated in the Table Q3 and "1" output represents an active display segment, while a "0" output represents an inactive segment.

1) Derive Karnaph map (K-map) for a, b, c, d, e, f, g output.
   Hint :
   For non-specified truth table rows use the "don't care" symbols (letter X).
   The horizontal axis of the K-map represents C and D values and the vertical axis represents the values of A and B.

Table Q3

INPUT				OUTPUT							
A	B	C	D	a	b	c	d	e	f	g	Display
0	0	0	0	1	1	1	1	1	1	0	"0"
0	0	0	1	0	1	1	0	0	0	0	"1"
0	0	1	0	1	1	0	1	1	0	1	"2"
0	0	1	1	1	1	1	1	0	0	1	"3"
0	1	0	0	0	1	1	0	0	1	1	"4"
0	1	0	1	1	0	1	1	0	1	1	"5"
0	1	1	0	1	0	1	1	1	1	1	"6"
0	1	1	1	1	1	1	0	0	0	0	"7"
1	0	0	0	1	1	1	1	1	1	1	"8"
1	0	0	1	1	1	1	1	0	1	1	"9"

Question 04

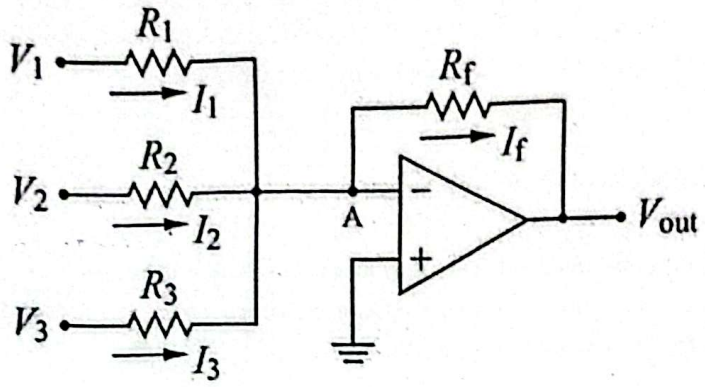

Figure Q4.1

1) Identify the circuit type of Figure Q4.1. [3 marks]

Inverting Summing

2) Derive an expression for the output voltage of the circuit in Figure Q4.1 in terms of the four input voltages. Simplify your result as much as possible. [7 marks]

3) Sate the assumptions that you have made to derive the above expression for Q4 (2). [3 marks]

4) Determine v_0 in Figure Q4.2 as a function of v_1 , v_2 , and v_3 . Simplify your result as much as possible. [7 marks]

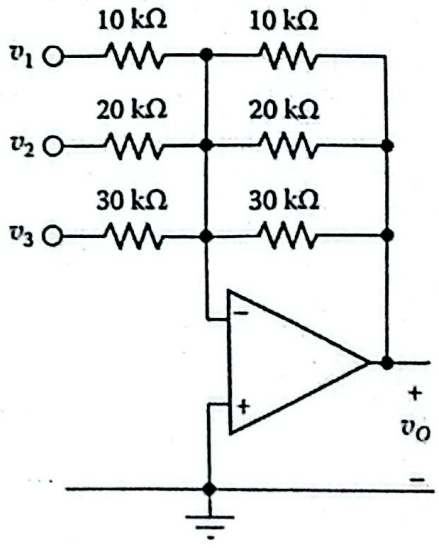

Figure Q4.2

Question 05

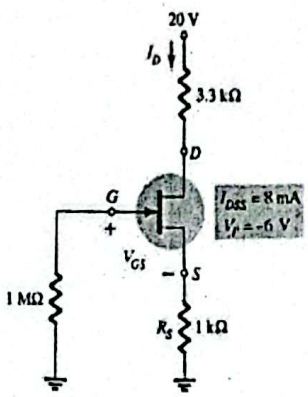

Figure 5

Determine the values for I_D, V_{DS} ,V_S ,V_G and V_D based on V_{GS} = -2.6v. [20 marks]

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

-End of Question Paper-