Pinbelegung Prozessor und Pinheader

Stand: 30.07.2015 v3.1

	Pin Header	Pin Proz.	Name	Modus	Signalname auf Cape	Pin Ziel-komponente	
WLAN							
	8.11	R12	GPIO1_13	mmc2_dat1	WL_SDIO_D1_WIFI	11	
	8.12	T12	GPIO1_12	mmc2_dat0	WL_SDIO_D0_WIFI	10	
	8.13	T10	EHRPWM2B	gpio0[23]	WL_EN_WIFI	40	
	8.14	T11	GPIO0_26	gpio0[26]	WL_IRQ_WIFI	14	
	8.15	U13	GPIO1_15	mmc2_dat3	WL_SDIO_D3_WIFI	13	
	8.16	V13	GPIO1_14	mmc2_dat2	WL_SDIO_D2_WIFI	12	
	8.18	V12	GPIO2_1	mmc2_clk	WL_SDIO_CLK_WIFI	8	
	8.26	**V6**	**GPIO1_29**	**gpmc_csn0**	BUF_EN_WIFI	-	
	9.15	T13	GPIO2_0	mmc2_cmd	WL_SDIO_CMD_WIFI	6	
		Dieser Pin ist via R160 und R161 mit dem Pin R13 (GPIO1_16) doppelt belegt					
	9.41	D14	CLKOUT2	clkout2	WL_SLOW_CLK_WIFI	36	
GSM							
	9.12	U18	GPIO1_28	gpio1[28]	ON/OFF*_GSM	R12	
	~~9.14~~	~~U14~~	~~EHRPWM1A~~	~~gpio1[18]~~	~~HW_SHUTDOWN*_GSM~~	~~R13~~	
		Buffer wird neu direkt über 3V3B aktiviert					
	9.16	T14	EHRPWM1B	gpio1[19]	VAUX/PWRMON_GSM	R11	
	9.19	D17	I2C2_SCL	uart1_rtsn	**C105/RTS_GSM**	**L14**	
	9.20	D18	I2C2_SDA	uart1_ctsn	**C106/CTS_GSM**	**P15**	
	9.24	D15	UART1_TXD	uart1_txd	**C103/TXD_GSM**	**N15**	
	9.26	D16	UART1_RXD	uart1_rxd	**C104/RXD_GSM**	**M15**	
	9.42	C18	GPIO0_7	gpio0[7]	BUF_ENABLE_GSM	-	
BLE							
	9.21	B17	UART2_TXD	gpio0[3]	uart2_txd	17	
	9.22	A17	UART2_RXD	gpio0[2]	uart2_rxd	15	
	9.23	V14	GPIO1_17	gpio1[17]	P0.13_BLE	19	Reserve
	9.27	C13	GPIO3_19	gpio3[19]	P0.12_BLE	18	Reserve
Display Touch							
	9.17	A16	I2C1_SCL	I2C1_SCL	SCL_LCD	7	
	9.18	B16	I2C1_SDA	I2C1_SDA	SDA_LCD	5	
Display							
	8.7	R7	TIMER4	gpio2[2]	/INT_LCD	1	
	8.8	T7	TIMER7	gpio2[3]	/WAKE_LCD	2	
	8.9	T6	TIMER5	gpio2[5]	/RST_LCD	3	
	8.10	U6	TIMER6	gpio2[4]	PWCTRL_LCD	42	
	8.19	U10	EHRPWM2A	ehrpwm2A	LEDCTRL_LCD	48	
	8.27	U5	GPIO2_22	lcd_vsync	VSYNC_LCD	11	
	8.28	V5	GPIO2_24	lcd_pclk	DCLK_LCD	13	
	8.29	R5	GPIO2_23	lcd_hsync	HSYNC_LCD	12	
	8.30	R6	GPIO2_25	lcd_ac_bias_en	NC_DE_LCD	9	
	8.31	V4	UART5_CTSN	lcd_data14	R6	34	
	8.32	T5	UART5_RTSN	lcd_data15	R7	33	
	8.33	V3	UART4_RTSN	lcd_data13	R5	35	
	8.34	U4	UART3_RTSN	lcd_data11	R3	37	
	8.35	V2	UART4_CTSN	lcd_data12	R4	36	
	8.36	U3	UART3_CTSN	lcd_data10	G7	24	
	8.37	U1	UART5_TXD	lcd_data8	G5	26	
	8.38	U2	UART5_RXD	lcd_data9	G6	25	

8.39	T3	GPIO2_12	lcd_data6	G3	28
8.40	T4	GPIO2_13	lcd_data7	G4	27
8.41	T1	GPIO2_10	lcd_data4	B7	15
8.42	T2	GPIO2_11	lcd_data5	G2	29
8.43	R3	GPIO2_8	lcd_data2	B5	17
8.44	R4	GPIO2_9	lcd_data3	B6	16
8.45	R1	GPIO2_6	lcd_data0	B3	19
8.46	R2	GPIO2_7	lcd_data1	B4	18

Bereits auf BBB belegt
eMMC

8.3	R9	GPIO1_6	mmc1_dat6
8.4	T9	GPIO1_7	mmc1_dat7
8.5	R8	GPIO1_2	mmc1_dat2
8.6	T8	GPIO1_3	mmc1_dat3
8.20	V9	GPIO1_31	mmc1_cmd
8.21	U9	GPIO1_30	mmc1_clk
8.22	V8	GPIO1_5	mmc1_dat5
8.23	U8	GPIO1_4	mmc1_dat4
8.24	V7	GPIO1_1	mmc1_dat1
8.25	U7	GPIO1_0	mmc1_dat0

Freie Pins

8.17	U12	GPIO0_27	frei	x
9.28	C12	SPI1_CS0	frei	x
9.29	B13	SPI1_D0	frei	x
9.30	D12	SPI1_D1	frei	x
9.31	A13	SPI1_SCLK	frei	x
9.32		VADC	frei	x
9.33	C8	AIN4	frei	x
9.34		AGND	frei	x
9.35	A8	AIN6	frei	x
9.36	B8	AIN5	frei	x
9.37	B7	AIN2	frei	x
9.38	A7	AIN3	frei	x
9.39	B6	AIN0	frei	x
9.40	C7	AIN1	frei	x

Power und Reset x

8.1	GND		x
8.2	GND		x
9.1	GND	DGND	x
9.2	GND	DGND	x
9.3	DC_3.3V	DGND	x
9.4	DC_3.3V	DGND	x
9.5	VDD_5V	VDD_3V3B	x
9.6	VDD_5V	VDD_3V3B	x
9.7	SYS_5V	VDD_5V	x
9.8	SYS_5V	VDD_5V	x
9.9	PWR_BUT	SYS_5V	x
9.10	SYS_RESETn	SYS_5V	x
9.43	GND	PWR_BUT	x
9.44	GND	SYS_RESETn	x
9.45	GND	DGND	x
9.46	GND	DGND	x
		DGND	x

			DGND	x

Darf nicht verwendet werden / muss hochohmig sein

(9.15)	R13	GPIO1_16_A	oder R160 entfernen	
	Dieser Pin ist via R160 und R161 mit dem Pin RT3 (MMC2_CMD) doppelt belegt			x

Sollte nicht verwendet werden

9.25	A14	GPIO3_21	*Clock für HDMI Audio