# SW Pipelined VLIW

Zurich University of Applied Sciences
School of Engineering
InES Institute of Embedded Systems

```
L9:
        B       .S2     L9          ; @@
||      LDW     .D2     *B5++, B4   ; @@@@
||      LDW     .D1     *A3++, A0   ; @@@@

        STW     .D1     A5, *A4++   ;
||      MPYSP   .M1X    B4, A0, A5  ; @@
||      SUM     .L2     B0, 1, B0   ; @@@
```

Executed in parallel

Iteration being performed (@@ = n+2)

- Example loop kernel for array multiplication on TI DSP
- Two VLIW Instructions
- Loops pipelined