Lecture Intro

Design of Embedded Hardware and Firmware

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TSM_EmbHardw
Feb. 22, 2016

Prof. A. Habegger
Bern University of Applied Sciences

Agenda

▶ **Course Information**
    ▶ Main Course Topics   ▶ Objectives and Organization

▶ **Practical Work**

▶ **Let's do a 20' test**

▶ **Homework**

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Course Information
Topics
Obj and Org
Lab
Test
Homework

Rev. – Intro.2

Where to Get the Stuff

All material will be available online on MS Engineering Moodle platform. Grading scheme may change within coming two weeks.

Duration
: Three lectures a week @ fourteen weeks.

Grading
: 1st intermediary test (20 %)
2nd intermediary test or miniProject (20 %)
Final exam at the end (100 %, 80 %, or 60 %)

Docs
: Online on MSE Moodle platform
`http://moodle.msengineering.ch`

Course
: TSM_EmbHardw

PWD
: SoPC

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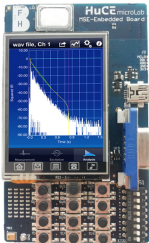Course Information
Topics
Obj and Org
Lab
Test
Homework

Rev. – Intro.3

Course Description

- This module introduces the student to advanced concepts in modern embedded systems engineering.

- The course concentrates on the architectures used in FPGA/SoC development and associated interfacing.

- Exercises are practice-oriented and will be tested on a mobile development platform. The goal is to consolidate acquired knowledge through hands-on practice.

- Each student get a development board until the end of the semester. (At last course day you have to give the board back to the lecturer.)

- The board documentation is public available on HuCE wiki platform (QR-Code on box cover or URL `https://www.microlab.ti.bfh.ch/wiki/huce:microlab:projects:internal:mse-em-board`)

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Course Information
Topics
Obj and Org
Lab
Test
Homework

Rev. – Intro.4

Notes

Learning objectives and acquired competencies

- The student will be able to design systems using state machines, soft-core processors, micro sequencers as well as interfacing peripherals to these automatons.

- The student will be able to design and commission complete designs in an FPGA.

- The student will understand and be able to apply methodologies and strategies for test and verification of embedded systems.

- Exercises will be completed and applied on an Altera Cyclone IV device.

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Course Information
Topics
Obj and Org
Lab
Test
Homework

Rev. – Intro.5

Notes

Course Organization

- 1st trimester (7 weeks): will be given by Andreas Habegger with a main focus on **Hardware Design**, **SoPC architectures**, **DMA transfers**.

- 2nd trimester (7 weeks): will be given by Hans Doran Kluter with a main focus on **HW/SW partition** and **optimization**.

- Material on Moodle `http://moodle.msengineering.ch`

- Each student get a development board

- The development environment is a live system based on Debian Linux

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Course Information
Topics
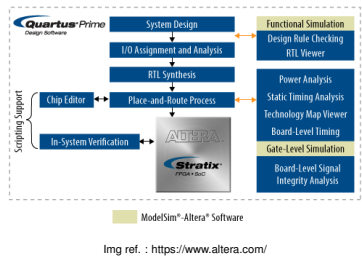Obj and Org
Lab
Test
Homework

Rev. – Intro.6

Notes

Practical Work : Tool-Set

- ▶ Hands-on-work practice:
    - ▶ QuartusPrime Lite Edition from Altera.
    - ▶ Qsys
    - ▶ Eclipse (C,C++)
- ▶ System setup:
    - ▶ You bring your own laptop...
    - ▶ You install tools and drivers at your own...
    - ▶ You run an Ubuntu distribution from USB stick.

Img ref. : https://www.altera.com/

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Course
Information
Topics
Obj and Org

Lab

Test

Homework

Rev. – Intro.7

Notes

Practical Work : MSE - Embedded Board

https://www.microlab.ti.bfh.ch/wiki/huce:microlab:
projects:internal:mse-em-board

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Course
Information
Topics
Obj and Org

Lab

Test

Homework

Rev. – Intro.8

Notes

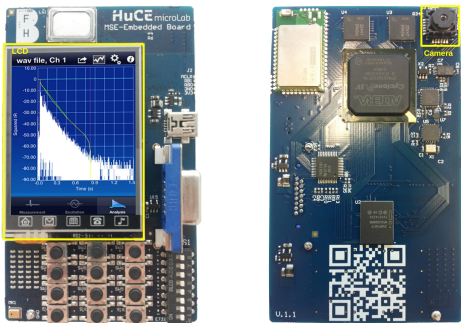## Practical Work 1st trimester (AH)

- ▶ Introduction to SoPC design tools: Quartus, Qsys, Eclipse.

- ▶ Build your own peripheral interface: LCD controller interface.

- ▶ Optimization of memory access: DMA for LCD controller interface.

- ▶ Optional: Camera data acquisition.

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Course
Information
Topics
Obj and Org

Lab

Test

Homework

Rev. – Intro.9

Notes

Topics of 2nd trimester (HD)

- ▶ Introduction - HW/SW co-design

- ▶ Scheduling and bus systems

- ▶ SW optimization

- ▶ Caches

- ▶ Algorithm Optimisations / HW acceleration / custom instructions

- ▶ Pipelines (HW and processor)

- ▶ Project presentation

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Course Information
Topics
Obj and Org
Lab
Test
Homework

Rev. – Intro.10

Notes

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Today...

- ▶ Evaluation Test

- ▶ Introduction to FPGAs (refresh of the topic only)

- ▶ Introduction to "System On Programmable Chip" (SoPC) focusing on Altera (Nios II – Avalon Bus)

- ▶ Board distribution and initial platform test

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Course Information
Topics
Obj and Org
Lab
Test
Homework

Rev. – Intro.11

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Homework

- ▶ Repeat stuff discussed in this week session

- ▶ Finish practical exercises of this week

- ▶ Repeat VHDL basics

- ▶ Check one day before next session for new course material

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Course Information
Topics
Obj and Org
Lab
Test
Homework

Rev. – Intro.12

Notes

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