Zürcher Hochschule
für Angewandte Wissenschaften

School of Engineering

InES Institute of Embedded Systems

TSM_EmbHardw
Exercises Week 8 / Lecture 1

Exercise Set A

Project: Port the solution file of a processor/LCD/DMA hardware onto your FPGA board. Get it to work

Exercise Set B

Exercise 1: Estimations – broadly estimate the processing time required for an implementation of the Sobel algorithm.

Exercise 2: The standard in testing is that a second engineer designs tests according to his/her understanding of a specification. This redundancy principle is intended to improve the probability that the specification and hence the final product is less susceptible to a misunderstanding of the specification or the clients intentions. In the case of units or algorithms such as implementations of the Sobel algorithm, it can be expected that the development engineer write his own tests.

Design a unit test for the Sobel algorithm.

Exercise 3: Estimate the amount of bus-time used by a single processor performing the Sobel algorithm test on the (50 MHz) NIOS II hardware you developed in part one of the module.

Exercise 4: V-Model COM – computer on modules on boards are a popular way of avoiding the expense of designing a processor board but still offering maximum flexibility with respect to design options. The market is such that these boards stop being cost-effective at between 500 and 1000 pieces per year, somewhere in-between it becomes cheaper to design-in the hardware.

Your company uses a COB module (http://phytec.com/products/system-on-modules/phycore/mpc5121e-tiny/) in one of their products. This product sells at 500 pcs. a year but the product manager is targeting 2000 pa. in the next three years. This module costs 279 USD retail in piece rates of 1000. Assume Phytec make a 50% margin on the board. Using your company's internal billing rate (for instance 60 CHF/hr and 172*12 billable hours per year) and estimating the development time if you were to start without any prior information, calculate when it becomes cheaper to do a hardware design-in.

Hint: Structure the development process using the V-Model and estimate times for the various points of the V-Model. Use the slide on page 24 of the link below to divide up the time proportionally http://de.slideshare.net/StephanCadene/embedded-mar1913
There is no wrong or right answer.

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Exercises: Exam Preparation

Exercise 1:
Draw the system-architecture diagram the binding and scheduling for a single processor system with DMA.

Exercise 2:
What O( ) function is the Sobel algorithm? (Google is your friend)

Exercise 3:
Explain what is meant by design space exploration and how this can lead to optimised designs. How do you decide what optimisations should be performed? How many iterations do you think a design needs?

Exercise 4: Current SoC design consists of defining a HW architecture and connecting the modules by a bus. What advantages and disadvantages are there in using such a process. What advantages might there be in describing the entire design in C/C++ and letting a synthesiser complete both the HW and software design?