Zürcher Hochschule
für Angewandte Wissenschaften

School of Engineering

InES Institute of Embedded Systems

TSM_EmbHardw
Exercises Week 12 / Lecture 5

Exercise Set A

Project n: Work on your project

Exercise Set B / Exam Preparation

Exercise 1: Custom Instruction and HW pipelining

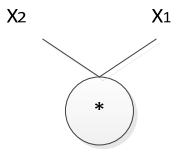
You have program code to perform the following operation

$$y = 5 * x_2*(x_1+x_2) = 5 * (x_1 * x_2 + x_2^2)$$

a.) Which expression form is cheaper to implement by measure of hardware resources assuming that each individual operation gets its own FU (functional unit i.e. adder or multiplier)?

Hint:

$x_1 * x_2$ can be implemented as:



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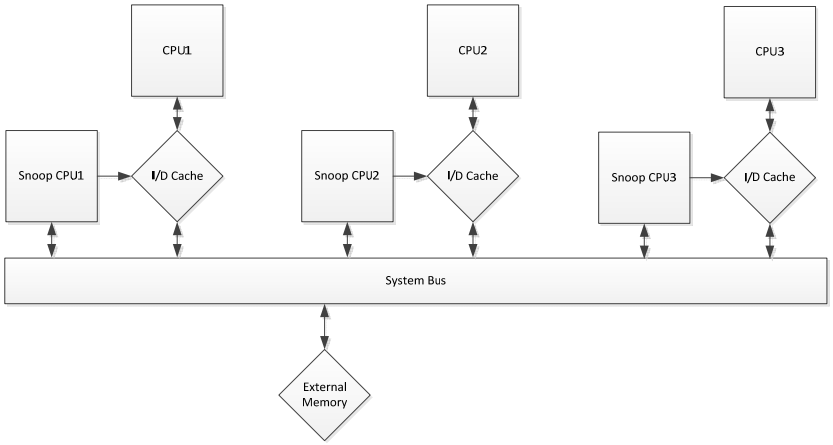
b.) If both designs were to be pipelined what is the resource usage then?

c.) If your NIOS is clocked at 50MHz. and your FPGA fabric clocked at 125MHz. the multiplier has a latency of 3 FPGA clock cycles and the adder 2 clock cycles, is the pipelined design a suitable candidate for a NIOS II combinational custom instruction?

Exercise 2: Cache coherence and MSI protocol:

Given the architecture below, presuming that the processors are clocked with the same clock and given the pieces of code from each of the processors, further below and knowing that `load a` means load some CPU register with the main memory variable a, and `add c, a, b` means add a and b and store the result in c, answer the following questions.



time	CPU 1	CPU2	CPU3
t = 0	nop	nop	nop
t = 1	nop	nop	load a
t = 2	load a	load b	load b
t = 3	load b	load d	load d
t = 4	load c	add d, a, b	nop
t = 5	add c, a, b	load c	add e, a, b
t = 6	sub f, a, b	load e	sub b, a, e
t = 7		sub c, c, e	move d, b

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a.) If there were no cache coherence protocol, at what time would variable d lose its coherence?

b.) @ t = 0, what state (clean, dirty, uncached) in memory is variable a in?

c.) @ t = 1, what state (clean, dirty, uncached) in memory is variable a in?

d.) @ t = 1, what state (invalid, shared, exclusive) in which cache is variable a in?

e.) @ t = 4, what state (invalid, shared, exclusive) in which cache is variable a in?

f.) If variable a is the first data to be written into line1 of CPU 1, what state does line 1 have at time t = 0?

g.) @ t = 5, what state (invalid, shared, exclusive) in which cache is variable a in?

h.) Using the snoop protocol explain what happens @ t= 4

i.) Using the snoop protocol explain what happens @ t= 7 CPU3

j.) When does the epoch read only on variable a end?

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Exercise 3: Software pipelining

Software pipeline this loop

```
for (i=1, i<100, i++) {
     load A[i];
     inc A[i];
     store A[i];
}
```