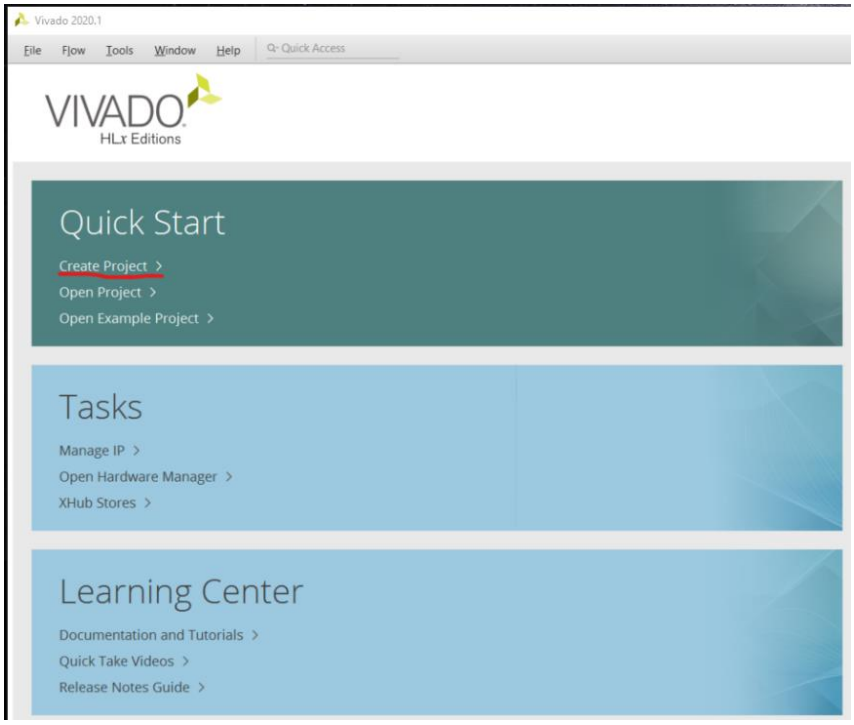
ECEN 240 Lab 6 - ALU

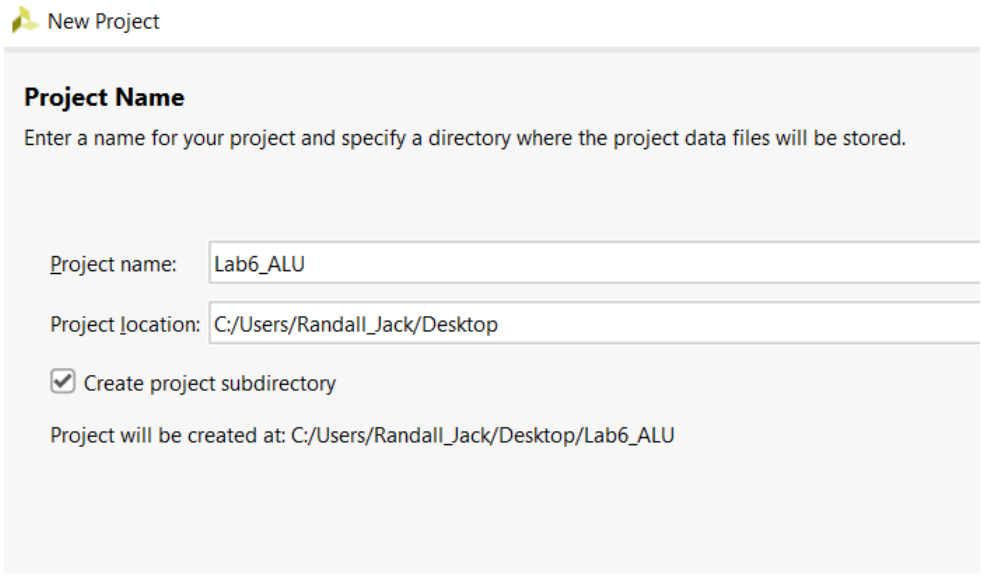
(Vivado and SystemVerilog Instructions)

1. Download the Lab6_ALU.sv file from canvas and place on your desktop. You will use this momentarily.

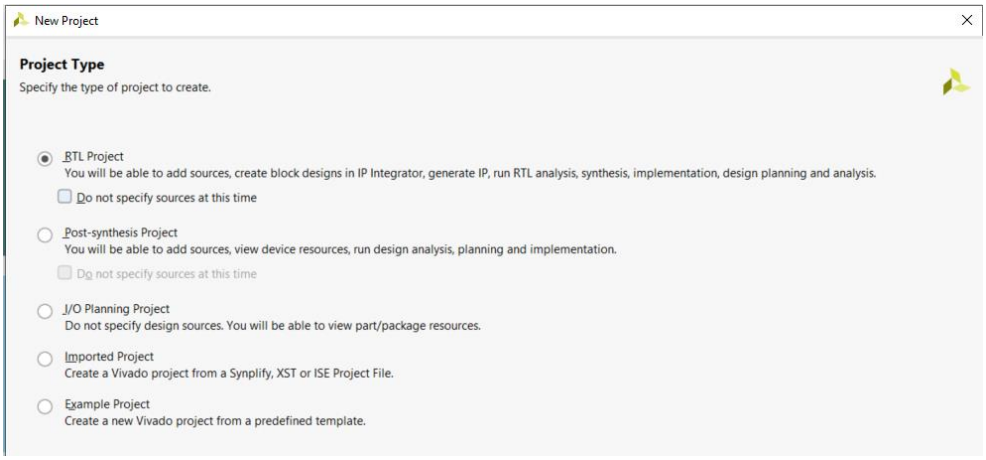
2. Start Vivado and Select “Create Project”



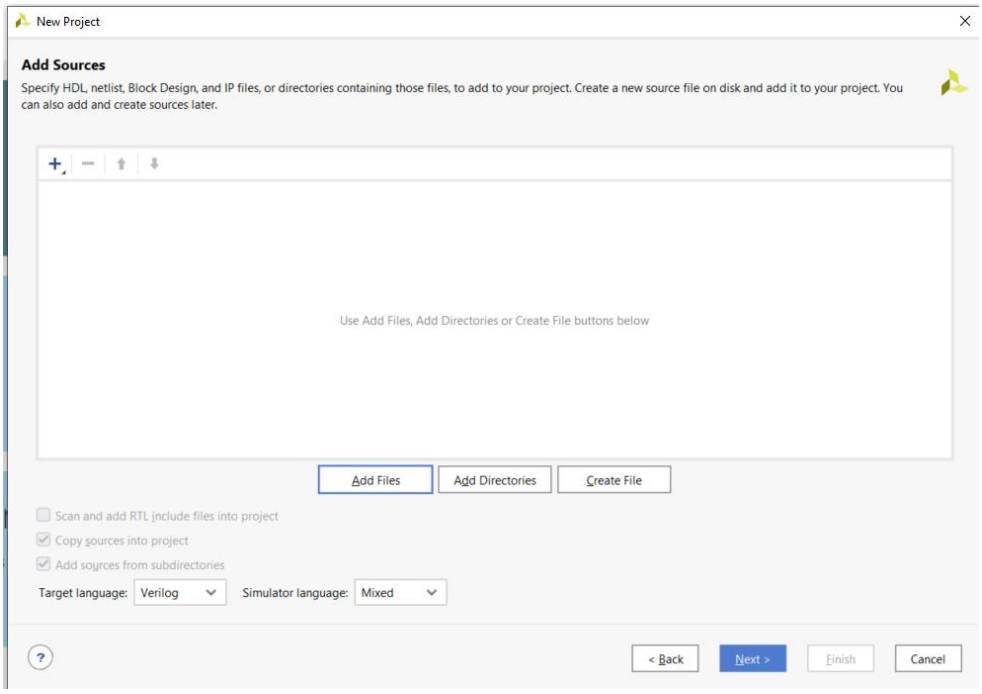
3. Type the project name as “Lab6_ALU” and select “Next”



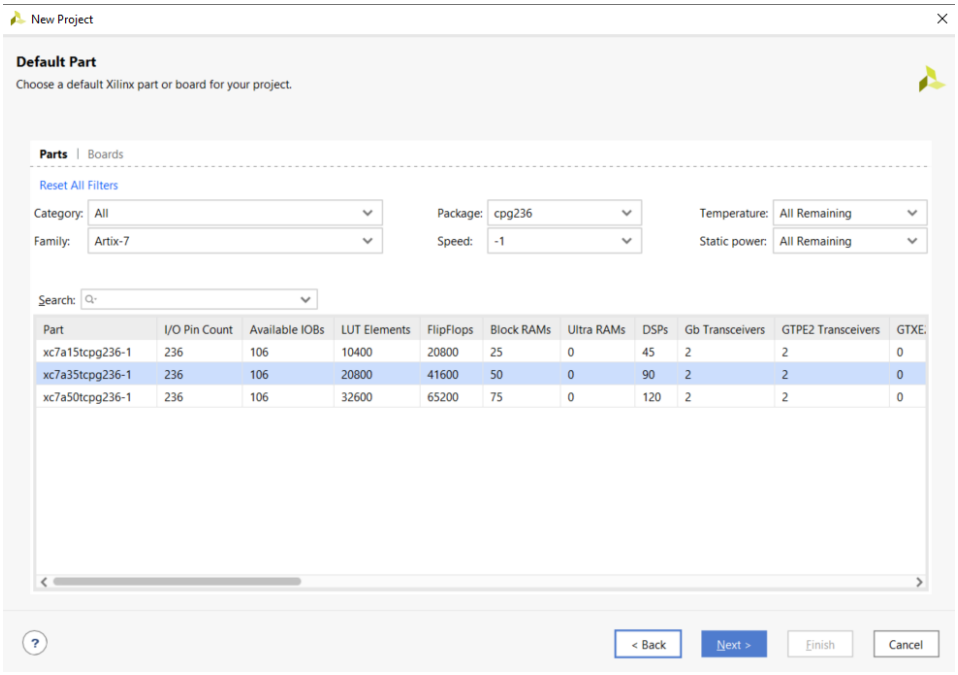
4. Select RTL Project and then “Next”



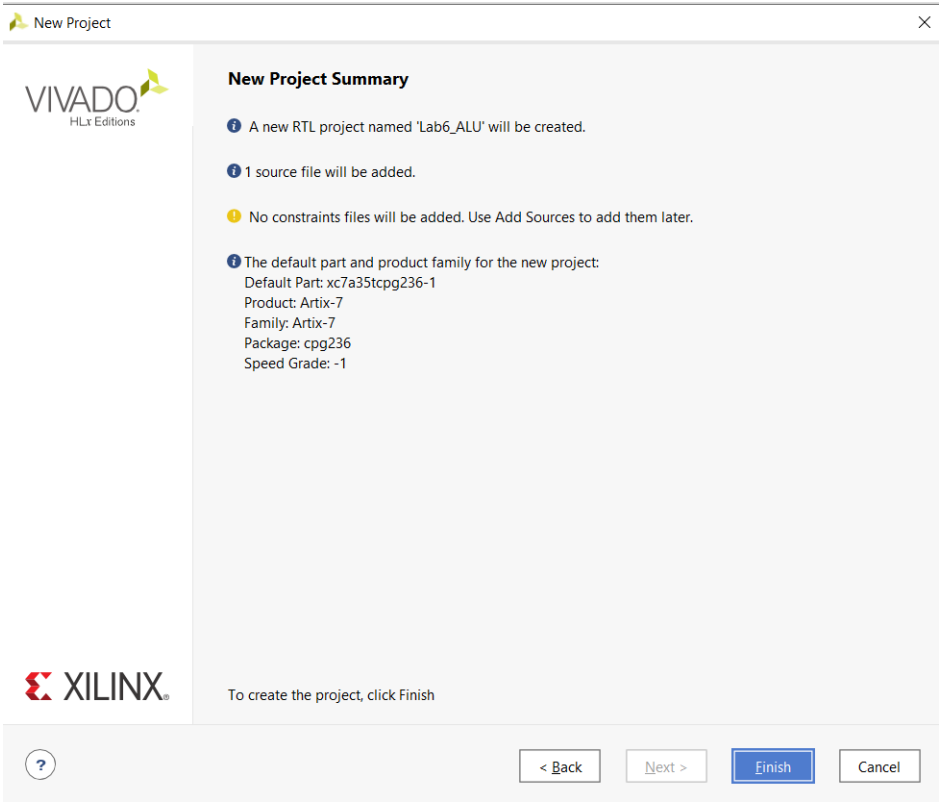
5. Select “Add Files” and navigate to the “Lab6_ALU.sv” file you downloaded from the “Lab6” Canvas module. Click on the file and select OK.



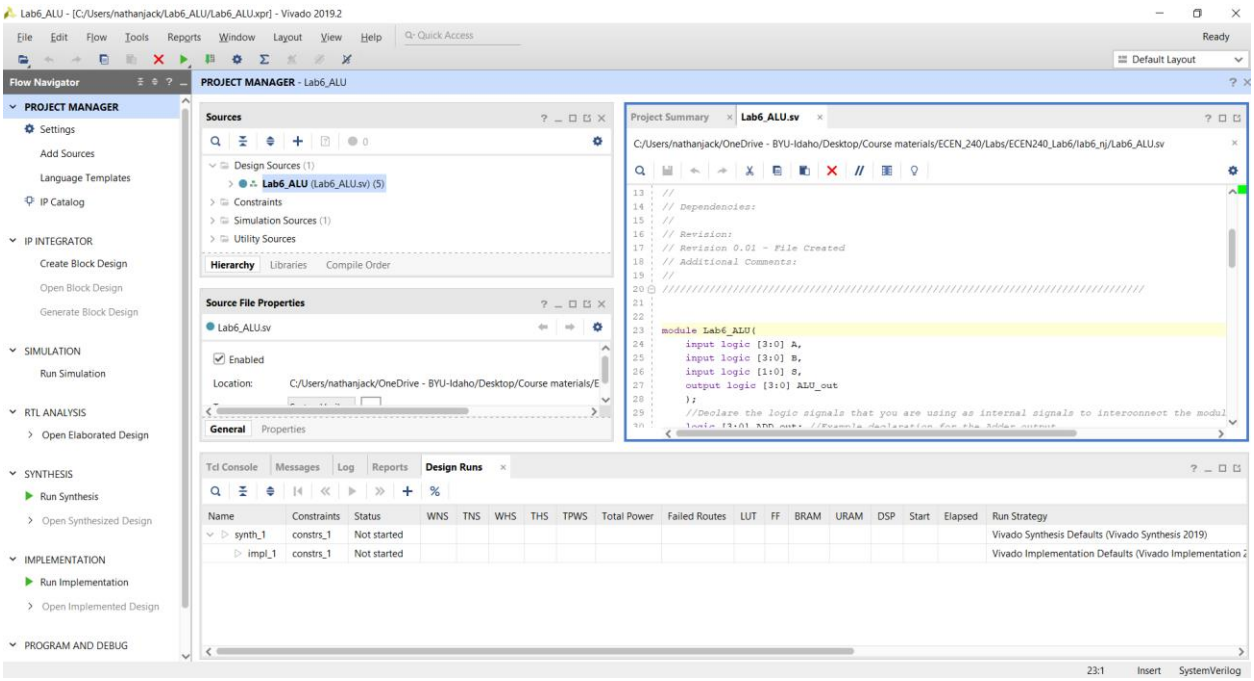
6. Skip the “Add Constraints” option and just select “Next”
7. Configure the project with the correct FPGA filter Settings:
    - Family: Artix-7.
    - Package: cpg236
    - Speed: -1
8. Select “xc7a35tcpg236-1” and then “Next”.



9. To Create the project, select “Finish”.



10. Open the “Lab6_ALU.sv” within Vivado file by double clicking on “Lab6_ALU” in the Sources window.

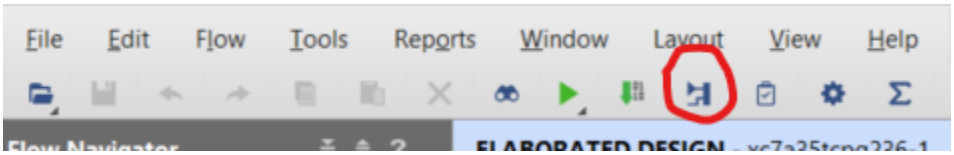


11. There are six modules within this file, Lab6_ALU, ADD4, AND4, OR4, XOR4, and MUX4bit_4to1. You will need to complete all six of these modules:

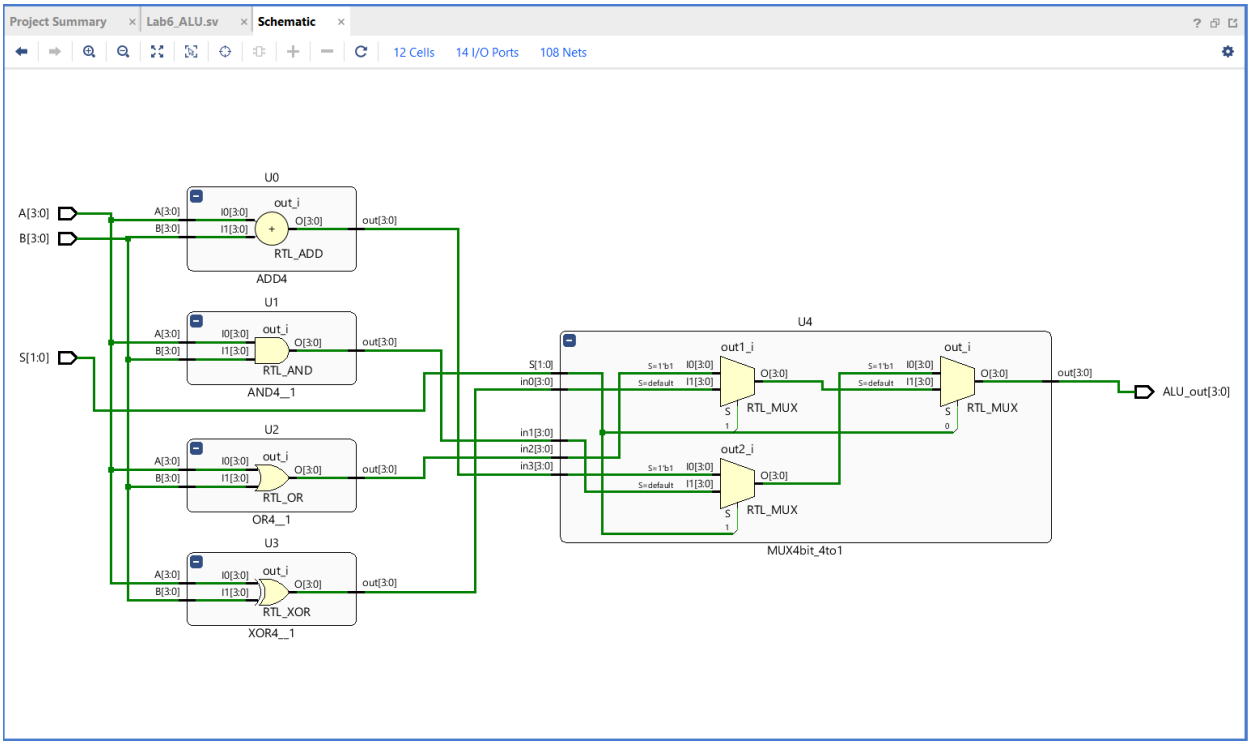
- Lab6_ALU is the top level. All other modules are "placed" or "instantiated" in this module. Each of the modules are wired together using the structural coding style of SystemVerilog. This module also has ports that connect to the switches, pushbuttons and LEDs on the Basys3 board.
- ADD4, AND4, OR4, XOR4 each have one assign statement. For example, to perform the add function in the "ADD4" module, type: assign out = A + B;
- MUX4bit_4to1 will be implemented with three, 2to1 four-bit multiplexers.

S[1:0]	Function
00	XOR
01	AND
10	OR
11	ADD

12. Open the elaborated design (side menu). Once this is done, click on the schematic symbol on the side menu (under RTL ANALYSIS) or at the top of the Vivado screen.



13. You will see a schematic diagram of the synthesized design. To view the various modules of your part of the design, click on the "+" of each of the modules to expand their views. You should be able to see your elaborated schematic.

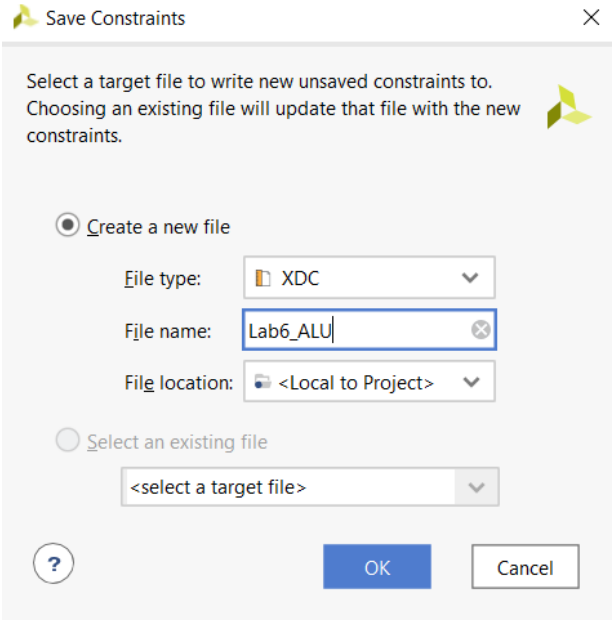


14. Tell Vivado which pins to use on the FPGA chip. Click on the blue "14 I/O Ports" at the top of the schematic menu. Type the following information into the I/O Ports list. This tells Vivado how to map the signal to the switches, seven segment display, and the clocks. You also need to tell Vivado to use 3.3V by selecting the "LVCMOS33" for the I/O Std of each of these signals (to see how these pin assignments were made, look at the last figure in this document).

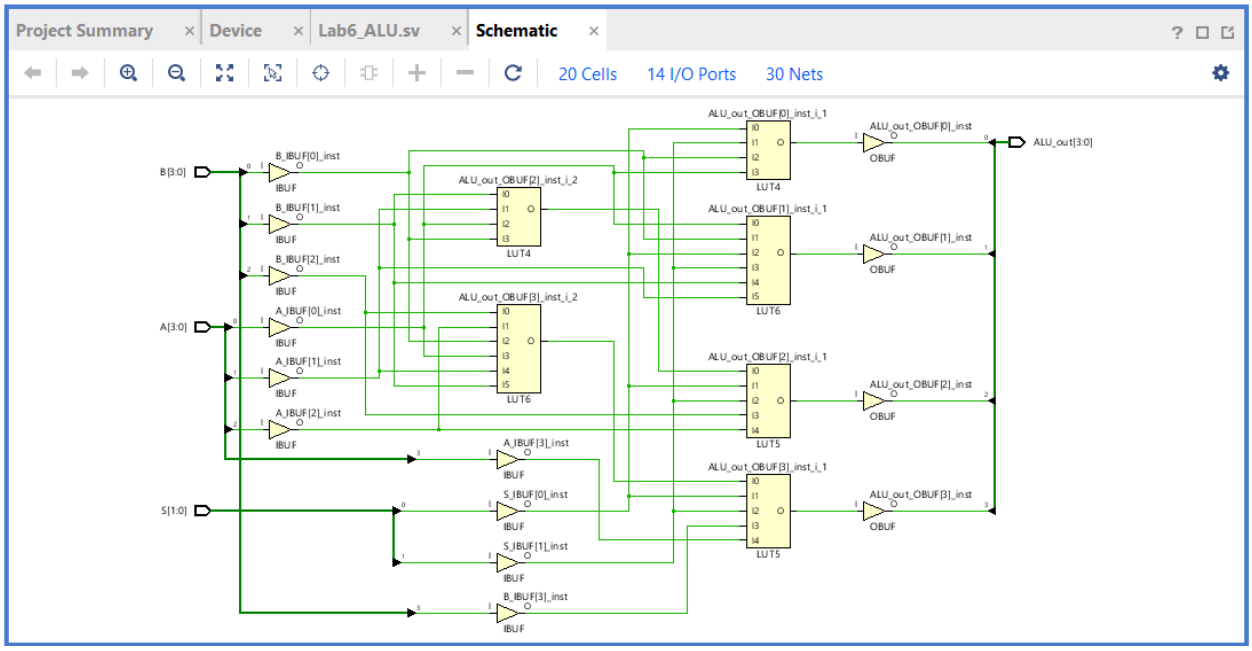
Tcl Console | Messages | Log | Reports | Design Runs | **Find Results** ×

Name	Direction	Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref
A[3]	IN			R2	✓	34	LVCMOS33*	3.300	
A[2]	IN			T1	✓	34	LVCMOS33*	3.300	
A[1]	IN			U1	✓	34	LVCMOS33*	3.300	
A[0]	IN			W2	✓	34	LVCMOS33*	3.300	
ALU_out[3]	OUT			V3	✓	34	LVCMOS33*	3.300	
ALU_out[2]	OUT			V13	✓	14	LVCMOS33*	3.300	
ALU_out[1]	OUT			V14	✓	14	LVCMOS33*	3.300	
ALU_out[0]	OUT			U14	✓	14	LVCMOS33*	3.300	
B[3]	IN			W17	✓	14	LVCMOS33*	3.300	
B[2]	IN			W16	✓	14	LVCMOS33*	3.300	
B[1]	IN			V16	✓	14	LVCMOS33*	3.300	
B[0]	IN			V17	✓	14	LVCMOS33*	3.300	
S[1]	IN			W19	✓	14	LVCMOS33*	3.300	
S[0]	IN			T17	✓	14	LVCMOS33*	3.300	

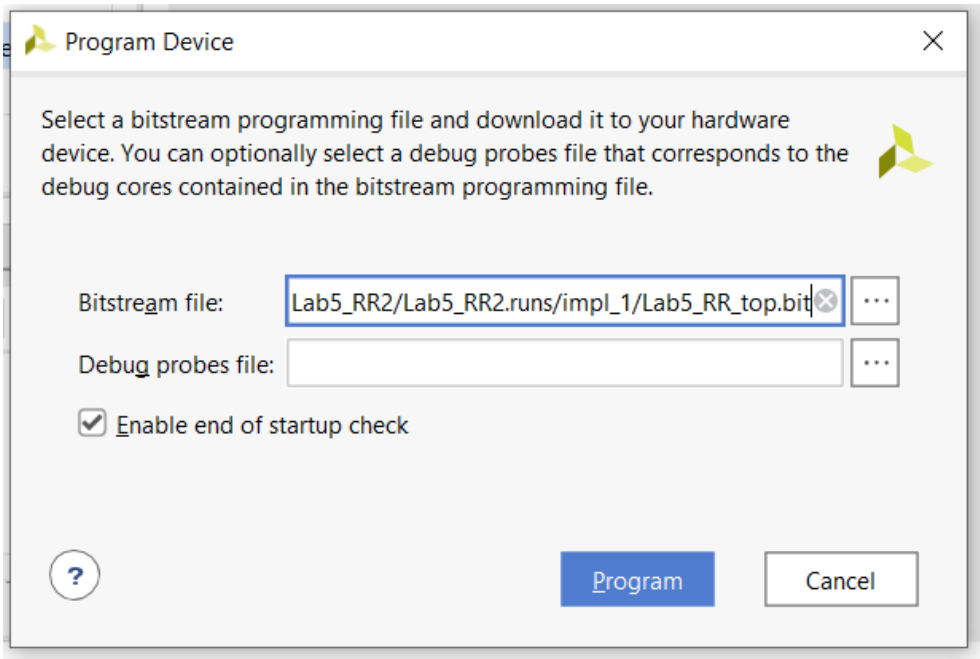
15. Now run the synthesis step (side menu). You will be prompted to save the configuration file (constraint file). Call it “Lab6_ALU”.



16. After successfully running Synthesis, select “Run Implementation” and open the implemented design. Open the schematic of the implemented design. You will see that the implemented design no longer shows basic function of each module. Instead, it shows that Vivado implemented your design with several small ROMs or LUTs (Look UP Tables).



17. Select “Generate Bitstream” from the bottom of the left menu. This is turning your design into a file that can be dumped into the FPGA. It can take a while to generate the bitstream. You can follow the progress by watching top right of the Vivado window.
18. Connect the Basys3 to the computer using the USB cable, and turn on the Basys3 power switch.
19. Select “Open Hardware Manager” from the bottom of the left menu, and select “Open Target”, then “Auto Connect”. Once the computer has connected to the Basys3, you are ready to dump the configuration data into the FPGA. Select “Program Device”.



You are now running the ALU on the Basys3!

- Use the four switches on the far left for your “A” input number
- Use the four switches on the far right for your “B” input number
- Use the left pushbutton as the “S[1]” input
- Use the right pushbutton as the “S[0]” input
- View the output on the middle four LEDs (above the switches)

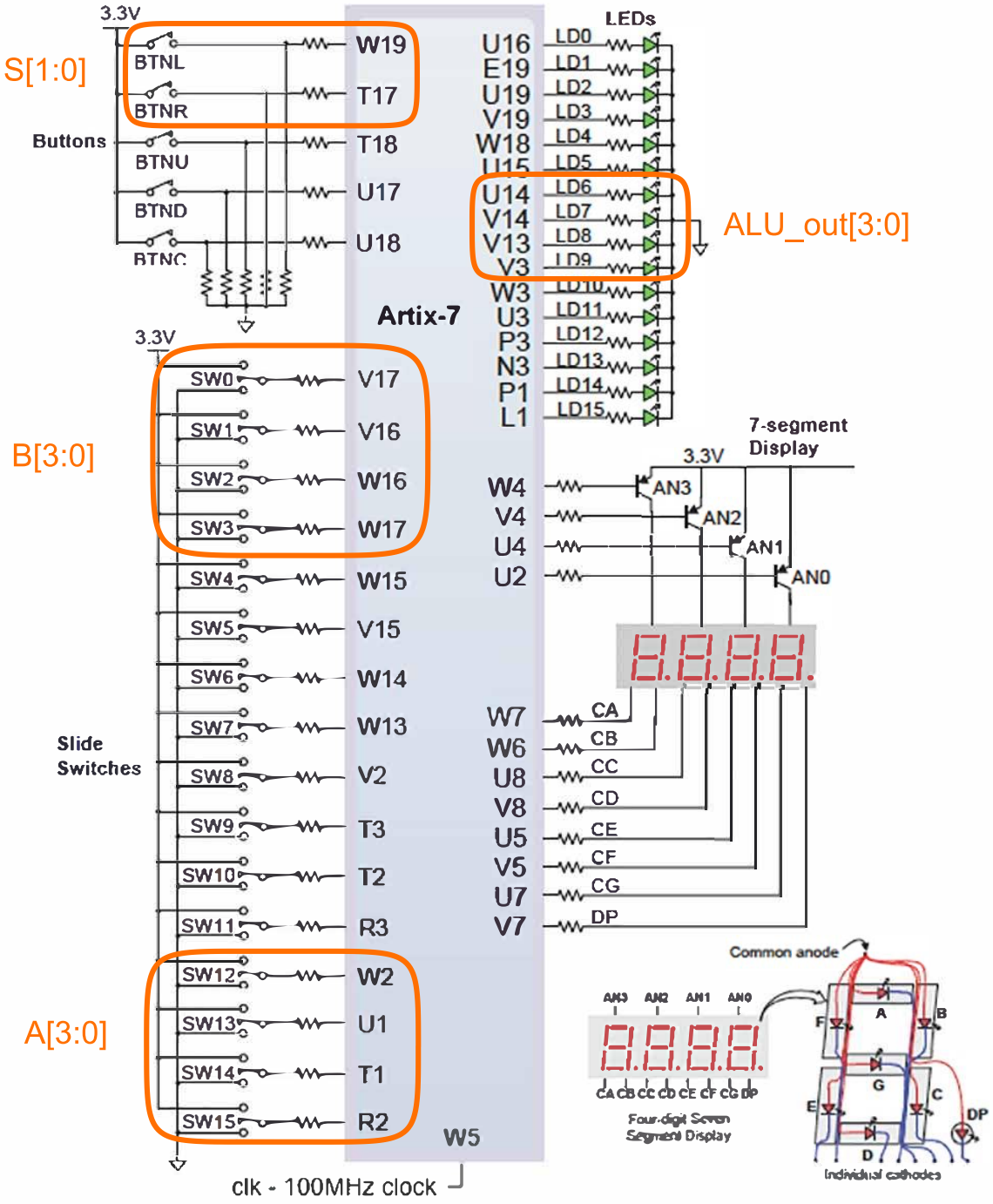


Figure 16. General purpose I/O devices on the Basys 3.