1. Description

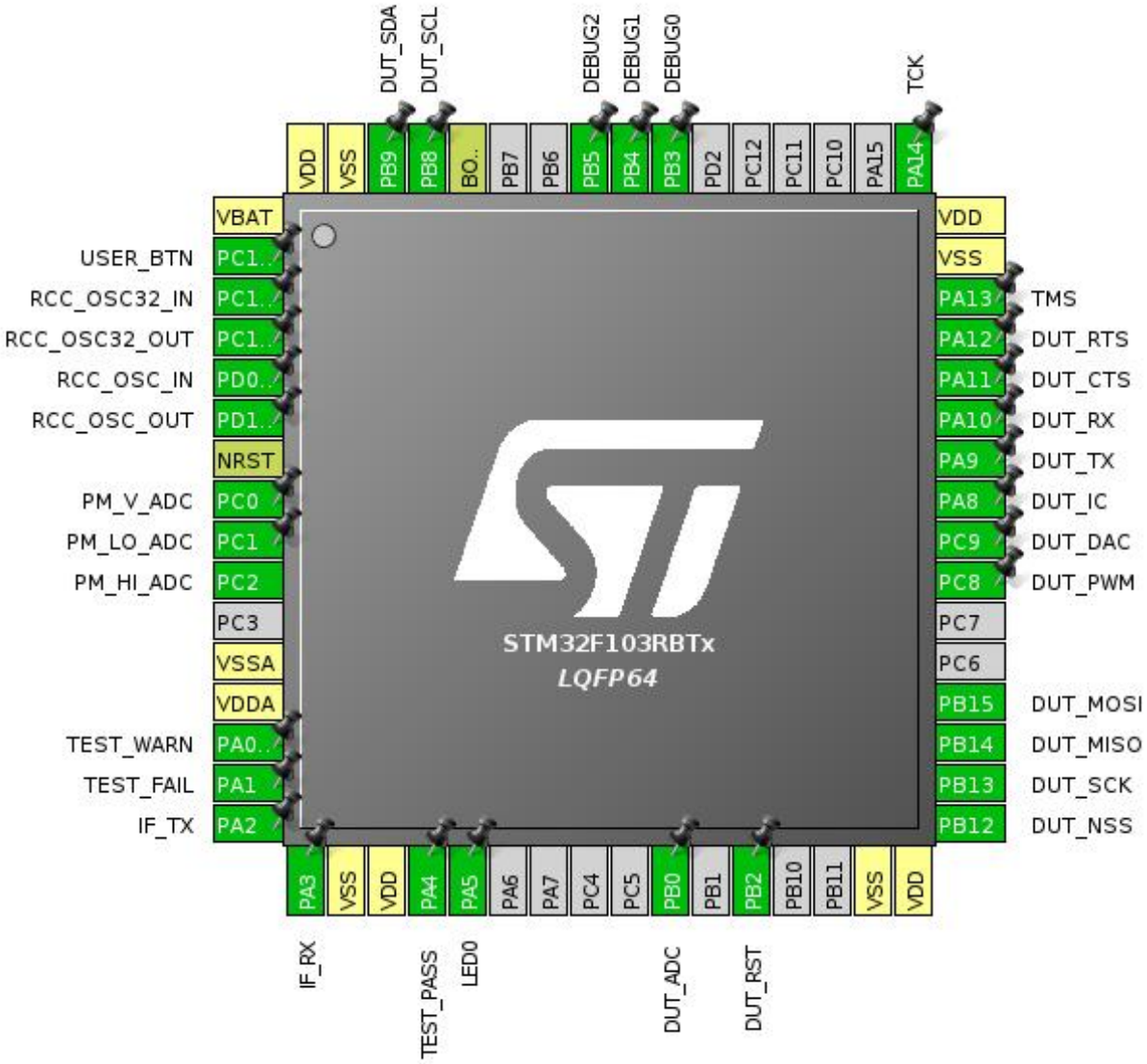
1.1. Project

Project Name	PHiLIP-NUCLEOF103RB
Board Name	NUCLEO-F103RB
Generated with:	STM32CubeMX 4.26.0
Date	08/23/2018

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103RBTx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



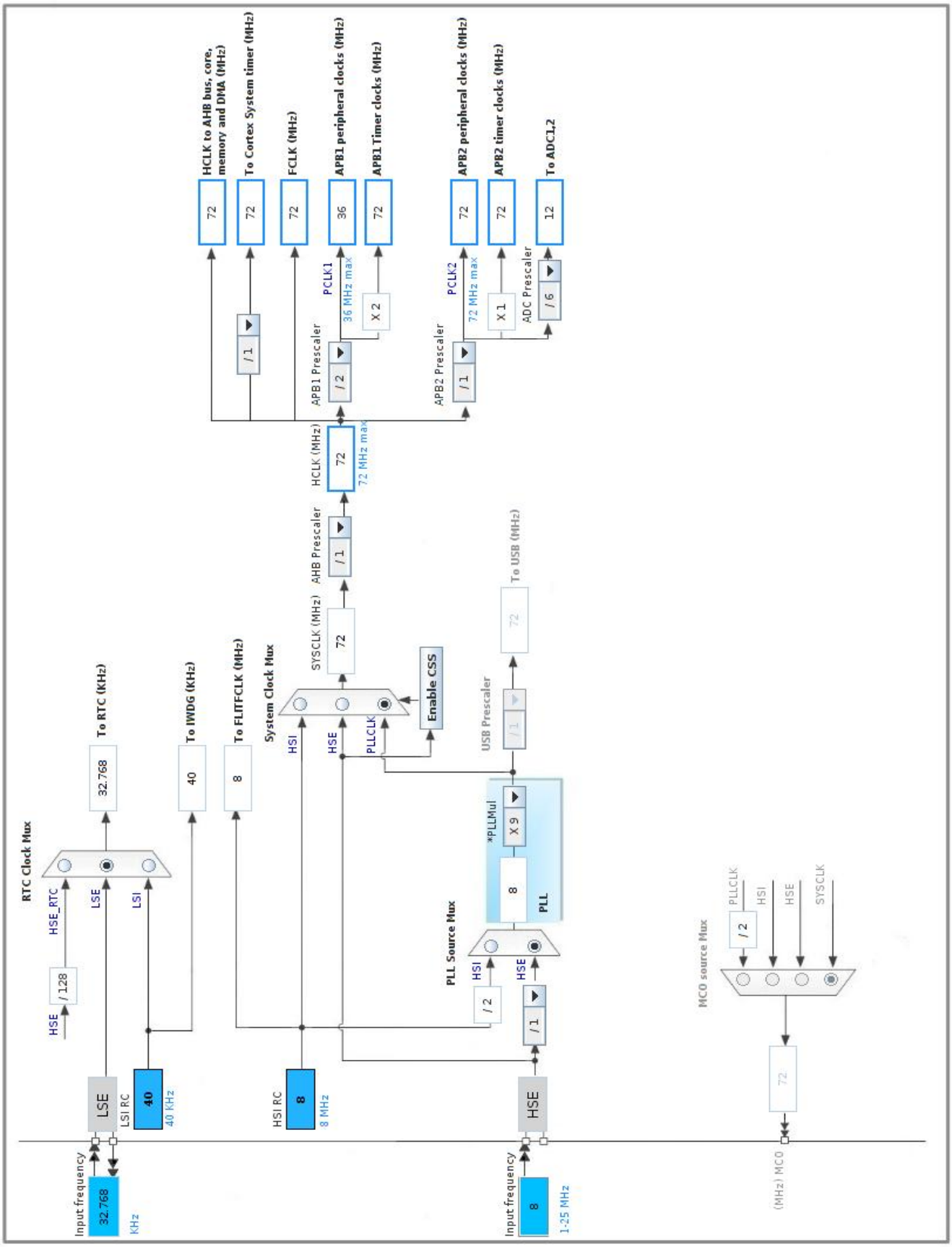
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-TAMPER-RTC *	I/O	GPIO_Input	USER_BTN
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	ADC1_IN10	PM_V_ADC
9	PC1	I/O	ADC1_IN11	PM_LO_ADC
10	PC2	I/O	ADC1_IN12	PM_HI_ADC
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP *	I/O	GPIO_Output	TEST_WARN
15	PA1 *	I/O	GPIO_Output	TEST_FAIL
16	PA2	I/O	USART2_TX	IF_TX
17	PA3	I/O	USART2_RX	IF_RX
18	VSS	Power		
19	VDD	Power		
20	PA4 *	I/O	GPIO_Output	TEST_PASS
21	PA5 *	I/O	GPIO_Output	LED0
26	PB0	I/O	ADC2_IN8	DUT_ADC
28	PB2 *	I/O	GPIO_Output	DUT_RST
31	VSS	Power		
32	VDD	Power		
33	PB12	I/O	SPI2_NSS	DUT_NSS
34	PB13	I/O	SPI2_SCK	DUT_SCK
35	PB14	I/O	SPI2_MISO	DUT_MISO
36	PB15	I/O	SPI2_MOSI	DUT_MOSI
39	PC8	I/O	TIM3_CH3	DUT_PWM
40	PC9	I/O	TIM3_CH4	DUT_DAC
41	PA8	I/O	TIM1_CH1	DUT_IC
42	PA9	I/O	USART1_TX	DUT_TX
43	PA10	I/O	USART1_RX	DUT_RX
44	PA11	I/O	GPIO_EXTI11	DUT_CTS
45	PA12 *	I/O	GPIO_Output	DUT_RTS
46	PA13	I/O	SYS_JTMS-SWDIO	TMS

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 *	I/O	GPIO_Output	DEBUG0
56	PB4 *	I/O	GPIO_Output	DEBUG1
57	PB5 *	I/O	GPIO_Output	DEBUG2
60	BOOT0	Boot		
61	PB8	I/O	I2C1_SCL	DUT_SCL
62	PB9	I/O	I2C1_SDA	DUT_SDA
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN10

mode: IN11

mode: IN12

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**3 ***
External Trigger Conversion Source	Regular Conversion launched by software
Rank	1
Channel	Channel 10
Sampling Time	1.5 Cycles
Rank	**2 ***
Channel	**Channel 11 ***
Sampling Time	1.5 Cycles
Rank	**3 ***
Channel	**Channel 12 ***
Sampling Time	1.5 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. ADC2

mode: IN8

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
Rank	1
Channel	Channel 8
Sampling Time	1.5 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.3. I2C1

I2C: I2C

5.3.1. Parameter Settings:

Master Features:

I2C Speed Mode	**Fast Mode ***
I2C Clock Speed (Hz)	400000
Fast Mode Duty Cycle	Duty cycle Tlow/Thigh = 2

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	**Enabled ***
Primary slave address	**85 ***
Secondary slave address	**64 ***
General Call address detection	**Enabled ***
Secondary Address Mask	No mask

5.4. IWDG

mode: Activated

5.4.1. Parameter Settings:

Clocking:

IWDG counter clock prescaler	**32 ***
IWDG down-counter reload value	4095

5.5. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

5.6. RTC

mode: Activate Clock Source

mode: Activate Calendar

RTC OUT: No RTC Output

5.6.1. Parameter Settings:

Calendar Time:

Data Format	**Binary data format ***
Hours	**1 ***
Minutes	0
Seconds	0

General:

Auto Predivider Calculation	Enabled
Asynchronous Predivider value	Automatic Predivider Calculation Enabled
Output	No output on the TAMPER pin

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	**18 ***

5.7. SPI2

Mode: Full-Duplex Slave

Hardware NSS Signal: Hardware NSS Input Signal

5.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**9.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Input Hardware

5.8. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.9. TIM1

Clock Source : Internal Clock

Channel1: Input Capture direct mode

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.10. TIM3

Clock Source : Internal Clock

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	**1 ***
Fast Mode	Disable

CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	**32768 ***
Fast Mode	Disable
CH Polarity	High

5.11. USART1

Mode: Asynchronous

5.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.12. USART2

Mode: Asynchronous

5.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	n/a	n/a	PM_V_ADC
	PC1	ADC1_IN11	Analog mode	n/a	n/a	PM_LO_ADC
	PC2	ADC1_IN12	Analog mode	n/a	n/a	PM_HI_ADC
ADC2	PB0	ADC2_IN8	Analog mode	n/a	n/a	DUT_ADC
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	n/a	**High ***	DUT_SCL
	PB9	I2C1_SDA	Alternate Function Open Drain	n/a	**High ***	DUT_SDA
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI2	PB12	SPI2_NSS	Input mode	No pull-up and no pull-down	n/a	DUT_NSS
	PB13	SPI2_SCK	Input mode	No pull-up and no pull-down	n/a	DUT_SCK
	PB14	SPI2_MISO	Alternate Function Push Pull	n/a	**High ***	DUT_MISO
	PB15	SPI2_MOSI	Input mode	No pull-up and no pull-down	**n/a**	DUT_MOSI
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM1	PA8	TIM1_CH1	Input mode	No pull-up and no pull-down	n/a	DUT_IC
TIM3	PC8	TIM3_CH3	Alternate Function Push Pull	n/a	Low	DUT_PWM
	PC9	TIM3_CH4	Alternate Function Push Pull	n/a	Low	DUT_DAC
USART1	PA9	USART1_TX	Alternate Function Push Pull	n/a	**High ***	DUT_TX
	PA10	USART1_RX	Input mode	No pull-up and no pull-down	**n/a**	DUT_RX
USART2	PA2	USART2_TX	Alternate Function Push Pull	n/a	Low	IF_TX
	PA3	USART2_RX	*	No pull-up and no pull-down	n/a	IF_RX
GPIO	PC13-TAMPER-RTC	GPIO_Input	Input mode	**Pull-up ***	n/a	USER_BTN
	PA0-WKUP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TEST_WARN
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TEST_FAIL

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TEST_PASS
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED0
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DUT_RST
	PA11	GPIO_EXTI11	External Interrupt Mode with Rising edge trigger detection	**Pull-down ***	n/a	DUT_CTS
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DUT_RTS
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DEBUG0
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DEBUG1
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DEBUG2

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low
USART1_RX	DMA1_Channel5	Peripheral To Memory	Low
USART1_TX	DMA1_Channel4	Memory To Peripheral	Low
USART2_RX	DMA1_Channel6	Peripheral To Memory	Low
USART2_TX	DMA1_Channel7	Memory To Peripheral	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

USART1_RX: DMA1_Channel5 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_TX: DMA1_Channel4 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_RX: DMA1_Channel6 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte

Memory Data Width:	Byte

USART2_TX: DMA1_Channel7 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel4 global interrupt	true	0	0
DMA1 channel5 global interrupt	true	0	0
DMA1 channel6 global interrupt	true	0	0
DMA1 channel7 global interrupt	true	0	0
ADC1 and ADC2 global interrupts	true	0	0
TIM1 update interrupt	true	0	0
I2C1 event interrupt	true	0	0
I2C1 error interrupt	true	0	0
SPI2 global interrupt	true	0	0
USART1 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
PVD interrupt through EXTI line 16	unused		
RTC global interrupt	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
USART2 global interrupt	unused		
RTC alarm interrupt through EXTI line 17	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103RBTx
Datasheet	13587_Rev17

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	PHiLIP-NUCLEOF103RB
Project Folder	/home/kevinweiss/WorkingDirectory/PHiLIP/STMCUBE_GENERATION/PHiLIP-
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F1 V1.6.1

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report