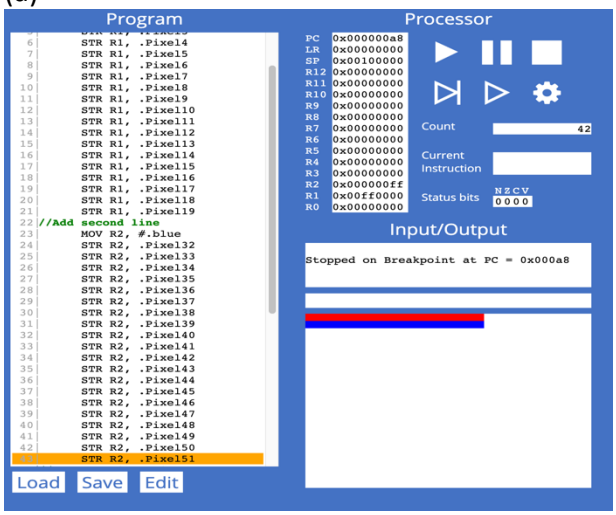
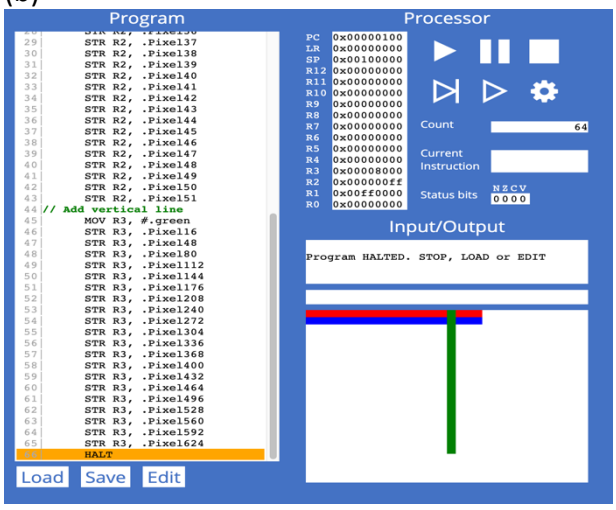
COMPUTER SYSTEMS

LAB 09

(a)



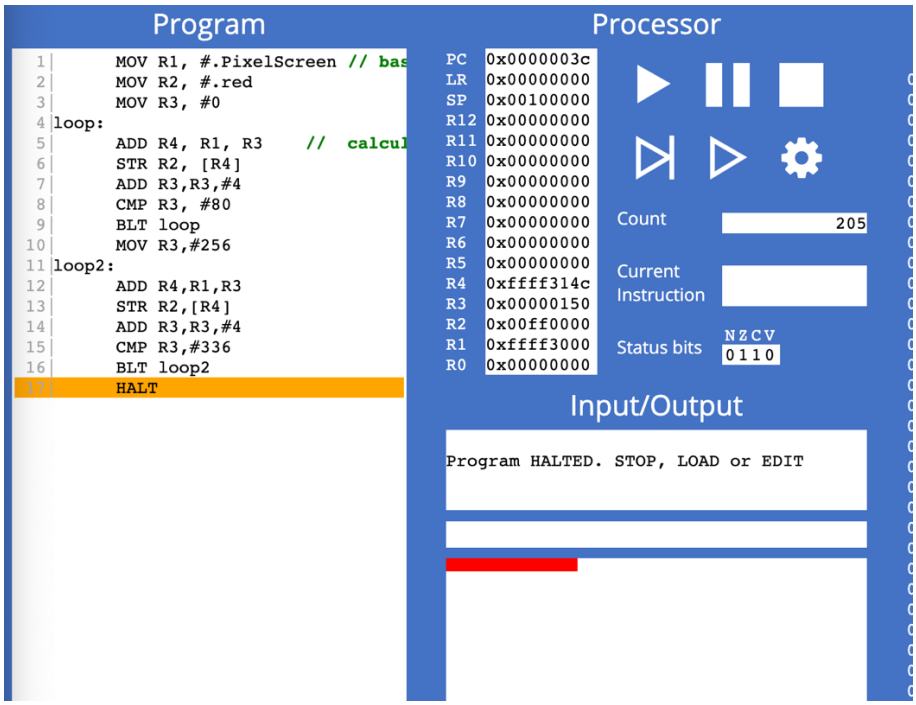
(b)



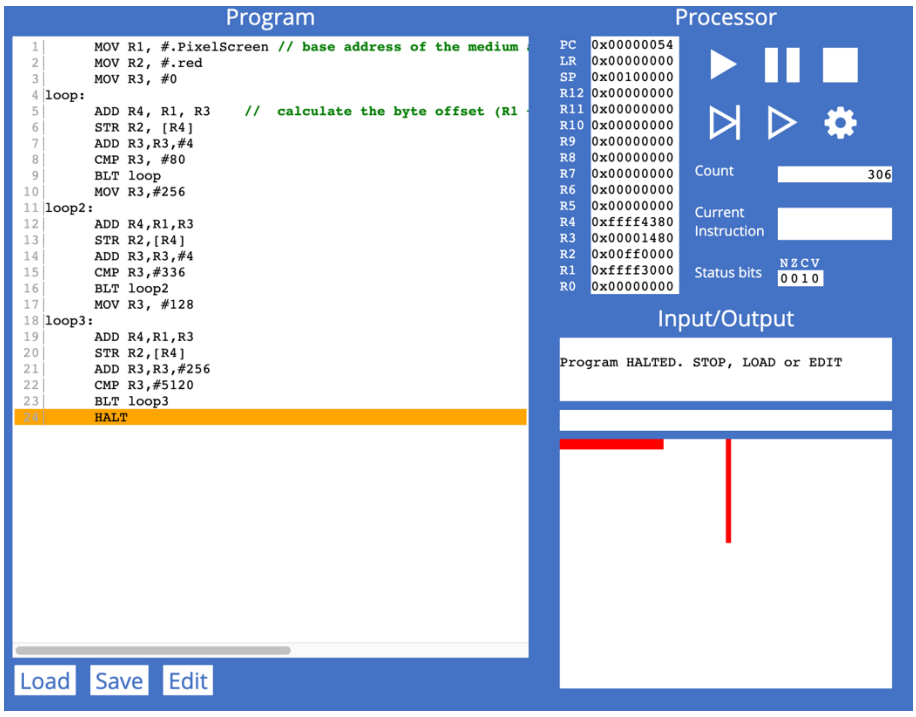
Exercise 9.1.3

(a) The given code is indirect addressing as it can store the specific value of r2 in [r4] which has a memory address and in its own value. In the code it is adding four bytes every time to the pixel until it reaches 80 and moving data to the memory address 4 bytes, 32 bits. and R1 is the base address if we add value in R3 it will add to the R1 which stores the address and which can form the new pointer to the next pixel.

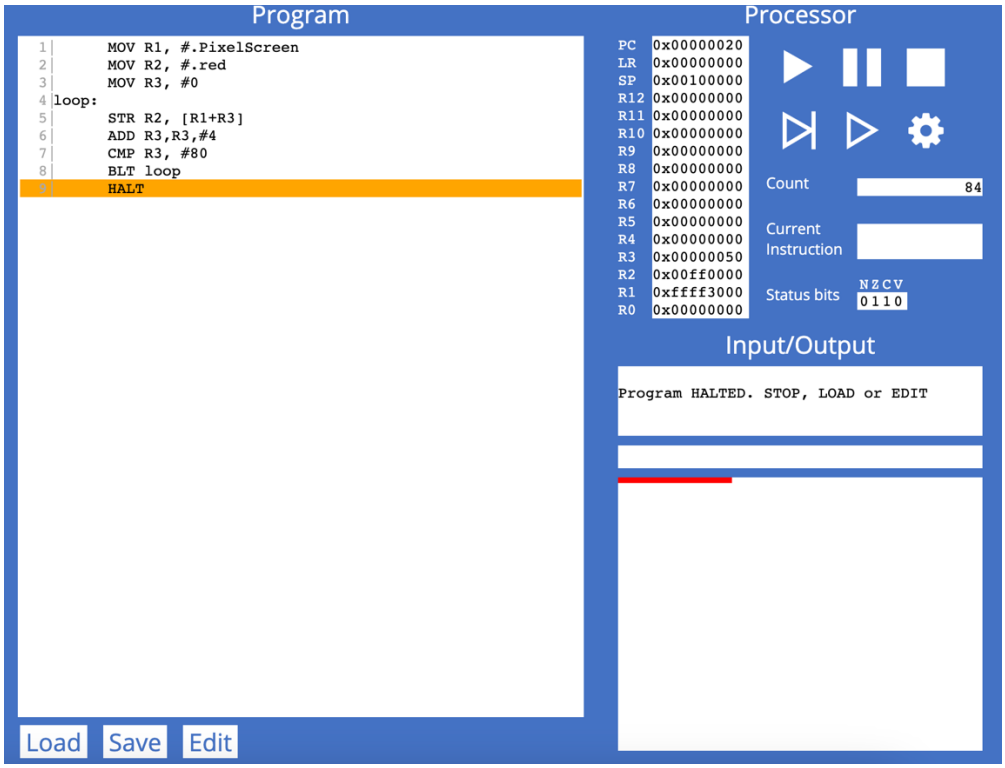
(b)


Program
1 MOV R1, #.PixelScreen // bas
2 MOV R2, #.red
3 MOV R3, #0
4 loop:
5 ADD R4, R1, R3 // calcul
6 STR R2, [R4]
7 ADD R3,R3,#4
8 CMP R3, #80
9 BLT loop
10 MOV R3,#256
11 loop2:
12 ADD R4,R1,R3
13 STR R2,[R4]
14 ADD R3,R3,#4
15 CMP R3,#336
16 BLT loop2
17 HALT
Processor
PC 0x0000003c
LR 0x00000000
SP 0x00100000
R12 0x00000000
R11 0x00000000
R10 0x00000000
R9 0x00000000
R8 0x00000000
R7 0x00000000
R6 0x00000000
R5 0x00000000
R4 0xffff314c
R3 0x00000150
R2 0x00ff0000
R1 0xffff3000
R0 0x00000000
Count 205
Current Instruction
Status bits N Z C V 0 1 1 0
Input/Output
Program HALTED. STOP, LOAD or EDIT

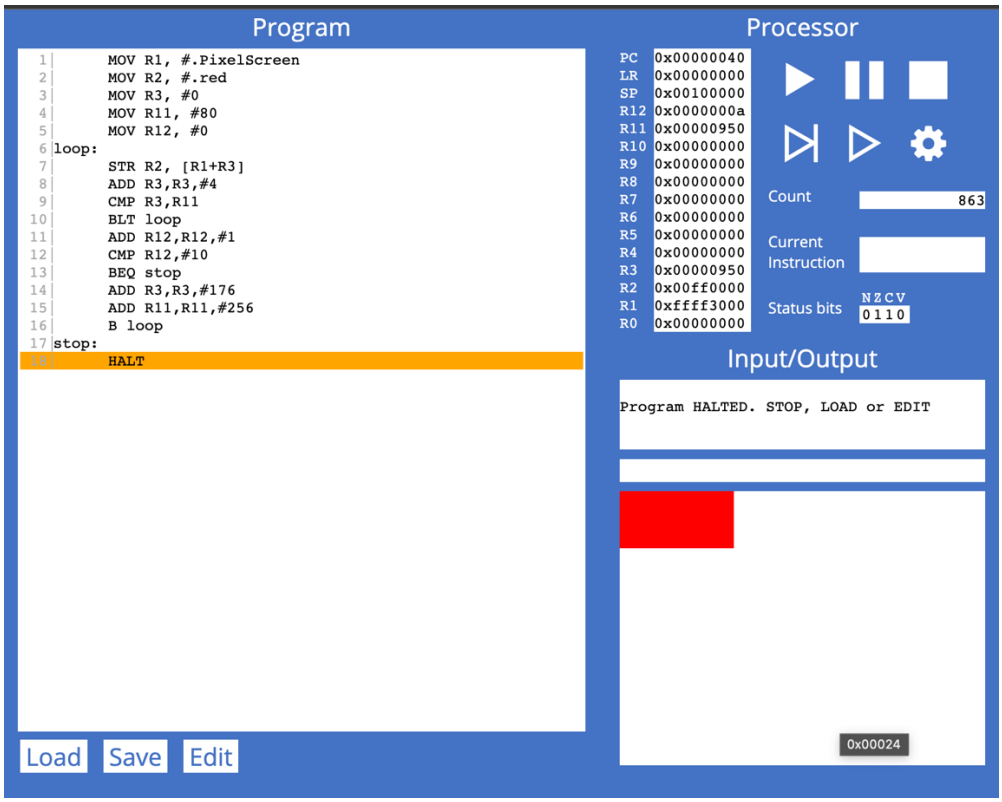
(c)


Program
1 MOV R1, #.PixelScreen // base address of the medium
2 MOV R2, #.red
3 MOV R3, #0
4 loop:
5 ADD R4, R1, R3 // calculate the byte offset (R1
6 STR R2, [R4]
7 ADD R3,R3,#4
8 CMP R3, #80
9 BLT loop
10 MOV R3,#256
11 loop2:
12 ADD R4,R1,R3
13 STR R2,[R4]
14 ADD R3,R3,#4
15 CMP R3,#336
16 BLT loop2
17 MOV R3, #128
18 loop3:
19 ADD R4,R1,R3
20 STR R2,[R4]
21 ADD R3,R3,#256
22 CMP R3,#5120
23 BLT loop3
24 HALT
Load
Save
Edit
Processor
PC 0x00000054
LR 0x00000000
SP 0x00100000
R12 0x00000000
R11 0x00000000
R10 0x00000000
R9 0x00000000
R8 0x00000000
R7 0x00000000
R6 0x00000000
R5 0x00000000
R4 0xffff4380
R3 0x00001480
R2 0x00ff0000
R1 0xffff3000
R0 0x00000000
Count 306
Current Instruction
Status bits N Z C V 0 0 1 0
Input/Output
Program HALTED. STOP, LOAD or EDIT

Exercise 9.2.1



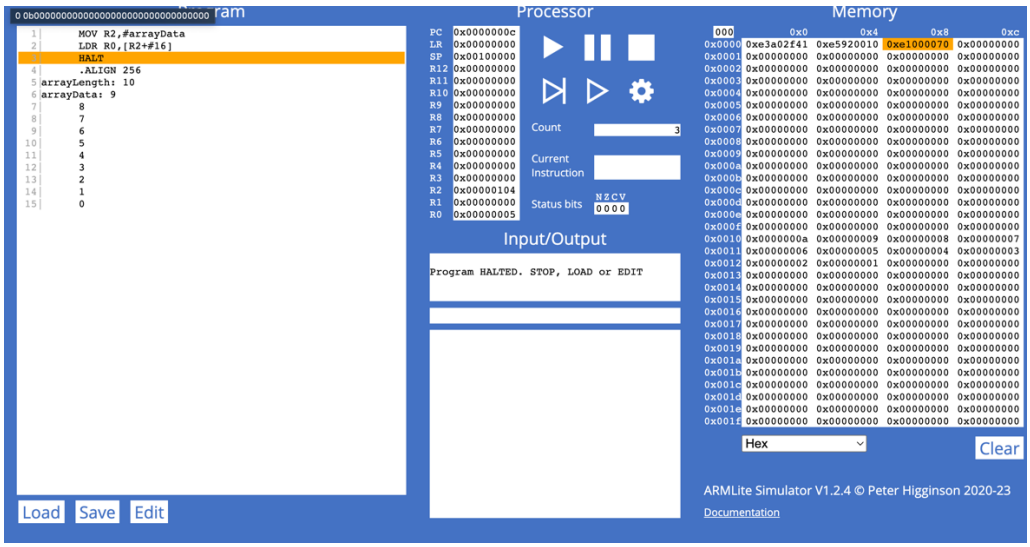
Exercise 9.2.2



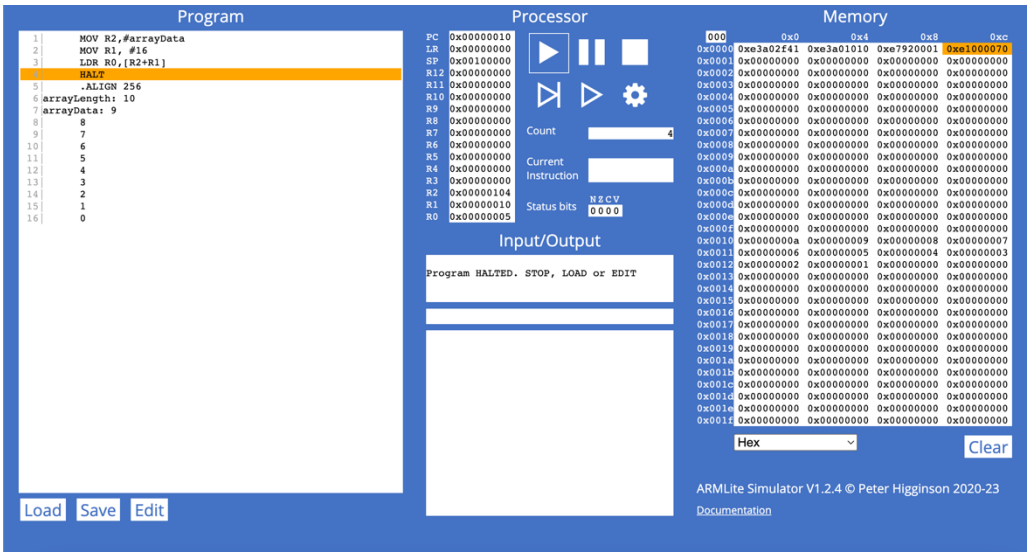
Exercise 9.3.1

(a) The .Align 256 instruction ensures the next instruction is aligned with a word address divisible by 256.

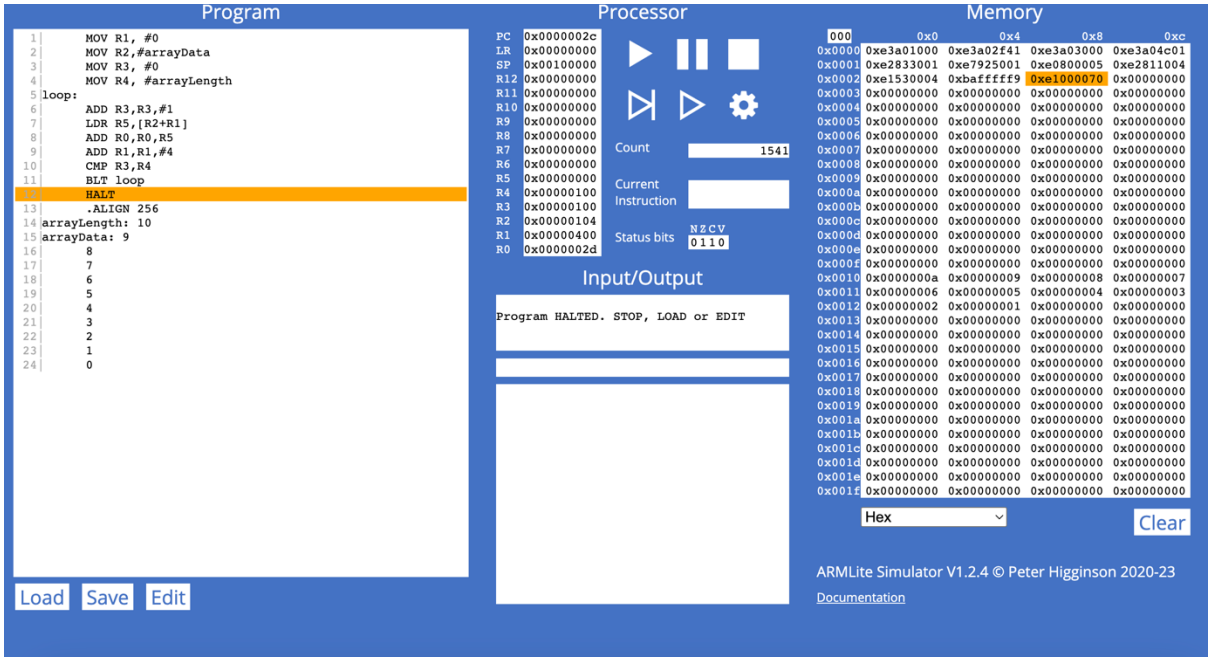
(b)



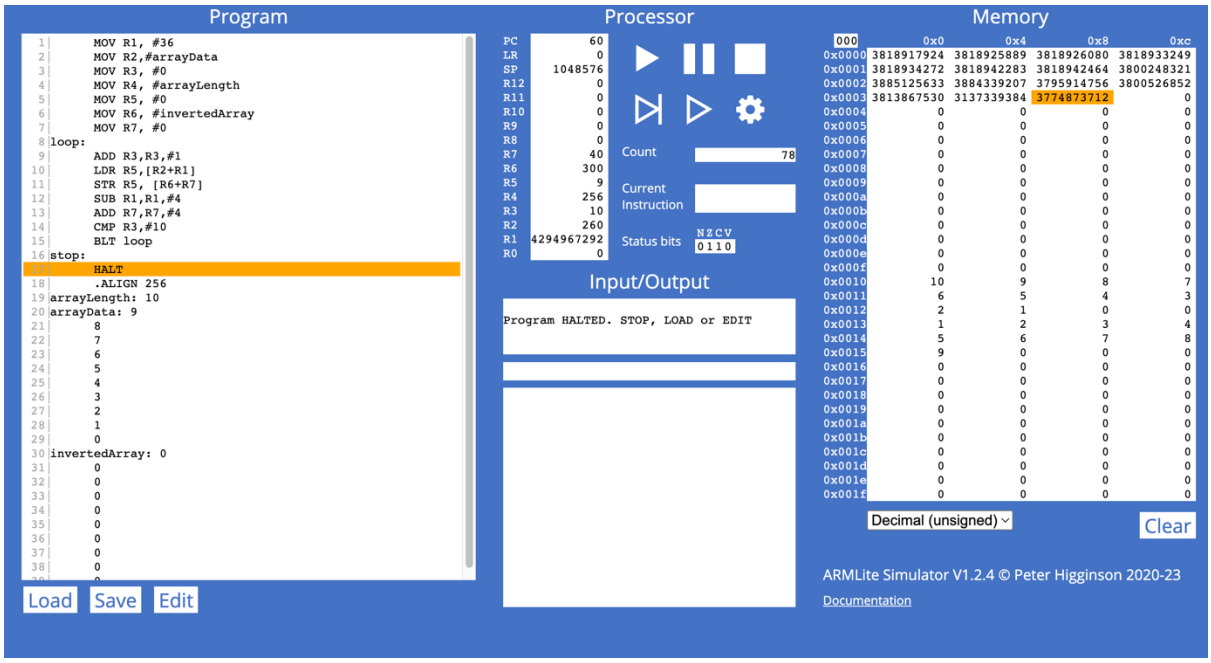
(c)



Exercise 9.3.2



Exercise 9.4.1



Exercise 9.4.2