Politecnico di Torino

Collegio di Elettronica, Telecomunicazioni e Fisica

Report for the course
Integrated Systems Architecture

Master degree in Electrical Engineering

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Contents

CHAPTER 1

Lab 2: Digital Arithmetic

The aim of this lab is to work with digital arithmetic circuits, as an example architecture a floating point unit (FPU) will be used. The activity is divided in two main parts:

- FPU model: In a first part the given architecture will be simulated and synthesized using different options for the synthesizer to evaluate the impact on speed and area of the resulting netlist.
- R8-MBE: In the second part the mantissa multiplier of the FPU will be realized using the radix 8 modified both encoding architecture and the changes compared to the previous synthesis results will be studied.

1.1 FPU model

1.1.1 Simulation

The FPU has been simulated using a testbench that generates random values and automatically compares the result obtained from the FPU with the reference values calculated via a direct multiplication in SystemVerilog.

In Figure 1.1 is reported a snapshot of the simulation, it is possible to see the input operands, the output of the FPU and the product calculated in the testbench, a signal ”Difference” is used to detect errors in the DUT.
The only known difference between the two products (found simulating one million random calculations) is that for the NaN results the signs and the values of the mantissa can be different, this difference is not relevant since the NaN value does not depend from the sign and the mantissa bits (as long as the mantissa is different from zero).

All the different implementations of the FPU have been simulated using the same testbench generating each time ten thousands input combinations (the seed for the random number generator is never changed so the input combinations will be the same for all the circuits).

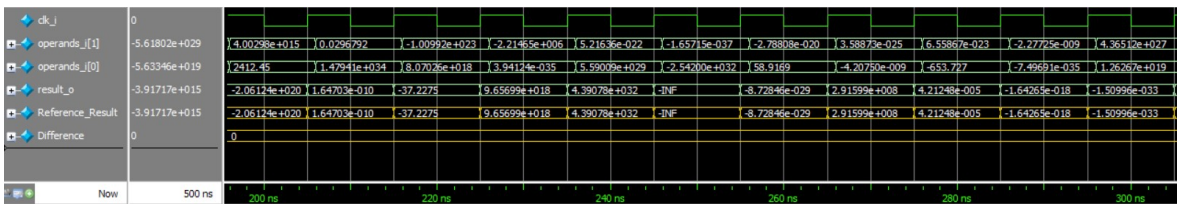

Figure 1.1: Simulation result of the FPU

1.1.2 Synthesis

The circuit has been synthesised using five different sequences of commands for the synthesizer:

- Normal compilation: No optimizations and no specific implementation for the components have been used.
- Optimize registers: Additional registers have been inserted in the circuit and the *compile_registers* command has been used to automatically apply retiming to the circuit. No implementation for the component has been specified.
- Compile ultra. The *compile_ultra* command has been used to automatically apply different optimizations on the circuit.
- CSA multiplier: Retiming has been applied and the multiplier's implementation has been forced to carry-save.
- PPARCH multiplier: Retiming has been applied and the multiplier's implementation has been forced to parallel prefix architecture.

Table 1.1 shows the results of the experiments required in the assignment.

Compiler options	Maximum delay	Maximum frequency	Required area	Pipeline stages	Latency (at f_{MAX})
Normal compilation	2.60 ns	378.8 MHz	10341 μm^2	3	7.8 ns
Optimize registers	1.29 ns	775.1 MHz	13125 μm^2	4	5.16 ns
Compile ultra	2.34 ns	427.3 MHz	14941 μm^2	3	7.2 ns
CSA multiplier	1.75 ns	571.4 MHz	18531 μm^2	11	19.25 ns
PPARCH mulitplier	1.10 ns	909.1 MHz	16364 μm^2	8	8.8 ns

Table 1.1: Results of the different synthesis

For the synthesis that apply retiming via the *optimize_registers* or *compile_ultra* commands (all the rows of the Table 1.1 except the first), to evaluate the optimal number of pipeline stages to maximize the working frequency of the circuit a bash script to synthesize the circuits with different numbers of pipeline registers (from 0 to 20 registers) has been exploited.
The maximum delay number indicates the data arrival time value of the signal on the critical path without considering the time of setup and hold of the registers.
To find the best solution, the placing of the registers has been tested after the multiplier and distributed in the circuit, for both cases the synthesis has been tried with and without the flatten option.

From the four tests the best solution found is distributing the registers in the circuit and not using the flatten command. These four combinations have been tried only with the second synthesis of the table 1.1 to reduce the synthesis time and than only the chosen pipelining method has been applied to the other synthesis.
The results of all the executed synthesis can be fount in appendix of the document.

After each synthesis the generated netlist has been simulated with the same testbench as before (just setting the correct number of pipelining registers to adjust the expected latency) to verify its correctness.

1.1.3 Explanations, comparisons and comments

The results of the five synthesis can be plotted on a plane (area versus delay) to more easily evaluate the differences between them.

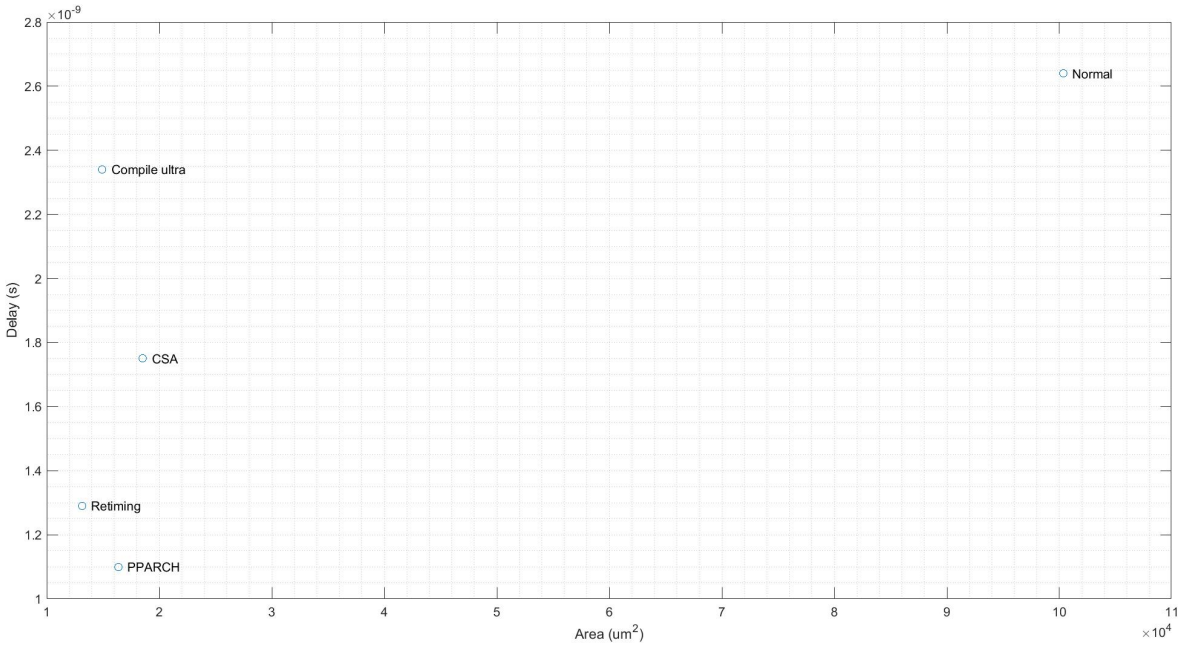

Figure 1.2: Plot of the synthesis results

As it is possible to see if no options are specified to the compiler the speed of the circuit is limited and it occupies a large area. The fastest circuit is the one where the multiplier is realized with the PPARCH architecture while the one with the smallest footprint is the one where only the retiming has been used, it also has the least latency compared with the other solutions.
All the other circuits are pareto-dominated (at least on the speed, area, latency metrics) because they do not have any advantages compared to the circuits with PPARCH multiplier and with retiming.

Looking at the resources reports it is possible to notice that with the compile_ultra option the multiplier has been implemented with a radix-4 booth encoding (benc_radix4). In the two synthesis where the architecture of the multiplier has been specified it as been implemented in the correct way; the other operators have been implemented in the same way in booth cases ad exception of the adder used to correct the exponent after the normalization, in fact in the CSA synthesis it has been realized as a ripple carry adder (rpl) while in the synthesis with the PPARCH it has been synthesizes as parallel prefix (pparch).

1.2 R8-MBE multiplier

The circuit implementing the R8-MBE is shown in Figure 1.3

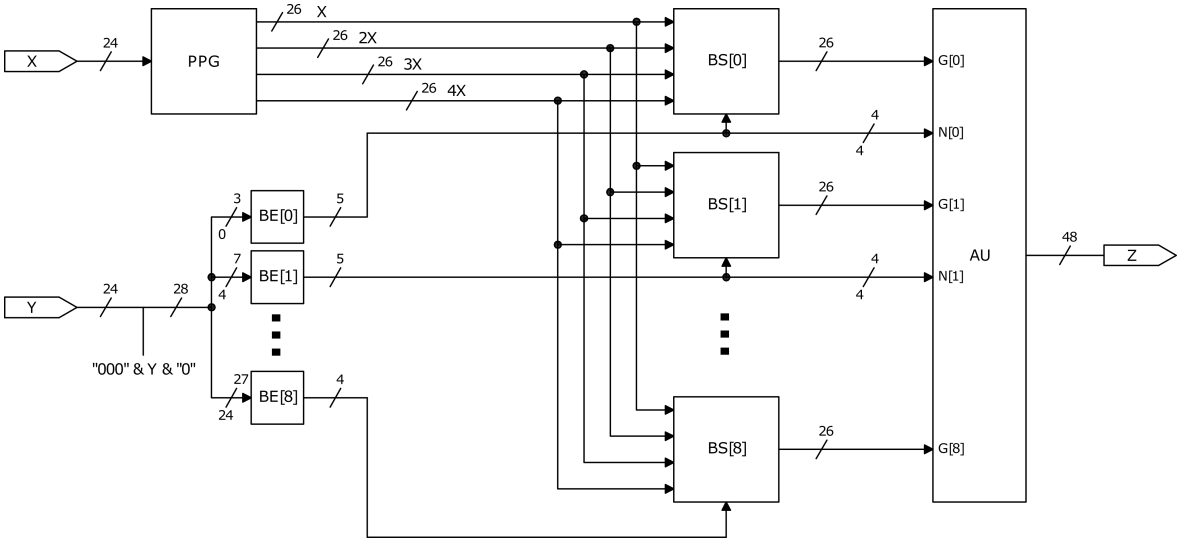

Figure 1.3: Schematic of the multiplier

The multiplier is based on the Radix-8 Modified Booth Encoding. The individual blocks are discussed in more detail below.

- BE (Booth Encoder): groups of 4 bits are extracted from the multiplier and, applying booth encoding to them, the number of partial products can be reduced by $\sim \frac{N}{3}$ (in this case it is reduced from 23 to 9). The multiplier is extended before the BE computation (three leading zeros and one trailing zero) so that the entire value can be correctly evaluated. The new representation of the multiplier is computed in parallel (9 BE blocks are instantiated), the output of each block is composed by four bits for the selection of the partial product and one for the sign extension.
- PPG (Partial Product Generator): it calculates the four possible values (X, 2X, 3X, 4X) that can be required for each partial product. The non-redundant version is implemented where the X, 2X and 4X output are generated directly via shifting and to generate 3X an adder is used.
- BS (Booth Selector): based on the signals generated by the booth encoder it selects which partial product must be provided to the input of the Dadda tree, if required by the encoding the selected partial product can also be inverted (Ones' complement).
- AU (Adder Unit): implementation of the Dadda tree. Using only 5/3 compressors, full adders and half adders the number of partial products that need to be summed is reduced. In the last level, only two operands need to be obtained so to calculate how many stages to implement, knowing the best compressor available (in this case the 5 to 3) and it is possible to calculate the maximum number of operands at each level of the tree using the equation:

$$l_i = l_{i-1} \cdot \frac{5}{3} \tag{1.1}$$

The resulting values are:

Tree level	Exact result	Number of operands (floor of the exact result)
l_1	2	2
l_2	$\frac{10}{3}$	3
l_3	5	5
l_4	$\frac{25}{3}$	8
l_5	$\frac{40}{3}$	13

Table 1.2: Number of operands at each tree level

The Dadda-like tree is shown in Figure 1.4, all the compressors required and theirs corresponding outputs are represented respectively as rectangles and lines between the dots. For the 5/3 compressors the third output is signaled by an arrow that connect the current compressor with the next compressor on the same level.

Moreover, the figure shows how sign extension has been simplified to avoid unnecessary compressors. The pink dots represent S while the blue dots indicate $\bar{S}$, they are the output n_i coming from the booth encoder of every partial product.

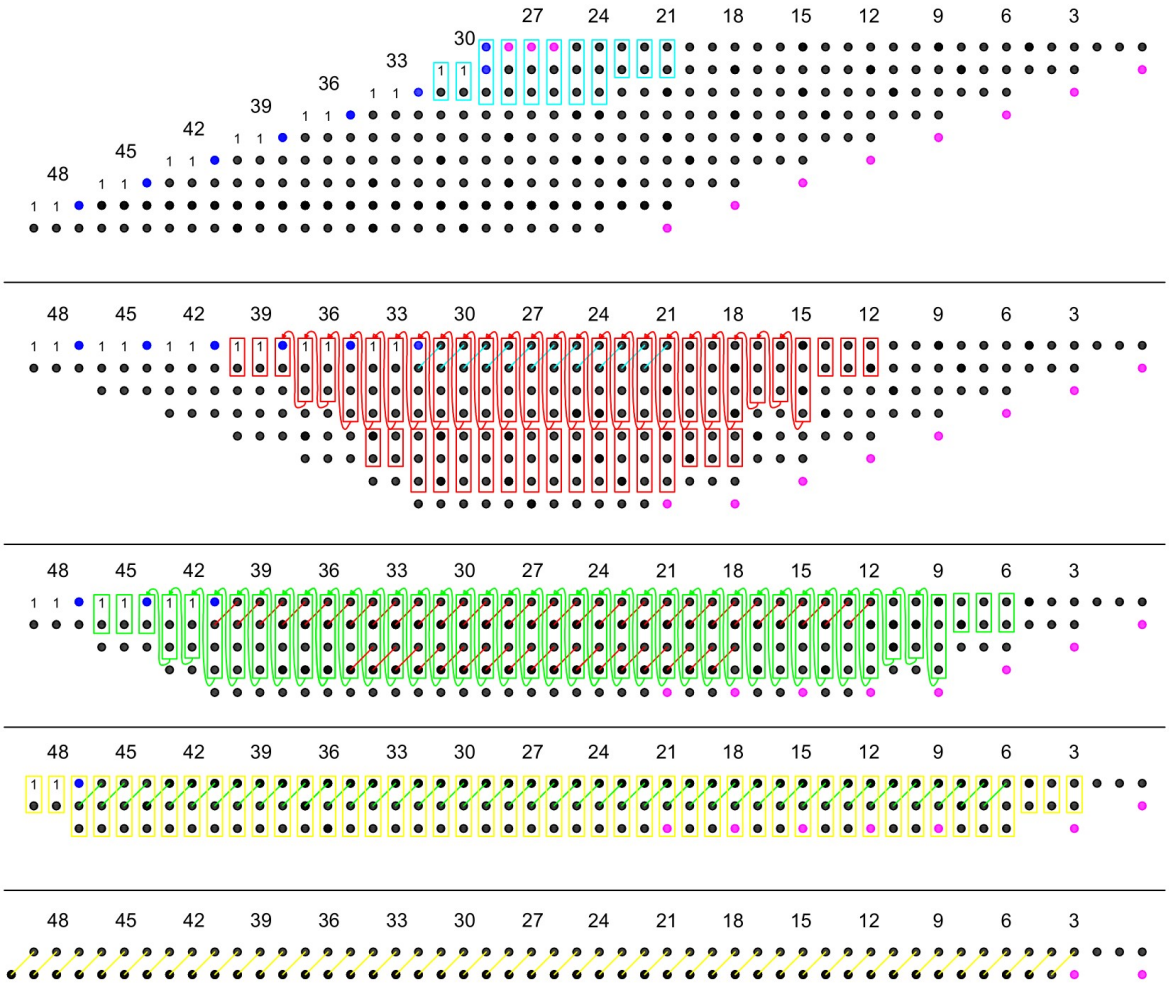

Figure 1.4: Operation in dot notation

To obtain only nine rows of partial product array the treatment of the bit sign extension has been simplified as shown in example in Figure 1.6.
In Figure 1.5 it is illustrated what would happen if all the partial products are negative (the last one is always positive due to the zeros added to the multiplier). As it can be seen it is necessary to add a '1' to every least significant bit to obtain the correct negative conversion of the two's complement number, it is also present a string of ones after the MSB that are simplified as shown.
To obtain a mixed partial product array as in Figure 1.6 the one at the LSB must not be added when there is a positive partial products and add a '1' (the $\bar{S}$) at the MSB+1 position to clean the the extension of ones. In the first row, due to the fact that the partial product only has ones at the MSBs, a different condition is obtained.
In Figure 1.4 the method applied is the same but for a Radix-8 Booth Encoder.
The S is equal to zero when the partial product is positive and to one when it is negative.

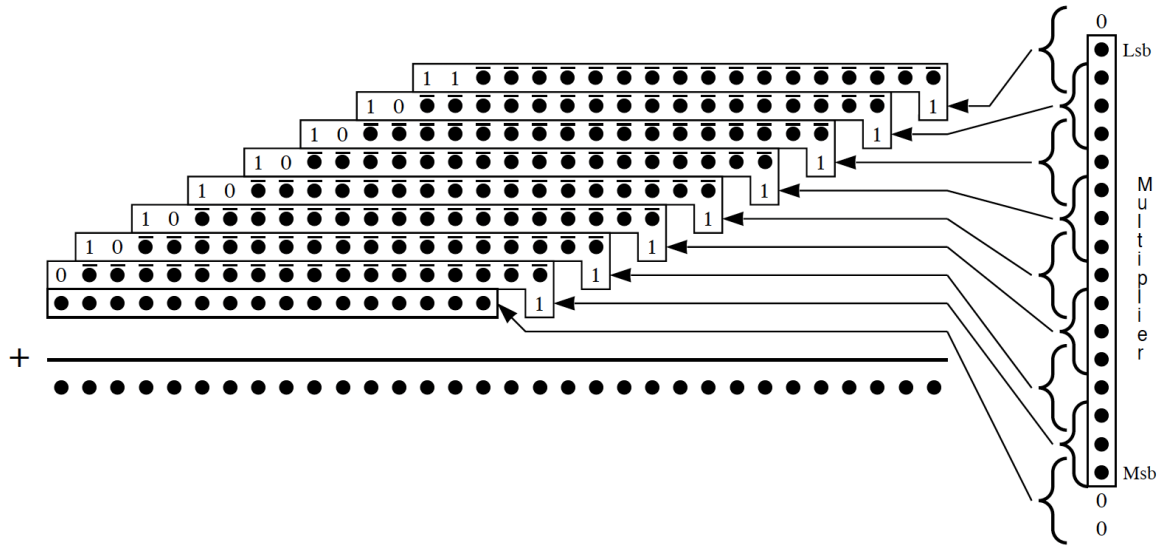

Figure 1.5: Negative partial products with summed sign extension

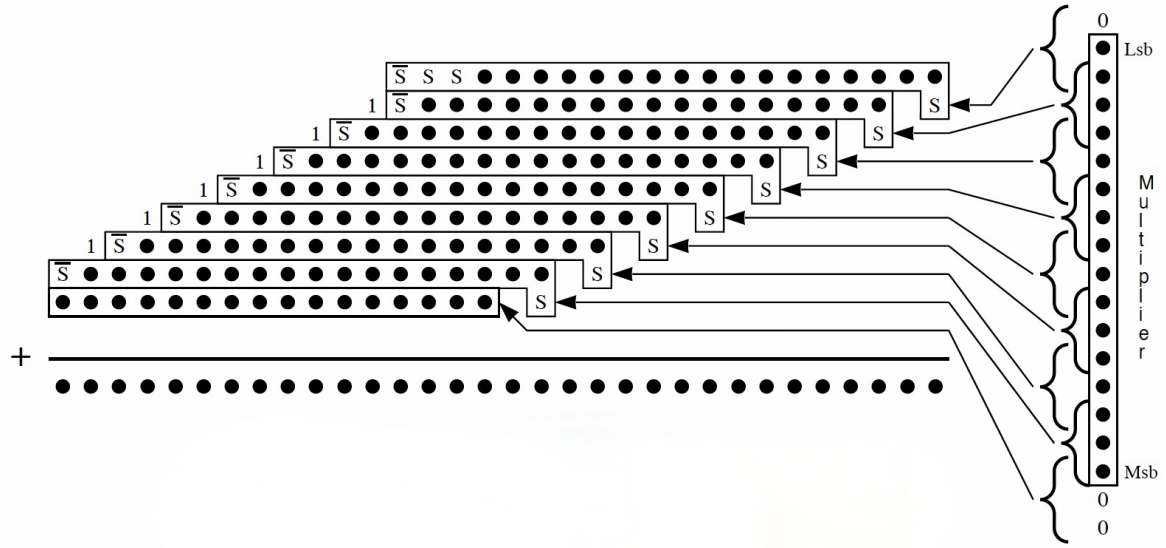

Figure 1.6: Complete Booth multiplication with height reduction

1.2.1 Simulation

Standalone multiplier

Figure 1.7 shows a snapshot of a simulation for the designed multiplier as a standalone block. Also in this case a testbench to automatically detect errors from the ideal behavior has been used.

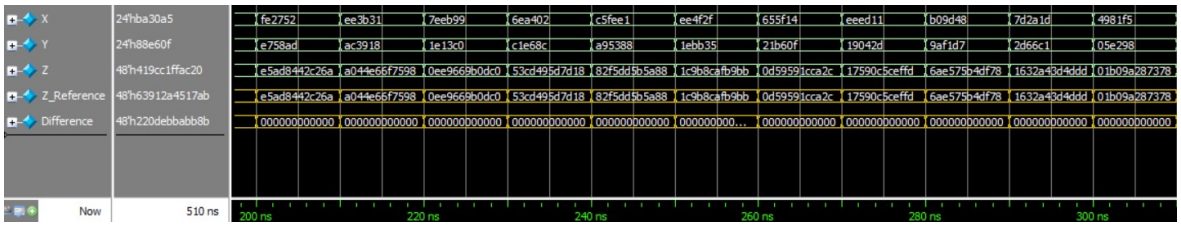

Figure 1.7: Simulation of the multiplier

Whole FPU

Figure 1.8 shows a snapshot of a simulation for the designed multiplier included in the whole FPU. The green waves are the I/O for the whole FPU, the yellow waves are the signal generated by the testbench, the purple waves are the I/O of the mantissa multiplier..

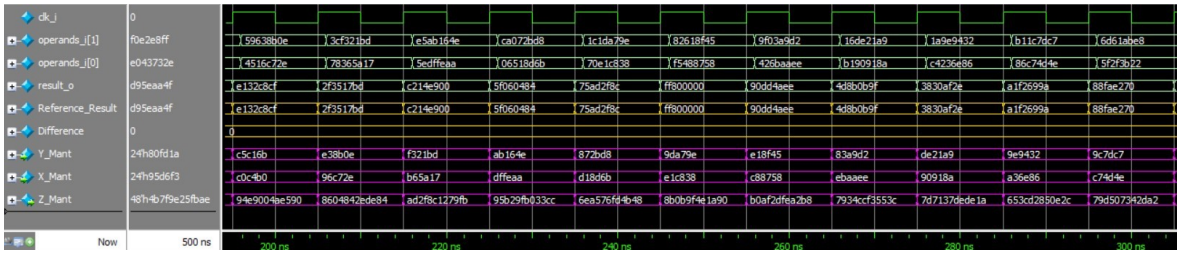

Figure 1.8: Simulation result of the FPU with the multiplier

1.2.2 Synthesis

The results of the synthesis are shown in 1.3.

Compiler options	Maximum delay	Maximum frequency	Required area	Pipeline stages	Latency (at f_{MAX})
R8-MBE	1.14 ns	877 MHz	15928 μm^2	4	4.56 ns

Table 1.3: Results of the synthesis of the FPU with the R8-MBE multiplier

1.2.3 Explanations, comparisons and comments

Also in this case it it possible to exploit a graph to study the solutions.

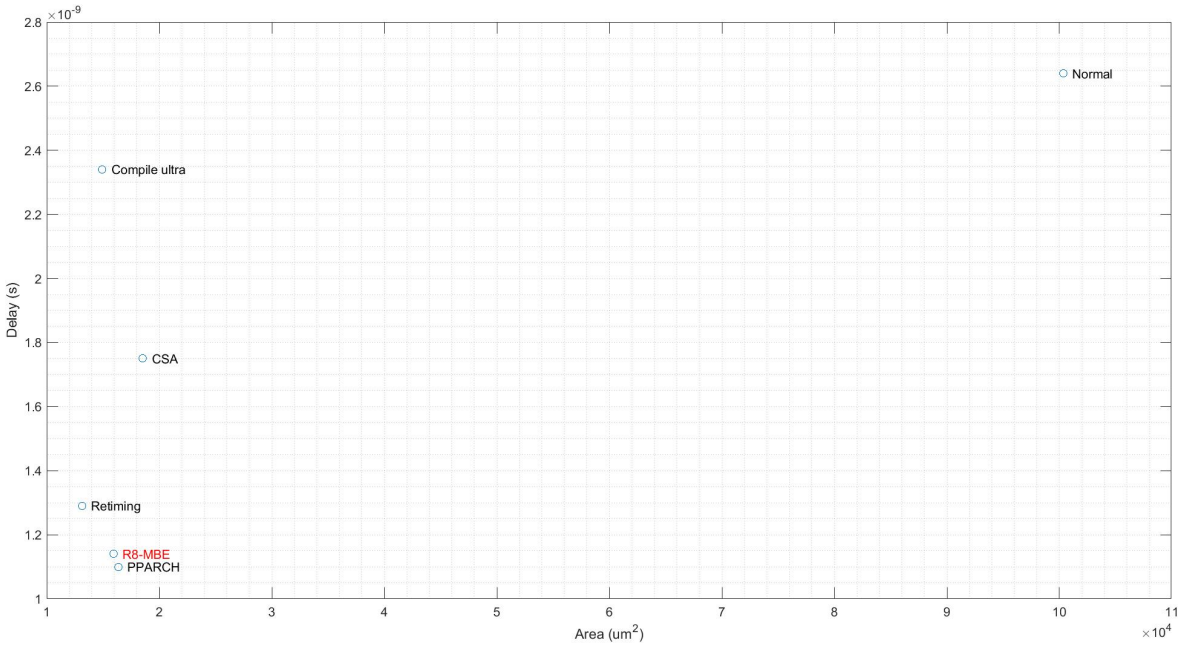

Figure 1.9: Plot of the synthesis results

The solution with the R8-MBE multiplier is not a pareto-optimal solution, indeed the fastest circuit is still the one with the PPARCH multiplier and the circuit with the smallest footprint is the one with only retiming.
The only advantage of the architecture with the R8-MBE multilier is that it as a reduced latency equal to four clock cycles (4.56 ns if working at the maximum frequency).

In the report resources it is possible to see that the two adders required for the R8-MBE multiplier (one for the partial product generator and one to sum the outputs of the Dadda tree) have booth been realized as PPARCH adders.

1.3 Appendix: Reports of the synthesis

1.3.1 Results of pipelining for optimize_registers synthesis

In these pages are reported the different results obtained with a bash script that automatically changes the number of register in the pipeline of the architecture and then synthesizes the circuit. The results indicate the number of stages of pipeline and the resulting slack (in every synthesis a constrain on the clock equal to 0.1 ns to minimize the delay is applied, so the printed number is the absolute value of the difference between the constraint and the maximum clock obtained).

Flatten-After

```
Using 0 stages of pipeline
4490 ps
Using 1 stages of pipeline
2240 ps
Using 2 stages of pipeline
4200 ps
Using 3 stages of pipeline
4180 ps
Using 4 stages of pipeline
4180 ps
Using 5 stages of pipeline
4230 ps
Using 6 stages of pipeline
4200 ps
Using 7 stages of pipeline
4130 ps
Using 8 stages of pipeline
4200 ps
Using 9 stages of pipeline
4140 ps
Using 10 stages of pipeline
4140 ps
```

Flatten-Distributed

```
Using 0 stages of pipeline
4490 ps
Using 1 stages of pipeline
2370 ps
Using 2 stages of pipeline
1780 ps
Using 3 stages of pipeline
1450 ps
Using 4 stages of pipeline
1230 ps
Using 5 stages of pipeline
1240 ps
Using 6 stages of pipeline
1380 ps
Using 7 stages of pipeline
1530 ps
Using 8 stages of pipeline
1440 ps
Using 9 stages of pipeline
1580 ps
Using 10 stages of pipeline
1480 ps
```

After

```
Using 0 stages of pipeline
4490 ps
Using 1 stages of pipeline
2300 ps
Using 2 stages of pipeline
4240 ps
Using 3 stages of pipeline
4230 ps
Using 4 stages of pipeline
4190 ps
Using 5 stages of pipeline
4300 ps
Using 6 stages of pipeline
4260 ps
Using 7 stages of pipeline
4180 ps
Using 8 stages of pipeline
4170 ps
Using 9 stages of pipeline
4170 ps
Using 10 stages of pipeline
4200 ps
Using 11 stages of pipeline
4230 ps
Using 12 stages of pipeline
4240 ps
Using 13 stages of pipeline
4220 ps
Using 14 stages of pipeline
4220 ps
Using 15 stages of pipeline
4200 ps
Using 16 stages of pipeline
4200 ps
Using 17 stages of pipeline
4210 ps
Using 18 stages of pipeline
4210 ps
Using 19 stages of pipeline
4210 ps
Using 20 stages of pipeline
4170 ps
```

Distributed

```
Using 0 stages of pipeline
4490 ps
Using 1 stages of pipeline
2420 ps
Using 2 stages of pipeline
1810 ps
Using 3 stages of pipeline
1450 ps
Using 4 stages of pipeline
1230 ps
Using 5 stages of pipeline
1240 ps
Using 6 stages of pipeline
1420 ps
Using 7 stages of pipeline
1580 ps
Using 8 stages of pipeline
1410 ps
Using 9 stages of pipeline
1600 ps
Using 10 stages of pipeline
1500 ps
Using 11 stages of pipeline
1500 ps
Using 12 stages of pipeline
1370 ps
Using 13 stages of pipeline
1410 ps
Using 14 stages of pipeline
1410 ps
Using 15 stages of pipeline
1500 ps
Using 16 stages of pipeline
1690 ps
Using 17 stages of pipeline
1710 ps
Using 18 stages of pipeline
1760 ps
Using 19 stages of pipeline
1350 ps
Using 20 stages of pipeline
1460 ps
```

1.3.2 Results of pipelining for compile_ultra synthesis

Distributed

```
Using 0 stages of pipeline
5810 ps
Using 1 stages of pipeline
3620 ps
Using 2 stages of pipeline
2510 ps
Using 3 stages of pipeline
2070 ps
Using 4 stages of pipeline
1740 ps
Using 5 stages of pipeline
1740 ps
Using 6 stages of pipeline
2390 ps
Using 7 stages of pipeline
2390 ps
Using 8 stages of pipeline
2390 ps
Using 9 stages of pipeline
2410 ps
Using 10 stages of pipeline
1940 ps
Using 11 stages of pipeline
1700 ps
Using 12 stages of pipeline
2520 ps
Using 13 stages of pipeline
2560 ps
Using 14 stages of pipeline
2100 ps
Using 15 stages of pipeline
2540 ps
Using 16 stages of pipeline
2510 ps
Using 17 stages of pipeline
2340 ps
Using 18 stages of pipeline
2660 ps
Using 19 stages of pipeline
1810 ps
Using 20 stages of pipeline
2630 ps
```

1.3.3 Results of pipelining for CSA synthesis

Distributed

```
Using 0 stages of pipeline
5810 ps
Using 1 stages of pipeline
3620 ps
Using 2 stages of pipeline
2510 ps
Using 3 stages of pipeline
2070 ps
Using 4 stages of pipeline
1740 ps
Using 5 stages of pipeline
1740 ps
Using 6 stages of pipeline
2390 ps
Using 7 stages of pipeline
2390 ps
Using 8 stages of pipeline
2390 ps
Using 9 stages of pipeline
2410 ps
Using 10 stages of pipeline
1940 ps
Using 11 stages of pipeline
1700 ps
Using 12 stages of pipeline
2520 ps
Using 13 stages of pipeline
2560 ps
Using 14 stages of pipeline
2100 ps
Using 15 stages of pipeline
2540 ps
Using 16 stages of pipeline
2510 ps
Using 17 stages of pipeline
2340 ps
Using 18 stages of pipeline
2660 ps
Using 19 stages of pipeline
1810 ps
Using 20 stages of pipeline
2630 ps
```

1.3.4 Results of pipelining for PPARCH synthesis

Distributed

```
Using 0 stages of pipeline
4330 ps
Using 1 stages of pipeline
2530 ps
Using 2 stages of pipeline
1840 ps
Using 3 stages of pipeline
1410 ps
Using 4 stages of pipeline
1210 ps
Using 5 stages of pipeline
1140 ps
Using 6 stages of pipeline
1460 ps
Using 7 stages of pipeline
1490 ps
Using 8 stages of pipeline
1040 ps
Using 9 stages of pipeline
1260 ps
Using 10 stages of pipeline
1590 ps
Using 11 stages of pipeline
1630 ps
Using 12 stages of pipeline
1590 ps
Using 13 stages of pipeline
1700 ps
Using 14 stages of pipeline
1650 ps
Using 15 stages of pipeline
1730 ps
Using 16 stages of pipeline
1350 ps
Using 17 stages of pipeline
1740 ps
Using 18 stages of pipeline
1420 ps
Using 19 stages of pipeline
1480 ps
Using 20 stages of pipeline
1490 ps
```

1.3.5 Results of pipelining for R8-MBE synthesis

Distributed

```
Using 0 stages of pipeline
4260 ps
Using 1 stages of pipeline
2220 ps
Using 2 stages of pipeline
1680 ps
Using 3 stages of pipeline
1320 ps
Using 4 stages of pipeline
1080 ps
Using 5 stages of pipeline
1080 ps
Using 6 stages of pipeline
1280 ps
Using 7 stages of pipeline
1320 ps
Using 8 stages of pipeline
1230 ps
Using 9 stages of pipeline
1510 ps
Using 10 stages of pipeline
1380 ps
Using 11 stages of pipeline
1430 ps
Using 12 stages of pipeline
1330 ps
Using 13 stages of pipeline
1450 ps
Using 14 stages of pipeline
1440 ps
Using 15 stages of pipeline
1560 ps
Using 16 stages of pipeline
1530 ps
Using 17 stages of pipeline
1580 ps
Using 18 stages of pipeline
1550 ps
Using 19 stages of pipeline
1170 ps
Using 20 stages of pipeline
1170 ps
```

1.3.6 Reports normal compilation

Report timing

```
Information: Updating design information... (UID-85)
Warning: There are infeasible paths detected in your design that were ignored during
    optimization. Please run 'report_timing -attributes' and/or 'create_qor_snapshot/
    query_qor_snapshot -infeasible_paths' to identify these paths. (OPT-1721)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 14 12:06:13 2022
****************************************

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/inp_pipe_operands_q_reg
      [1][1][24]
            (rising edge-triggered flip-flop clocked by MY_CLK)
  Endpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/mid_pipe_sum_q_reg
      [1][68]
          (rising edge-triggered flip-flop clocked by MY_CLK)
  Path Group: MY_CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fpnew_top          5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
  clock MY_CLK (rise edge)                                0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/inp_pipe_operands_q_reg[1][1][24]/CK
       (DFFR_X1)
                                                          0.00       0.00 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/inp_pipe_operands_q_reg[1][1][24]/Q
      (DFFR_X1)
                                                          0.08       0.08 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/i_class_inputs/operands_i[1][24] (
      fpnew_classifier_0_3)
                                                          0.00       0.08 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/i_class_inputs/U60/ZN (INV_X1)
                                                          0.03       0.11 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/i_class_inputs/U13/ZN (AND4_X2)
                                                          0.07       0.18 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/i_class_inputs/U74/ZN (NAND3_X1)
                                                          0.03       0.21 f
```

```
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/i_class_inputs/U75/ZN (AOI21_X1)
                                                0.05       0.26 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/i_class_inputs/info_o[1][
    is_subnormal] (fpnew_classifier_0_3)
                                                0.00       0.26 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U1042/ZN (OR2_X1)
                                                0.04       0.30 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_1_root_sub_287/CI (
    fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_add_8)
                                                0.00       0.30 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_1_root_sub_287/U132/
    ZN (INV_X1)
                                                0.02       0.32 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_1_root_sub_287/U131/
    ZN (OAI21_X1)
                                                0.05       0.37 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_1_root_sub_287/U137/
    ZN (AOI21_X1)
                                                0.04       0.41 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_1_root_sub_287/U142/
    ZN (INV_X1)
                                                0.04       0.45 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_1_root_sub_287/U146/
    ZN (XNOR2_X1)
                                                0.07       0.51 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_1_root_sub_287/SUM[3]
     (fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_add_8)
                                                0.00       0.51 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U1074/ZN (INV_X1)
                                                0.03       0.55 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U1075/ZN (NOR3_X1)
                                                0.07       0.61 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U460/ZN (XNOR2_X1)
                                                0.06       0.67 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U459/ZN (NOR2_X1)
                                                0.03       0.70 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/B[4] (
    fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_sub_12)
                                                0.00       0.70 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U145/ZN (INV_X1)
                                                0.03       0.73 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U89/ZN (OR2_X1)
                                                0.04       0.77 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U156/ZN (NAND2_X1)
```

```
                                                  0.03       0.80 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U152/ZN (OAI21_X1)
                                                  0.06       0.85 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U137/ZN (AOI21_X2)
                                                  0.05       0.90 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U159/ZN (OAI21_X1)
                                                  0.05       0.95 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/U106/ZN (XNOR2_X1)
                                                  0.07       1.02 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293/DIFF[8] (
    fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_sub_12)
                                                  0.00       1.02 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U240/ZN (OAI211_X1)
                                                  0.05       1.06 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U241/ZN (INV_X1)
                                                  0.03       1.09 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U1105/ZN (NAND2_X1)
                                                  0.03       1.12 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U1123/ZN (NAND2_X1)
                                                  0.04       1.16 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U749/ZN (OAI211_X1)
                                                  0.05       1.21 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U748/Z (BUF_X2)
                                                  0.05       1.27 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U284/ZN (NAND2_X1)
                                                  0.05       1.31 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U282/Z (BUF_X1)
                                                  0.04       1.35 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U1239/ZN (INV_X1)
                                                  0.03       1.38 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U663/ZN (NAND2_X1)
                                                  0.04       1.42 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U375/ZN (AND4_X1)
                                                  0.08       1.50 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U1515/ZN (OAI22_X1)
                                                  0.04       1.53 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U1516/ZN (INV_X1)
                                                  0.03       1.56 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U1517/ZN (OAI211_X1)
                                                  0.04       1.61 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U1518/ZN (INV_X1)
                                                  0.04       1.64 r
```

```
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U1627/Z (MUX2_X1)
                                                  0.08       1.72 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U1628/ZN (NAND2_X1)
                                                  0.03       1.75 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/B[12] (
    fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_add_11)
                                                  0.00       1.75 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U1282/ZN (
    NAND2_X1)
                                                  0.04       1.79 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U1279/ZN (
    OAI21_X1)
                                                  0.05       1.84 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U1167/ZN (
    AOI21_X1)
                                                  0.03       1.87 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U1438/ZN (
    OAI21_X1)
                                                  0.03       1.90 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U1157/ZN (
    AOI21_X1)
                                                  0.03       1.94 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U963/ZN (
    OAI21_X1)
                                                  0.07       2.00 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U889/Z (
    CLKBUF_X3)
                                                  0.07       2.07 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U1378/ZN (
    AOI21_X1)
                                                  0.04       2.11 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/U1184/ZN (
    XNOR2_X1)
                                                  0.06       2.17 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_1_root_add_368_2/SUM[59] (
    fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_add_11)
                                                  0.00       2.17 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/B[59] (
    fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_sub_7)
                                                  0.00       2.17 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U710/ZN (NOR2_X1)
                                                  0.05       2.22 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U525/ZN (NAND2_X1)
                                                  0.03       2.25 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U687/ZN (NOR2_X1)
```

```
                                                  0.04       2.29 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U755/ZN (NAND2_X1)
                                                  0.03       2.32 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U713/ZN (NOR2_X1)
                                                  0.05       2.37 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U449/ZN (NAND2_X1)
                                                  0.05       2.42 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U752/ZN (NOR2_X1)
                                                  0.05       2.47 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U727/ZN (XNOR2_X1)
                                                  0.06       2.53 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/DIFF[68] (
    fpnew_fma_0_00000003_3__logic_Z_1yB___logic_Z_1yB__DW01_sub_7)
                                                  0.00       2.53 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U1811/ZN (NAND2_X1)
                                                  0.03       2.56 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U1812/ZN (OAI221_X1)
                                                  0.03       2.59 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mid_pipe_sum_q_reg[1][68]/D (DFFR_X1
    )
                                                  0.01       2.60 r
data arrival time                                            2.60

clock MY_CLK (rise edge)                          0.10       0.10
clock network delay (ideal)                       0.00       0.10
clock uncertainty                                -0.01       0.09
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mid_pipe_sum_q_reg[1][68]/CK (
    DFFR_X1)
                                                  0.00       0.09 r
library setup time                               -0.04       0.05
data required time                                           0.05
-------------------------------------------------------------------
data required time                                           0.05
data arrival time                                           -2.60
-------------------------------------------------------------------
slack (VIOLATED)                                            -2.55
```

1

Report area

```
****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 14 12:06:13 2022
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
        NangateOpenCellLibrary_typical_ecsm_nowlm.db)

Number of ports:                         3458
Number of nets:                         11218
Number of cells:                         7870
Number of combinational cells:           7500
Number of sequential cells:               297
Number of macros/black boxes:               0
Number of buf/inv:                       2006
Number of references:                      18

Combinational area:               8753.527994
Buf/Inv area:                     1286.907997
Noncombinational area:            1587.488051
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 10341.016045
Total area:                 undefined
1
```

1.3.7 Reports optimize registers

Report timing

```
Information: Updating design information... (UID-85)
Warning: Design 'fpnew_top' contains 1 high-fanout nets. A fanout number of 1000 will be
    used for delay calculations involving these nets. (TIM-134)
Warning: There are infeasible paths detected in your design that were ignored during
    optimization. Please run 'report_timing -attributes' and/or 'create_qor_snapshot/
    query_qor_snapshot -infeasible_paths' to identify these paths. (OPT-1721)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 14 12:14:42 2022
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/i_lzc/MY_CLK_r_REG243_S3
            (rising edge-triggered flip-flop clocked by MY_CLK)
  Endpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/MY_CLK_r_REG61_S4
          (rising edge-triggered flip-flop clocked by MY_CLK)
  Path Group: MY_CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fpnew_top          5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
  clock MY_CLK (rise edge)                                0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/i_lzc/MY_CLK_r_REG243_S3/CK (DFFS_X1
      )
                                                          0.00 #     0.00 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/i_lzc/MY_CLK_r_REG243_S3/Q (DFFS_X1)
                                                          0.09       0.09 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/i_lzc/U28/ZN (NAND2_X1)
                                                          0.03       0.11 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/i_lzc/U152/ZN (AOI221_X1)
                                                          0.08       0.20 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/i_lzc/U162/ZN (OAI221_X1)
                                                          0.05       0.25 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/i_lzc/cnt_o[1] (lzc_00000033_1)
                                                          0.00       0.25 f
```

```
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U30/Z (CLKBUF_X1)
                                                    0.05       0.30 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U837/ZN (XNOR2_X1)
                                                    0.05       0.35 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U743/ZN (NOR2_X1)
                                                    0.03       0.38 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U738/ZN (AND4_X1)
                                                    0.06       0.45 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U737/ZN (AND2_X1)
                                                    0.04       0.49 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U489/ZN (NAND3_X1)
                                                    0.03       0.52 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U317/ZN (OAI22_X1)
                                                    0.04       0.56 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U2147/ZN (INV_X1)
                                                    0.03       0.58 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U560/ZN (NAND2_X2)
                                                    0.05       0.63 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U827/ZN (OAI222_X1)
                                                    0.06       0.70 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U27/Z (BUF_X1)
                                                    0.05       0.75 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U40/ZN (AND2_X2)
                                                    0.05       0.79 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U507/Z (BUF_X2)
                                                    0.06       0.85 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U2305/ZN (AOI22_X1)
                                                    0.06       0.91 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U2306/ZN (OAI221_X1)
                                                    0.05       0.97 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U2309/ZN (AOI221_X1)
                                                    0.09       1.06 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U2310/ZN (OAI221_X1)
                                                    0.05       1.11 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U587/ZN (OAI211_X1)
                                                    0.04       1.16 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U246/ZN (OAI211_X1)
                                                    0.05       1.21 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U390/ZN (INV_X1)
                                                    0.04       1.25 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/U776/ZN (NAND3_X1)
```

```
                                                                0.03       1.28 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/MY_CLK_r_REG61_S4/D (DFFS_X1)
                                                                0.01       1.29 f
  data arrival time                                                        1.29

  clock MY_CLK (rise edge)                                      0.10       0.10
  clock network delay (ideal)                                   0.00       0.10
  clock uncertainty                                            -0.01       0.09
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/MY_CLK_r_REG61_S4/CK (DFFS_X1)
                                                                0.00       0.09 r
  library setup time                                           -0.04       0.05
  data required time                                                       0.05
  ---------------------------------------------------------------------------
  data required time                                                       0.05
  data arrival time                                                       -1.29
  ---------------------------------------------------------------------------
  slack (VIOLATED)                                                        -1.23
```

1

Report area

```
****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 14 12:14:42 2022
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
        NangateOpenCellLibrary_typical_ecsm_nowlm.db)

Number of ports:                         3398
Number of nets:                          9973
Number of cells:                         7834
Number of combinational cells:           6436
Number of sequential cells:              1029
Number of macros/black boxes:               0
Number of buf/inv:                       1476
Number of references:                      15

Combinational area:               7646.435992
Buf/Inv area:                      848.008003
Noncombinational area:            5479.334175
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 13125.770167
Total area:                 undefined
1
```

1.3.8 Reports compile ultra

Report timing

```
Information: Updating design information... (UID-85)
Warning: There are infeasible paths detected in your design that were ignored during
    optimization. Please run 'report_timing -attributes' and/or 'create_qor_snapshot/
    query_qor_snapshot -infeasible_paths' to identify these paths. (OPT-1721)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 14 12:24:28 2022
****************************************

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/inp_pipe_op_q_reg[3][0]
           (rising edge-triggered flip-flop clocked by MY_CLK)
  Endpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/mid_pipe_sum_q_reg[1][8]
           (rising edge-triggered flip-flop clocked by MY_CLK)
  Path Group: MY_CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fpnew_top          5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
  clock MY_CLK (rise edge)                                0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/inp_pipe_op_q_reg[3][0]/CK (DFFR_X1)
                                                          0.00       0.00 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/inp_pipe_op_q_reg[3][0]/Q (DFFR_X1)
                                                          0.12       0.12 r
  U1249/ZN (OR2_X2)                                       0.06       0.18 r
  U224/ZN (AND2_X2)                                       0.06       0.24 r
  U1263/ZN (XNOR2_X1)                                     0.06       0.30 r
  U1656/ZN (NOR2_X1)                                      0.03       0.34 f
  U1675/ZN (OAI21_X1)                                     0.06       0.40 r
  U1676/ZN (INV_X1)                                       0.03       0.42 f
  U1678/ZN (OAI21_X1)                                     0.04       0.46 r
  U1679/ZN (AOI21_X1)                                     0.03       0.49 f
  U1300/ZN (XNOR2_X1)                                     0.06       0.55 f
  U1072/ZN (OR2_X1)                                       0.06       0.62 f
  U1335/ZN (NAND3_X1)                                     0.03       0.65 r
  U1391/ZN (NOR2_X1)                                      0.03       0.68 f
  U311/ZN (NOR2_X2)                                       0.05       0.73 r
  U1824/ZN (NAND2_X1)                                     0.03       0.77 f
  U1827/ZN (OAI21_X1)                                     0.06       0.83 r
  U1836/ZN (XNOR2_X1)                                     0.06       0.89 r
  U1336/ZN (NAND4_X1)                                     0.04       0.93 f
```

```
U610/ZN (AND2_X2)                                                    0.05       0.98 f
U1289/ZN (NOR2_X1)                                                   0.05       1.02 r
U1247/ZN (NAND2_X1)                                                  0.04       1.06 f
U2141/ZN (INV_X2)                                                    0.07       1.13 r
U2260/Z (MUX2_X1)                                                    0.08       1.22 f
U2261/ZN (AOI22_X1)                                                  0.07       1.28 r
U2262/ZN (OR2_X1)                                                    0.04       1.33 r
U2263/ZN (OAI211_X1)                                                 0.06       1.39 f
U3116/ZN (OR2_X1)                                                    0.07       1.45 f
U130/ZN (AND4_X2)                                                    0.04       1.50 f
U596/ZN (OAI21_X1)                                                   0.05       1.55 r
U3132/S (FA_X1)                                                      0.12       1.67 f
U1253/ZN (NOR2_X2)                                                   0.06       1.73 r
U3164/ZN (OAI21_X1)                                                  0.04       1.78 f
U3173/ZN (AOI21_X1)                                                  0.05       1.83 r
U3174/ZN (OAI21_X1)                                                  0.04       1.86 f
U3200/ZN (AOI21_X1)                                                  0.05       1.92 r
U3628/ZN (OAI21_X1)                                                  0.04       1.95 f
U3690/ZN (AOI21_X1)                                                  0.04       2.00 r
U3691/ZN (XNOR2_X1)                                                  0.06       2.06 r
U3692/ZN (NAND2_X1)                                                  0.04       2.10 f
U1282/ZN (OR2_X2)                                                    0.07       2.17 f
U1229/Z (BUF_X2)                                                     0.06       2.23 f
U5978/ZN (OR2_X1)                                                    0.07       2.30 f
U1213/ZN (NAND3_X1)                                                  0.03       2.33 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mid_pipe_sum_q_reg[1][8]/D (DFFR_X2)
                                                                     0.01       2.34 r
data arrival time                                                               2.34

clock MY_CLK (rise edge)                                             0.10       0.10
clock network delay (ideal)                                          0.00       0.10
clock uncertainty                                                   -0.01       0.09
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mid_pipe_sum_q_reg[1][8]/CK (DFFR_X2
    )
                                                                     0.00       0.09 r
library setup time                                                  -0.03       0.06
data required time                                                              0.06
-------------------------------------------------------------------------------------
data required time                                                              0.06
data arrival time                                                              -2.34
-------------------------------------------------------------------------------------
slack (VIOLATED)                                                               -2.28
```

1

Report area

```
****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 14 12:24:28 2022
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
        NangateOpenCellLibrary_typical_ecsm_nowlm.db)

Number of ports:                          160
Number of nets:                          9540
Number of cells:                         8872
Number of combinational cells:           7902
Number of sequential cells:               963
Number of macros/black boxes:               0
Number of buf/inv:                       1166
Number of references:                      59

Combinational area:               9795.981987
Buf/Inv area:                      705.166002
Noncombinational area:            5145.238165
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 14941.220152
Total area:                 undefined
1
```

Report resources

```
****************************************
Report : resources
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 14 12:24:28 2022
****************************************


Resource Report for this hierarchy in file ../src/fpnew_top.sv
===============================================================================
| Cell            | Module          | Parameters | Contained Operations       |
===============================================================================
| lte_x_4         | DW_cmp          | width=2    | i_arbiter/lte_209_G4 (rr_arb_tree.sv:209)
   |
| DP_OP_354_134_8861              |            |                              |
|                 | DP_OP_354_134_8861 |        |                              |
| DP_OP_355_135_8861              |            |                              |
|                 | DP_OP_355_135_8861 |        |                              |
| DP_OP_115_136_6795              |            |                              |
|                 | DP_OP_115_136_6795 |        |                              |
| DP_OP_116_137_5515              |            |                              |
|                 | DP_OP_116_137_5515 |        |                              |
===============================================================================

Datapath Report for DP_OP_354_134_8861
===============================================================================
| Cell                | Contained Operations                                  |
===============================================================================
| DP_OP_354_134_8861  | add_542 (fpnew_fma.sv:542)                            |
===============================================================================

===============================================================================
|      |      | Data    |       |                                              |
| Var  | Type | Class   | Width | Expression                                   |
===============================================================================
| I1   | PI   | Signed  | 10    |                                              |
| O1   | PO   | Unsigned| 10    | I1 + $unsigned(1'b1) (fpnew_fma.sv:542)      |
===============================================================================

Datapath Report for DP_OP_355_135_8861
===============================================================================
| Cell                | Contained Operations                                  |
===============================================================================
| DP_OP_355_135_8861  | sub_549 (fpnew_fma.sv:549)                            |
===============================================================================

===============================================================================
|      |      | Data    |       |                                              |
| Var  | Type | Class   | Width | Expression                                   |
===============================================================================
| I1   | PI   | Signed  | 10    |                                              |
| O1   | PO   | Signed  | 10    | I1 - $unsigned(1'b1) (fpnew_fma.sv:549)      |
===============================================================================

Datapath Report for DP_OP_115_136_6795
===============================================================================
| Cell                | Contained Operations                                  |
===============================================================================
| DP_OP_115_136_6795  | add_514 (fpnew_fma.sv:514)                            |
```

```
============================================================================

============================================================================
|      |      | Data     |       |                                        |
| Var  | Type | Class    | Width | Expression                             |
============================================================================
| I1   | PI   | Unsigned | 6     |                                        |
| O1   | PO   | Unsigned | 7     | $unsigned(5'b11010) + I1 (fpnew_fma.sv:514) |
============================================================================

Datapath Report for DP_OP_116_137_5515
============================================================================
| Cell                | Contained Operations                             |
============================================================================
| DP_OP_116_137_5515  | add_519 (fpnew_fma.sv:519)                       |
============================================================================

============================================================================
|      |      | Data     |       |                                        |
| Var  | Type | Class    | Width | Expression                             |
============================================================================
| I1   | PI   | Signed   | 7     |                                        |
| O1   | PO   | Unsigned | 7     | $unsigned(5'b11010) + I1 (fpnew_fma.sv:519) |
============================================================================


Resource Report for Ungrouped Hierarchy
        gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
            i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma
        in file ../src/fpnew_fma.sv
============================================================================
| Cell            | Module          | Parameters | Contained Operations       |
============================================================================
| gt_x_41         | DW_cmp          | width=10   | gt_295 (fpnew_fma.sv:295)  |
| lte_x_43        | DW_cmp          | width=10   | lte_302 (fpnew_fma.sv:302) |
| lte_x_44        | DW_cmp          | width=10   | lte_305 (fpnew_fma.sv:305) |
| ashr_46         | DW_rightsh      | A_width=100 | srl_349 (fpnew_fma.sv:349) |
                |                 | SH_width=7 |                            |
| lte_x_94        | DW_cmp          | width=10   | lte_510 (fpnew_fma.sv:510) |
| lte_x_95        | DW_cmp          | width=10   | lte_510_2 (fpnew_fma.sv:510) |
| ash_99          | DW_leftsh       | A_width=77 | sll_530 (fpnew_fma.sv:530) |
|                 |                 | SH_width=7 |                            |
| gt_x_100        | DW_cmp          | width=10   | gt_547 (fpnew_fma.sv:547)  |
| gte_x_103       | DW_cmp          | width=10   | gte_576 (fpnew_fma.sv:576) |
| add_x_140       | DW01_add        | width=31   | i_fpnew_rounding/add_63 (fpnew_rounding.sv
    :63) |
| DP_OP_358J1_122_9434            |            |                            |
|                 | DP_OP_358J1_122_9434 |       |                            |
| DP_OP_359J1_123_7663            |            |                            |
|                 | DP_OP_359J1_123_7663 |       |                            |
| DP_OP_360J1_124_4836            |            |                            |
|                 | DP_OP_360J1_124_4836 |       |                            |
| DP_OP_361J1_125_9568            |            |                            |
|                 | DP_OP_361J1_125_9568 |       |                            |
============================================================================

Datapath Report for DP_OP_358J1_122_9434
============================================================================
| Cell                | Contained Operations                             |
============================================================================
| DP_OP_358J1_122_9434 | add_285 (fpnew_fma.sv:285)                      |
|                     | sub_293 (fpnew_fma.sv:293)                       |
```

```
|                       | sub_306 (fpnew_fma.sv:306)                                  |
===============================================================================

===============================================================================
|        |      | Data     |       |                                             |
| Var    | Type | Class    | Width | Expression                                  |
===============================================================================
| I1     | PI   | Unsigned | 8     |                                             |
| I2     | PI   | Unsigned | 1     |                                             |
| I3     | PI   | Signed   | 10    |                                             |
| T206   | IFO  | Signed   | 7     | O2[6:0]                                     |
| O1     | PO   | Unsigned | 10    | I1 + I2 (fpnew_fma.sv:285)                  |
| O2     | PO   | Signed   | 10    | O1 - I3 (fpnew_fma.sv:293)                  |
| O3     | PO   | Signed   | 7     | $unsigned(5'b11011) - T206 (fpnew_fma.sv:306) |
===============================================================================

Datapath Report for DP_OP_359J1_123_7663
===============================================================================
| Cell                  | Contained Operations                                |
===============================================================================
| DP_OP_359J1_123_7663 | add_287 (fpnew_fma.sv:287)                           |
|                       | add_287_2 (fpnew_fma.sv:287)                        |
|                       | add_287_3 (fpnew_fma.sv:287)                        |
|                       | sub_287 (fpnew_fma.sv:287)                          |
===============================================================================

===============================================================================
|        |      | Data     |       |                                             |
| Var    | Type | Class    | Width | Expression                                  |
===============================================================================
| I1     | PI   | Unsigned | 8     |                                             |
| I2     | PI   | Unsigned | 1     |                                             |
| I3     | PI   | Unsigned | 8     |                                             |
| I4     | PI   | Unsigned | 1     |                                             |
| O1     | PO   | Signed   | 10    | I1 + I2 + I3 + I4 - $unsigned(7'b1111111) (fpnew_fma.sv
    :287) |
===============================================================================

Datapath Report for DP_OP_360J1_124_4836
===============================================================================
| Cell                  | Contained Operations                                |
===============================================================================
| DP_OP_360J1_124_4836 | mult_325 (fpnew_fma.sv:325)                          |
|                       | add_368 (fpnew_fma.sv:368)                          |
|                       | add_368_2 (fpnew_fma.sv:368)                        |
|                       | sub_372 (fpnew_fma.sv:372)                          |
===============================================================================

===============================================================================
|        |      | Data     |       |                                             |
| Var    | Type | Class    | Width | Expression                                  |
===============================================================================
| I1     | PI   | Unsigned | 24    |                                             |
| I2     | PI   | Unsigned | 24    |                                             |
| I3     | PI   | Unsigned | 76    |                                             |
| I4     | PI   | Unsigned | 1     |                                             |
| T52    | IFO  | Unsigned | 48    | I1 * I2 (fpnew_fma.sv:325)                  |
| T212   | IFO  | Unsigned | 50    | T52 << 2                                    |
| T214   | IFO  | Signed   | 76    | O1[75:0]                                    |
| O1     | PO   | Unsigned | 77    | T212 + I3 + I4 (fpnew_fma.sv:368)           |
| O2     | PO   | Signed   | 76    | $unsigned(1'b0) - T214 (fpnew_fma.sv:372) |
===============================================================================
```

Datapath **Report for** DP_OP_361J1_125_9568

Cell	Contained Operations
DP_OP_361J1_125_9568	sub_512 (fpnew_fma.sv:512)
	add_512 (fpnew_fma.sv:512)
	sub_515 (fpnew_fma.sv:515)
	add_515 (fpnew_fma.sv:515)
	gte_512 (fpnew_fma.sv:512)

Var	**Type**	Data Class	Width	Expression
I1	PI	Unsigned	6	
I2	PI	Signed	10	
T351	IFO	Signed	7	-I1 + $unsigned(1'b1) (fpnew_fma.sv:512 fpnew_fma.sv:515)
T347	IFO	Signed	12	I2 + T351 (fpnew_fma.sv:512)
O1	PO	Signed	1	T347 >= $signed(1'b0) (fpnew_fma.sv:512)
O2	PO	Signed	10	I2 + T351 (fpnew_fma.sv:515)

Implementation **Report**

Cell	Module	Current Implementation	Set Implementation
lte_x_4	DW_cmp	apparch (area)	
gt_x_41	DW_cmp	apparch (area)	
lte_x_43	DW_cmp	apparch (area)	
lte_x_44	DW_cmp	apparch (area)	
ashr_46	DW_rightsh	astr (area)	
lte_x_94	DW_cmp	apparch (area)	
lte_x_95	DW_cmp	apparch (area)	
ash_99	DW_leftsh	astr (area)	
gt_x_100	DW_cmp	apparch (area)	
gte_x_103	DW_cmp	apparch (area)	
add_x_140	DW01_add	pparch (area,speed)	
DP_OP_354_134_8861	DP_OP_354_134_8861	str (area,speed)	
DP_OP_355_135_8861	DP_OP_355_135_8861	str (area,speed)	
DP_OP_115_136_6795	DP_OP_115_136_6795	str (area,speed)	
DP_OP_116_137_5515	DP_OP_116_137_5515	str (area)	
DP_OP_358J1_122_9434			
	DP_OP_358J1_122_9434	str (area,speed)	
DP_OP_359J1_123_7663			
	DP_OP_359J1_123_7663	str (area,speed)	
DP_OP_360J1_124_4836			
	DP_OP_360J1_124_4836	str (area,speed)	
		mult_arch: benc_radix4	
DP_OP_361J1_125_9568			
	DP_OP_361J1_125_9568	str (area,speed)	

1

1.3.9 Reports for CSA architecture multiplier

Report timing

```
Information: Updating design information... (UID-85)
Warning: Design 'fpnew_top' contains 2 high-fanout nets. A fanout number of 1000 will be
    used for delay calculations involving these nets. (TIM-134)
Warning: There are infeasible paths detected in your design that were ignored during
    optimization. Please run 'report_timing -attributes' and/or 'create_qor_snapshot/
    query_qor_snapshot -infeasible_paths' to identify these paths. (OPT-1721)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 14 12:32:29 2022
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/
      MY_CLK_r_REG1573_S5
            (rising edge-triggered flip-flop clocked by MY_CLK)
  Endpoint: MY_CLK_r_REG410_S7
           (rising edge-triggered flip-flop clocked by MY_CLK)
  Path Group: MY_CLK
  Path Type: max

  Des/Clust/Port      Wire Load Model       Library
  ------------------------------------------------
  fpnew_top           5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                 Incr       Path
  ------------------------------------------------------------------------
  clock MY_CLK (rise edge)                              0.00       0.00
  clock network delay (ideal)                           0.00       0.00
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/MY_CLK_r_REG1573_S5/CK (
      DFFR_X1)
                                                        0.00 #     0.00 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/MY_CLK_r_REG1573_S5/Q (
      DFFR_X1)
                                                        0.10       0.10 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/U11/Z (BUF_X2)
                                                        0.05       0.15 r
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/U727/ZN (NOR2_X1)
                                                        0.03       0.19 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/S2_19_4/CO (FA_X1)
                                                        0.10       0.29 f
  gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
      gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/S2_20_4/CO (FA_X1)
```

```
                                                  0.11       0.40 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/S2_21_4/CO (FA_X1)
                                                  0.11       0.50 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/S2_22_4/S (FA_X1)
                                                  0.13       0.63 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/S4_3/S (FA_X1)
                                                  0.14       0.77 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/U67/Z (XOR2_X1)
                                                  0.10       0.86 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/FS_1/A[24] (
    fpnew_top_DW01_add_11)
                                                  0.00       0.86 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/FS_1/U36/ZN (OR2_X1)
                                                  0.05       0.91 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/FS_1/U2/ZN (AND4_X1)
                                                  0.07       0.98 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/FS_1/U17/ZN (NAND2_X1)
                                                  0.04       1.02 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/FS_1/U197/ZN (OAI21_X1)
                                                  0.06       1.07 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/FS_1/U172/ZN (OAI21_X1)
                                                  0.03       1.10 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/FS_1/U237/ZN (NAND2_X1)
                                                  0.03       1.13 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/FS_1/U236/ZN (XNOR2_X1)
                                                  0.06       1.19 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/FS_1/SUM[35] (
    fpnew_top_DW01_add_11)
                                                  0.00       1.19 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325/PRODUCT[37] (
    fpnew_top_DW02_mult_0)
                                                  0.00       1.19 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/A[39] (
    fpnew_top_DW01_add_13)
                                                  0.00       1.19 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1195/ZN (
    NOR2_X1)
                                                  0.03       1.22 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1324/ZN (
    NOR2_X1)
                                                  0.06       1.29 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1272/ZN (
    NAND2_X1)
                                                  0.04       1.33 f
```

```
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1269/ZN (
    NOR2_X1)
                                                  0.05       1.37 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1307/ZN (
    AOI21_X1)
                                                  0.03       1.41 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1222/Z (
    BUF_X1)
                                                  0.04       1.45 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U797/Z (
    CLKBUF_X3)
                                                  0.06       1.51 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1360/ZN (
    OAI21_X1)
                                                  0.06       1.57 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1130/ZN (
    XNOR2_X1)
                                                  0.06       1.63 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/SUM[72] (
    fpnew_top_DW01_add_13)
                                                  0.00       1.63 r
U4875/ZN (INV_X1)                                 0.02       1.65 f
U2641/ZN (OR2_X1)                                 0.05       1.71 f
U2531/ZN (AND2_X1)                                0.04       1.74 f
MY_CLK_r_REG410_S7/D (DFFS_X1)                    0.01       1.75 f
data arrival time                                            1.75

clock MY_CLK (rise edge)                          0.10       0.10
clock network delay (ideal)                       0.00       0.10
clock uncertainty                                -0.01       0.09
MY_CLK_r_REG410_S7/CK (DFFS_X1)                   0.00       0.09 r
library setup time                               -0.04       0.05
data required time                                           0.05
-------------------------------------------------------------------
data required time                                           0.05
data arrival time                                           -1.75
-------------------------------------------------------------------
slack (VIOLATED)                                            -1.70
```

1

Report area

```
****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 14 12:32:29 2022
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
        NangateOpenCellLibrary_typical_ecsm_nowlm.db)

Number of ports:                         1097
Number of nets:                          9782
Number of cells:                         8070
Number of combinational cells:           6184
Number of sequential cells:              1862
Number of macros/black boxes:               0
Number of buf/inv:                       1053
Number of references:                      48

Combinational area:               8622.921983
Buf/Inv area:                      617.386002
Noncombinational area:            9909.032319
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 18531.954301
Total area:                 undefined
1
```

Report resources

```
****************************************
Report : resources
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 14 12:32:29 2022
****************************************

Resource Sharing Report for design fpnew_top in file ../src/fpnew_top.sv

================================================================================
|          |              |            | Contained     |                       |
| Resource | Module       | Parameters | Resources     | Contained Operations  |
================================================================================
| r524     | DW01_cmp2    | width=3    |               | gen_operation_groups[0].
    i_opgroup_block/i_arbiter/gt_208_G4 |
|          |              |            |               |
|          |              |            |               | gen_operation_groups[0].
    i_opgroup_block/i_arbiter/lte_209_G4 |
| r525     | DW01_cmp2    | width=3    |               | gen_operation_groups[1].
    i_opgroup_block/i_arbiter/gt_208_G4 |
|          |              |            |               |
|          |              |            |               | gen_operation_groups[1].
    i_opgroup_block/i_arbiter/lte_209_G4 |
| r526     | DW01_cmp2    | width=3    |               | gen_operation_groups[2].
    i_opgroup_block/i_arbiter/gt_208_G4 |
|          |              |            |               |
|          |              |            |               | gen_operation_groups[2].
    i_opgroup_block/i_arbiter/lte_209_G4 |
| r527     | DW01_cmp2    | width=3    |               | gen_operation_groups[3].
    i_opgroup_block/i_arbiter/gt_208_G4 |
|          |              |            |               |
|          |              |            |               | gen_operation_groups[3].
    i_opgroup_block/i_arbiter/lte_209_G4 |
| r528     | DW01_cmp2    | width=2    |               | i_arbiter/gt_208_G4   |
|          |              |            |               | i_arbiter/lte_209_G4 |
| r558     | DW01_add     | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/add_285 |
| r566     | DW01_sub     | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/sub_293 |
| r568     | DW_cmp       | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/gt_295 |
| r570     | DW_cmp       | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/lte_302 |
| r572     | DW_cmp       | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/lte_305 |
| r574     | DW01_sub     | width=7    |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/sub_306 |
| r576     | DW02_mult    | A_width=24 |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/mult_325 |
|          |              | B_width=24 |               |                       |
| r578     | DW_rightsh   | A_width=100 |              | gen_operation_groups[0].
```

```
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/sr1_349 |
|
|          |               | SH_width=7 |               |                          |
| r580     | DW01_add      | width=77   |               | add_1_root_gen_operation_groups
    [0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/add_368_2 |
| r582     | DW01_sub      | width=76   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/sub_372 |
| r584     | DW_cmp        | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/lte_510 |
| r586     | DW_cmp        | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/lte_510_2 |
| r592     | DW_cmp        | width=12   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/gte_512 |
| r594     | DW01_add      | width=7    |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/add_514 |
| r600     | DW01_add      | width=7    |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/add_519 |
| r602     | DW_leftsh     | A_width=77 |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/sll_530 |
|
|          |               | SH_width=7 |               |                          |
| r604     | DW_cmp        | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/gt_547 |
| r606     | DW01_inc      | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/add_542 |
| r608     | DW01_dec      | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/sub_549 |
| r610     | DW_cmp        | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/gte_576 |
| r612     | DW01_add      | width=31   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/i_fpnew_rounding/add_63 |
| r1340    | DW01_add      | width=10   |               |
    add_1_root_add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_287 |
| r1342    | DW01_sub      | width=10   |               |
    sub_2_root_add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_287 |
| r1344    | DW01_add      | width=10   |               |
    add_0_root_add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_287 |
| r2064    | DW01_sub      | width=11   |               | sub_1_root_gen_operation_groups
    [0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/add_512 |
| r2066    | DW01_inc      | width=12   |               | add_0_root_gen_operation_groups
    [0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/add_512 |
| r2786    | DW01_sub      | width=10   |               | sub_1_root_gen_operation_groups
    [0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
```

```
    active_lane.lane_instance.i_fma/add_515 |
| r2788     | DW01_inc      | width=10    |                | add_0_root_gen_operation_groups
    [0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/add_515 |
===============================================================================


Implementation Report
===============================================================================
|                      |                  | Current          | Set            |
| Cell                 | Module           | Implementation   | Implementation |
===============================================================================
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372 |
|                      | DW01_sub         | pparch (area,speed)                |
| add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2 |
|                      | DW01_add         | pparch (area,speed)                |
| add_0_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_515 |
|                      | DW01_inc         | pparch (speed)     |               |
| sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_515 |
|                      | DW01_sub         | pparch (speed)     |               |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/i_fpnew_rounding/add_63 |
|                      | DW01_add         | pparch (area,speed)                |
| add_1_root_add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_287 |
|                      | DW01_add         | pparch (area,speed)                |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293 |
|                      | DW01_sub         | pparch (area,speed)                |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325 |
|                      | DW02_mult        | csa              | csa           |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_542 |
|                      | DW01_inc         | rpl              |               |
===============================================================================

1
```

1.3.10 Reports for PPARCH architecture multiplier

Report timing

```
Information: Updating design information... (UID-85)
Warning: Design 'fpnew_top' contains 1 high-fanout nets. A fanout number of 1000 will be
    used for delay calculations involving these nets. (TIM-134)
Warning: There are infeasible paths detected in your design that were ignored during
    optimization. Please run 'report_timing -attributes' and/or 'create_qor_snapshot/
    query_qor_snapshot -infeasible_paths' to identify these paths. (OPT-1721)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 14 12:41:20 2022
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: MY_CLK_r_REG810_S4
              (rising edge-triggered flip-flop clocked by MY_CLK)
  Endpoint: gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/
      MY_CLK_r_REG218_S5
            (rising edge-triggered flip-flop clocked by MY_CLK)
  Path Group: MY_CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fpnew_top          5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
  clock MY_CLK (rise edge)                                0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  MY_CLK_r_REG810_S4/CK (DFFS_X1)                         0.00 #     0.00 r
  MY_CLK_r_REG810_S4/Q (DFFS_X1)                          0.09       0.09 f
  U2529/ZN (AND2_X1)                                      0.05       0.14 f
  U2531/ZN (NOR3_X1)                                      0.06       0.20 r
  U4011/ZN (OAI211_X1)                                    0.05       0.25 f
  U2729/ZN (INV_X1)                                       0.03       0.28 r
  U4126/ZN (AOI22_X1)                                     0.03       0.31 f
  U4127/Z (XOR2_X1)                                       0.08       0.39 f
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/B[8] (
      fpnew_top_DW01_add_23)
                                                          0.00       0.39 f
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1079/ZN (
      OR2_X2)
                                                          0.06       0.45 f
  add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
      i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1384/ZN (
      AOI21_X1)
```

```
                                                    0.04       0.49 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1590/ZN (
    OAI21_X1)
                                                    0.04       0.53 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1259/ZN (
    AOI21_X1)
                                                    0.06       0.59 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1339/ZN (
    OAI21_X1)
                                                    0.03       0.62 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1571/ZN (
    AOI21_X1)
                                                    0.07       0.69 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1036/Z (
    BUF_X2)
                                                    0.06       0.76 r
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1641/ZN (
    OAI21_X1)
                                                    0.04       0.79 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/U1168/Z (
    XOR2_X1)
                                                    0.07       0.86 f
add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2/SUM[53] (
    fpnew_top_DW01_add_23)
                                                    0.00       0.86 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/B[53] (fpnew_top_DW01_sub_7)
                                                    0.00       0.86 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U600/ZN (NOR2_X1)
                                                    0.05       0.91 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U699/ZN (NAND2_X1)
                                                    0.03       0.94 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U695/ZN (NOR2_X1)
                                                    0.04       0.99 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U714/ZN (NAND2_X1)
                                                    0.03       1.02 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U434/ZN (NOR2_X1)
                                                    0.04       1.06 r
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/U406/ZN (NAND2_X1)
                                                    0.03       1.09 f
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/MY_CLK_r_REG218_S5/D (
    DFFR_X1)
                                                    0.01       1.10 f
data arrival time                                              1.10

clock MY_CLK (rise edge)                            0.10       0.10
clock network delay (ideal)                         0.00       0.10
```

```
clock uncertainty                                                    -0.01       0.09
gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372/MY_CLK_r_REG218_S5/CK (
    DFFR_X1)
                                                                          0.00       0.09 r
library setup time                                                   -0.04       0.05
data required time                                                               0.05
-------------------------------------------------------------------------------------------
data required time                                                               0.05
data arrival time                                                               -1.10
-------------------------------------------------------------------------------------------
slack (VIOLATED)                                                                -1.04
```

1

Report area

```
****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 14 12:41:21 2022
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
        NangateOpenCellLibrary_typical_ecsm_nowlm.db)

Number of ports:                          961
Number of nets:                          9479
Number of cells:                         8153
Number of combinational cells:           6599
Number of sequential cells:              1534
Number of macros/black boxes:               0
Number of buf/inv:                       1324
Number of references:                      55

Combinational area:               8197.055983
Buf/Inv area:                      772.198002
Noncombinational area:            8166.998263
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 16364.054246
Total area:                 undefined
1
```

Report resources

```
****************************************
Report : resources
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 14 12:41:21 2022
****************************************

Resource Sharing Report for design fpnew_top in file ../src/fpnew_top.sv

================================================================================
|          |              |            | Contained     |                       |
| Resource | Module       | Parameters | Resources     | Contained Operations  |
================================================================================
| r487     | DW01_cmp2    | width=3    |               | gen_operation_groups[0].
    i_opgroup_block/i_arbiter/gt_208_G4 |
|          |              |            |               |
|          |              |            |               | gen_operation_groups[0].
    i_opgroup_block/i_arbiter/lte_209_G4 |
| r488     | DW01_cmp2    | width=3    |               | gen_operation_groups[1].
    i_opgroup_block/i_arbiter/gt_208_G4 |
|          |              |            |               |
|          |              |            |               | gen_operation_groups[1].
    i_opgroup_block/i_arbiter/lte_209_G4 |
| r489     | DW01_cmp2    | width=3    |               | gen_operation_groups[2].
    i_opgroup_block/i_arbiter/gt_208_G4 |
|          |              |            |               |
|          |              |            |               | gen_operation_groups[2].
    i_opgroup_block/i_arbiter/lte_209_G4 |
| r490     | DW01_cmp2    | width=3    |               | gen_operation_groups[3].
    i_opgroup_block/i_arbiter/gt_208_G4 |
|          |              |            |               |
|          |              |            |               | gen_operation_groups[3].
    i_opgroup_block/i_arbiter/lte_209_G4 |
| r491     | DW01_cmp2    | width=2    |               | i_arbiter/gt_208_G4   |
|          |              |            |               | i_arbiter/lte_209_G4  |
| r521     | DW01_add     | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/add_285 |
| r529     | DW01_sub     | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/sub_293 |
| r531     | DW_cmp       | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/gt_295 |
| r533     | DW_cmp       | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/lte_302 |
| r535     | DW_cmp       | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/lte_305 |
| r537     | DW01_sub     | width=7    |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/sub_306 |
| r539     | DW02_mult    | A_width=24 |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/mult_325 |
|          |              | B_width=24 |               |                       |
| r541     | DW_rightsh   | A_width=100 |              | gen_operation_groups[0].
```

```
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/sr1_349 |
|
|          |               | SH_width=7 |               |                                |
| r543     | DW01_add      | width=77   |               | add_1_root_gen_operation_groups
    [0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/add_368_2 |
| r545     | DW01_sub      | width=76   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/sub_372 |
| r547     | DW_cmp        | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/lte_510 |
| r549     | DW_cmp        | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/lte_510_2 |
| r555     | DW_cmp        | width=12   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/gte_512 |
| r557     | DW01_add      | width=7    |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/add_514 |
| r563     | DW01_add      | width=7    |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/add_519 |
| r565     | DW_leftsh     | A_width=77 |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/sll_530 |
|
|          |               | SH_width=7 |               |                                |
| r567     | DW_cmp        | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/gt_547 |
| r569     | DW01_inc      | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/add_542 |
| r571     | DW01_dec      | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/sub_549 |
| r573     | DW_cmp        | width=10   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/gte_576 |
| r575     | DW01_add      | width=31   |               | gen_operation_groups[0].
    i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/i_fpnew_rounding/add_63 |
| r1303    | DW01_add      | width=10   |               |
    add_1_root_add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_287 |
| r1305    | DW01_sub      | width=10   |               |
    sub_2_root_add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_287 |
| r1307    | DW01_add      | width=10   |               |
    add_0_root_add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_287 |
| r2027    | DW01_sub      | width=11   |               | sub_1_root_gen_operation_groups
    [0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/add_512 |
| r2029    | DW01_inc      | width=12   |               | add_0_root_gen_operation_groups
    [0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/add_512 |
| r2749    | DW01_sub      | width=10   |               | sub_1_root_gen_operation_groups
    [0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
```

```
    active_lane.lane_instance.i_fma/add_515 |
| r2751     | DW01_inc      | width=10    |                | add_0_root_gen_operation_groups
    [0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].
    active_lane.lane_instance.i_fma/add_515 |
===============================================================================


Implementation Report
===============================================================================
|                      |                    | Current            | Set            |
| Cell                 | Module             | Implementation     | Implementation |
===============================================================================
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293 |
|                      | DW01_sub           | pparch (area,speed)                 |
| add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_368_2 |
|                      | DW01_add           | pparch (area,speed)                 |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/mult_325 |
|                      | DW02_mult          | pparch (area,speed) | pparch       |
|                      |                    | mult_arch: benc_radix4              |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_542 |
|                      | DW01_inc           | pparch (area,speed)                 |
| add_0_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_515 |
|                      | DW01_inc           | pparch (speed)      |              |
| sub_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.
    i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_515 |
|                      | DW01_sub           | pparch (speed)      |              |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/i_fpnew_rounding/add_63 |
|                      | DW01_add           | pparch (area,speed)                 |
| add_1_root_add_1_root_gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_287 |
|                      | DW01_add           | pparch (area,speed)                 |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_372 |
|                      | DW01_sub           | pparch (speed)      |              |
===============================================================================

1
```

1.3.11 Reports for R8-MBE architecture multiplier

Report timing

```
Information: Updating design information... (UID-85)
Warning: Design 'fpnew_top' contains 2 high-fanout nets. A fanout number of 1000 will be
    used for delay calculations involving these nets. (TIM-134)
Warning: There are infeasible paths detected in your design that were ignored during
    optimization. Please run 'report_timing -attributes' and/or 'create_qor_snapshot/
    query_qor_snapshot -infeasible_paths' to identify these paths. (OPT-1721)

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 14 12:54:23 2022
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: MY_CLK_r_REG1043_S1
              (rising edge-triggered flip-flop clocked by MY_CLK)
  Endpoint: MY_CLK_r_REG738_S2
            (rising edge-triggered flip-flop clocked by MY_CLK)
  Path Group: MY_CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fpnew_top          5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  ------------------------------------------------------------
  clock MY_CLK (rise edge)                 0.00       0.00
  clock network delay (ideal)              0.00       0.00
  MY_CLK_r_REG1043_S1/CK (DFFR_X1)         0.00 #     0.00 r
  MY_CLK_r_REG1043_S1/Q (DFFR_X1)          0.11       0.11 r
  U5903/Z (MUX2_X1)                        0.08       0.19 f
  U5904/ZN (AOI21_X1)                      0.05       0.24 r
  U3806/ZN (AND4_X2)                       0.06       0.31 r
  U5906/ZN (INV_X1)                        0.02       0.33 f
  U5915/ZN (AND2_X1)                       0.04       0.37 f
  U6216/ZN (NOR2_X1)                       0.04       0.41 r
  U6217/ZN (XNOR2_X1)                      0.06       0.47 r
  U6362/S (FA_X1)                          0.12       0.59 f
  U4774/ZN (OR2_X1)                        0.06       0.65 f
  U6373/ZN (AND2_X1)                       0.04       0.69 f
  U6374/ZN (XNOR2_X1)                      0.06       0.75 f
  U9970/ZN (OR2_X1)                        0.06       0.80 f
  U6451/ZN (NAND2_X1)                      0.03       0.83 r
  U6452/ZN (XNOR2_X1)                      0.07       0.90 r
  U10524/ZN (NOR2_X1)                      0.03       0.93 f
  U6561/ZN (NOR2_X1)                       0.05       0.98 r
  U6666/ZN (NAND2_X1)                      0.03       1.01 f
  U7160/ZN (OAI21_X1)                      0.05       1.05 r
  U8365/ZN (INV_X1)                        0.04       1.09 f
```

U8495/ZN (OAI21_X1)	0.04	1.13 r
MY_CLK_r_REG738_S2/D (DFFR_X2)	0.01	1.14 r
data arrival time		1.14
clock MY_CLK (rise edge)	0.10	0.10
clock network delay (ideal)	0.00	0.10
clock uncertainty	−0.01	0.09
MY_CLK_r_REG738_S2/CK (DFFR_X2)	0.00	0.09 r
library setup time	−0.03	0.06
data required time		0.06
data required time		0.06
data arrival time		−1.14
slack (VIOLATED)		−1.08

1

Report area

```
****************************************
Report : area
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 14 12:54:23 2022
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /eda/dk/nangate45/synopsys/
        NangateOpenCellLibrary_typical_ecsm_nowlm.db)

Number of ports:                        160
Number of nets:                       10639
Number of cells:                      10208
Number of combinational cells:         9068
Number of sequential cells:            1139
Number of macros/black boxes:             0
Number of buf/inv:                     1461
Number of references:                    52

Combinational area:               9854.767963
Buf/Inv area:                      826.994006
Noncombinational area:            6073.312193
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 15928.080156
Total area:                 undefined
1
```

Report resources

```
****************************************
Report : resources
Design : fpnew_top
Version: S-2021.06-SP4
Date   : Wed Dec 14 12:54:23 2022
****************************************

Resource Report for this hierarchy in file ../src/fpnew_top.sv
===============================================================================
| Cell            | Module          | Parameters | Contained Operations       |
===============================================================================
| gt_x_43         | DW_cmp          | width=10   | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/gt_295 (fpnew_fma_R8B_MBE.sv:295) |
| lte_x_47        | DW_cmp          | width=10   | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/lte_302 (fpnew_fma_R8B_MBE.sv:302) |
| lte_x_48        | DW_cmp          | width=10   | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/lte_305 (fpnew_fma_R8B_MBE.sv:305) |
| ashr_51         | DW_rightsh      | A_width=100 | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/srl_350 (fpnew_fma_R8B_MBE.sv:350) |
| SH_width=7 |  |
| lte_x_58        | DW_cmp          | width=10   | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/lte_511 (fpnew_fma_R8B_MBE.sv:511) |
| lte_x_59        | DW_cmp          | width=10   | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/lte_511_2 (fpnew_fma_R8B_MBE.sv:511) |
| ash_64          | DW_leftsh       | A_width=77 | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/sll_531 (fpnew_fma_R8B_MBE.sv:531) |
| SH_width=7 |  |
| gt_x_65         | DW_cmp          | width=10   | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/gt_548 (fpnew_fma_R8B_MBE.sv:548) |
| gte_x_69        | DW_cmp          | width=10   | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/gte_577 (fpnew_fma_R8B_MBE.sv:577) |
| add_x_80        | DW01_add        | width=26   | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/MUL/PPG/add_11 (ppg.sv:11) |
| add_x_105       | DW01_add        | width=48   | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/MUL/au/add_199 (au.sv:199) |
| add_x_137       | DW01_add        | width=31   | gen_operation_groups[0].i_opgroup_block/
    gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.
    lane_instance.i_fma/i_fpnew_rounding/add_63 (fpnew_rounding.sv:63) |
| lte_x_155       | DW_cmp          | width=2    | i_arbiter/lte_209_G4 (rr_arb_tree.sv:209)
    |
| DP_OP_312J1_122_9228            |                 |                                |
|                 | DP_OP_312J1_122_9228 |          |                                |
| DP_OP_313J1_123_2996            |                 |                                |
|                 | DP_OP_313J1_123_2996 |          |                                |
| DP_OP_314J1_124_1851            |                 |                                |
|                 | DP_OP_314J1_124_1851 |          |                                |
| DP_OP_315J1_125_1241            |                 |                                |
|                 | DP_OP_315J1_125_1241 |          |                                |
```

```
| DP_OP_51_134_568                |                                 |                                 |
|                 | DP_OP_51_134_568 |                                 |                                 |
| DP_OP_52_135_9767               |                                 |                                 |
|                 | DP_OP_52_135_9767 |                                 |                                 |
| DP_OP_308_136_3574              |                                 |                                 |
|                 | DP_OP_308_136_3574 |                                 |                                 |
| DP_OP_309_137_3574              |                                 |                                 |
|                 | DP_OP_309_137_3574 |                                 |                                 |
================================================================================

Datapath Report for DP_OP_312J1_122_9228
================================================================================
| Cell                  | Contained Operations                                    |
================================================================================
| DP_OP_312J1_122_9228 | gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_287 (
    fpnew_fma_R8B_MBE.sv:287) |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_287_2 (fpnew_fma_R8B_MBE.sv:287) |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/add_287_3 (fpnew_fma_R8B_MBE.sv:287) |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_287 (fpnew_fma_R8B_MBE.sv:287) |
================================================================================

================================================================================
|       |      | Data     |       |                                            |
| Var   | Type | Class    | Width | Expression                                 |
================================================================================
| I1    | PI   | Unsigned | 8     |                                            |
| I2    | PI   | Unsigned | 1     |                                            |
| I3    | PI   | Unsigned | 8     |                                            |
| I4    | PI   | Unsigned | 1     |                                            |
| O1    | PO   | Signed   | 10    | I1 + I2 + I3 + I4 - $unsigned(7'b1111111) (
    fpnew_fma_R8B_MBE.sv:287) |
================================================================================

Datapath Report for DP_OP_313J1_123_2996
================================================================================
| Cell                  | Contained Operations                                    |
================================================================================
| DP_OP_313J1_123_2996 | gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_285 (
    fpnew_fma_R8B_MBE.sv:285) |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293 (fpnew_fma_R8B_MBE.sv:293) |
| gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/
    gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_306 (fpnew_fma_R8B_MBE.sv:306) |
================================================================================

================================================================================
|       |      | Data     |       |                                            |
| Var   | Type | Class    | Width | Expression                                 |
================================================================================
| I1    | PI   | Unsigned | 8     |                                            |
| I2    | PI   | Unsigned | 1     |                                            |
| I3    | PI   | Signed   | 10    |                                            |
| T160  | IFO  | Signed   | 7     | O2[6:0]                                    |
| O1    | PO   | Unsigned | 10    | I1 + I2 (fpnew_fma_R8B_MBE.sv:285)         |
| O2    | PO   | Signed   | 10    | O1 - I3 (fpnew_fma_R8B_MBE.sv:293)         |
| O3    | PO   | Signed   | 7     | $unsigned(5'b11011) - T160 (fpnew_fma_R8B_MBE.sv:306) |
================================================================================
```

Datapath **Report for** DP_OP_314J1_124_1851

Cell	Contained Operations
DP_OP_314J1_124_1851	gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_369 (fpnew_fma_R8B_MBE.sv:369)
	gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_369_2 (fpnew_fma_R8B_MBE.sv:369)
	gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_373 (fpnew_fma_R8B_MBE.sv:373)

Var	**Type**	Data Class	Width	Expression
I1	PI	Unsigned	50	
I2	PI	Unsigned	76	
I3	PI	Unsigned	1	
T166	IFO	Signed	76	O1[75:0]
O1	PO	Unsigned	77	I1 + I2 + I3 (fpnew_fma_R8B_MBE.sv:369)
O2	PO	Signed	76	$unsigned(1'b0) - T166 (fpnew_fma_R8B_MBE.sv:373)

Datapath **Report for** DP_OP_315J1_125_1241

Cell	Contained Operations
DP_OP_315J1_125_1241	gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_513 (fpnew_fma_R8B_MBE.sv:513)
	gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_513 (fpnew_fma_R8B_MBE.sv:513)
	gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_516 (fpnew_fma_R8B_MBE.sv:516)
	gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_516 (fpnew_fma_R8B_MBE.sv:516)
	gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/gte_513 (fpnew_fma_R8B_MBE.sv:513)

Var	**Type**	Data Class	Width	Expression
I1	PI	Unsigned	6	
I2	PI	Signed	10	
T305	IFO	Signed	7	-I1 + $unsigned(1'b1) (fpnew_fma_R8B_MBE.sv:513 fpnew_fma_R8B_MBE.sv:516)
T301	IFO	Signed	12	I2 + T305 (fpnew_fma_R8B_MBE.sv:513)
O1	PO	Signed	1	T301 >= $signed(1'b0) (fpnew_fma_R8B_MBE.sv:513)
O2	PO	Signed	10	I2 + T305 (fpnew_fma_R8B_MBE.sv:516)

Datapath **Report for** DP_OP_51_134_568

Cell	Contained Operations
DP_OP_51_134_568	gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_515 (

```
    fpnew_fma_R8B_MBE.sv:515) |
================================================================================

================================================================================
|      |      | Data    |       |                                              |
| Var  | Type | Class   | Width | Expression                                   |
================================================================================
| I1   | PI   | Unsigned | 6    |                                              |
| O1   | PO   | Unsigned | 7    | $unsigned(5'b11010) + I1 (fpnew_fma_R8B_MBE.sv:515) |
================================================================================

Datapath Report for DP_OP_52_135_9767
================================================================================
| Cell                | Contained Operations                                   |
================================================================================
| DP_OP_52_135_9767   | gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_520 (
    fpnew_fma_R8B_MBE.sv:520) |
================================================================================

================================================================================
|      |      | Data    |       |                                              |
| Var  | Type | Class   | Width | Expression                                   |
================================================================================
| I1   | PI   | Signed   | 7    |                                              |
| O1   | PO   | Unsigned | 7    | $unsigned(5'b11010) + I1 (fpnew_fma_R8B_MBE.sv:520) |
================================================================================

Datapath Report for DP_OP_308_136_3574
================================================================================
| Cell                | Contained Operations                                   |
================================================================================
| DP_OP_308_136_3574  | gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_543 (
    fpnew_fma_R8B_MBE.sv:543) |
================================================================================

================================================================================
|      |      | Data    |       |                                              |
| Var  | Type | Class   | Width | Expression                                   |
================================================================================
| I1   | PI   | Signed   | 10   |                                              |
| O1   | PO   | Unsigned | 10   | I1 + $unsigned(1'b1) (fpnew_fma_R8B_MBE.sv:543) |
================================================================================

Datapath Report for DP_OP_309_137_3574
================================================================================
| Cell                | Contained Operations                                   |
================================================================================
| DP_OP_309_137_3574  | gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].
    active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_550 (
    fpnew_fma_R8B_MBE.sv:550) |
================================================================================

================================================================================
|      |      | Data    |       |                                              |
| Var  | Type | Class   | Width | Expression                                   |
================================================================================
| I1   | PI   | Signed   | 10   |                                              |
| O1   | PO   | Signed   | 10   | I1 - $unsigned(1'b1) (fpnew_fma_R8B_MBE.sv:550) |
================================================================================
```

Datapath Extraction **Report**

Information: Operator associated **with** resources 'gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/gt_295 (fpnew_fma_R8B_MBE.sv:295)' **in** design 'fpnew_top' breaks the datapath extraction because there **is** leakage due **to** truncation **on** the fanout **of** its driver 'gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_293 (fpnew_fma_R8B_MBE.sv:293)'. (HDL-120)

Information: Operator associated **with** resources 'gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_369 (fpnew_fma_R8B_MBE.sv:369) gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_369_2 (fpnew_fma_R8B_MBE.sv:369)' **in** design 'fpnew_top' breaks the datapath extraction because there **is** leakage due **to** truncation **on** the fanout **of** its driver 'gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/MUL/au/add_199 (au.sv:199)'. (HDL-120)

Information: Operator associated **with** resources 'gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/sub_516 (fpnew_fma_R8B_MBE.sv:516) gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/add_516 (fpnew_fma_R8B_MBE.sv:516)' **in** design 'fpnew_top' breaks the datapath extraction because there **is** leakage due **to** truncation **on** its fanout **to** operator **of** resources 'gen_operation_groups[0].i_opgroup_block/gen_parallel_slices[0].active_format.i_fmt_slice/gen_num_lanes[0].active_lane.lane_instance.i_fma/C3223 (fpnew_fma_R8B_MBE.sv:513)'. (HDL-120)

Implementation **Report**

Cell	Module	Current Implementation	Set Implementation
gt_x_43	DW_cmp	apparch (area)	
lte_x_47	DW_cmp	apparch (area)	
lte_x_48	DW_cmp	apparch (area)	
ashr_51	DW_rightsh	astr (area)	
lte_x_58	DW_cmp	apparch (area)	
lte_x_59	DW_cmp	apparch (area)	
ash_64	DW_leftsh	astr (area)	
gt_x_65	DW_cmp	apparch (area)	
gte_x_69	DW_cmp	apparch (area)	
add_x_80	DW01_add	pparch (area,speed)	
add_x_105	DW01_add	pparch (area,speed)	
add_x_137	DW01_add	pparch (area,speed)	
lte_x_155	DW_cmp	apparch (area)	
DP_OP_312J1_122_9228	DP_OP_312J1_122_9228	str (area,speed)	
DP_OP_313J1_123_2996	DP_OP_313J1_123_2996	str (area,speed)	
DP_OP_314J1_124_1851	DP_OP_314J1_124_1851	str (area,speed)	
DP_OP_315J1_125_1241	DP_OP_315J1_125_1241	str (area,speed)	
DP_OP_51_134_568	DP_OP_51_134_568	str (area,speed)	
DP_OP_52_135_9767	DP_OP_52_135_9767	str (area)	
DP_OP_308_136_3574	DP_OP_308_136_3574	str (area,speed)	
DP_OP_309_137_3574	DP_OP_309_137_3574	str (area,speed)	

1