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# Quadcopter Electronic Speed Controller PCB Design

# Contents

# Chapter 1

# HW Design

In this chapter, the hardware design will be presented, starting with a general overview of the main conceptual blocks of the PCB. This will be followed by a more detailed explanation of the decisions made during the design process, particularly regarding the selection of components as well as the overall structure of the PCB itself. Key challenges associated with implementing an ESC on a printed circuit board will be highlighted, along with the countermeasures taken during the design phase to address these issues.

## 1.1 Main Block Description and Component Selection

A drone ESC has the following primary task: regulating the speed of the connected brushless motor based on signals received from the flight controller. In order to achieve this, both a logic circuit and a power circuit are required. Respectively, they manage the motor phase switching and then perform the actual switching. Additionally, a power supply block is necessary to serve both the logic and power circuits. Down below there is a general scheme of the HW blocks.

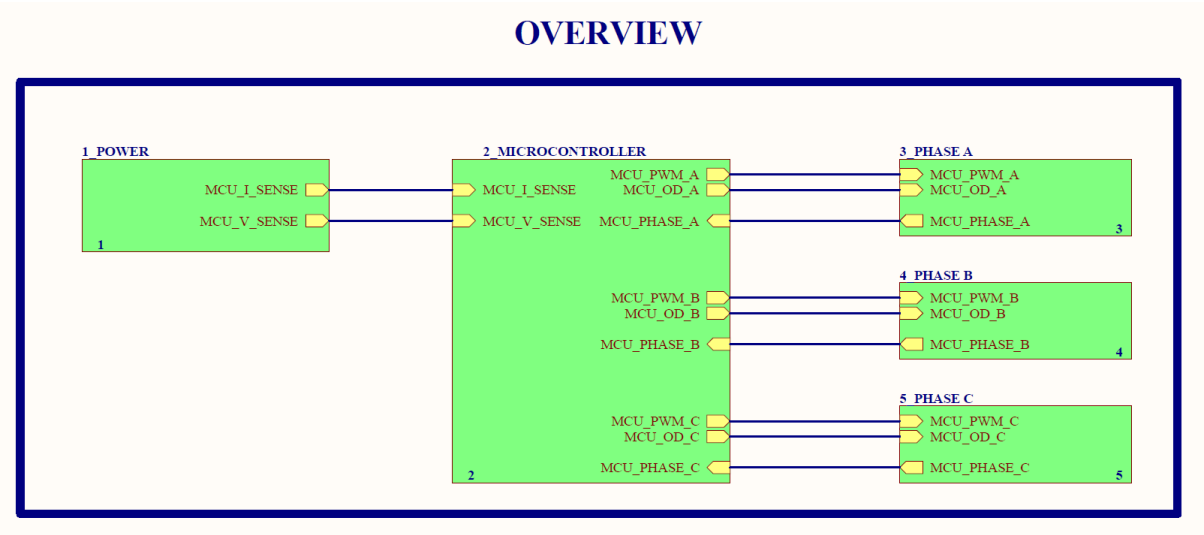


Figure 1.1: Schematic overview

The following is a detailed description of each block and the main components selected for its

implementation. For the sake of completeness, the full schematics will also be provided.

### 1.1.1 Power Supply and Battery Status Monitoring

Typically, in a drone, power is supplied by a LiPo battery. This type of battery is capable of delivering a significant amount of current, but also needs to be managed carefully. An excessive current absorption could lead to dangerous consequences. The ESC is designed to accept an input voltage range between 10 and 12.6 V, compatible with a battery. Both the battery's current output and its voltage are monitored to ensure there is no excessive current absorption or significant drops in the input voltage to the board, which could lead to malfunctions in some circuit components.

The Figure 1.2 shows the schematic for the Battery Status Monitoring circuit that allows the MCU to monitor both the current and voltage of the battery system.

To measure the current, a 2 m$\Omega$ shunt resistor was chosen to minimize the voltage drop across it under high current conditions. A maximum current of 15 A is expected to be absorbed by the motor at maximum speed, which would lead to a 30 mV voltage drop across the shunt resistor. In this scenario, the maximum dissipated power would be 450 mW. The chosen resistor is capable of dissipating 1 W of maximum power, which is well above the previous estimate. Since the voltage drop is quite small, a differential amplifier is used to amplify it in order to fully exploit the input range of the internal ADC of the MCU. To this purpose, we used the INA180A2IDBVT amplifier, which has a gain of 100. The amplifier is powered by a 3.3 V supply (as we will see next, the same one that powers on the MCU) and has a capacitor ($C_3$) of 100 nF for decoupling. The low pass filter, constituted by the resistor $R_8$ and the capacitor $C_4$, is used to filter the signal at the output of the differential amplifier and send the MCU_I_SENSE signal to the MCU. The filters have a cutoff frequency of about 100 Hz, since the ADC sampling frequency that is used to monitor the battery status is between 200 and 500 Hz. A voltage divider circuit is formed by resistors $R_12$ (33 k$\Omega$) and $R_{15}$ (10 k$\Omega$) to scale down the battery voltage VBAT to a safe level for the MCU's ADC input. The divided voltage is filtered by a capacitor ($C_{11}$, 1 nF) and is available as MCU_V_SENSE.

Instead of a simple linear voltage regulator, a buck converter was chosen to step down the battery voltage to 3.3 V, a voltage required for powering both the microcontroller and the differential amplifier used in the battery monitoring circuit. A buck converter offers a significant advantage over a linear regulator: it is more efficient, which is crucial in battery-powered applications, especially when there is a large difference between the input and output voltages, as in this case. In linear regulators, excess energy is dissipated as heat, effectively wasting battery power. However, there are some drawbacks to consider. A buck converter requires an external inductor, which occupies additional PCB space, and it generates more noise due to the internal switching transistors. Moreover, its placement in the circuit, along with the positioning of the associated components, demands greater attention during the design process. Since these drawbacks are not negligible, the use of a linear regulator in place of the buck converter is a good design alternative, mainly to reduce the required space on the PCB for the voltage conversion and reduce noise.

The image shows the buck converter circuit that steps down the input voltage VCC to +3.3 V. The main component is the AP64060QWU-7 buck converter IC ($U_2$). This buck IC has been chosen especially for its several protection features: Undervoltage Lockout Protection, Output Overvoltage Protection, Peak Current Limit, and Thermal Shutdown. The presence of this protection circuitry is very useful to increase the safety and reliability of the ESC, and justifies the choice of the buck converter in place of a simple linear regulator.

$L_1$ (47 $\mu$H) is the main inductor for the buck converter, creating the output ripple necessary for

step-down regulation. The inductor value has been chosen based on the following formula (which can be found in the datasheet of the AP64060QWU-7).

$$\begin{aligned} L &= \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{sw}} \\ &= \frac{3.3 \cdot (12.6 - 3.3)}{12.6 \cdot 30 \cdot 10^{-3} \cdot 2.2 \cdot 10^{6}} \\ &= 37\mu H \end{aligned} \tag{1.1}$$

We assume that the load draws from the buck converter a current of about 150 mA, which is a conservative choice since the buck converter supplies only the MCU and the amplifier; we estimate the ripple to be around 30 mA (20% of the load current), as the datasheet recommends. The value that we picked is quite close to the estimated one. The inductor we chose is the NRS3015T470MNGH. The other important considerations about the choice of the inductor regard the saturation current, the size and the DC resistance. The saturation current is 325 mA, which is well above the 150 mA of load current, ensuring that the inductance value doesn't change too much with respect to the nominal value. The size and the DC resistance present a trade-off. We chose to prioritize the small size of the inductor, since one of our main constraints is about the board size. Unfortunately, this means that the DC resistance is not low, decreasing the overall efficiency of the buck converter. Capacitors $C_5$ (100 nF) and $C_6$ (100 pF), $C_7$ and $C_8$ are placed in order to filter the switching noise and stabilize the output (the values are the ones recommended by the datasheet of the buck IC). A voltage divider with resistors $R_9$ (22 k$\Omega$) and $R_{11}$ (69.8 k$\Omega$) is used to set the output voltage. The divided voltage is fed back to the FB pin to maintain a stable 3.3 V output.

The UnderVoltage Lockout Protection (UVLP) feauture is implemented to prevent the IC from insufficient input voltage. The threshold of the UVLP can be programmed by connecting the $V_{IN}$ to the EN pin of $U_2$ via an appropriately sized resistor, $R_{10}$ in the schematic. The value of this resistor must be designed with the following formula (provided by the datasheet):

$$R = 480k\Omega \frac{(V_{th} - 1.21V)}{1.21V} \tag{1.2}$$

For example, to set the turn on threshold to 8V, a resistor of 2.7 M$\Omega$ must be used.

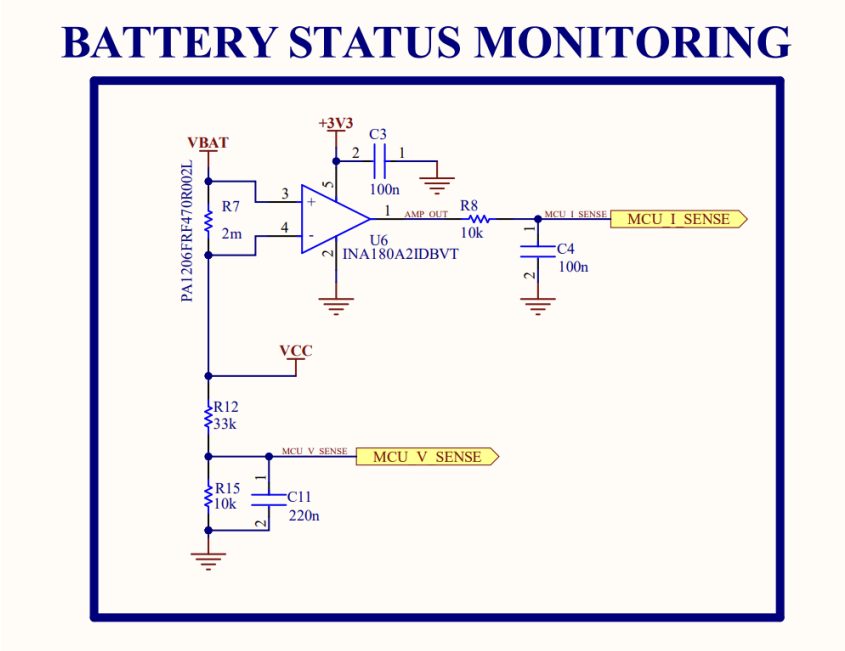


Figure 1.2: Battery status monitoring

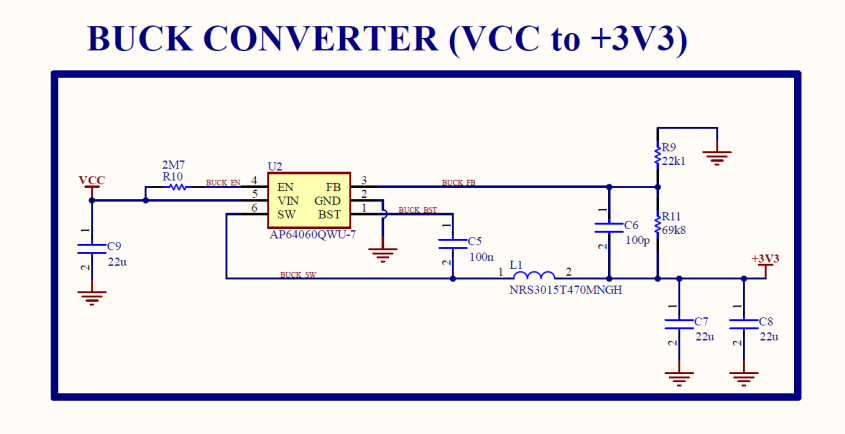


Figure 1.3: Buck converter schematic

### 1.1.2 Microcontroller

We now describe the low-power logic circuit, beginning with the rationale behind the selection of the microcontroller on the board. To do so, we analyze the essential requirements for the proper functioning of the implemented ESC.

First, the system clock speed must be sufficient to perform real-time calculations. For trapezoidal control, a frequency of at least 16 ÷ 32 MHz is generally adequate. A too high frequency would be a waste of power. High-resolution timers are required to generate PWM signals with sufficient precision to control motor speed. Specifically, at least three independent channels are necessary (and sufficient, as will become clear from the choice of drivers) to drive the three phases of the BLDC motor. An ADC, with at least two channels is required to measure the supply voltage and the current drawn. A GPIO in input capture mode is needed to read the input speed target signal from the flight controller. Since a sensorless control strategy is employed, relying on monitoring the back EMF generated

by the motor, and no external comparators were used, the microcontroller must include internal comparators. This choice of using internal comparators has the big advance of reducing the cost and size of the board. Lastly, but no less importantly, the microcontroller must meet the requirements for reliability, robustness, energy efficiency (essential for battery-powered applications) and cost. For these reasons, the STM32 M0+ family was chosen, as it is known to offer a good balance between functionality, simplicity, and affordability. Specifically, the STM32G071K8T3 microcontroller was selected, as it fulfills all the mentioned requirements and represents a solid compromise between reliability, performance, cost, and availability. The package only has 32 pins, which is more than enough for our needs. Below, a diagram outlines the main features of this microcontroller.

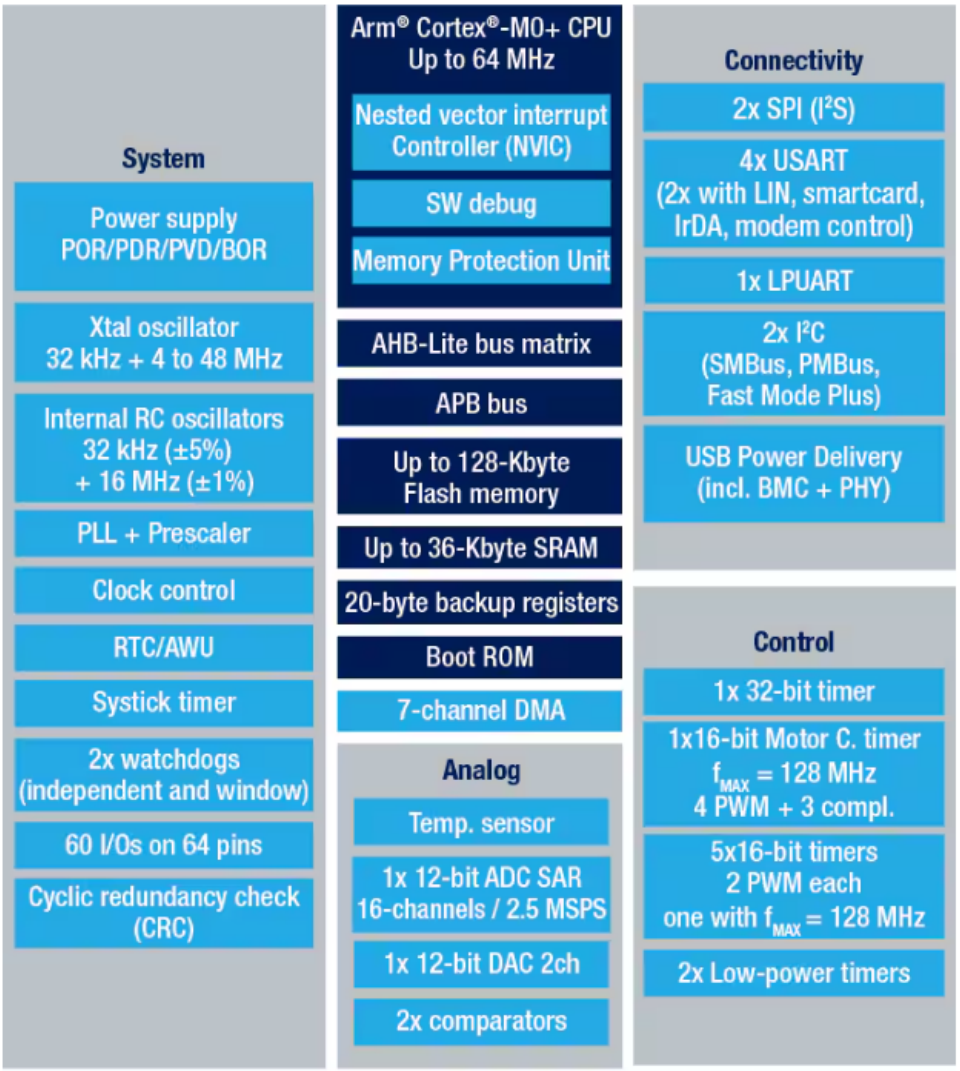


Figure 1.4: MCU features

We now analyze the schematic related to the microcontroller, briefly outlining the signals entering and exiting the chip.

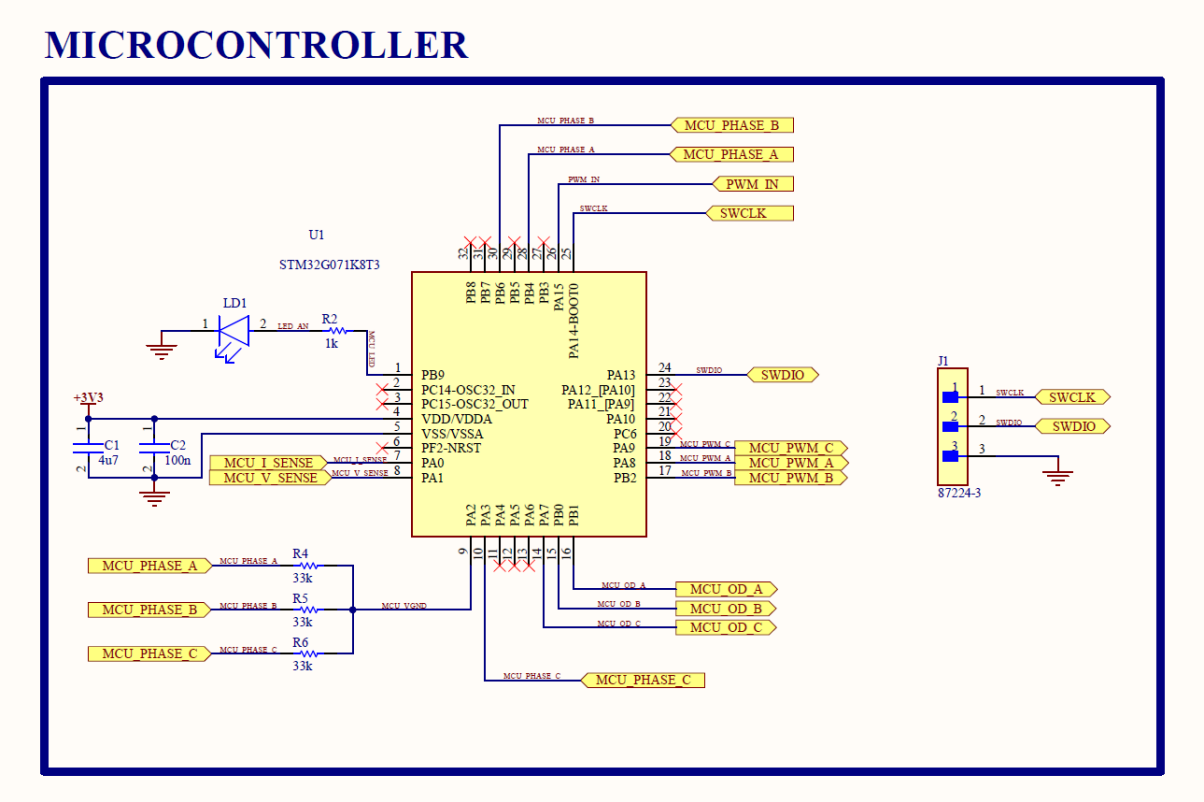


Figure 1.5: MCU schematic

The schematic shows the microcontroller interface circuit for controlling the three motor phases (A, B, and C) and monitoring both voltage and current. The main component is the STM32G071K8T3 microcontroller (U1) powered by the +3.3 V supply (coming from the buck converter output), which is decoupled by capacitors $C_1$ and $C_2$ (values recommended by the datasheet). A $PWM_{IN}$ input pin allows an external PWM signal to control the motor speed. The labels MCU_PWM_A, MCU_PWM_B, and MCU_PWM_C represent the PWM signals from which the drivers generate two complementary PWM signals that drive the half-bridges. MCU_OD_A, MCU_OD_B, and MCU_OD_C represent the gate driver output enable signals. At the pins PB4, PB6, PA3 are connected the scaled down phase voltage signals labeled MCU_PHASE_A, MCU_PHASE_B, and MCU_PHASE_C, whereas the pin PA2 is connected to the virtual neutral. These pins are the inputs of an internal comparator, thus they are used to implement the zero crossing detection. The SWD protocol is used to flash the firmware, needing a dedicated connector. No actions are needed for the BOOT0 and NRST pins, since the former is configured by default to boot from the flash at startup and the latter is internally pulled up.

In Figure 1.6, we show the pinout of the microcontroller as configured in the .ioc file using CubeMX.

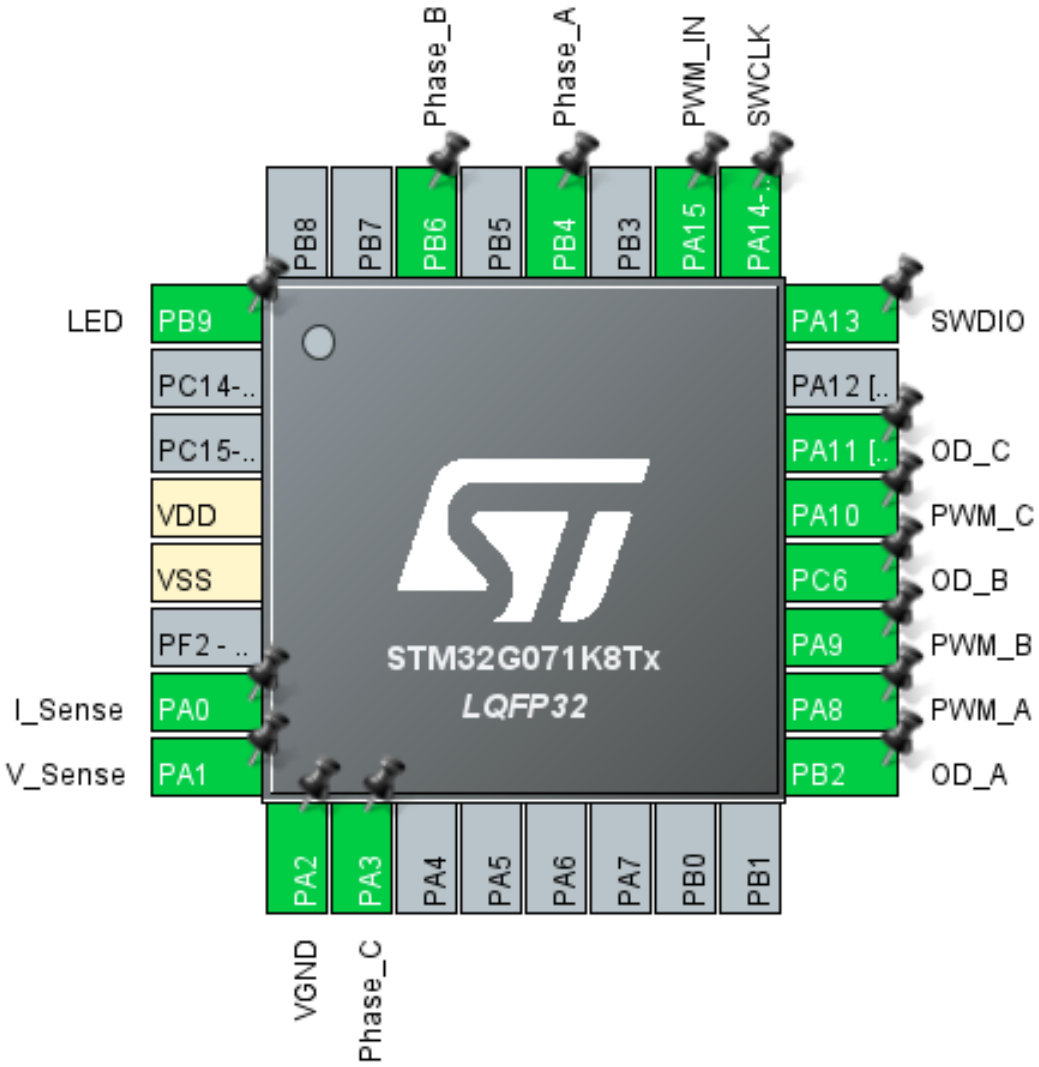


Figure 1.6: Pinout MCU PCB

### 1.1.3 Power Circuit

Before diving into the details of the components selected for the circuit, let's first take a brief look at its main building blocks and how it fundamentally operates. The power circuit includes the components required to implement the so-called three-phase full-bridge inverter, responsible for managing power delivery to the motor. The main components of this circuit are 6 power MOSFETs, arranged in three complementary pairs (high-side and low-side), with each pair controlling one of the motor's three phases. Additionally, driver circuits independently control the high-side and low-side MOSFETs, provide the necessary gate drive voltage to switch the transistors on, and ensure proper timing to prevent shoot-through (a condition where both high-side and low-side MOSFETs in the same phase conduct simultaneously, which can be fatal for the FETs).

This configuration is highly efficient and is the standard for driving three-phase brushless DC motors. By alternating the switching of the MOSFETs in each phase, the circuit generates a sinusoidal or trapezoidal waveform, depending on the control strategy (trapezoidal in this ESC implementation). This process ensures proper sequencing of current flow in the motor windings, creating a rotating

magnetic field that drives the motor.

The basic functional workflow is as follows:

1. The microcontroller generates PWM signals for control (one for each phase).
2. MOSFET drivers amplify these signals and pass them to the power MOSFETs.
3. Power MOSFETs modulate the voltage delivered to the brushless motor windings according to the microcontroller's commands.
4. Feedback (back-EMF in sensorless trapezoidal control) ensures accurate speed and position regulation.

Let's consider the full-bridge schematic and discuss the component selection:

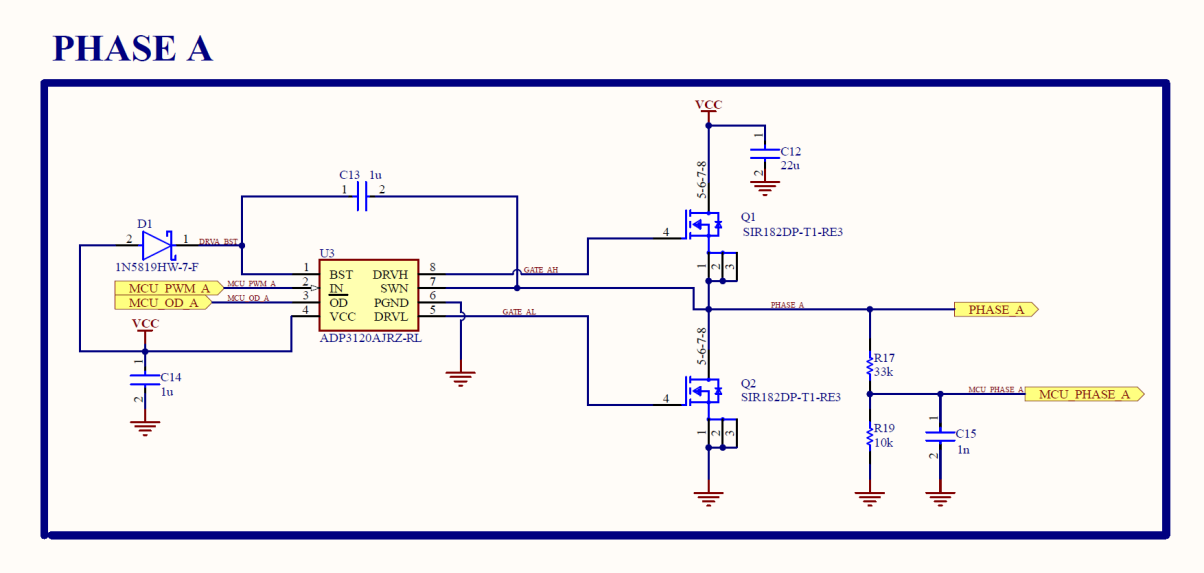


Figure 1.7: Full-bridge schematic: Phase A

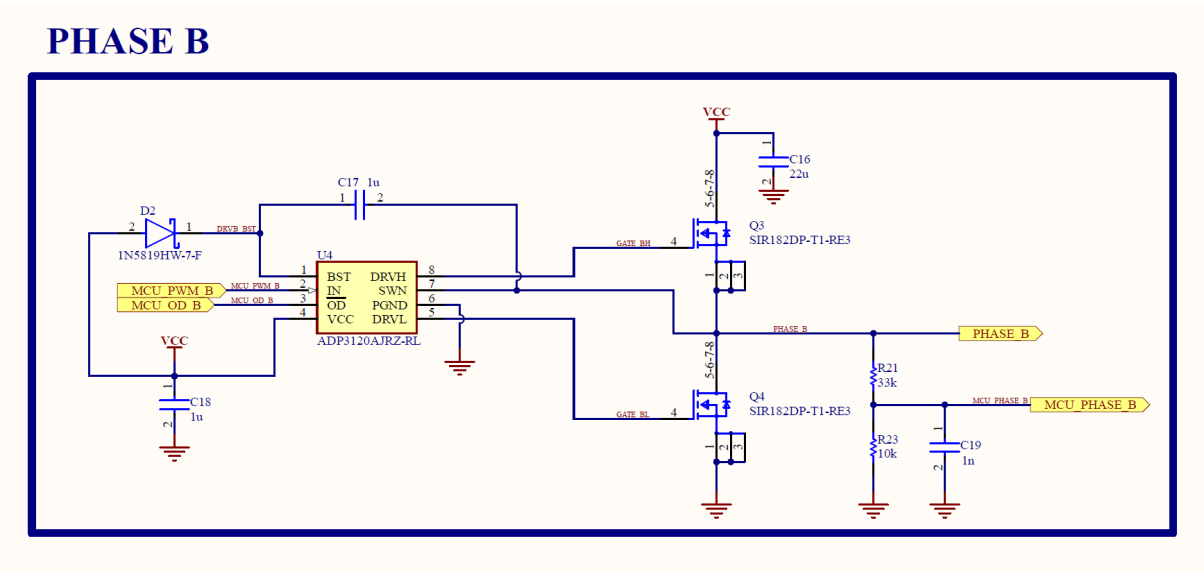


Figure 1.8: Full-bridge schematic: Phase B

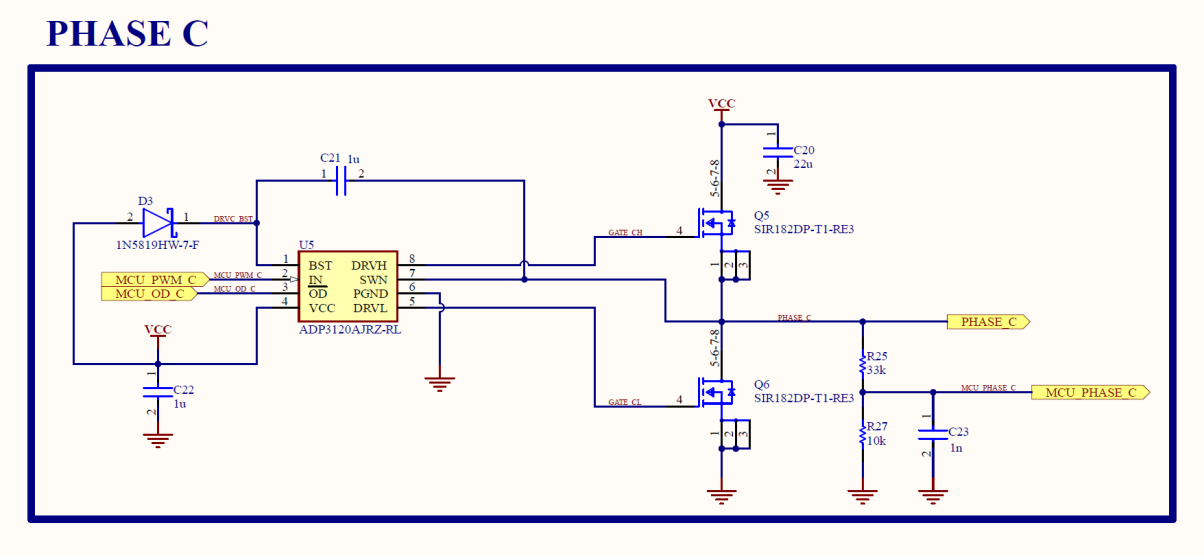


Figure 1.9: Full-bridge schematic: Phase C

The schematics show the phase A, B and C driver circuits of the three-phase motor control system. The three schematics are equivalent, so we will analyze only one of them (i.e. phase A driver circuit). This phase driver circuit controls one of the motor phases (phase A). MCU_PWM_A and MCU_OD_A are control signals from the microcontroller connected to the ADP3120A chip, which is a high-speed gate driver IC ($U_3$) responsible for driving the high-side (DRVH) and low-side (DRVL) MOSFETs, that control the motor phase. The first signal is the one that actually is amplified in order to drive the high-side MOSFET and thus controls the voltage that is applied to the phase. From this PWM signal of the MCU, the driver automatically generates the complementary PWM signal to efficiently drive the low-side MOSFET. The second signal generated by the MCU is a digital GPIO output that allows to enable or disable the output of the driver. The bootstrap diode ($D_1$) (1N5819HW) and capacitor $C_{13}$ (1 $\mu$F) create a floating voltage supply for the high-side MOSFET driver. This allows the high-side MOSFET ($Q_1$) to be properly turned on and off by the gate driver. The gate signals control the N-channel MOSFETs $Q_1$ and $Q_2$, serving as the high-side and low-side switches for Phase A. $C_{14}$ (1 $\mu$F) is a decoupling capacitor for the driver chip as well as $C_{12}$ (22 $\mu$F) is a decoupling capacitor connected to the VCC line to stabilize the supply voltage and filter any noise that could affect the MOSFETs' performance. $R_{17}$ (33 k$\Omega$) and $R_{19}$ (10 k$\Omega$) create a voltage divider to scale down the phase A voltage in order readable by the MCU. The capacitor $C_{15}$ (1 nF) is added with the purpose of reducing the noise before feeding the signal into the MCU for the ZC detection.

### Mosfet choice

Let's take a moment to delve into the key considerations behind the selection of the MOSFETs used in the three-phase half-bridge inverter. In the next subsection, we will also explore how these considerations influenced the selection of the gate drivers, as well as the supporting components needed to ensure their proper operation. Below, we outline the key factors to consider when selecting MOSFETs for these kind of applications:

1. Drain-Source Voltage $V_{DS}$: the MOSFET must withstand voltages higher than the nominal supply voltage of the system. The MOSFET's nominal voltage should be at least 1.5 to 2 times the battery voltage. For example: MOSFET with $V_{DS} \geq 30\,\mathrm{V}$ is required when using a

3S LiPo battery.

2. Drain Current $I_D$: the MOSFET must handle peak currents required by the motor under maximum load conditions. $I_D$ must be at least 150% ÷ 200% of the expected motor's maximum current. Cause we expect a maximum value of 15 A, $I_D \geq 30\,\mathrm{A}$ is more than enough.

3. On-State Resistance $R_{DS}$ : the channel resistance during conduction should be as low as possible to reduce power losses and heating. In fact, the power dissipated during conduction (conduction losses):

$$P_{DISS} = R_{DS} \cdot I_D^2 \tag{1.3}$$

   $R_{DS}$ in the milliohm range (e.g., 1-10 mΩ) is optimal.

4. MOSFETs in an inverter for ESC must switch quickly to minimize switching losses. At steady state, in this application, the FETs are either in triode or cut-off region. In the former case the power consumption is minimal due to the small channel resistance, in the latter is only related to leakage currents. Instead, during transients between the on and off state, the MOSFETs operate in saturation region, where the voltage drop across the channel is higher causing a larger power disspitation. Therefore, to minimize switching losses, switching times are then crucial. Specifically, the turn-on and turn-off times, as well as the rise and fall times, directly impact these losses. The shorter they are, the better the overall efficiency of the inverter. These time parameters are strictly connected to the total gate charge $Q_G$: the larger $Q_G$ the higher the switching times and viceversa. A low value of $Q_G$ is then also essential for achieving high switching frequencies (typically 20-50 kHz is required for ESCs, 42 kHz in our case ). Ideally, should be $Q_G \leq 50\,\mathrm{nC}$ to facilitate driving with standard gate drivers. Unavoidably, higher switching frequencies cause larger switching losses.

5. Gate Threshold Voltage $V_{GSth}$: the MOSFET must be fully conductive at the driver's gate voltage levels.

6. MOSFETs must effectively manage heat dissipation to avoid overheating during intensive use. The addition of heat sinks can greatly improve the heat dissipation, keeping the MOSFET at a low temperature.

The SIR182DP-T1-RE3 model was selected. Table 1.1 outlines the key MOSFET characteristics relevant for choosing components for an ESC. As shown, all parameters fall within the previously specified limits.

| SIR182DP-T1-RE3 Relevant Characteristics | |
|---|---|
| $V_{DS}$ | 60 V |
| $I_D$ | 31.4 A @ $T_A = 25$ °C (Strongly depends on $T_A$ and $T_C$) |
| $R_{DS}$ | 2.8 mΩ @ $V_{GS} = 10$V |
| $Q_G$ | 42.2 nC |
| $V_{GS(th)}$ | 2 ÷ 3.6 V |
| $t_{d(on)}$ | 15 ns (typ.) |
| $t_r$ | 23 ns (typ.) |
| $t_{d(off)}$ | 21 ns (typ.) |
| $t_f$ | 10 ns (typ.) |
| $P_D$ | 5 W @ $T_A = 25$ °C (Strongly depends on $T_A$ and $T_C$) |
| $R_{thJA}$ | 25 °C/W ( $t \leq 10$ s) (Maximum under steady state conditions is 65 °C/W) |

Table 1.1: SIR182DP-T1-RE3 Relevant Characteristics

### Switching frequency selection

Even though it's not strictly speaking a component choice, let's address now the MOSFET's switching frequency selection, which is strongly connected, as we will see, to the component choice. The PWM switching frequency is a design choice that should be carefully carried out. In fact, the optimal PWM frequency is a trade-off between several aspects. A low switching frequency causes several issues, the main ones being current ripples and annoying acoustic noise. Current ripples are related to the inductance of the motor's windings. Let's see why in greater detail. We need to control the speed of a BLDC motor that is equivalent to a resistance, an inductor, and a voltage source (representing the BEMF) connected in series as shown in Figure 1.10.

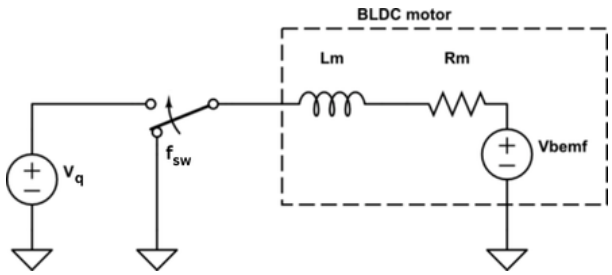


Figure 1.10: Equivalent Motor Circuit

The differential equation that describes this model is:

$$V_q = R_m \cdot i + L_m \cdot \frac{di}{dt} + V_{bemf} \tag{1.4}$$

and can be rewritten, in the Laplace domain, as:

$$V_q(s) = R_m \cdot i(s) + L_m \cdot i(s) \cdot s + V_{bemf}(s) \tag{1.5}$$

$$\Rightarrow \quad \frac{i(s)}{V_q(s) - V_{bemf}(s)} = \frac{1}{R_m + L_m \cdot s} \tag{1.6}$$

So, we will have that the ratio between the equivalent inductance and the equivalent resistance of the BLDC motor (i.e. $\tau = \frac{L_m}{R_m}$) constitutes a time constant. The time constant must be much longer than the PWM period, it means that ($\frac{L_m}{R_m}$) defines a constraint on the minimum switching frequency. When the switching frequency is not sufficiently high, the switching period increases. This increases the time during which the voltage V acts on the inductor, causing a large current variation in each cycle. This results in a large torque ripple that causes the motor to not run smoothly. At some point, an increasing of the frequency doesn't provide a considerable improvement of the ripple.

As for the audible noises, they are caused when the mechanical vibrations generated by the switching process emit frequencies in the human audible range. To overcome this issue, we need to use a switching frequency at least of 20 kHz.

The maximum PWM frequency, instead, is mainly limited by MOSFET switching losses, as explained in the previous subsection on MOSFET choice. There are also other drawbacks in using a too high switching frequency, for instance: increased thermal stress (related to the higher losses), increased stress on motor windings due to high voltage and current rates, etc...

For these reasons, we have chosen a switching frequency of approximately 40 kHz, which represents a good compromise for these trade-offs.

### Gate driver choice

Once we have selected the MOSFETs, here are the key factors to consider when choosing gate drivers:

- Supply Voltage Range $V_{CC}$: ensure the gate driver can provide a voltage sufficient to fully turn on the MOSFETs (10-12V is enough for the selected MOSFETs because $V_{GS(th)}$ 2 ÷ 3.6 V).
- Input voltage $V_{HI}$: ensure the minimum input voltage high must be lower than the high state voltage level of the MCU.
- Peak Output Current $I_P$: The gate driver must supply enough current to charge and discharge the MOSFET gate quickly. The average current that the driver must provide during switching depends on the gate charge and the rise (fall) and turn-on (turn-off) times of the employed FETs, and it is given by the following formula:

$$I_{g,avg} = \frac{Q_g}{t_r + t_{on}} = \frac{42.2nC}{(15+23)ns} = 1.11A \tag{1.7}$$

  The peak output current of the driver must be well above this estimate, ensuring rapid charging and discharging of the gate capacitances. Sometimes this specification is directly provided in the datasheet, other times it must instead be derived from the output resistance $R_{OH/OL}$, which is a common driver specification. To estimate the theoretical peak current we can rely on the following formula:

$$I_p = \frac{V_{cc}}{R_{OH/OL}} \tag{1.8}$$

  Choose a driver that can provide peak currents at least 2-3 times higher than the calculated value for fast switching.

- The gate driver should have low propagation delays and high slew rates to support fast switching, which reduces switching losses.
- Driving Configuration: choose a driver that matches the topology of your circuit. In the case of a half-bridge inverter, we need a high and low side gate driver. The driver must support bootstrap operation, needed to drive the upper MOSFETs of the half bridges.
- Verify that the driver's power supply matches the available voltage in your system (12.6V in our case).
- If the application requires dead time to prevent shoot-through, look for gate drivers with built-in dead time control or ensure your controller can manage this.
- For added reliability, consider gate drivers with built-in protections, such as: overcurrent protection, thermal shutdown or undervoltage lockout (UVLO).

Considering all the requirements listed above, the ADP3120AJRZ-RL gate driver was selected. In Table 1.2, we outline the key features of the chosen driver. As shown, the requirements are fully met. In particular:

| **ADP3120AJRZ-RL Relevant Characteristics** | |
|---|---|
| $V_{CC}$ | Min: 4.6V, Max: 13.2V |
| $V_{HI}$ | Min: 2.0V |
| $R_{OH}$ | Max: 3.9 Ω (Sourcing), 2.6 Ω (Sinking) |
| $R_{OL}$ | Max: 3.9 Ω (Sourcing), 2.6 Ω (Sinking) |
| $t_{r,DRVH}$ | 40 ns (max) |
| $t_{f,DRVH}$ | 30 ns (max) |
| $t_{pdh,DRVH}$ | 70 ns (max) |
| $t_{pdl,DRVH}$ | 35 ns (max) |
| $t_{r,DRVL}$ | 35 ns (max) |
| $t_{f,DRVL}$ | 30 ns (max) |
| $t_{pdh,DRVL}$ | 35 ns (max) |
| $t_{pdl,DRVL}$ | 45 ns (max) |

Table 1.2: ADP3120AJRZ-RL Relevant Characteristics

The features of the selected driver are summarized in the following:

*"The ADP3120A is a single Phase 12 V MOSFET gate driver optimized to drive the gates of both high-side and low-side power MOSFETs in a synchronous buck converter. The high-side and low-side driver is capable of driving a 3000 pF load with a 45 ns propagation delay and a 25 ns transition time. With a wide operating voltage range, high or low side MOSFET gate drive voltage can be optimized for the best efficiency. Internal adaptive nonoverlap circuitry further reduces switching losses by preventing simultaneous conduction of both MOSFETs. The floating top driver design can accommodate VBST voltages as high as 35 V, with transient voltages as high as 40 V. Both gate outputs can be driven low by applying a low logic level to the Output Disable (OD) pin. An Undervoltage Lockout function ensures that both driver outputs are low when the supply voltage is low, and a Thermal Shutdown function provides the IC with overtemperature protection."* - source, datasheet

A few words now about the safety timer and overlap protection circuit. It's crucial that the low and high side MOSFETs do not conduct simultaneously. Excessive shoot-through or cross conduction

can damage the MOSFETs and reduce the overall efficiency of the ESC. The ADP3120A prevents cross conduction by monitoring the MOSFETs' status and applying appropriate "dead-time" between the turn-off of one MOSFET and the turn-on of the other. When the PWM input pin goes high, the DRVL pin will go low after a propagation delay ($t_{pdlDRVL}$), and the low-side MOSFET's turn-off time ($t_{fDRVL}$) depends on its gate charge. The ADP3120A monitors the gate voltages of both MOSFETs and the switch node voltage to determine their conduction status. Once the low-side MOSFET turns off, an internal timer delays the high-side MOSFET's turn-on ($t_{pdhDRVH}$). Similarly, when the PWM input pin goes low, the DRVH pin goes low after a propagation delay ($t_{pdDRVH}$). The high-side MOSFET turn-off time ($t_{fDRVH}$) depends on its gate charge. A timer then delays the low-side MOSFET's turn-on ($t_{pdhDRVL}$) after the high-side MOSFET stops conducting.

To conclude this section, we present the calculations performed for sizing the bootstrap capacitor, which were done following the guidelines in the datasheet.

The bootstrap circuit uses a charge storage capacitor ($C_{BST}$) and the internal (or an external) diode. Selection of these components can be done after the high-side MOSFET has been chosen. The bootstrap capacitor must have a voltage rating that is able to withstand twice the maximum supply voltage. A minimum 50 V rating is recommended. The capacitance is determined using the following equation:

$$C_{BST} = \frac{Q_G}{\Delta V_{BST}} \tag{1.9}$$

where $Q_G$ is the total gate charge of the high-side MOSFET, and $\Delta V_{BST}$ is the voltage drop allowed on the high-side MOSFET drive. The SIR182DP-T1-RE3 Mosfet has a total gate charge of about 42 nC. For an allowed drop of 30 mV (considering 2.8 m$\Omega$ on-state resistance and 15 A for $I_D$ ), the required bootstrap capacitance is 1 $\mu$F. A good quality ceramic capacitor should be used.

The bootstrap diode must be rated to withstand the maximum supply voltage plus any peak ringing voltages that may be present on SW.

The average forward current can be estimated by:

$$I_{F(AVG)} = Q_G \cdot f_{SW} = 1.8mA \tag{1.10}$$

Where:

- $f_{SW}$ is the switching frequency of the controller

### 1.1.4 Component Packages

Since the ESC is designed for a drone application, size, weight, and performance are critical design considerations, and also apply to the choice of the package of each component. The component packages were selected as the best compromise between compactness, ease of assembly and rework (facilitating repairs of damaged components), and electrical performance.

All the components in this PCB are Surface Mount Devices (SMD). This choice allows to minimize the space occupied by each component, and also has important consequences on the electrical performance of the overall circuit. SMD components inherently have fewer parasitics due to their construction. The absence of metal leads (typical of through-hole components) reduces the parasitic

inductance of the component. Smaller packages further reduce parasitics, because the current loop area inside the component is reduced.

However, the size of the components cannot be too small, since, as already said, it must be possible for the customer to manually repair faulty components. Lower limits on the physical size are also due to the lower power dissipation of smaller components and to the tighter tolerance requirements in PCB design.

## 1.2 PCB design

When designing a PCB for a BLDC motor ESC in a drone, several technical specifications must be considered to ensure proper performance, reliability, and safety. Let's go through the key ones. The PCB must be capable of handling high currents depending on the motor and power requirements of the drone. Adequate trace width and copper thickness are essential to handle these currents without excessive heating. The PCB should be compact and lightweight to minimize the impact on the overall weight of the drone, while still providing sufficient space for all components and heat dissipation. Efficient power distribution and layout are crucial for managing high currents and minimizing power loss. The PCB should feature low-resistance power traces and dedicated ground planes to minimize voltage drops and noise. Low-inductance traces are also a fundamental requirement to be able to supply a large amount of current to the motor in short time intervals, which is essential during drone maneuvers. Proper routing of low-voltage control signals (PWM signals, feedback signals) is critical to prevent signal degradation and noise coupling. The use of ground planes is essential to maintain signal integrity, especially for high-frequency signals. Drones typically operate in environments sensitive to electromagnetic interference. The PCB should be designed to minimize EMI by using techniques such as proper grounding, signal routing and decoupling capacitors. Proper component placement is essential to minimize the loop area for high-current paths, reducing parasitic inductances and improving overall efficiency. Components should be placed to ensure good thermal management and minimize noise interference between high and low voltage sections. Let's now move on to describing the PCB topology and layout, highlighting the design choices made to meet the specifications and requirements outlined above.

### 1.2.1 Topology

To optimize space we decided to go for a 4-layer PCB. Using a 4-layer PCB for an ESC is preferable over a 2-layer design because it allows for better separation of power and ground planes along with signal traces, reducing noise and improving signal integrity. The additional layers enable dedicated ground planes, which enhance thermal management and proper grounding, i.e. lower EMI. This is especially important in high-speed and high-power applications like ESCs for drones. As a drawback, 4-layer boards are significantly more expensive to manufacture compared to 2-layer boards and requires more stringent design rules, such as layer stack-up considerations.

Figure 1.11 shows the layer stackup assigned to the four layers of the PCB.

| # | Name | Material | Type | Weight | Thickness | Dk | Df |
|---|---|---|---|---|---|---|---|
| | Top Overlay | | Overlay | | | | |
| | Top Solder | Solder Resist | Solder Mask | | 0.01016mm | 3.5 | |
| 1 | Top Layer | CF-004 | Signal | 1oz | 0.035mm | | |
| | Dielectric 1 | PP-006 | Prepreg | | 0.2mm | 4.6 | 0.02 |
| 2 | In1 (GND) | CF-003 | Plane | 1/2oz | 0.0175mm | | |
| | Dielectric 2 | Core-025 | Core | | 1.065mm | 4.6 | 0.02 |
| 3 | In2 (GND) | CF-003 | Plane | 1/2oz | 0.0175mm | | |
| | Dielectric 3 | PP-006 | Prepreg | | 0.2mm | 4.6 | 0.02 |
| 4 | Bottom Layer | CF-004 | Signal | 1oz | 0.035mm | | |
| | Bottom Solder | Solder Resist | Solder Mask | | 0.01016mm | 3.5 | |
| | Bottom Overlay | | Overlay | | | | |

Figure 1.11: Altium layers

The top and bottom layers are dedicated to signal and power traces, while the two inner layers serve as ground planes. Having the inner layers fully dedicated to ground offers several advantages. One of the main benefits is that signals traveling directly above or below a ground plane have a low-impedance return path. This reduces crosstalk and electromagnetic interference, ensuring cleaner signals. The reduced parasitic inductance in the current return paths significantly improves high-frequency signal performance and minimizes the risk of overvoltage-related issues. Ultimately, a continuous ground plane helps contain the electromagnetic fields generated by high-speed signals, reducing electromagnetic interference emissions to the outside (EMI improvement). Additionally, having both central layers grounded ensures uniform ground potential distribution, reducing ground loop formation and minimizing ground noise problems. Finally, the ground planes also act, albeit marginally as they are internal layers, as heat sinks, enhancing the thermal management of the board. Standard thicknesses were chosen for the dielectric and copper layers.

### 1.2.2 Layout

Figures 1.12 and 1.13 shows the top view and the bottom view of the PCB.

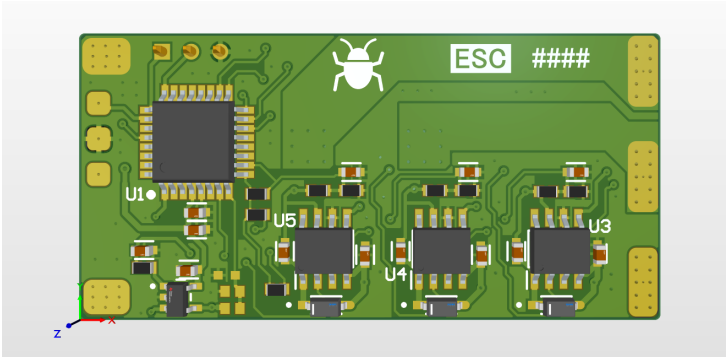


Figure 1.12: PCB top view

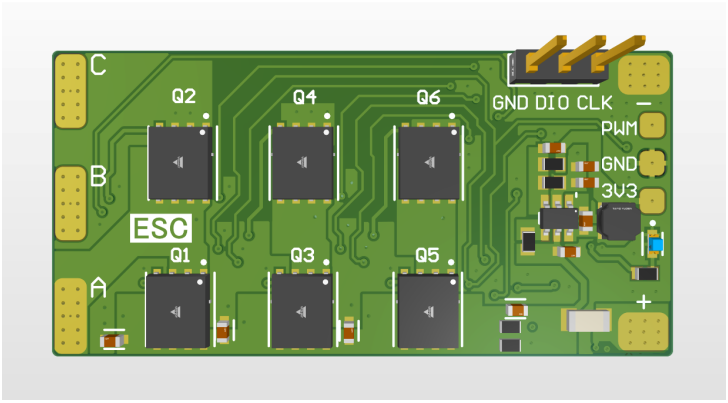


Figure 1.13: PCB bottom view

Before describing the component placement, let's take a moment to focus on the signals that must enter and exit the board. As high-power inputs and outputs, we have the battery's power and ground connections, as well as the three motor phases. To ensure low resistance for the current and a robust connection, appropriately sized pads are used for directly soldering the positive and negative battery wires and the three motor phase wires. For low-power signals, such as $PWM_{IN}$, 3.3 V, and GND (the 3.3 V is exposed for flexibility), smaller pads have been used. Finally, a 3-pin male header connector is included for interfacing with the board via the SWD protocol. Both the pads and the connector have been placed along the edges of the board for convenience. The bottom layer of the design is actually the one that will face upwards, which explains the choice of positioning the connector as it is. Careful component placement was necessary to meet two essential requirements for an ESC: separating the low-power control section from the high-power section as much as possible, while also achieving a compact and small-sized board of just 50.8 x 25 mm, slightly larger than a commercial ESC. Let's take a closer look at how the top and bottom layers were utilized. The top layer is dedicated to hosting the logic and low-power components, including the microcontroller, the three gate drivers, the differential amplifier, and all the associated components (capacitors, resistors, and diodes). The bottom layer, on the other hand, houses the high-power components, such as the buck converter, the shunt resistor for current monitoring, and the six MOSFETs of the three-phase half-bridge. To minimize the loop area of the half-bridge circuits, MOSFETs and gate drivers were placed overlapped on the top and bottom layer, in order to be close to each other. Let's now take a moment to highlight the considerations made for the placement of the buck converter and its associated components. As mentioned in section 4.1.3, one of the drawbacks of using a buck converter instead of a linear regulator is the added complexity to the PCB circuit design. The following precautions have been taken. High-current components like the inductor, output capacitor, and the switching MOSFETs are placed in such a way as to minimize the length of current paths. This helps reduce losses, noise and improves overall efficiency. High-power traces (such as those between the MOSFET and inductor) should be kept separate from low-power traces (such as those for the control circuitry) to avoid interference. A continuous ground plane, under the high-power components, is present for providing a low-impedance return path for current. Capacitors are placed as close as possible to the power pins to reduce parasitic resistance and inductance in the power lines. Components such as MOSFETs and inductors generate heat during operation. That is why large copper areas beneath have been placed to improve thermal dissipation. Figures 1.14, 1.17, 1.15 and 1.16 show the images of the PCB's four copper layers. Below, the decisions made regarding trace dimensions, polygon pours, and vias are explained.

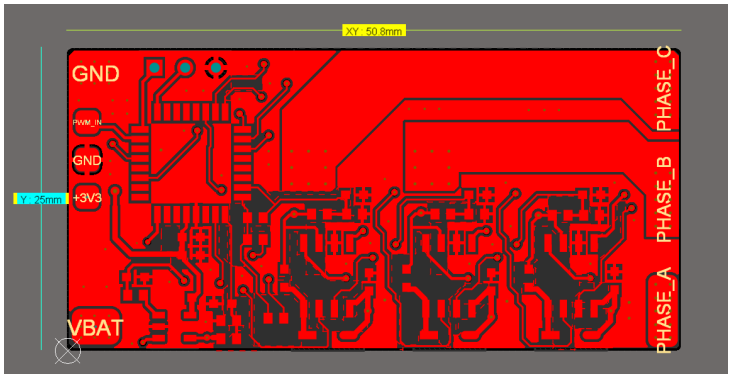


Figure 1.14: Top layer

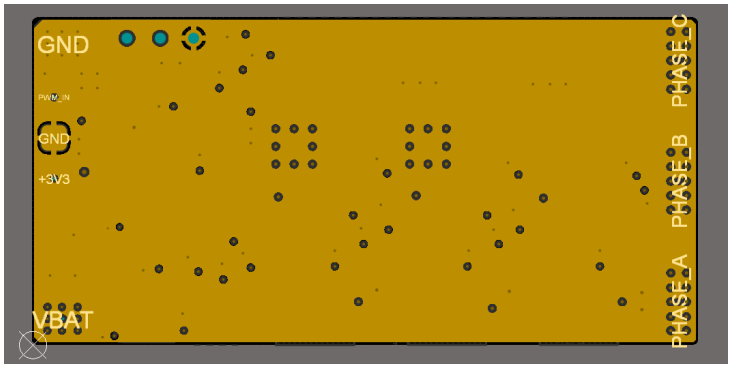


Figure 1.15: Internal layer 1

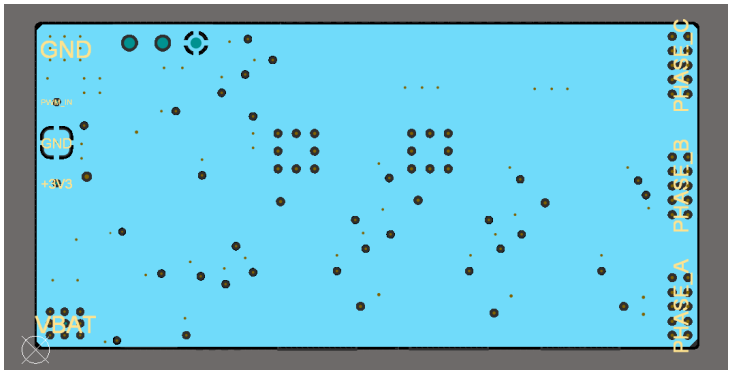


Figure 1.16: Internal layer 2

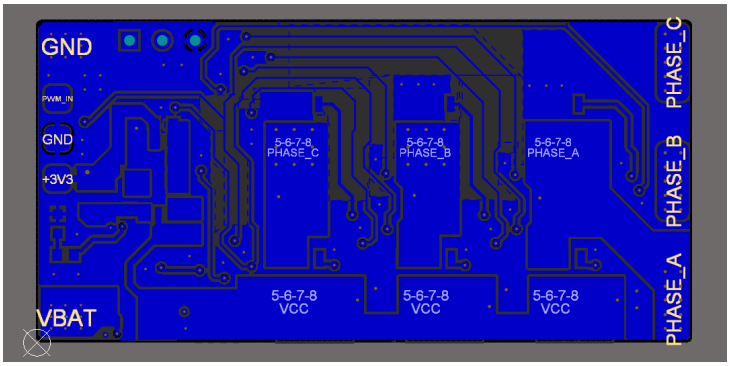


Figure 1.17: Bottom layer

Given the limited space, signal traces were generally designed with a width of 0.2 mm—a small dimension but still above the minimum thickness that a reliable PCB manufacturer can guarantee. Power traces must be wide enough to handle high currents without excessive heating and kept as short as possible to reduce resistance and voltage drops, as well as to provide a low-impedance path for the current. For distributing power to the high-power circuit, a polygon pour was implemented on the bottom layer, connected to the three high-side MOSFETs of the bridge. An advantage of using polygons is that they ensure adequate areas to manage the thermal load from MOSFETs and other high-power components. Polygon pours were also used to connect the three motor phases to the pads for motor connection. Direct connections were used for the MOSFET-pad and the shunt resistor-pad connection to reduce resistance and avoid overheating. Thermal reliefs were used otherwise, whenever high current was not an issue, for easier soldering. Lastly, the power supply traces for the integrated circuits (MCU and drivers) were made 0.5 mm wide to minimize parasitic inductance and ensure a stable power delivery distribution across the board. As a rule of thumb, we tried to maintain where possible a distance between the traces of at least 3 times the thickness of the dielectric between the external and internal layers, i.e. 0.6 mm, to prevent signal coupling and cross-talk. Due to limited space, many vias are used to connect different layers of the PCB. The vias have sizes ranging from 0.25 to 0.6 mm and from 0.3 to 0.7 mm. Vias have been employed for different purposes:

- Signal vias are used to route signals between layers.
- Transfer vias ensure the return path for signals transitioning between layers and help contain the electromagnetic field dispersion.
- Via stitching connects the ground planes of different layers as much as possible, ensuring a stable reference voltage all over the board.

All vias have been designed with a "tented" finish to prevent potential shorts caused by soldering components on the board. To carry large currents between the top and bottom layers, multiple vias have been used in parallel on the battery and phases' pads.