RRAM-Based Analog Circuit for Matrix Inversion: Simulation and Analysis

Marco Mura

Outline

- RRAM-based Matrix Inversion Circuit
- Simulation and Results
- Final Remarks

RRAM-Based Matrix Inversion Circuit

The Linear Inverse Problem

$$\boldsymbol{Ax} = \boldsymbol{y}$$

$$\boldsymbol{x} = \boldsymbol{A}^{-1}\mathbf{y}$$

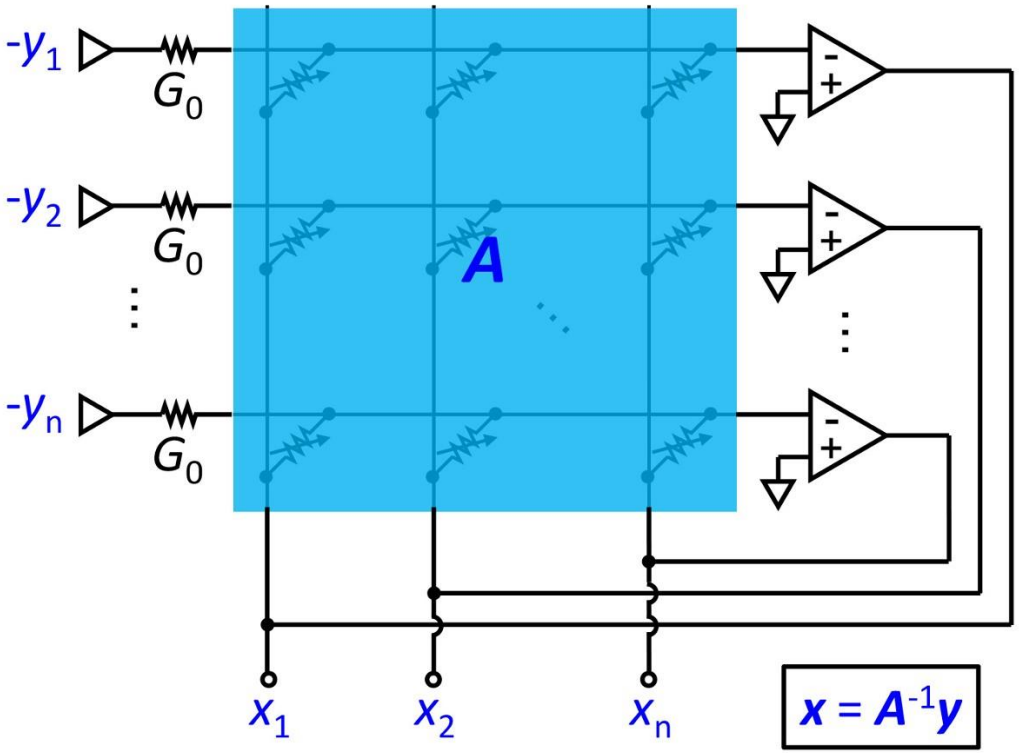
$\boldsymbol{A}$ nxn , $\det(\boldsymbol{A}) \neq 0$

Matrix Inversion in Digital Computer

Latency

High Energy Dissipation

RRAM-Based Analog Circuit for Matrix Inversion



Source: “Invited Tutorial: Analog Matrix Computing With Cross point Resistive Memory Arrays”, Sun and Ielmini, 2022.

A ➡ G

Kirchhoff’s current law

Analog vs Digital

High speed

Low power

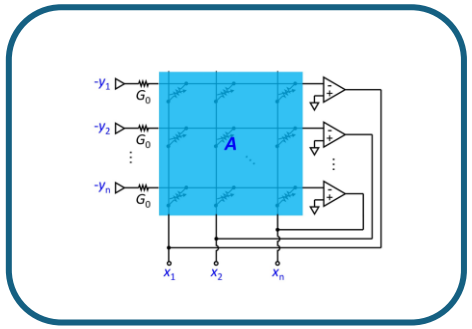
BUT

Non-idealities:

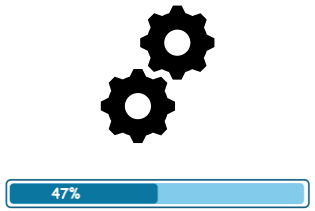
Accuracy degradation

Simulation and Results

Workflow



$A \longleftrightarrow G$

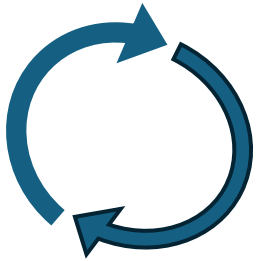


Circuit Model

Mapping

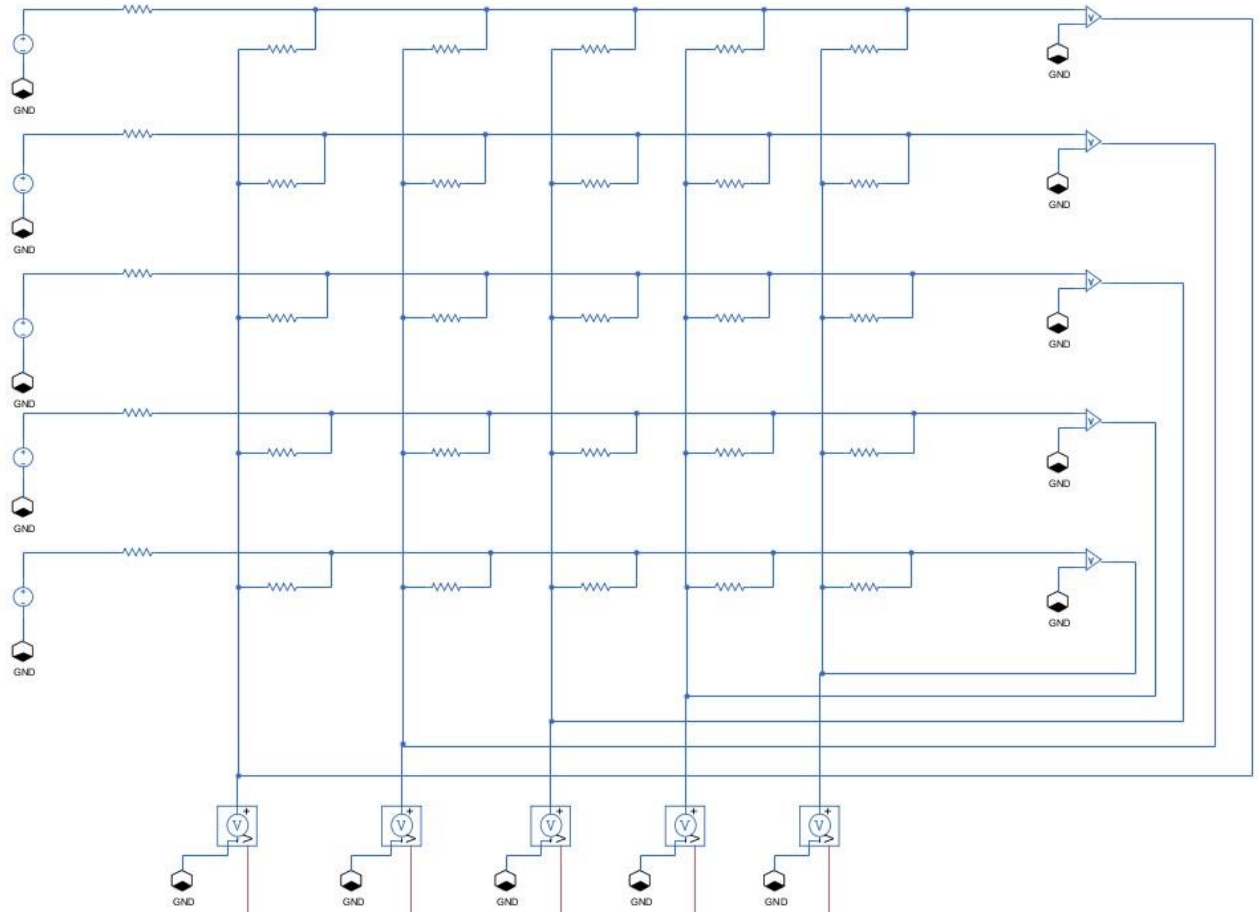
Simulation

Comparison



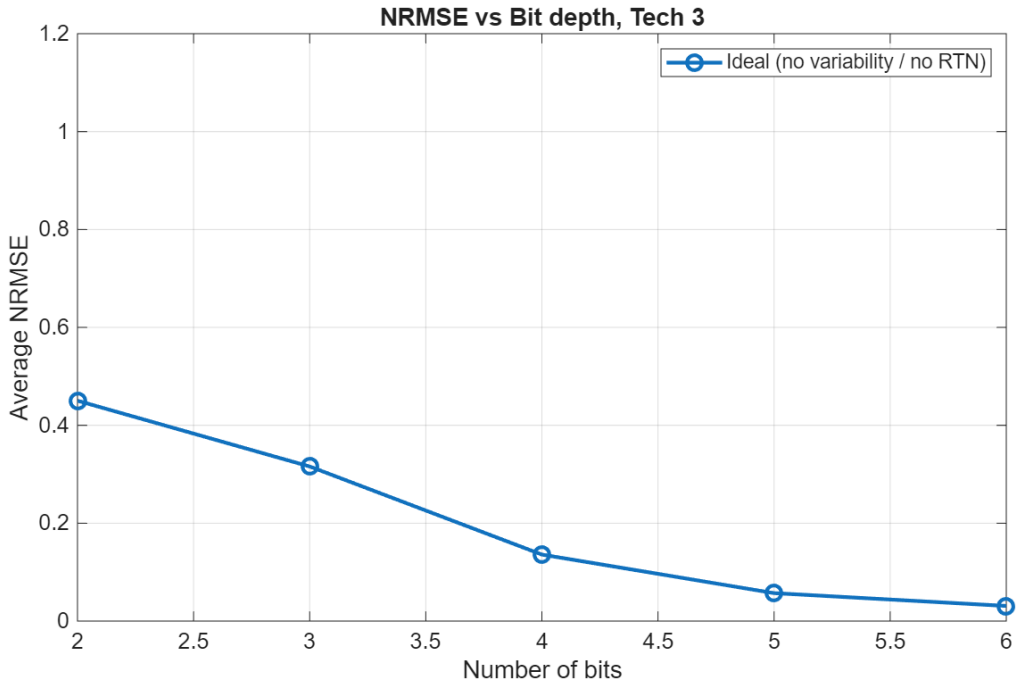
Evaluation of Encoding Strategies under Variability and RTN Effects

Evaluation of Encoding Strategies under Variability and RTN Effects: **Icomp, Vreset**

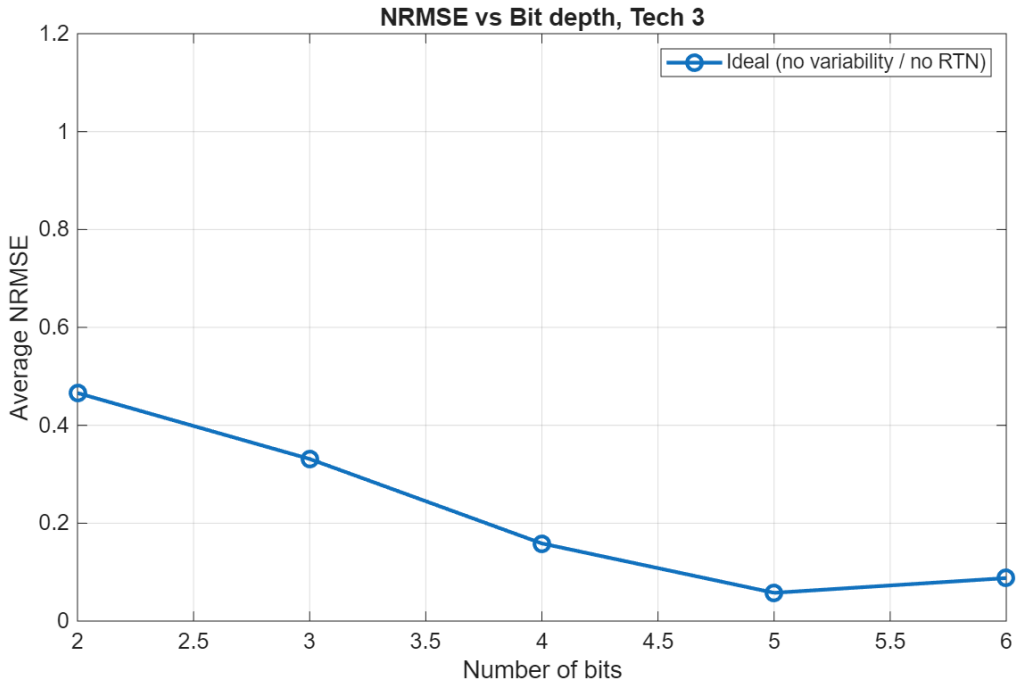


Evaluation of Encoding Strategies under Variability and RTN Effects: **Icomp, Vreset**

Compliance current

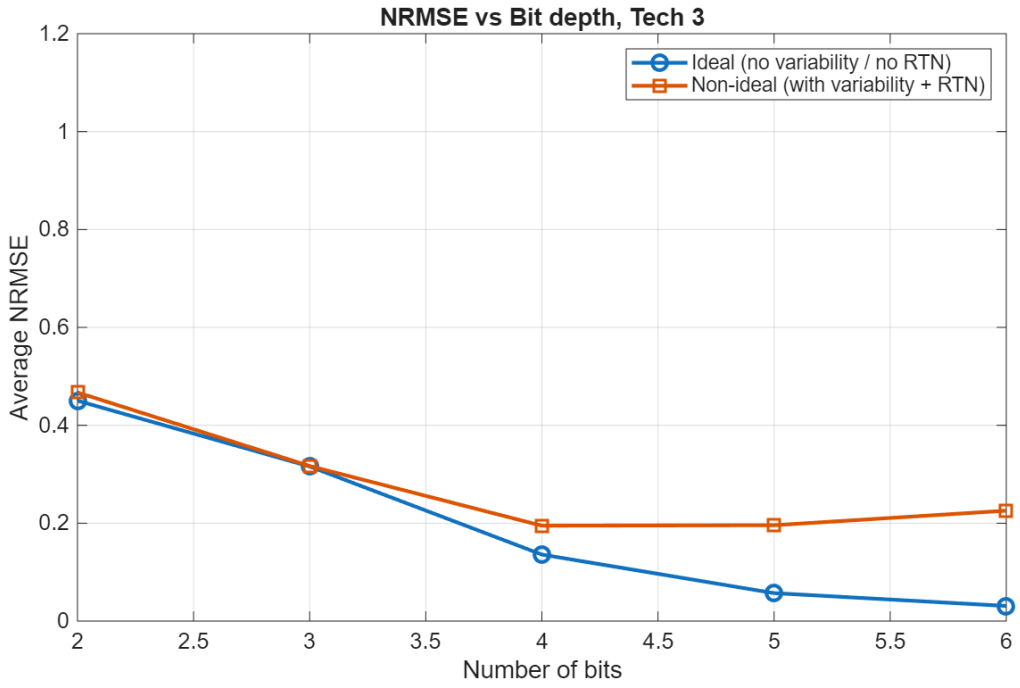


V RESET

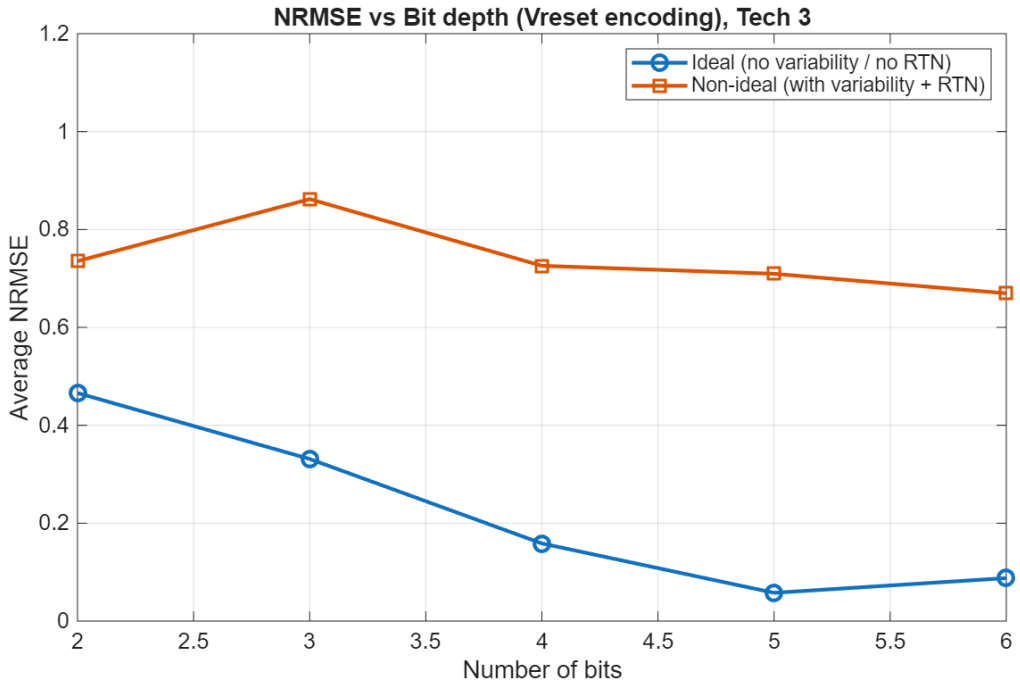


Evaluation of Encoding Strategies under Variability and RTN Effects: **Icomp, Vreset**

Compliance Current Encoding

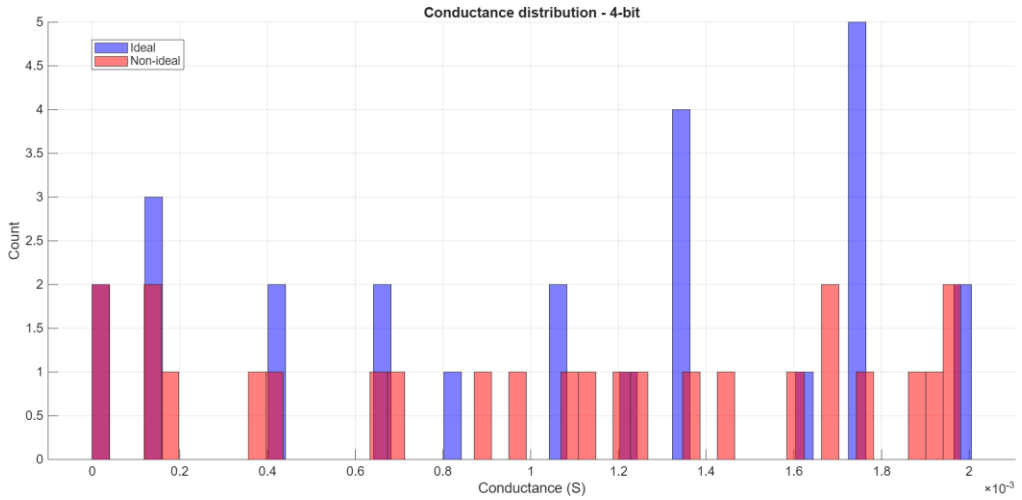


V Reset Encoding



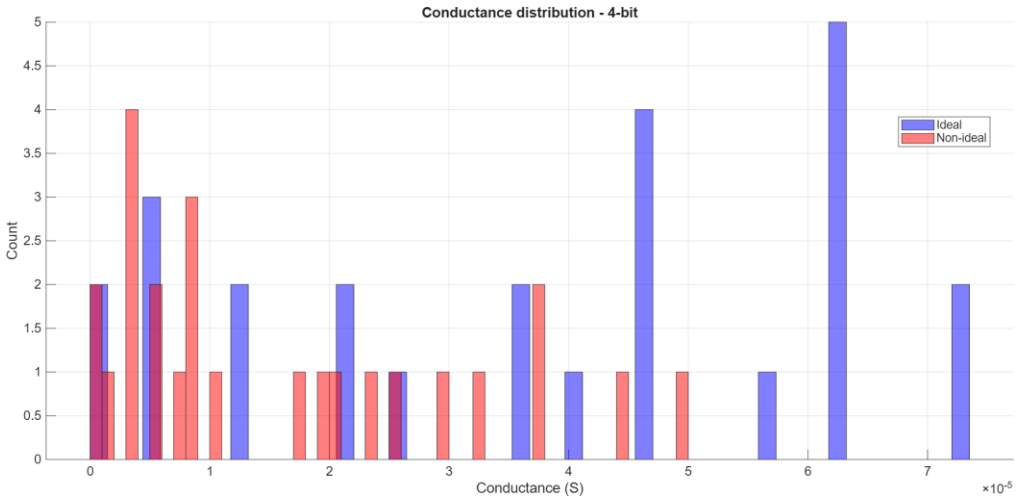
Evaluation of Encoding Strategies under Variability and RTN Effects: **Icomp, Vreset**

Compliance current



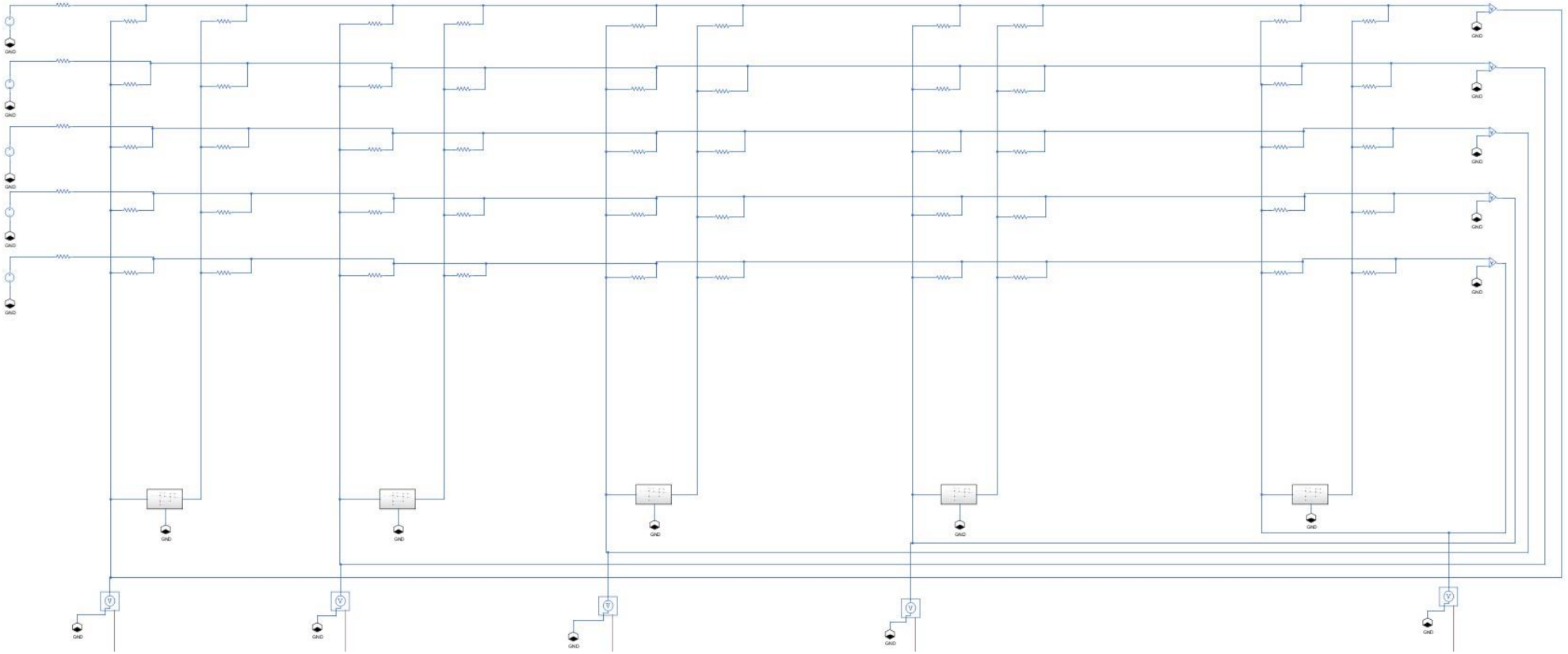
$$NRMSE = 0,0822$$

V RESET



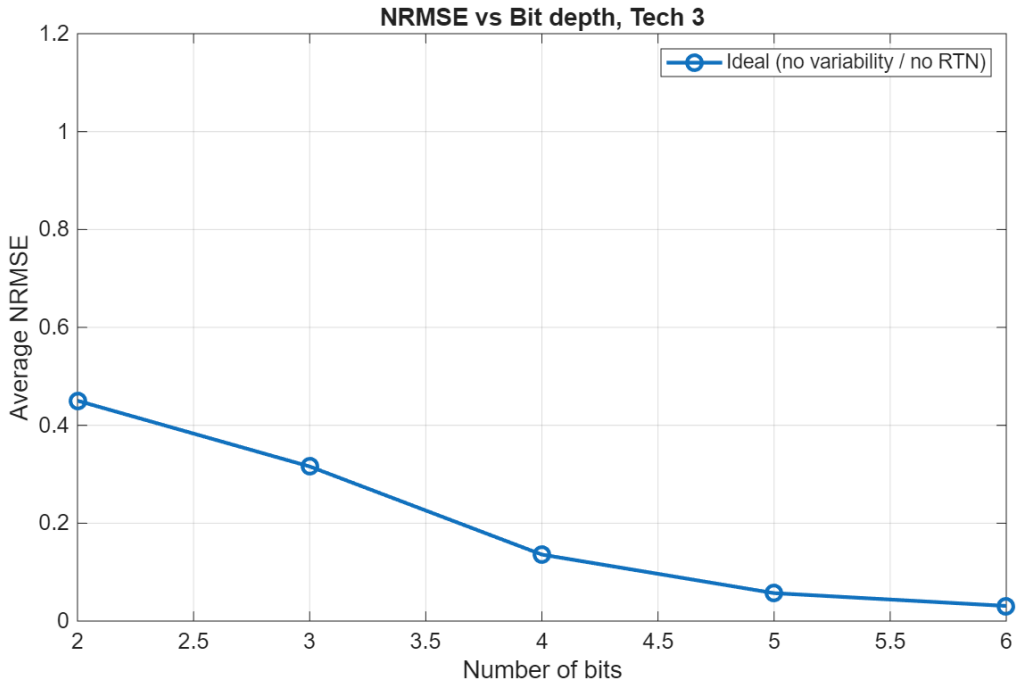
$$NRMSE = 0,7358$$

Evaluation of Encoding Strategies under Variability and RTN Effects: **Multiple Devices**

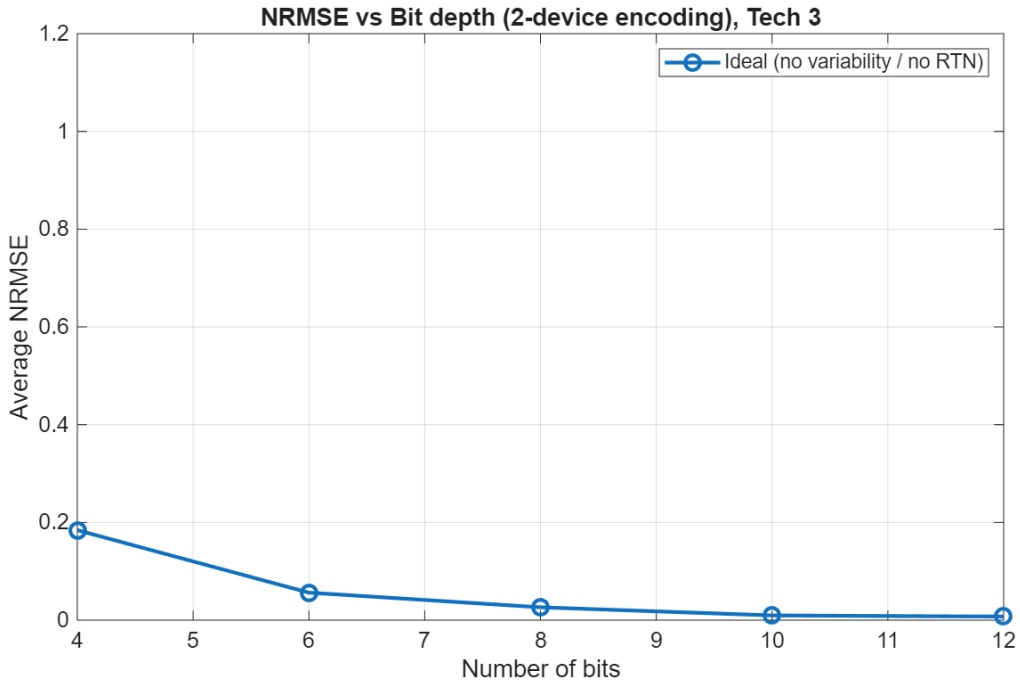


Evaluation of Encoding Strategies under Variability and RTN Effects: **Multiple Devices**

Compliance current

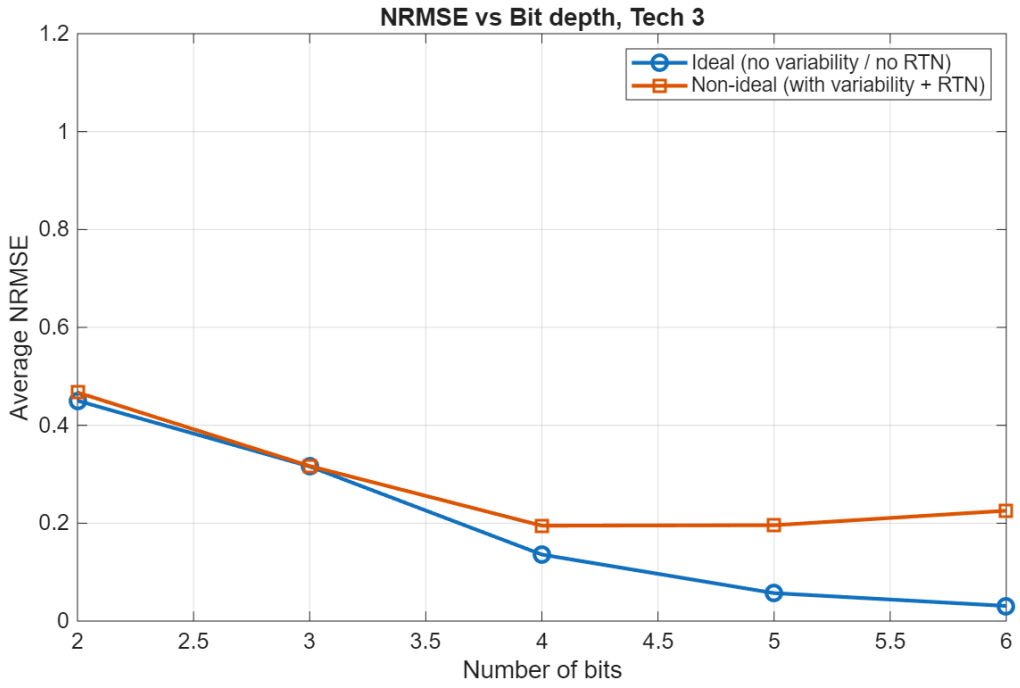


Compliance current, 2 devices per weight

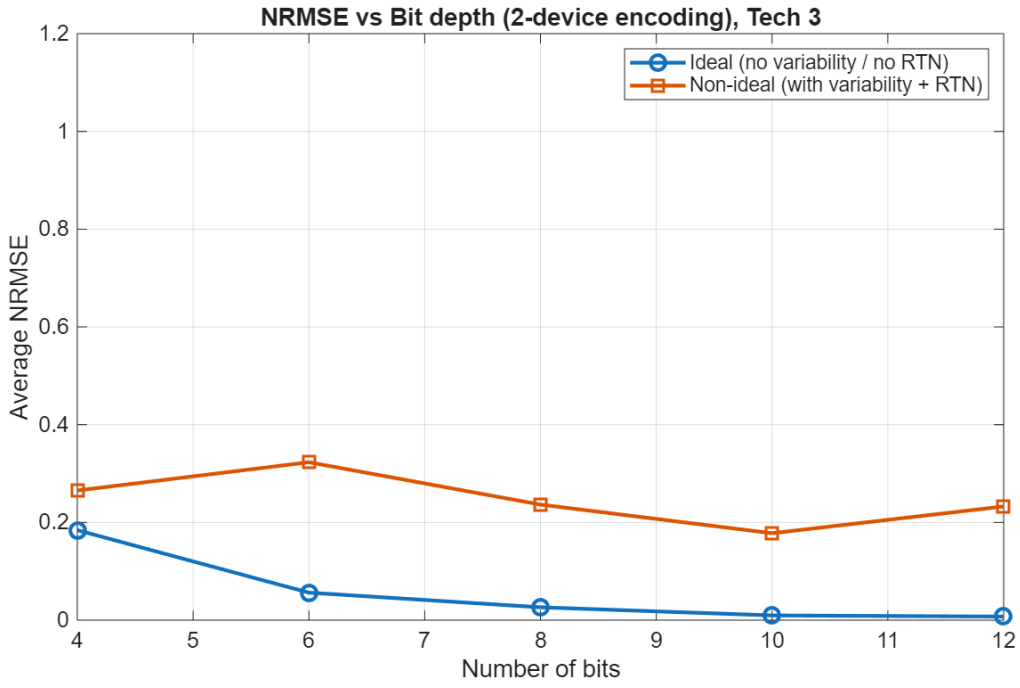


Evaluation of Encoding Strategies under Variability and RTN Effects: **Multiple Devices**

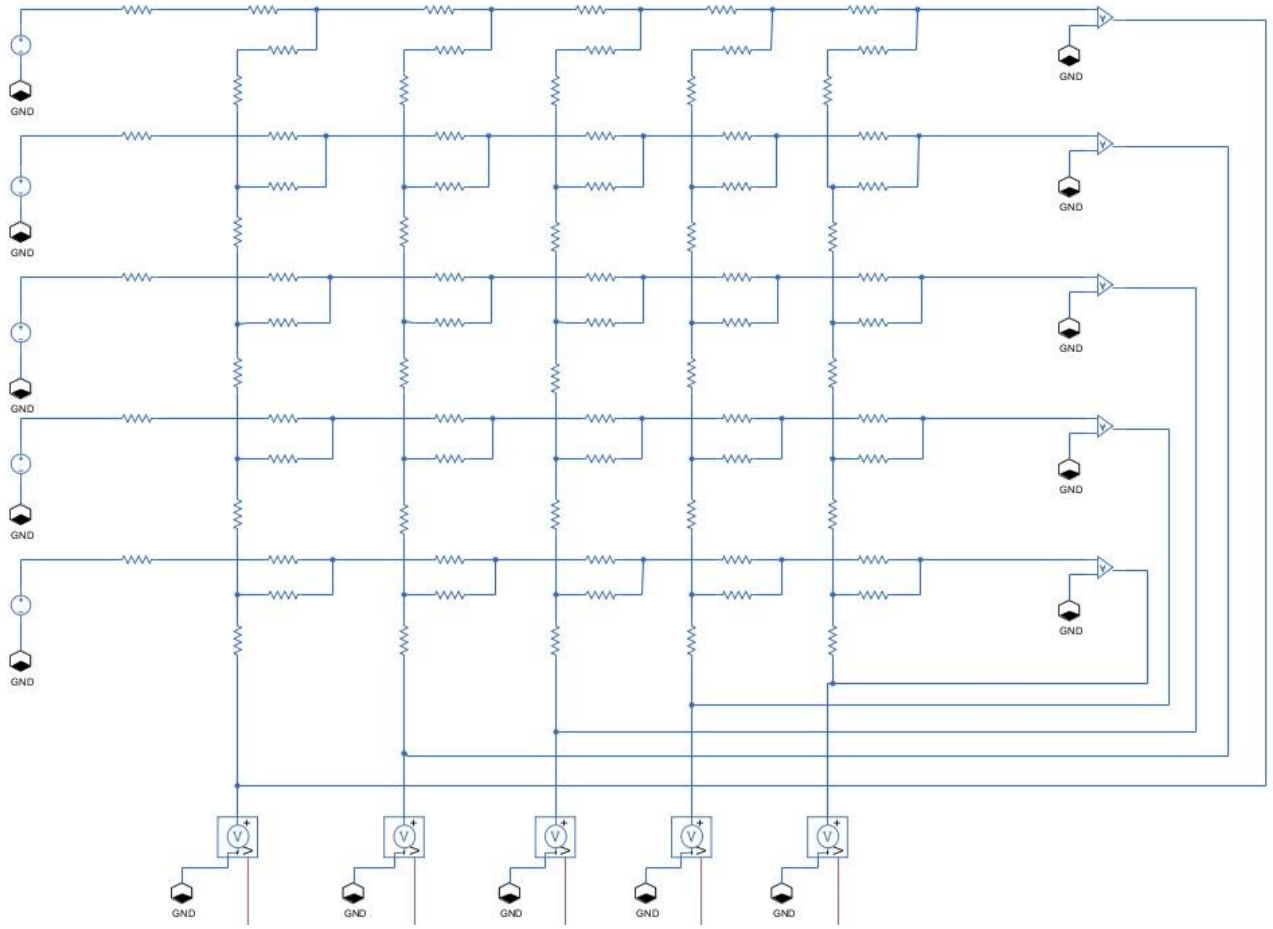
Compliance current



Compliance current, 2 devices per weight

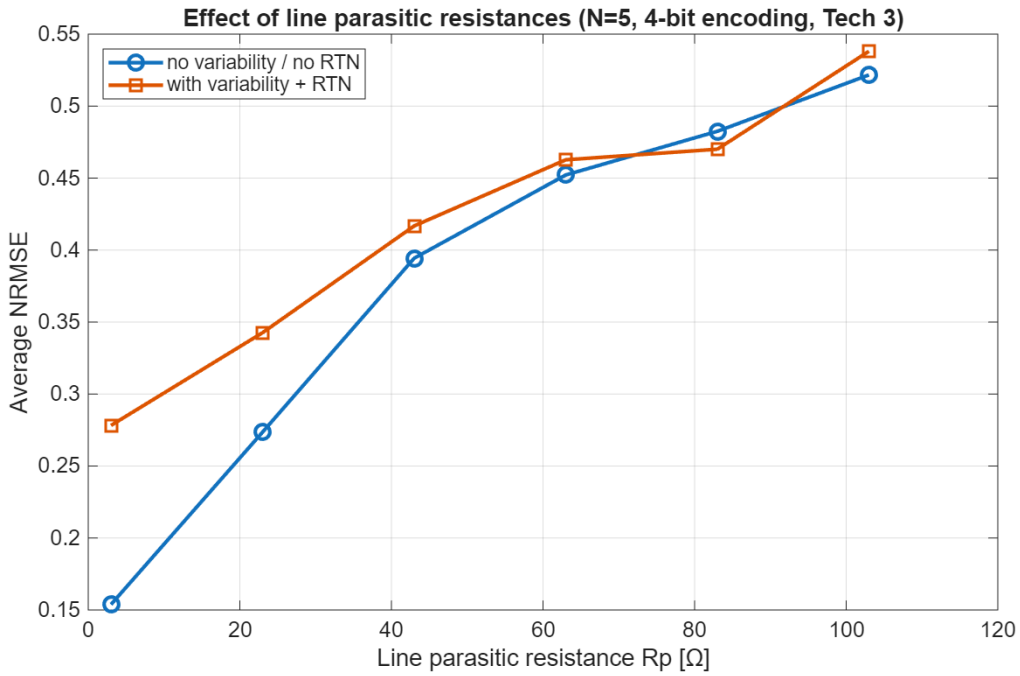


Effects of Line Parasitic Resistances

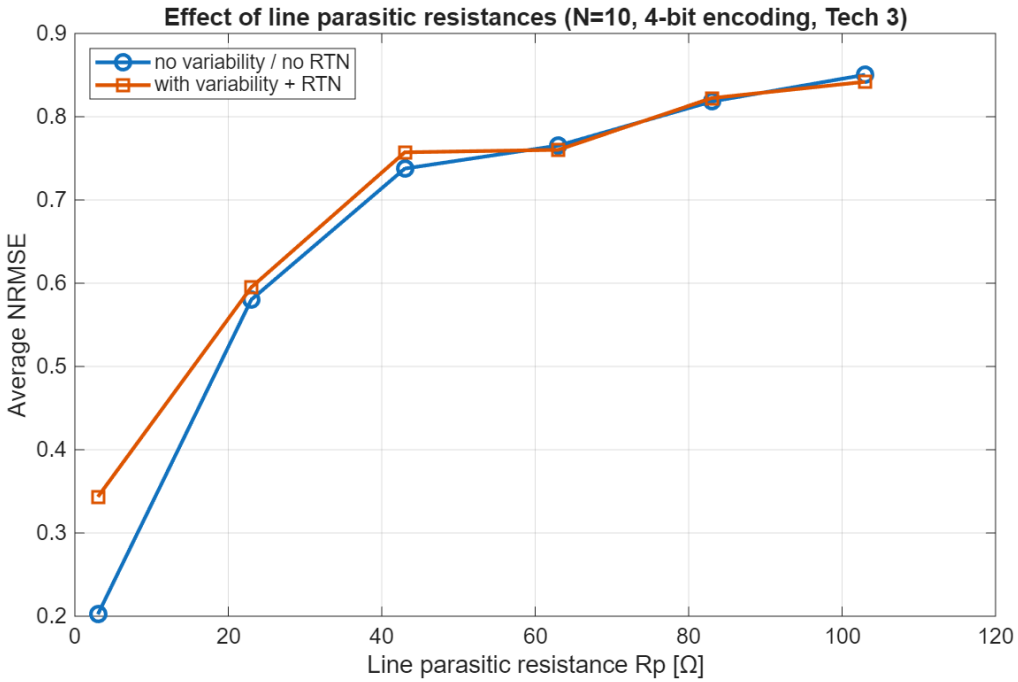


Effects of Line Parasitic Resistances

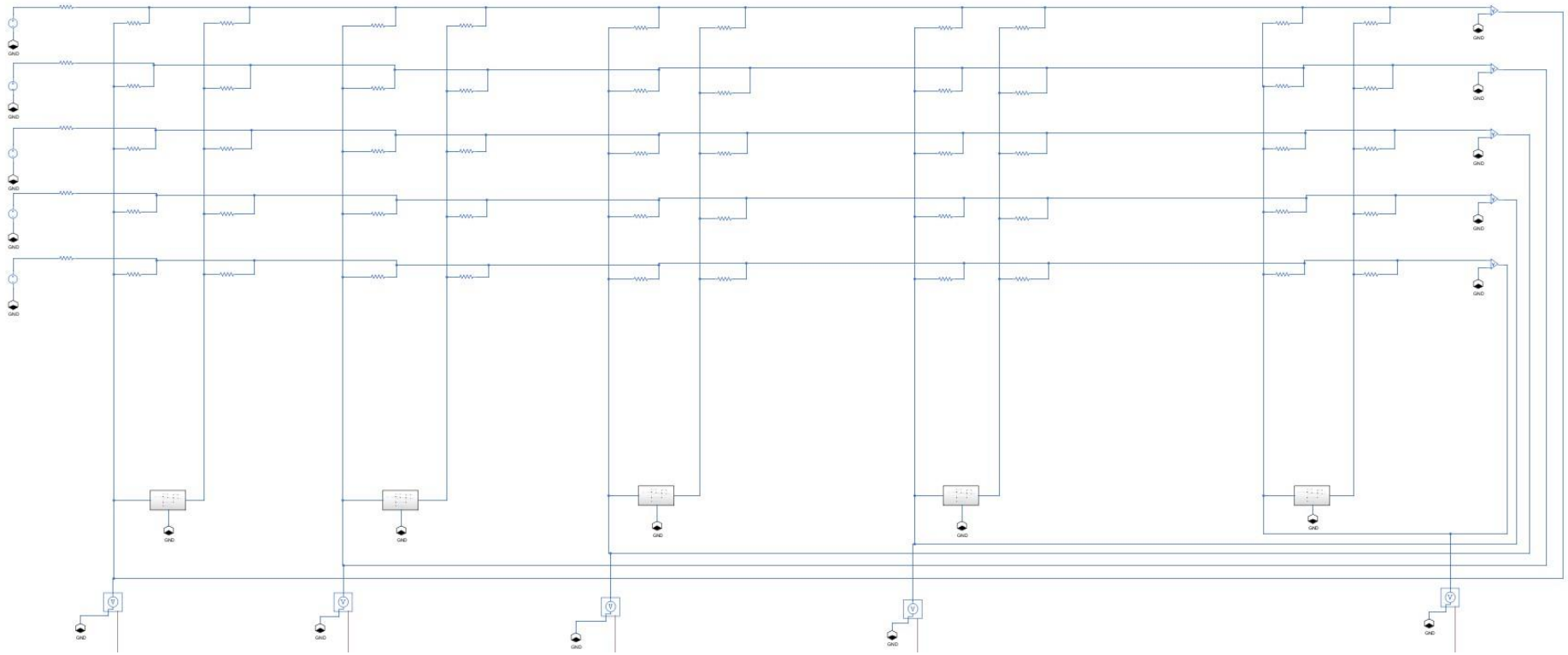
5x5 crossbar



10x10crossbar

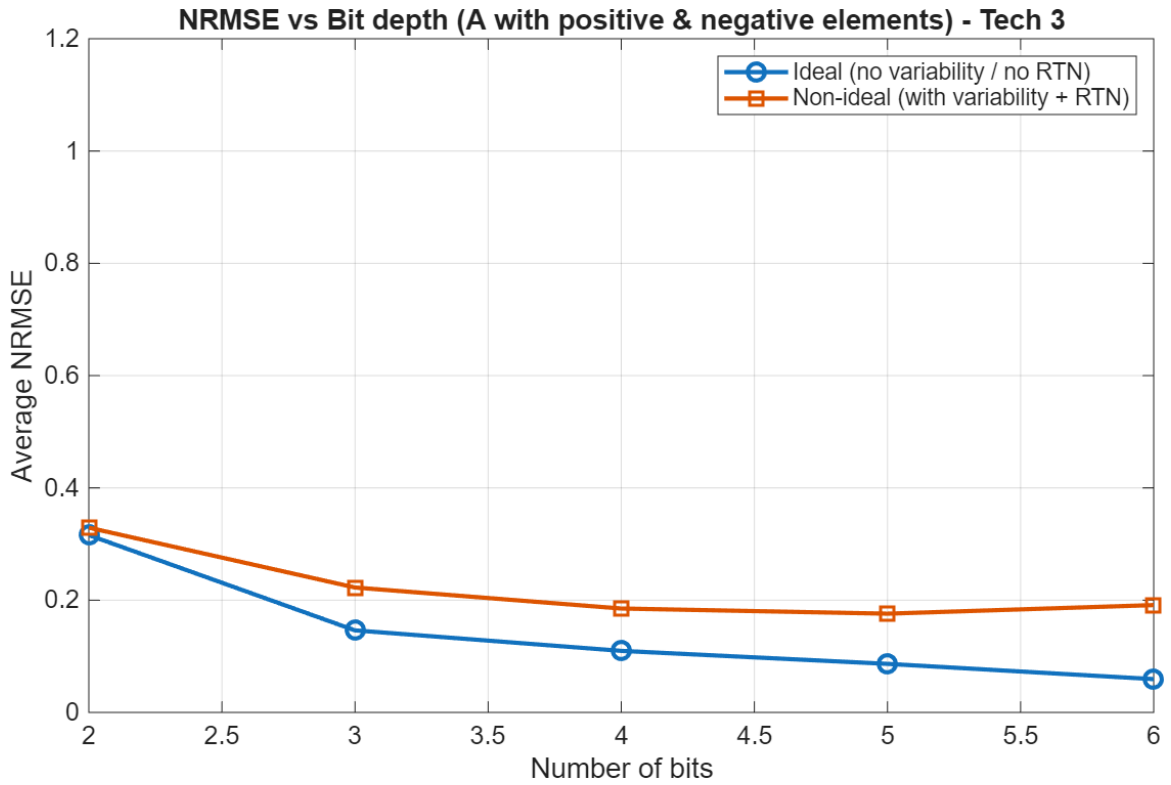


Handling Matrices with Positive and Negative Entries

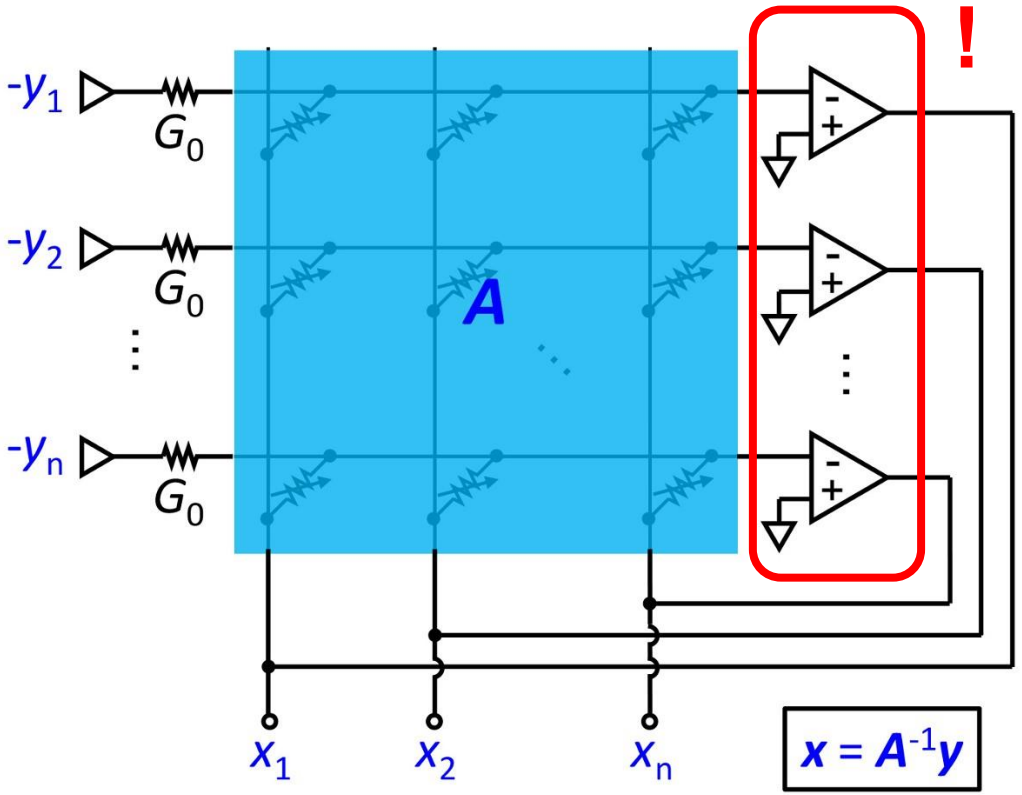


Handling Matrices with Positive and Negative Entries

Current compliance



Power Consumption Estimation



Source: “Invited Tutorial: Analog Matrix Computing With Cross point Resistive Memory Arrays”, Sun and Ielmini, 2022.

$Vread \leq 0.01V$

5x5 basic circuit $\sim tens\ \mu W$

More complex circuit $\sim hundreds\ \mu W$

Final Remarks

Final Remarks

Promising alternative 

Non-idealities 

Bibliography

[1] Zhong Sun and Daniele Ielmini. “Invited Tutorial: Analog Matrix Computing With Cross point Resistive Memory Arrays”. In: IEEE Transactions on Circuits and Systems II: Ex-press Briefs 69.7 (2022).