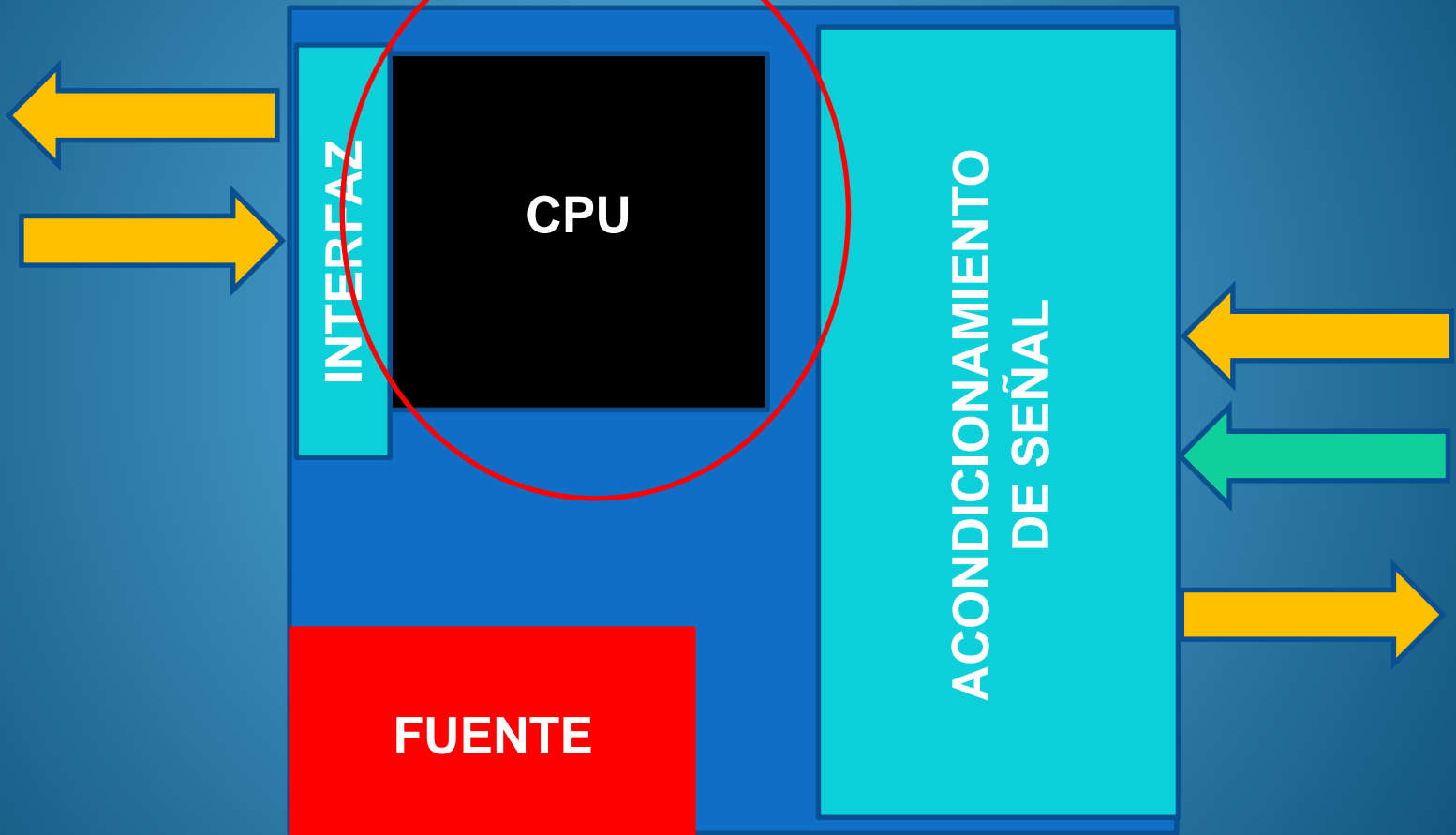




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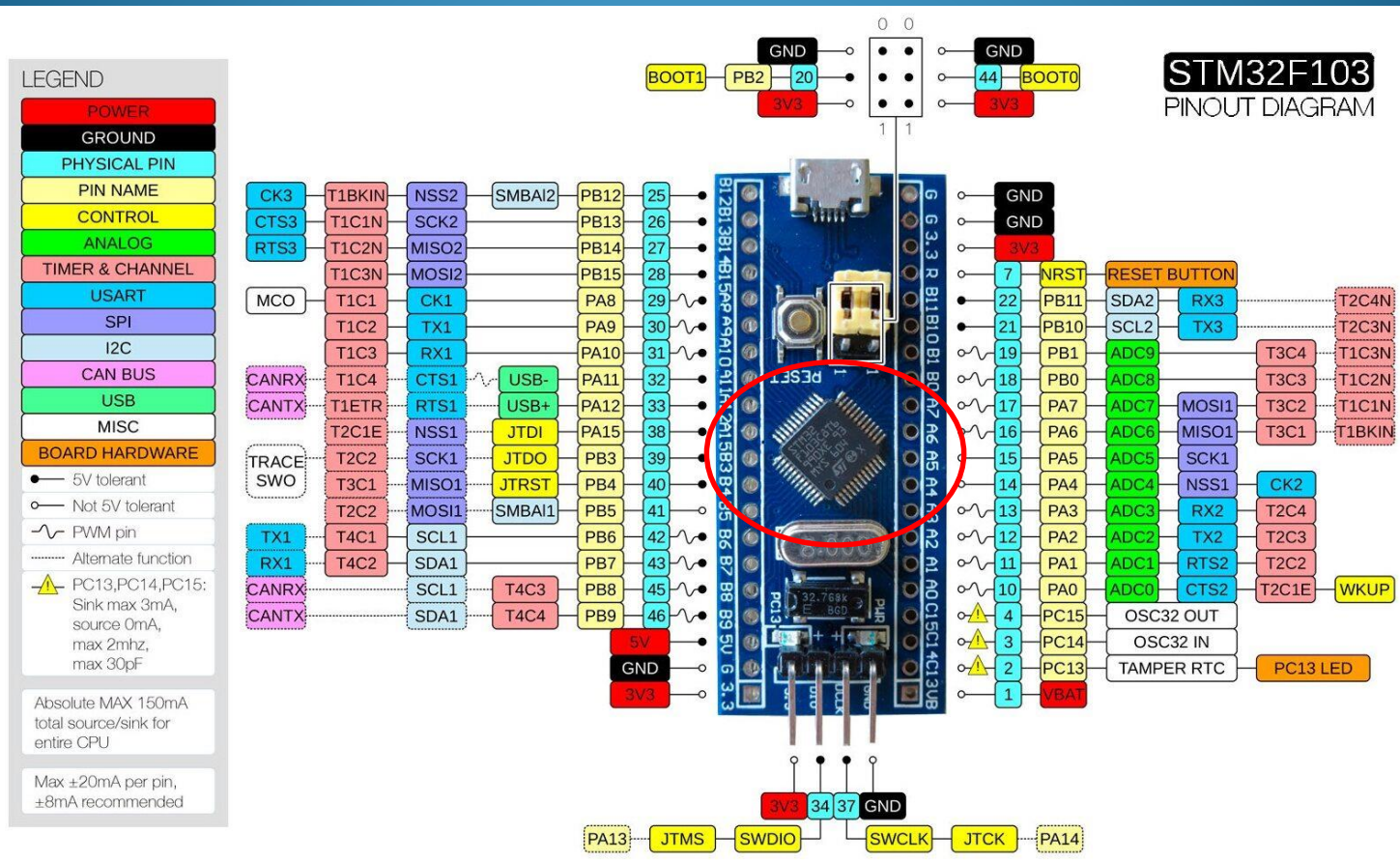
Instrumento Virtual

Placa de Adquisición



Instrumento Virtual

CPU

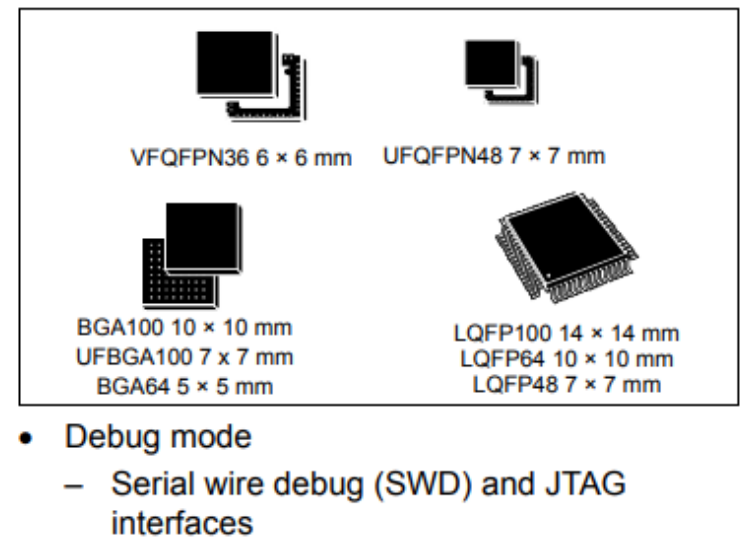


STM32F106T8

CPU

Features

- Arm® 32-bit Cortex®-M3 CPU core
 - 72 MHz maximum frequency, 1.25 DMIPS / MHz (Dhrystone 2.1) performance at 0 wait state memory access
 - Single-cycle multiplication and hardware division
- Memories
 - 64 or 128 Kbytes of Flash memory
 - 20 Kbytes of SRAM
- Up to nine communication interfaces
 - Up to two I²C interfaces (SMBus/PMBus®)
 - Up to three USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
 - Up to two SPIs (18 Mbit/s)
 - CAN interface (2.0B Active)
 - USB 2.0 full-speed interface



STM32F103T8

Table 2. STM32F103xx medium-density device features and peripheral counts

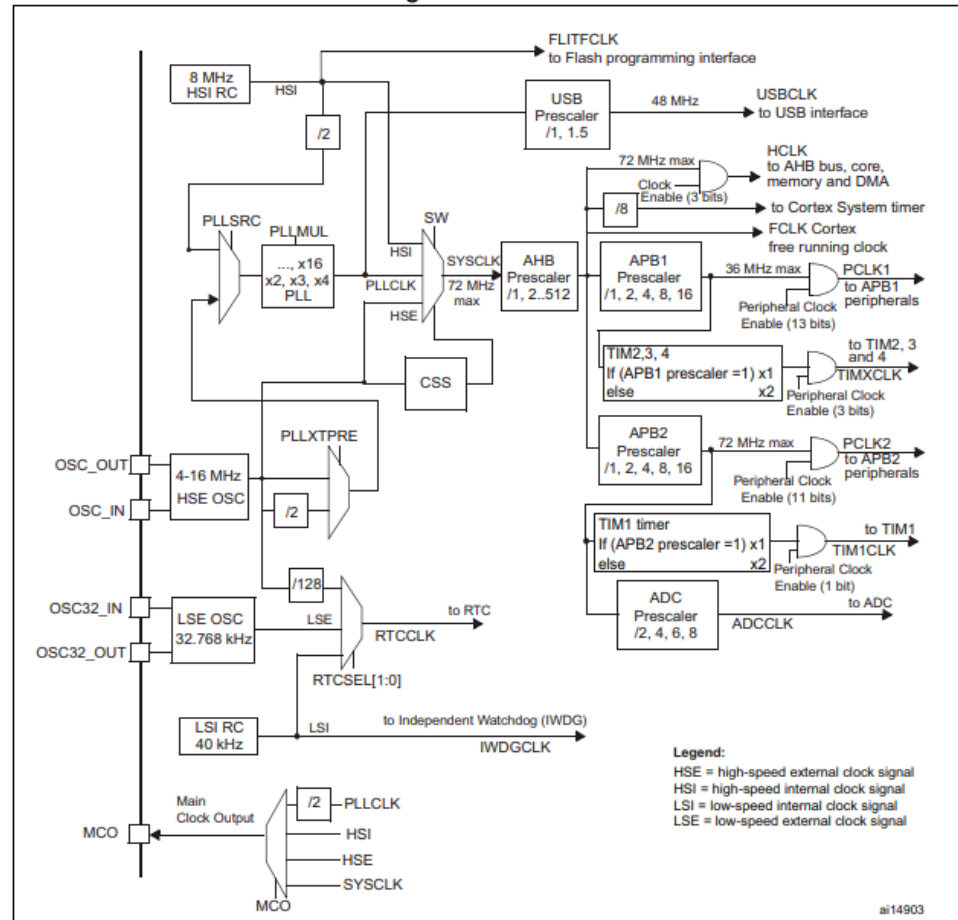
Peripheral		STM32F103Tx		STM32F103Cx		STM32F103Rx		STM32F103Vx	
Flash - Kbytes		64	128	64	128	64	128	64	128
SRAM - Kbytes		20		20		20		20	
Timers	General-purpose	3		3		3		3	
	Advanced-control	1		1		1		1	
Communication	SPI	1		2		2		2	
	I ² C	1		2		2		2	
	USART	2		3		3		3	
	USB	1		1		1		1	
	CAN	1		1		1		1	
GPIOs		26		37		51		80	
12-bit synchronized ADC		2		2		2		2	
Number of channels		10 channels		10 channels		16 channels ⁽¹⁾		16 channels	
CPU frequency		72 MHz							
Operating voltage		2.0 to 3.6 V							
Operating temperatures		Ambient temperatures: -40 to +85 °C / -40 to +105 °C (see Table 9) Junction temperature: -40 to + 125 °C (see Table 9)							
Packages		VFQFPN36		LQFP48, UFQFPN48		LQFP64, TFBGA64		LQFP100, LFBGA100, UFBGA100	

Figure 1. STM32F103xx performance line block diagram



STM32F103T8

Figure 2. Clock tree



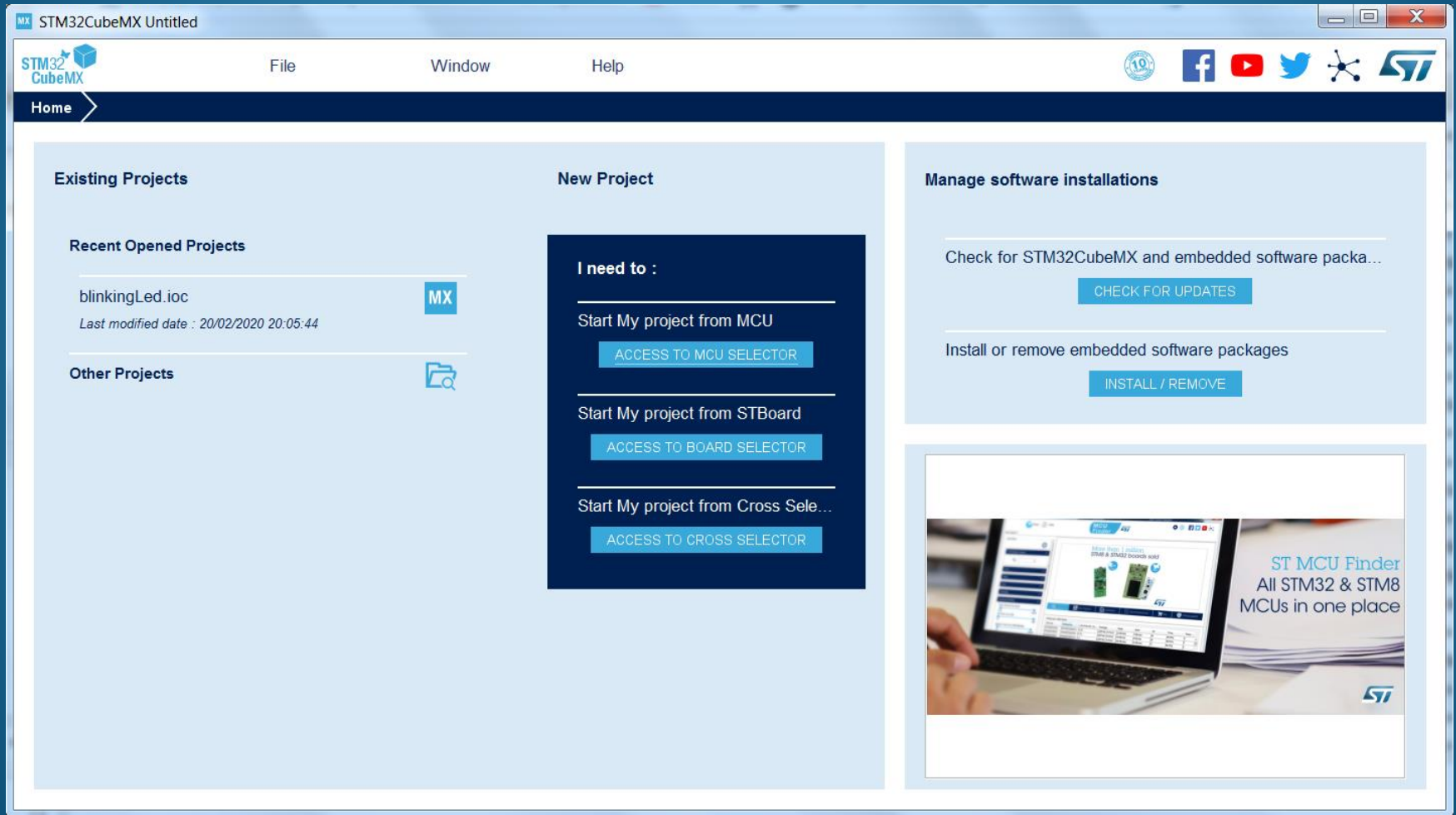
1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
2. For the availability of the USB function both HSE and PLL must be enabled, with USBCLK running at 48 MHz.
3. To have an ADC conversion time of 1 μ s, APB2 must be at 14 MHz, 28 MHz or 56 MHz.

STM32F103T8

Table 5. Medium-density STM32F103xx pin definitions

Pins							Pin name	Type ⁽¹⁾	I/O Level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions ⁽⁴⁾	
LFBGA100	UFBG100	LQFP48/UFQFPN48	TFBGA64	LQFP64	LQFP100	VQFPN36					Default	Remap
A3	B2	-	-	-	1	-	PE2	I/O	FT	PE2	TRACECK	-
B3	A1	-	-	-	2	-	PE3	I/O	FT	PE3	TRACED0	-
C3	B1	-	-	-	3	-	PE4	I/O	FT	PE4	TRACED1	-
D3	C2	-	-	-	4	-	PE5	I/O	FT	PE5	TRACED2	-
E3	D2	-	-	-	5	-	PE6	I/O	FT	PE6	TRACED3	-
B2	E2	1	B2	1	6	-	V _{BAT}	S	-	V _{BAT}	-	-
A2	C1	2	A2	2	7	-	PC13-TAMPER-RTC ⁽⁵⁾	I/O	-	PC13 ⁽⁶⁾	TAMPER-RTC	-
A1	D1	3	A1	3	8	-	PC14-OSC32_IN ⁽⁵⁾	I/O	-	PC14 ⁽⁶⁾	OSC32_IN	-
B1	E1	4	B1	4	9	-	PC15-OSC32_OUT ⁽⁵⁾	I/O	-	PC15 ⁽⁶⁾	OSC32_OUT	-
C2	F2	-	-	-	10	-	V _{SS_5}	S	-	V _{SS_5}	-	-
D2	G2	-	-	-	11	-	V _{DD_5}	S	-	V _{DD_5}	-	-
C1	F1	5	C1	5	12	2	OSC_IN	I	-	OSC_IN	-	PD0 ⁽⁷⁾
D1	G1	6	D1	6	13	3	OSC_OUT	O	-	OSC_OUT	-	PD1 ⁽⁷⁾
E1	H2	7	E1	7	14	4	NRST	I/O	-	NRST	-	-
F1	H1	-	E3	8	15	-	PC0	I/O	-	PC0	ADC12_IN10	-
F2	J2	-	E2	9	16	-	PC1	I/O	-	PC1	ADC12_IN11	-
E2	J3	-	F2	10	17	-	PC2	I/O	-	PC2	ADC12_IN12	-
F3	K2	-	.(8)	11	18	-	PC3	I/O	-	PC3	ADC12_IN13	-
G1	J1	8	F1	12	19	5	V _{SSA}	S	-	V _{SSA}	-	-
H1	K1	-	-	-	20	-	V _{REF-}	S	-	V _{REF-}	-	-
J1	L1	-	G1 ⁽⁸⁾	-	21	-	V _{REF+}	S	-	V _{REF+}	-	-
K1	M1	9	H1	13	22	6	V _{DDA}	S	-	V _{DDA}	-	-

STM32CubeMX



STM32FCubeMX

MCU/MPU Filters



Part Number Search



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Price From 0.0 to 11.543



IO From 0 to 176



Eeprom From 0 to 16384 (Bytes)



Flash From 0 to 2048 (kBytes)



Ram From 0 to 1184 (kBytes)



Freq. From 24 to 800 (MHz)



Peripheral >

Features

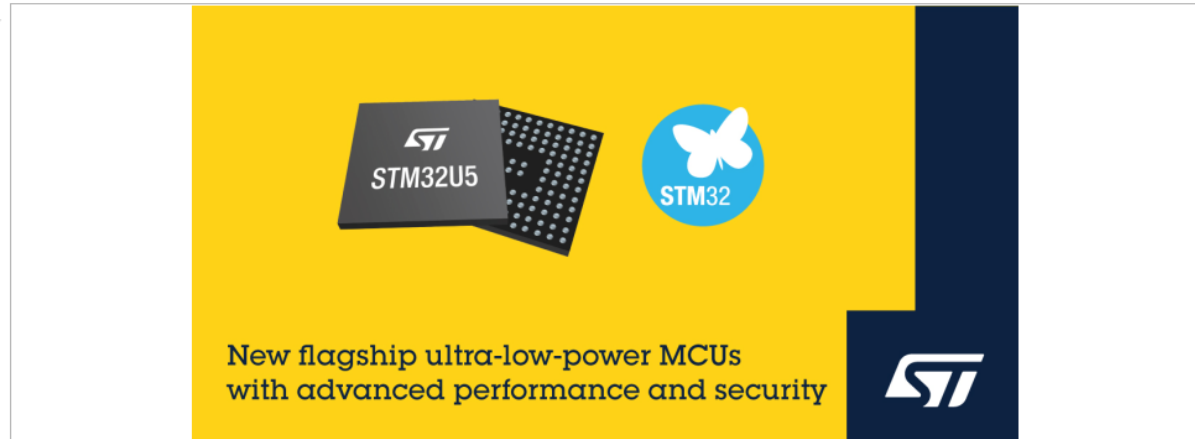
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*	Part No	Reference	Marketing Stat.	Unit Price for 10kU (U..	Board	Package	Flash	RAM	IO	Freq.	
☆	STM32F030C6	STM32F030C6Tx	Active	0.722		LQFP48	32 kBytes	4 kBytes	39	48 MHz	
☆	STM32F030C8	STM32F030C8Tx	Active	0.874		LQFP48	64 kBytes	8 kBytes	39	48 MHz	
☆	STM32F030CC	STM32F030CCTx	Active	1.331		LQFP48	256 kBytes	32 kBytes	37	48 MHz	
☆	STM32F030F4	STM32F030F4Px	Active	0.513		TSSOP20	16 kBytes	4 kBytes	15	48 MHz	
☆	STM32F030K6	STM32F030K6Tx	Active	0.627		LQFP32	32 kBytes	4 kBytes	25	48 MHz	
☆	STM32F030R8	STM32F030R8Tx	Active	0.912	NUCLEO-F030R8	32F0308DISCOVERY	LQFP64	64 kBytes	8 kBytes	55	48 MHz
☆	STM32F030RC	STM32F030RCTx	Active	1.464		LQFP64	256 kBytes	32 kBytes	51	48 MHz	
☆	STM32F031C4	STM32F031C4Tx	Active	1.174		LQFP48	16 kBytes	4 kBytes	39	48 MHz	
☆	STM32F031C6	STM32F031C6Tx	Active	1.226		LQFP48	32 kBytes	4 kBytes	39	48 MHz	
☆	STM32F031E6	STM32F031E6Yx	Active	0.939		WLCSP25	32 kBytes	4 kBytes	20	48 MHz	
☆	STM32F031F4	STM32F031F4Px	Active	0.861		TSSOP20	16 kBytes	4 kBytes	15	48 MHz	
☆	STM32F031F6	STM32F031F6Px	Active	0.913		TSSOP20	32 kBytes	4 kBytes	15	48 MHz	
☆	STM32F031G4	STM32F031G4Ux	Active	0.887		UFQFPN28	16 kBytes	4 kBytes	23	48 MHz	
☆	STM32F031G6	STM32F031G6Ux	Active	0.939		UFQFPN28	32 kBytes	4 kBytes	23	48 MHz	
☆	STM32F031K4	STM32F031K4Ux	Active	1.043		UFQFPN32	16 kBytes	4 kBytes	27	48 MHz	

STM32FCubeMX

MCU/MPU Selector

Board Selector

Cross Selector

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Part Number Search

Core

Check/Uncheck All

☐ ARM Cortex-A7
 ☐ ARM Cortex-A7 + ARM Cortex-M4
 ☐ ARM Cortex-M0
 ☐ ARM Cortex-M0+
 ☒ ARM Cortex-M3
 ☐ ARM Cortex-M4
 ☐ ARM Cortex-M7
 ☐ ARM Cortex-M7 + ARM Cortex-M4
 ☐ ARM Cortex-M33

Series

Line

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Price From 0.0 to 8.375

0.0 8.375

IO From 26 to 140

26 140

Eeprom From 0 to 16384 (Bytes)

0 16384

Flash From 16 to 1024 (kBytes)

16 1024

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☆ STM32F103C8




Mainstream Performance line, Arm Cortex-M3 MCU with 64 Kbytes of Flash memory, 72 MHz CPU, motor control, USB and CAN

ACTIVE Active

Product is in mass production

Unit Price for 10kU (US\$) : 2.419

 LQFP48

The STM32F103xx medium-density performance line family incorporates the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 20 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general purpose 16-bit timers plus one PWM timer, as well as standard and advanced communication interfaces: up to two I²Cs and SPIs, three USARTs, an USB and a CAN.

The devices operate from a 2.0 to 3.6 V power supply. They are available in both the 40 to +85 °C temperature range and the 40 to +105 °C extended temperature range. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F103xx medium-density performance line family includes devices in six different package types: from 36 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

MCUs/MPUs List: 303 items

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*	Part No	Reference	Marketing Stat.	Unit Price for 10kU (U	Board	Package	Flash	RAM	IO	Freq
☆	STM32F102R6	STM32F102R6Tx	Active	2.114		LQFP64	32 kBytes	6 kBytes	51	48 MHz
☆	STM32F102R8	STM32F102R8Tx	Active	2.375		LQFP64	64 kBytes	10 kBytes	51	48 MHz
☆	STM32F102RB	STM32F102RBTx	Active	2.662		LQFP64	128 kBytes	16 kBytes	51	48 MHz
☆	STM32F103C4	STM32F103C4Tx	Active	2.028		LQFP48	16 kBytes	6 kBytes	37	72 MHz
☆	STM32F103C6	STM32F103C6Tx	Active	2.08		LQFP48	32 kBytes	10 kBytes	37	72 MHz
☆	STM32F103C6	STM32F103C6Ux	Active	2.08		UFQFPN48	32 kBytes	10 kBytes	37	72 MHz
☆	STM32F103C8	STM32F103C8Tx	Active	2.419		LQFP48	64 kBytes	20 kBytes	37	72 MHz
☆	STM32F103CB	STM32F103CBTx	Active	2.706		LQFP48	128 kBytes	20 kBytes	37	72 MHz
☆	STM32F103CB	STM32F103CBUx	Active	2.706		UFQFPN48	128 kBytes	20 kBytes	37	72 MHz
☆	STM32F103R4	STM32F103R4Hx	Active	2.213		TFBGA64	16 kBytes	6 kBytes	50	72 MHz
☆	STM32F103R4	STM32F103R4Tx	Active	2.213		LQFP64	16 kBytes	6 kBytes	51	72 MHz
☆	STM32F103R6	STM32F103R6Hx	Active	2.343		TFBGA64	32 kBytes	10 kBytes	50	72 MHz
☆	STM32F103R6	STM32F103R6Tx	Active	2.343		LQFP64	32 kBytes	10 kBytes	51	72 MHz
☆	STM32F103R8	STM32F103R8Hx	Active	2.604		TFBGA64	64 kBytes	20 kBytes	50	72 MHz
☆	STM32F103R8	STM32F103R8Tx	Active	2.604		LQFP64	64 kBytes	20 kBytes	51	72 MHz

STM32FCubeMX

MX STM32CubeMX Untitled: STM32F103C8Tx

File Window Help

Home > STM32F103C8Tx > **Untitled - Pinout & Configuration** > GENERATE CODE

Pinout & Configuration Clock Configuration Project Manager Tools

Additional Software Pinout

Pinout view System view

Categories A->Z

- System Core >
- Analog >
- Timers >
- Connectivity >
- Computing >
- Middleware >

STM32F103C8Tx LQFP48

MCUs Selection Output

Series	Lines	Mcu	Package	Required Peripherals
STM32F1	STM32F100 Value Line	STM32F100C4Tx	LQFP48	None
STM32F1	STM32F100 Value Line	STM32F100C6Tx	LQFP48	None

STM32F..

11 Analog-to-digital converter (ADC)

Low-density devices are STM32F101xx, STM32F102xx and STM32F103xx microcontrollers where the Flash memory density ranges between 16 and 32 Kbytes.

Medium-density devices are STM32F101xx, STM32F102xx and STM32F103xx microcontrollers where the Flash memory density ranges between 64 and 128 Kbytes.

High-density devices are STM32F101xx and STM32F103xx microcontrollers where the Flash memory density ranges between 256 and 512 Kbytes.

XL-density devices are STM32F101xx and STM32F103xx microcontrollers where the Flash memory density ranges between 768 Kbytes and 1 Mbyte.

Connectivity line devices are STM32F105xx and STM32F107xx microcontrollers.

This section applies to the whole STM32F10xxx family, unless otherwise specified.

11.1 ADC introduction

The 12-bit ADC is a successive approximation analog-to-digital converter. It has up to 18 multiplexed channels allowing it measure signals from sixteen external and two internal sources. A/D conversion of the various channels can be performed in single, continuous, scan or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.

The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined high or low thresholds.

The ADC input clock is generated from the PCLK2 clock divided by a prescaler and it must not exceed 14 MHz, refer to [Figure 8](#) for low-, medium-, high- and XL-density devices, and to [Figure 11](#) for connectivity line devices.

STM32F..

11.2 ADC main features

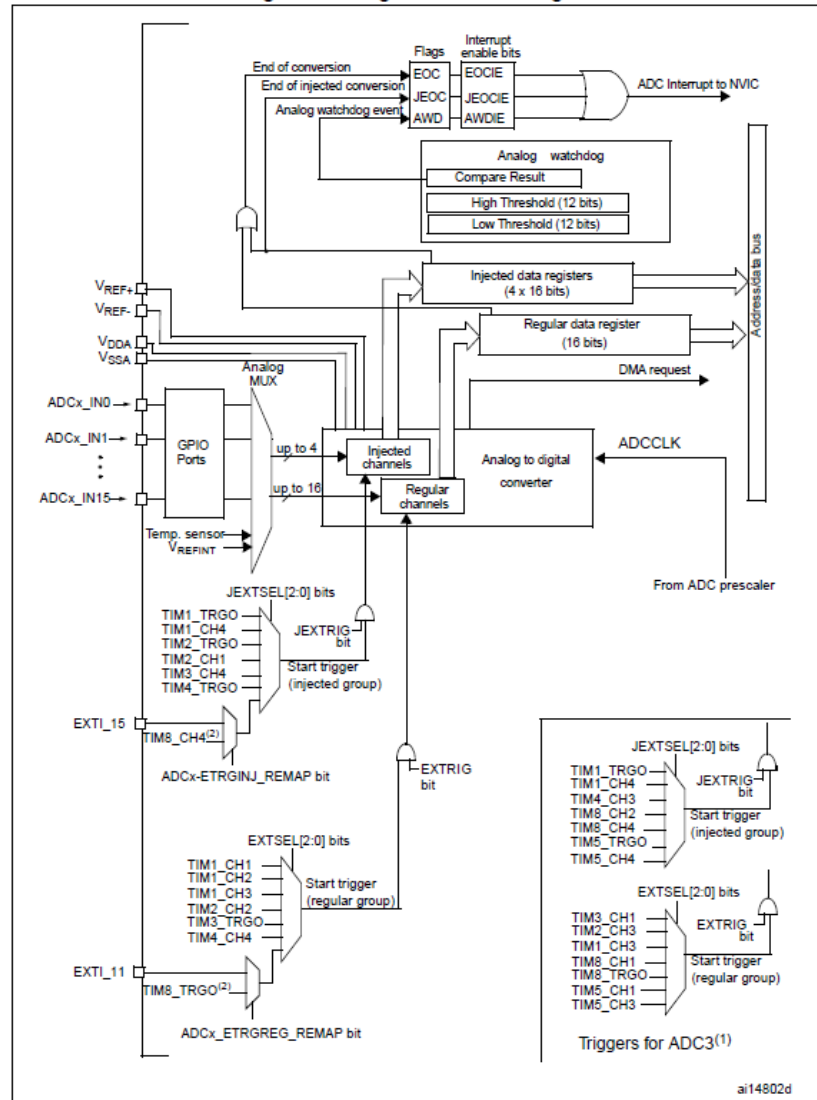
- 12-bit resolution
- Interrupt generation at End of Conversion, End of Injected conversion and Analog watchdog event
- Single and continuous conversion modes
- Scan mode for automatic conversion of channel 0 to channel 'n'
- Self-calibration
- Data alignment with in-built data coherency
- Channel by channel programmable sampling time
- External trigger option for both regular and injected conversion
- Discontinuous mode
- Dual mode (on devices with 2 ADCs or more)
- ADC conversion time:
 - STM32F103xx performance line devices: 1 μ s at 56 MHz (1.17 μ s at 72 MHz)
 - STM32F101xx access line devices: 1 μ s at 28 MHz (1.55 μ s at 36 MHz)
 - STM32F102xx USB access line devices: 1.2 μ s at 48 MHz
 - STM32F105xx and STM32F107xx devices: 1 μ s at 56 MHz (1.17 μ s at 72 MHz)
- ADC supply requirement: 2.4 V to 3.6 V
- ADC input range: $V_{REF-} \leq V_{IN} \leq V_{REF+}$
- DMA request generation during regular channel conversion

The block diagram of the ADC is shown in [Figure 22](#).

Note: V_{REF-} , if available (depending on package), must be tied to V_{SSA} .

STM32F..

Figure 22. Single ADC block diagram



1. ADC3 has regular and injected conversion triggers different from those of ADC1 and ADC2.
2. TIM8_CH4 and TIM8_TRGO with their corresponding remap bits exist only in High-density and XL-density products.

STM32F..

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Marcadores

- and clock control (RCC)
- > 9 General-purpose and alternate-function I/Os (GPIOs and AFIOs)
- > 10 Interrupts and events
- ✓ 11 Analog-to-digital converter (ADC)
 - 11.1 ADC introduction
 - 11.2 ADC main features
 - > 11.3 ADC functional description
 - 11.4 Calibration
 - 11.5 Data alignment
 - 11.6 Channel-by-channel programmable sample time
 - > 11.7 Conversion on external trigger
 - 11.8 DMA request
 - > 11.9 Dual ADC mode
 - > 11.10 Temperature sensor
 - > 11.11 ADC interrupts
 - > **11.12 ADC registers**
- > 12 Digital-to-analog converter (DAC)

11.12 ADC registers

Refer to [Section 2.2 on page 45](#) for a list of abbreviations used in register descriptions.

The peripheral registers have to be accessed by words (32-bit).

11.12.1 ADC status register (ADC_SR)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											STRT	JSTRT	JEOC	EOC	AWD
Reserved											rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

Bits 31:5 Reserved, must be kept at reset value.

Bit 4 STRT: Regular channel Start flag
This bit is set by hardware when regular channel conversion starts. It is cleared by software.
0: No regular channel conversion started
1: Regular channel conversion has started

Bit 3 JSTRT: Injected channel Start flag
This bit is set by hardware when injected channel group conversion starts. It is cleared by software.
0: No injected group conversion started
1: Injected group conversion has started

Bit 2 JEOC: Injected channel end of conversion
This bit is set by hardware at the end of all injected group channel conversion. It is cleared by software.
0: Conversion is not complete
1: Conversion complete

Bit 1 EOC: End of conversion
This bit is set by hardware at the end of a group channel conversion (regular or injected). It is cleared by software or by reading the ADC_DR.
0: Conversion is not complete
1: Conversion complete

Bit 0 AWD: Analog watchdog flag
This bit is set by hardware when the converted voltage crosses the values programmed in the ADC_LTR and ADC_HTR registers. It is cleared by software.
0: No Analog watchdog event occurred
1: Analog watchdog event occurred

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Figure 13. Basic structure of a standard I/O port bit

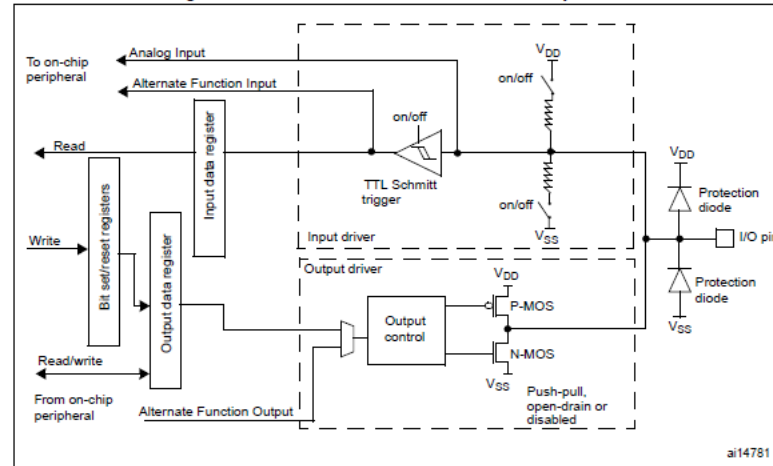
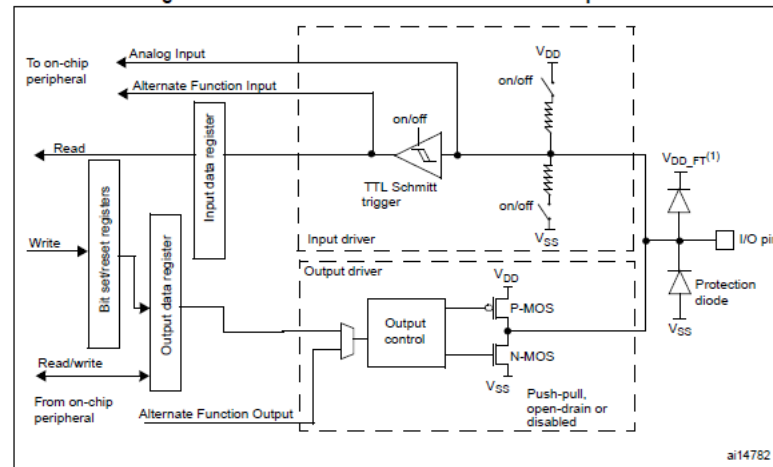


Figure 14. Basic structure of a 5-Volt tolerant I/O port bit



1. V_{DD_FT} is a potential specific to 5-Volt tolerant I/Os, and different from V_{DD} .

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