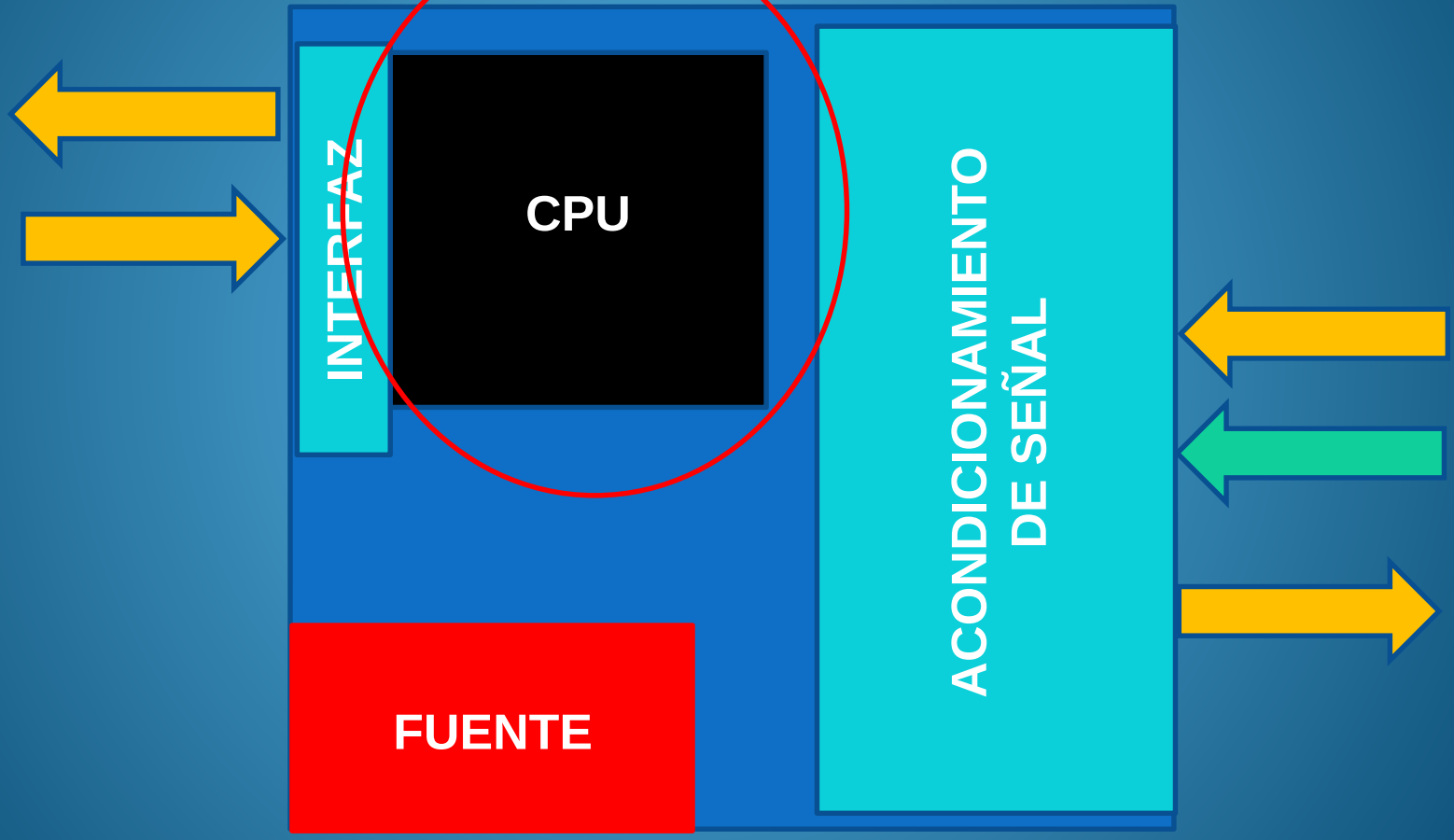
CENTRO UNIVERSITARIO DE AUTOMACIÓN Y ROBÓTICA

Facultad Regional Córdoba

TECNICAS DIGITALES III

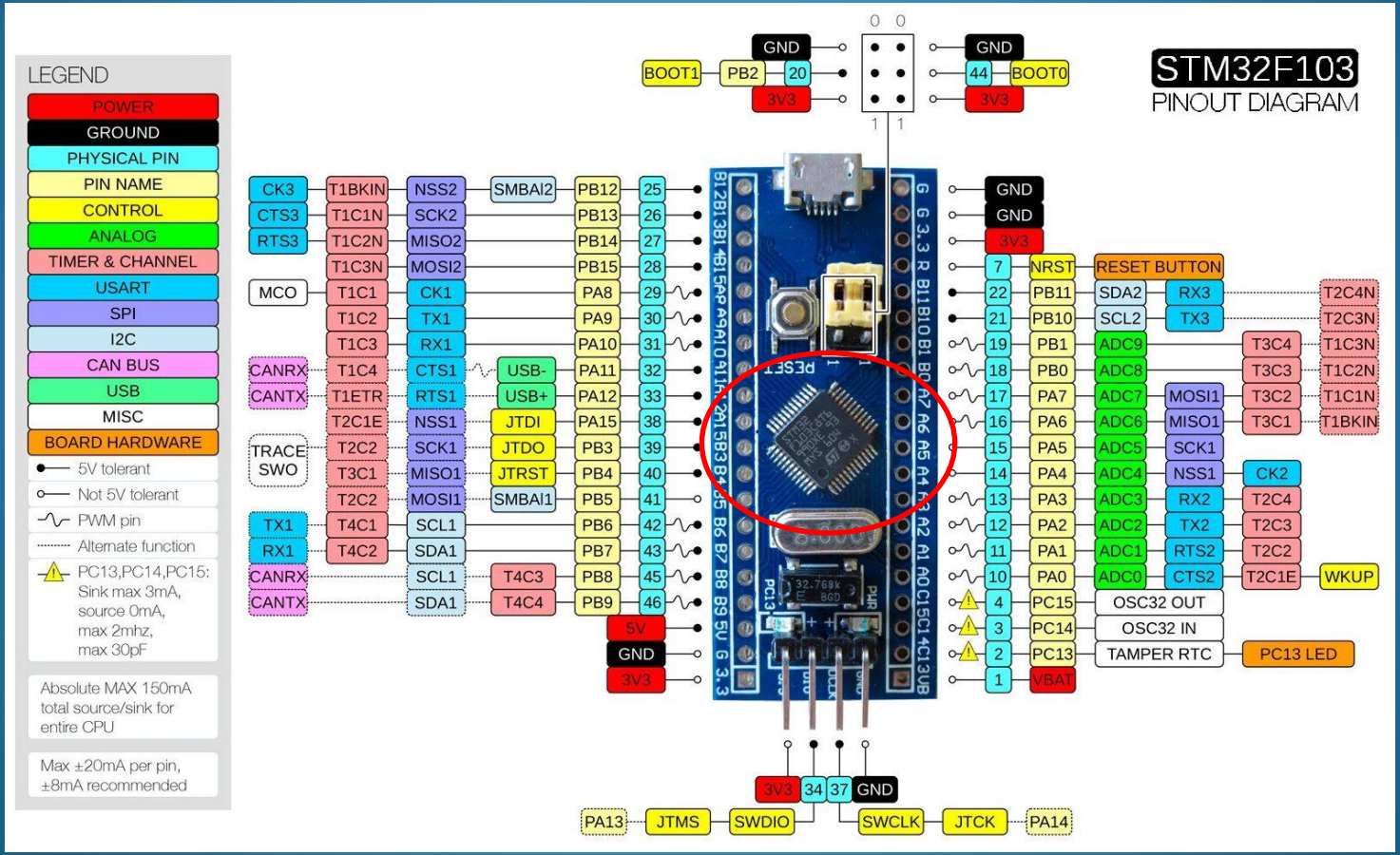
Instrumento Virtual

Placa de Adquisición



Instrumento Virtual

CPU

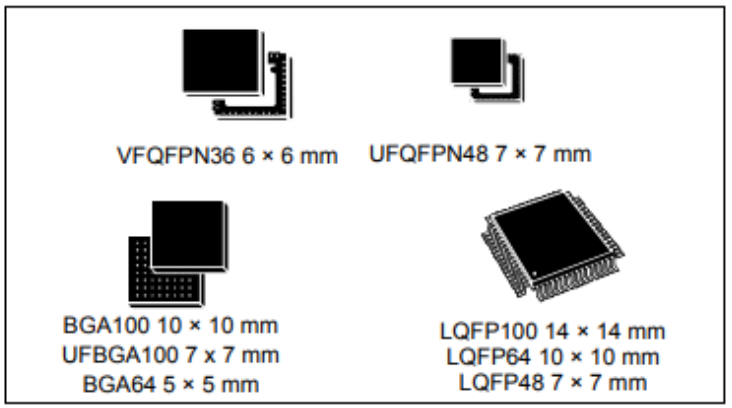


STM32F106T8

CPU

Features

- Arm® 32-bit Cortex®-M3 CPU core
  - 72 MHz maximum frequency, 1.25 DMIPS / MHz (Dhrystone 2.1) performance at 0 wait state memory access
  - Single-cycle multiplication and hardware division
- Memories
  - 64 or 128 Kbytes of Flash memory
  - 20 Kbytes of SRAM



- Debug mode
  - Serial wire debug (SWD) and JTAG interfaces

- Up to nine communication interfaces
  - Up to two I^2C interfaces (SMBus/PMBus®)
  - Up to three USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - Up to two SPIs (18 Mbit/s)
  - CAN interface (2.0B Active)
  - USB 2.0 full-speed interface

https://www.st.com/resource/en/datasheet/cd00161566.pdf

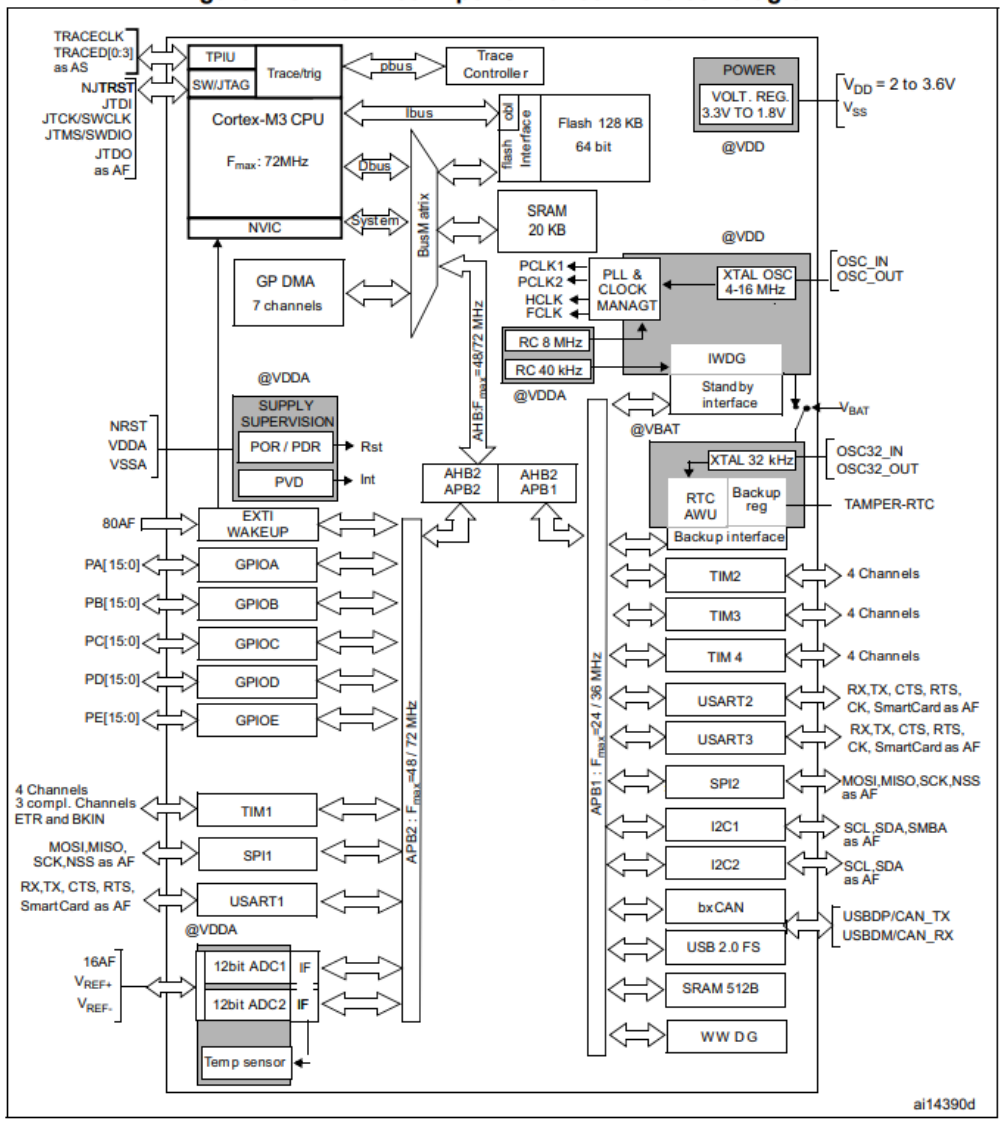
STM32F103T8

Table 2. STM32F103xx medium-density device features and peripheral counts

Peripheral		STM32F103Tx		STM32F103Cx		STM32F103Rx		STM32F103Vx	
Flash - Kbytes		64	128	64	128	64	128	64	128
SRAM - Kbytes		20		20		20		20	
Timers	General-purpose	3		3		3		3	
	Advanced-control	1		1		1		1	
Communication	SPI	1		2		2		2	
	I^2C	1		2		2		2	
	USART	2		3		3		3	
	USB	1		1		1		1	
	CAN	1		1		1		1	
GPIOs		26		37		51		80	
12-bit synchronized ADC Number of channels		2 10 channels		2 10 channels		2 16 channels(1)		2 16 channels	
CPU frequency		72 MHz							
Operating voltage		2.0 to 3.6 V							
Operating temperatures		Ambient temperatures: -40 to +85 °C / -40 to +105 °C (see *Table 9*) Junction temperature: -40 to + 125 °C (see *Table 9*)							
Packages		VFQFPN36		LQFP48, UFQFPN48		LQFP64, TFBGA64		LQFP100, LFBGA100, UFBGA100	

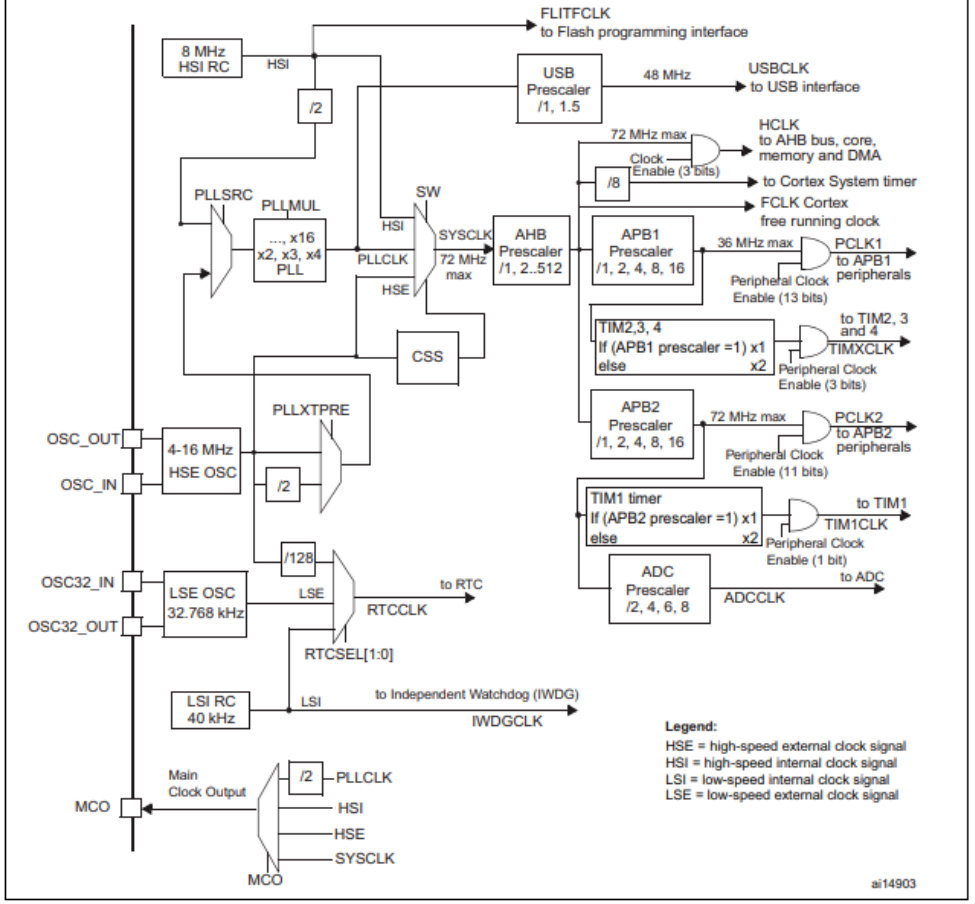
STM32F103T8

Figure 1. STM32F103xx performance line block diagram



STM32F103T8

Figure 2. Clock tree



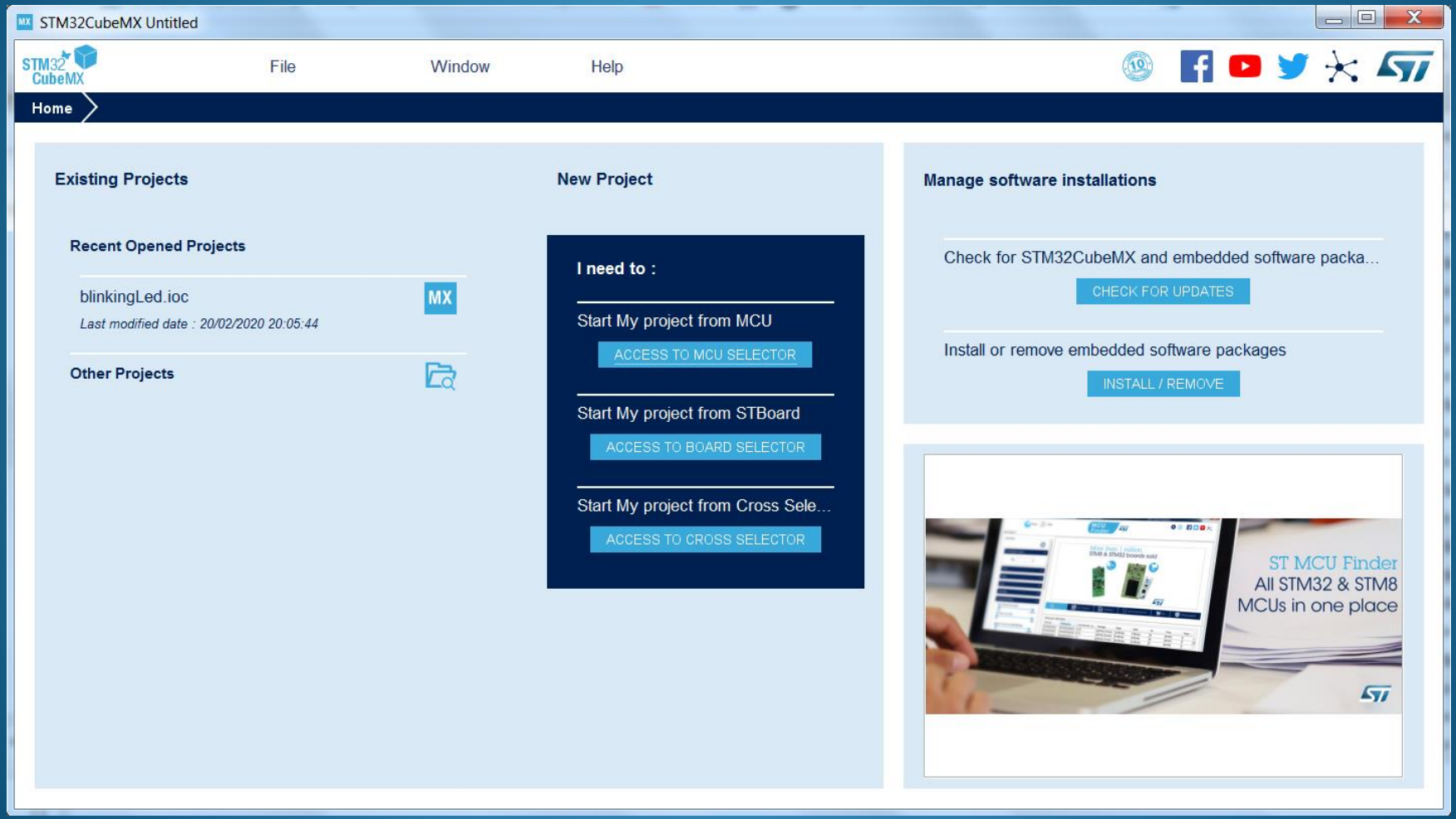
1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
2. For the availability of the USB function both HSE and PLL must be enabled, with USBCLK running at 48 MHz.
3. To have an ADC conversion time of 1 µs, APB2 must be at 14 MHz, 28 MHz or 56 MHz.

STM32F103T8

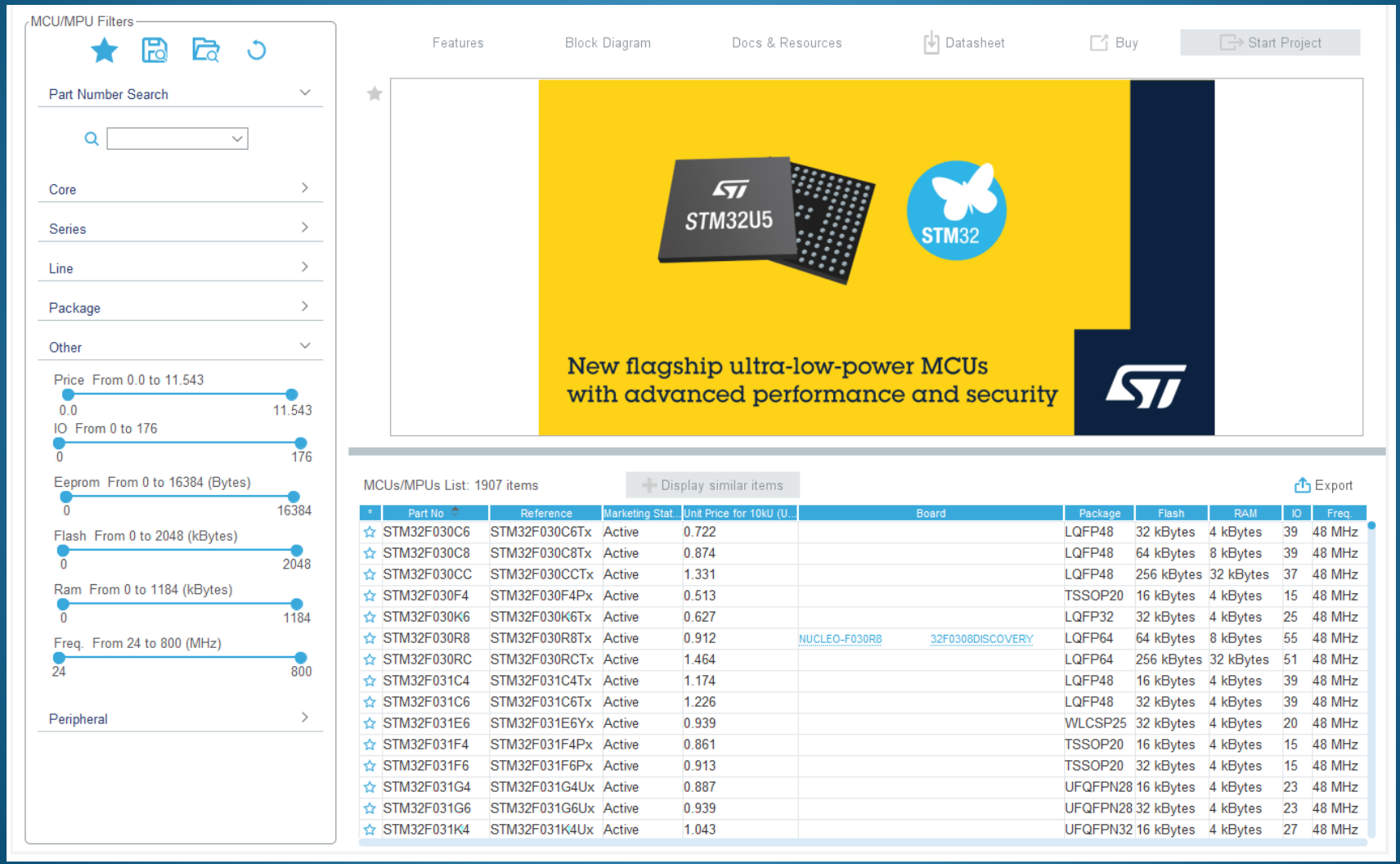
Table 5. Medium-density STM32F103xx pin definitions

Pins							Pin name	Type[1]	I / O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LFBGA100	UFBG100	LQFP48/UFQFPN48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
A3	B2	-	-	-	1	-	PE2	I/O	FT	PE2	TRACECK	-
B3	A1	-	-	-	2	-	PE3	I/O	FT	PE3	TRACED0	-
C3	B1	-	-	-	3	-	PE4	I/O	FT	PE4	TRACED1	-
D3	C2	-	-	-	4	-	PE5	I/O	FT	PE5	TRACED2	-
E3	D2	-	-	-	5	-	PE6	I/O	FT	PE6	TRACED3	-
B2	E2	1	B2	1	6	-	V_{BAT}	S	-	V_{BAT}	-	-
A2	C1	2	A2	2	7	-	PC13-TAMPER-RTC[5]	I/O	-	PC13[6]	TAMPER-RTC	-
A1	D1	3	A1	3	8	-	PC14-OSC32_IN[5]	I/O	-	PC14[6]	OSC32_IN	-
B1	E1	4	B1	4	9	-	PC15-OSC32_OUT[5]	I/O	-	PC15[6]	OSC32_OUT	-
C2	F2	-	-	-	10	-	V_{SS_5}	S	-	V_{SS_5}	-	-
D2	G2	-	-	-	11	-	V_{DD_5}	S	-	V_{DD_5}	-	
C1	F1	5	C1	5	12	2	OSC_IN	I	-	OSC_IN	-	PD0[7]
D1	G1	6	D1	6	13	3	OSC_OUT	O	-	OSC_OUT		PD1[7]
E1	H2	7	E1	7	14	4	NRST	I/O	-	NRST	-	-
F1	H1	-	E3	8	15	-	PC0	I/O	-	PC0	ADC12_IN10	-
F2	J2	-	E2	9	16	-	PC1	I/O	-	PC1	ADC12_IN11	-
E2	J3	-	F2	10	17	-	PC2	I/O	-	PC2	ADC12_IN12	-
F3	K2	-	-[8]	11	18	-	PC3	I/O	-	PC3	ADC12_IN13	-
G1	J1	8	F1	12	19	5	V_{SSA}	S	-	V_{SSA}	-	-
H1	K1	-	-	-	20	-	V_{REF-}	S	-	V_{REF-}	-	-
J1	L1	-	G1[8]	-	21	-	V_{REF+}	S	-	V_{REF+}	-	-
K1	M1	9	H1	13	22	6	V_{DDA}	S	-	V_{DDA}	-	-

STM32FCubeMX

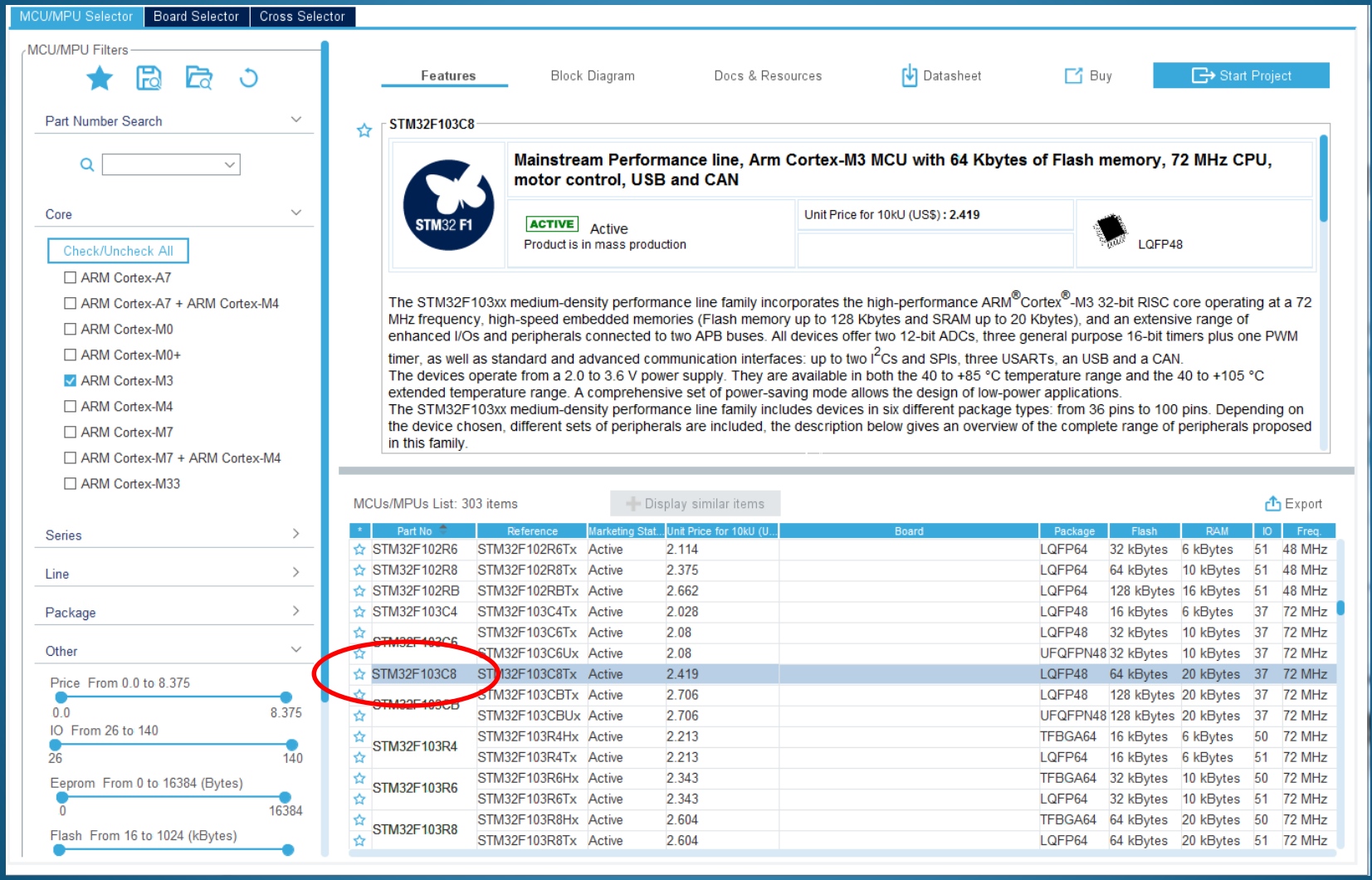


STM32FCubeMX

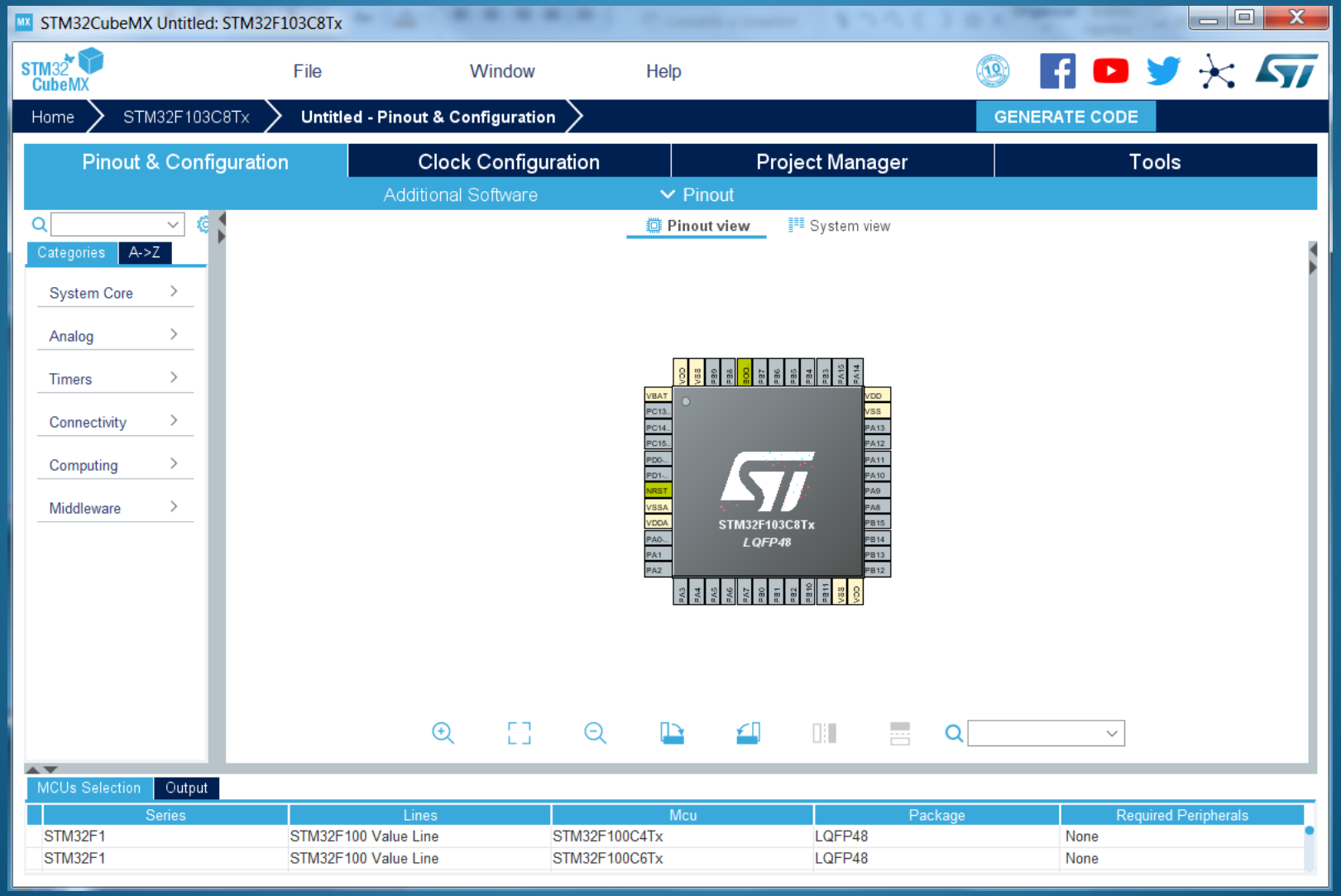


*	Part No	Reference	Marketing Stat..	Unit Price for 10kU (U...	Board		Package	Flash	RAM	IO	Freq.
☆	STM32F030C6	STM32F030C6Tx	Active	0.722			LQFP48	32 kBytes	4 kBytes	39	48 MHz
☆	STM32F030C8	STM32F030C8Tx	Active	0.874			LQFP48	64 kBytes	8 kBytes	39	48 MHz
☆	STM32F030CC	STM32F030CCTx	Active	1.331			LQFP48	256 kBytes	32 kBytes	37	48 MHz
☆	STM32F030F4	STM32F030F4Px	Active	0.513			TSSOP20	16 kBytes	4 kBytes	15	48 MHz
☆	STM32F030K6	STM32F030K6Tx	Active	0.627			LQFP32	32 kBytes	4 kBytes	25	48 MHz
☆	STM32F030R8	STM32F030R8Tx	Active	0.912	NUCLEO-F030R8	32F0308DISCOVERY	LQFP64	64 kBytes	8 kBytes	55	48 MHz
☆	STM32F030RC	STM32F030RCTx	Active	1.464			LQFP64	256 kBytes	32 kBytes	51	48 MHz
☆	STM32F031C4	STM32F031C4Tx	Active	1.174			LQFP48	16 kBytes	4 kBytes	39	48 MHz
☆	STM32F031C6	STM32F031C6Tx	Active	1.226			LQFP48	32 kBytes	4 kBytes	39	48 MHz
☆	STM32F031E6	STM32F031E6Yx	Active	0.939			WLCSP25	32 kBytes	4 kBytes	20	48 MHz
☆	STM32F031F4	STM32F031F4Px	Active	0.861			TSSOP20	16 kBytes	4 kBytes	15	48 MHz
☆	STM32F031F6	STM32F031F6Px	Active	0.913			TSSOP20	32 kBytes	4 kBytes	15	48 MHz
☆	STM32F031G4	STM32F031G4Ux	Active	0.887			UFQFPN28	16 kBytes	4 kBytes	23	48 MHz
☆	STM32F031G6	STM32F031G6Ux	Active	0.939			UFQFPN28	32 kBytes	4 kBytes	23	48 MHz
☆	STM32F031K4	STM32F031K4Ux	Active	1.043			UFQFPN32	16 kBytes	4 kBytes	27	48 MHz

STM32FCubeMX



STM32FCubeMX



STM32F..

11 Analog-to-digital converter (ADC)

Low-density devices are STM32F101xx, STM32F102xx and STM32F103xx microcontrollers where the Flash memory density ranges between 16 and 32 Kbytes.

Medium-density devices are STM32F101xx, STM32F102xx and STM32F103xx microcontrollers where the Flash memory density ranges between 64 and 128 Kbytes.

High-density devices are STM32F101xx and STM32F103xx microcontrollers where the Flash memory density ranges between 256 and 512 Kbytes.

XL-density devices are STM32F101xx and STM32F103xx microcontrollers where the Flash memory density ranges between 768 Kbytes and 1 Mbyte.

Connectivity line devices are STM32F105xx and STM32F107xx microcontrollers.

This section applies to the whole STM32F10xxx family, unless otherwise specified.

11.1 ADC introduction

The 12-bit ADC is a successive approximation analog-to-digital converter. It has up to 18 multiplexed channels allowing it measure signals from sixteen external and two internal sources. A/D conversion of the various channels can be performed in single, continuous, scan or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.

The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined high or low thresholds.

The ADC input clock is generated from the PCLK2 clock divided by a prescaler and it must not exceed 14 MHz, refer to *Figure 8* for low-, medium-, high- and XL-density devices, and to *Figure 11* for connectivity line devices.

STM32F..

11.2 ADC main features

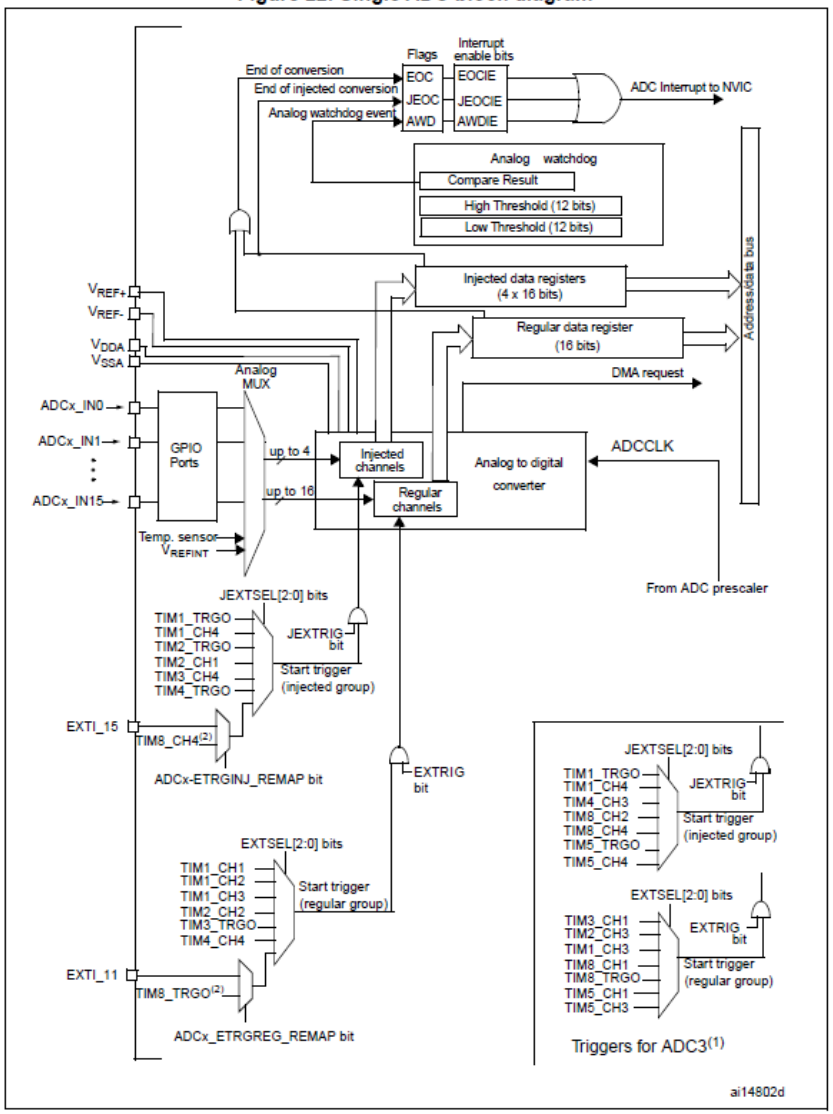
- 12-bit resolution
- Interrupt generation at End of Conversion, End of Injected conversion and Analog watchdog event
- Single and continuous conversion modes
- Scan mode for automatic conversion of channel 0 to channel ‘n’
- Self-calibration
- Data alignment with in-built data coherency
- Channel by channel programmable sampling time
- External trigger option for both regular and injected conversion
- Discontinuous mode
- Dual mode (on devices with 2 ADCs or more)
- ADC conversion time:
  - STM32F103xx performance line devices: 1 µs at 56 MHz (1.17 µs at 72 MHz)
  - STM32F101xx access line devices: 1 µs at 28 MHz (1.55 µs at 36 MHz)
  - STM32F102xx USB access line devices: 1.2 µs at 48 MHz
  - STM32F105xx and STM32F107xx devices: 1 µs at 56 MHz (1.17 µs at 72 MHz)
- ADC supply requirement: 2.4 V to 3.6 V
- ADC input range: $V_{REF-} \leq V_{IN} \leq V_{REF+}$
- DMA request generation during regular channel conversion

The block diagram of the ADC is shown in *Figure 22*.

Note: V_{REF-}, if available (depending on package), must be tied to V_{SSA}.

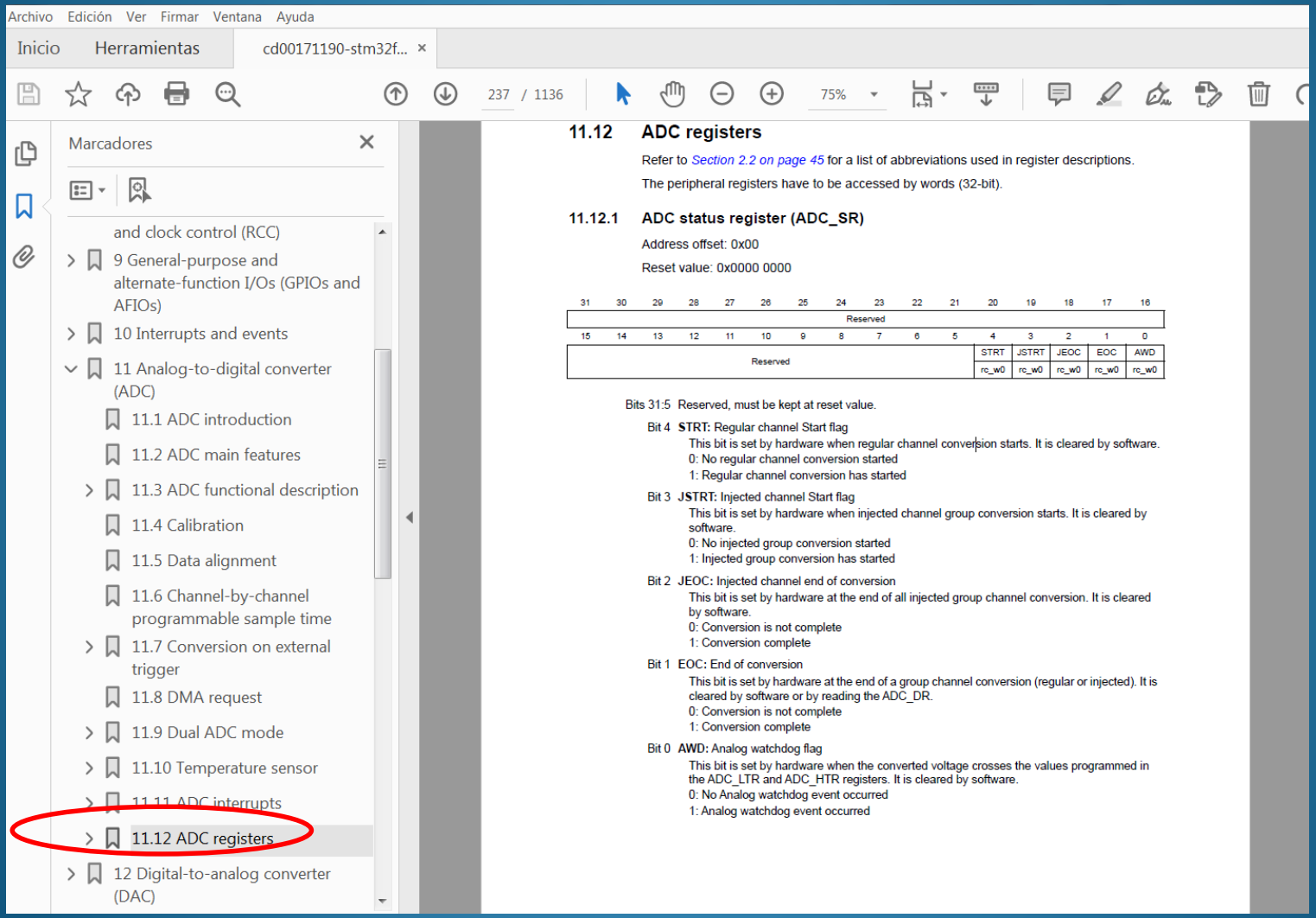
STM32F..

Figure 22. Single ADC block diagram



1. ADC3 has regular and injected conversion triggers different from those of ADC1 and ADC2.
2. TIM8_CH4 and TIM8_TRGO with their corresponding remap bits exist only in High-density and XL-density products.

STM32F..



11.12 ADC registers

Refer to *Section 2.2 on page 45* for a list of abbreviations used in register descriptions.

The peripheral registers have to be accessed by words (32-bit).

11.12.1 ADC status register (ADC_SR)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											STRT	JSTRT	JEOC	EOC	AWD
											rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

Bits 31:5 Reserved, must be kept at reset value.

Bit 4 **STRT:** Regular channel Start flag
This bit is set by hardware when regular channel conversion starts. It is cleared by software.
0: No regular channel conversion started
1: Regular channel conversion has started

Bit 3 **JSTRT:** Injected channel Start flag
This bit is set by hardware when injected channel group conversion starts. It is cleared by software.
0: No injected group conversion started
1: Injected group conversion has started

Bit 2 **JEOC:** Injected channel end of conversion
This bit is set by hardware at the end of all injected group channel conversion. It is cleared by software.
0: Conversion is not complete
1: Conversion complete

Bit 1 **EOC:** End of conversion
This bit is set by hardware at the end of a group channel conversion (regular or injected). It is cleared by software or by reading the ADC_DR.
0: Conversion is not complete
1: Conversion complete

Bit 0 **AWD:** Analog watchdog flag
This bit is set by hardware when the converted voltage crosses the values programmed in the ADC_LTR and ADC_HTR registers. It is cleared by software.
0: No Analog watchdog event occurred
1: Analog watchdog event occurred

Eclipse

Figure 13. Basic structure of a standard I/O port bit

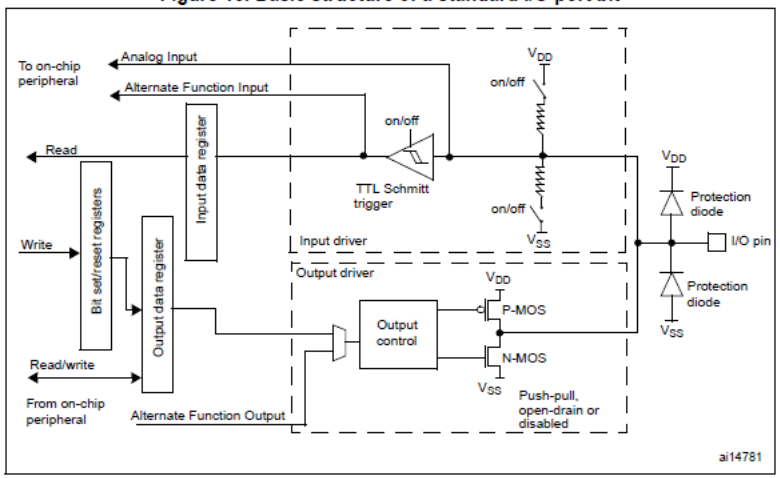
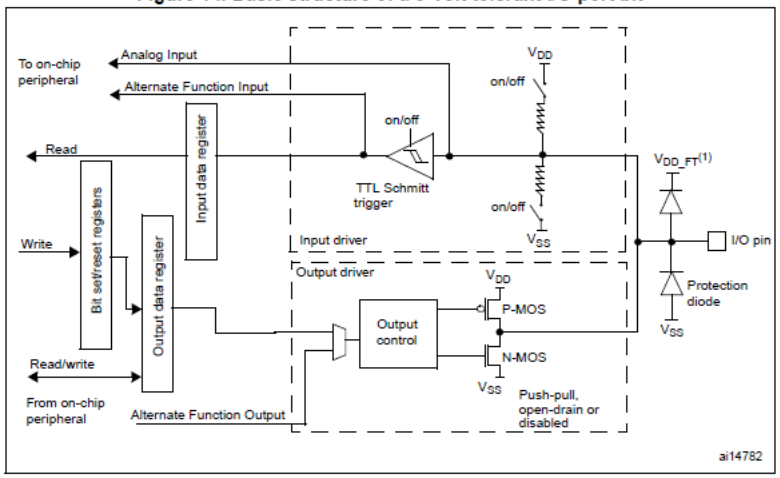
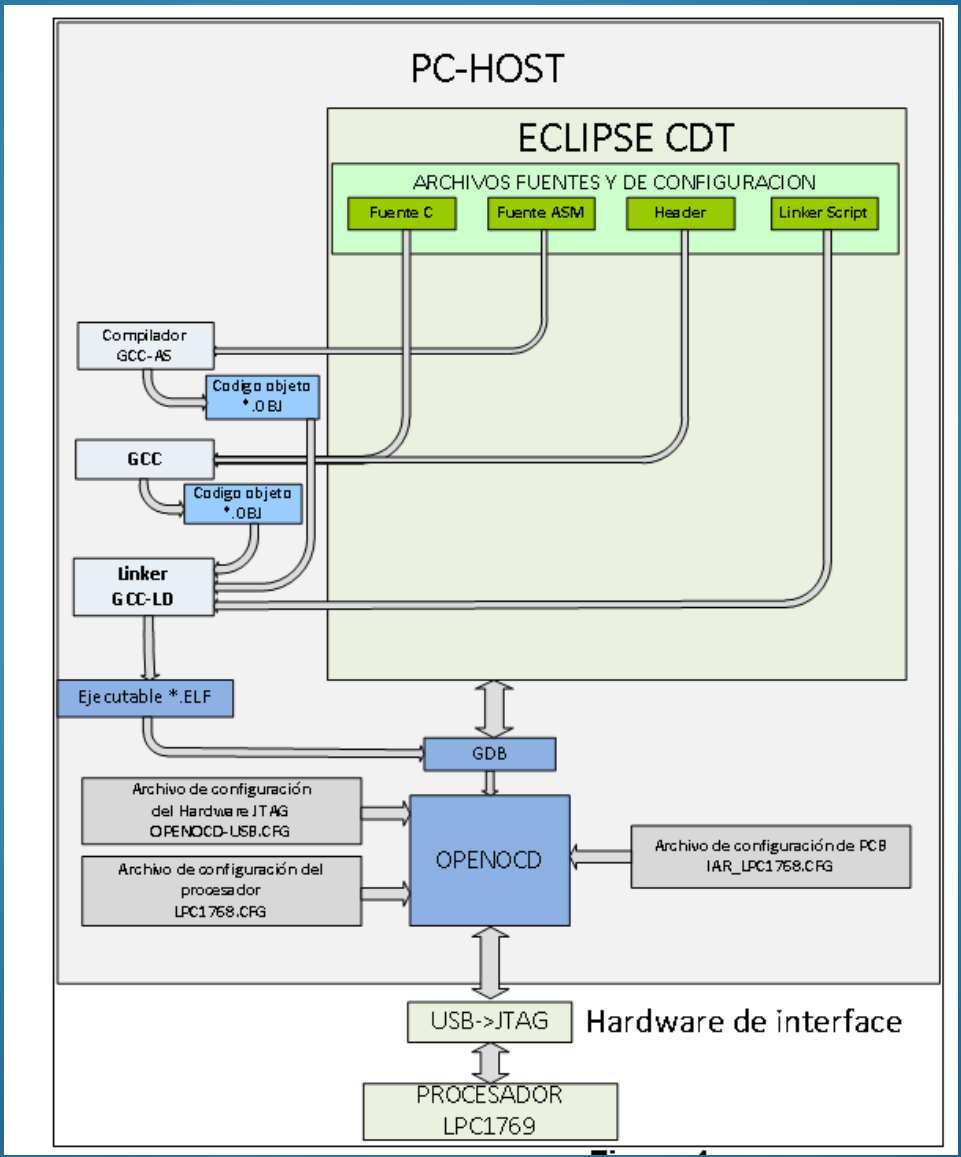


Figure 14. Basic structure of a 5-Volt tolerant I/O port bit



1. V_{DD_FT} is a potential specific to 5-Volt tolerant I/Os, and different from V_{DD}.

Eclipse


PC-HOST
ECLIPSE CDT
ARCHIVOS FUENTES Y DE CONFIGURACION
Fuente C
Fuente ASM
Header
Linker Script
Compilador GCC-AS
Codigo objeto *.OBJ
GCC
Codigo objeto *.OBJ
Linker GCC-LD
Ejecutable *.ELF
GDB
Archivo de configuración del Hardware JTAG OPENOCD-USB.CFG
Archivo de configuración del procesador LPC1768.CFG
OPENOCD
Archivo de configuración de PCB IAR_LPC1768.CFG
USB->JTAG
Hardware de interface
PROCESADOR LPC1769