Jinming Ren

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Education

University of Electronic Science and Technology of China (UESTC) Sept 2022 — Present

University of Glasgow, Dual Degree Program Sept 2022 — Present

- **Major**: Communication Engineering; GPA: 3.87/4.0, Ranking: 2/164 (Top 1.2%).
- **Relevant Coursework**: Signals and Systems, Stochastic Processes, Artificial Intelligence and Machine Learning, Information Theory, Electrodynamics, Digital Circuit Design, etc.
- **Online Course**: Abstract Algebra, Complex Analysis, Differential Geometry, Control Theory, etc.

Research & Projects

System-level Co-Design of RISCV Accelerators for TinyML at the Edge Ongoing

Research Assistant, Professor Yun Li, UESTC

- Designing, implementing and verifying hardware-accelerated DSC and attention kernels in ViT using `C++` with RVV intrinsics that are adaptable and efficient for edge computing in Coral NPU framework open-sourced by Google and VeriSilicon.
- Exploring a large multi-dimensional design space using automated methods (e.g. heuristic and evolutionary algorithms) to identify optimal configurations balancing accuracy, energy, and latency.

GAT-based Multi-Task RL for Robust PVT-Aware Analog Design Aug 2025 — Oct 2025

Research Assistant, Professor Yun Li, UESTC

- Proposed a GAT-based multi-task Reinforcement Learning framework to optimize analog circuits under diverse PVT corners.
- Modeled PVT conditions as graph nodes, enabling adaptive attention to corner-specific bottlenecks.
- Reduced specific violations by 19× and simulations by 69% on `AnalogGym` benchmarks.

YOPO: You Only Pick Once – Light Object Tracking Algorithm Sept 2025

- Developed a lightweight object tracking algorithm that requires only one initial selection, successfully mitigate the intense computation of DNN forward propagation on every frame.
- Utilized NCC-based matching, adaptive kernel updating, capable of tracking objects with gradual color and size changes.

Design and Visualization of a Complete Single-cycle RV32I CPU Core Jan 2025 — Mar 2025

- Designed and simulated an entire RISCV 32-bit CPU from scratch in `Verilog` for RTL simulation and in `Digital` Software for working principle visualization.
- Supported basic peripherals: GPIOs, IIC, UART, etc.
- Implemented a simple boot ROM in assembly, minimal interrupt service for running a Linux kernel.

CNN for Embedded Systems Feb 2024 — May 2024

- Integrated a convolutional neural network (CNN) into an MCU using `C` in `MbedOS`.
- Enabled smart fall detection, body temperature monitoring and real-time data visualization for patients.

Relevant Skills

IT Skills	Latex, Quarto Markdown, Typst, Manim, Github.
Programming	`C/C++`, `Python`, `Matlab`, `Verilog`, `Chisel`, `RISCV Assembly`, `Makefile`, `Bazel`.
Language	Native Chinese, Fluent English.

Awards

Top Academic Scholarship of UESTC (Top 5%) Dec 2023, Dec 2024

China National Scholarship (Top 3%) Dec 2024

First Prize: 7th National College Art Exhibition and Performance Sept 2024